



**THE DATASHEET OF  
IS62WV2568BLL-70HI-TR**



# IS62WV2568ALL IS62WV2568BLL



## 256K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

JANUARY 2013

### FEATURES

- High-speed access time: 45ns, 55ns, 70ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V--2.2V  $V_{CC}$  (62WV2568ALL)
  - 2.5V--3.6V  $V_{CC}$  (62WV2568BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Lead-free available

### DESCRIPTION

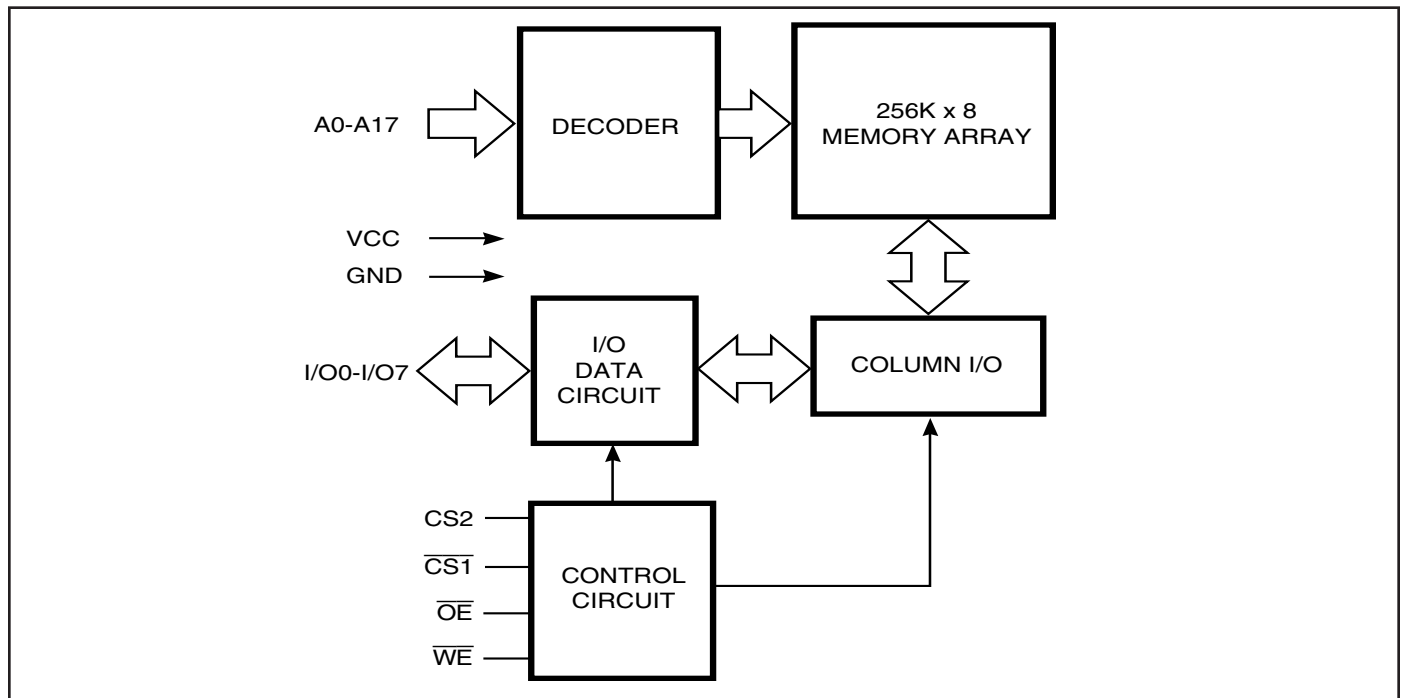
The *ISSI* IS62WV2568ALL / IS62WV2568BLL are high-speed, 2M bit static RAMs organized as 256K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IS62WV2568ALL and IS62WV2568BLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), sTSOP (TYPE I), and 36-pin mini BGA.

### FUNCTIONAL BLOCK DIAGRAM



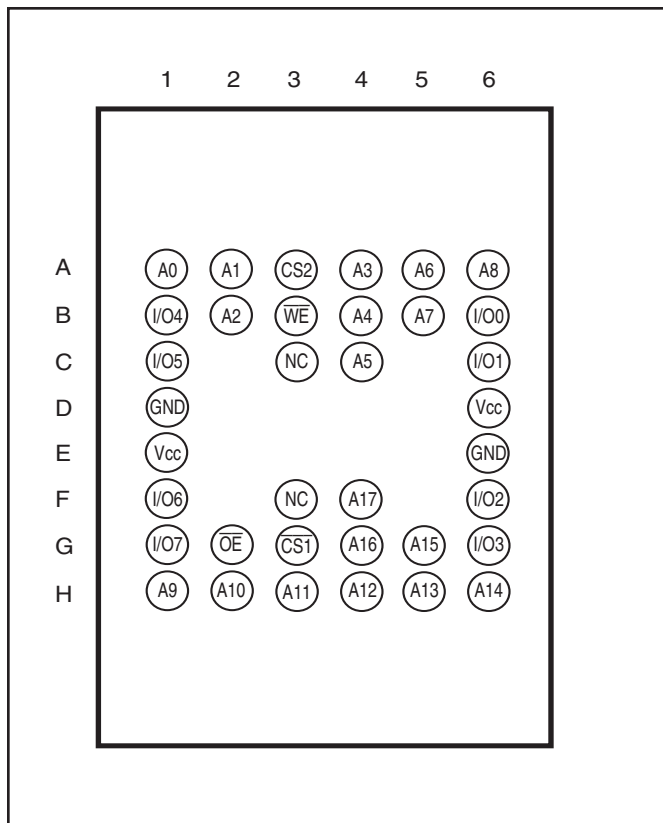
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**PIN DESCRIPTIONS**

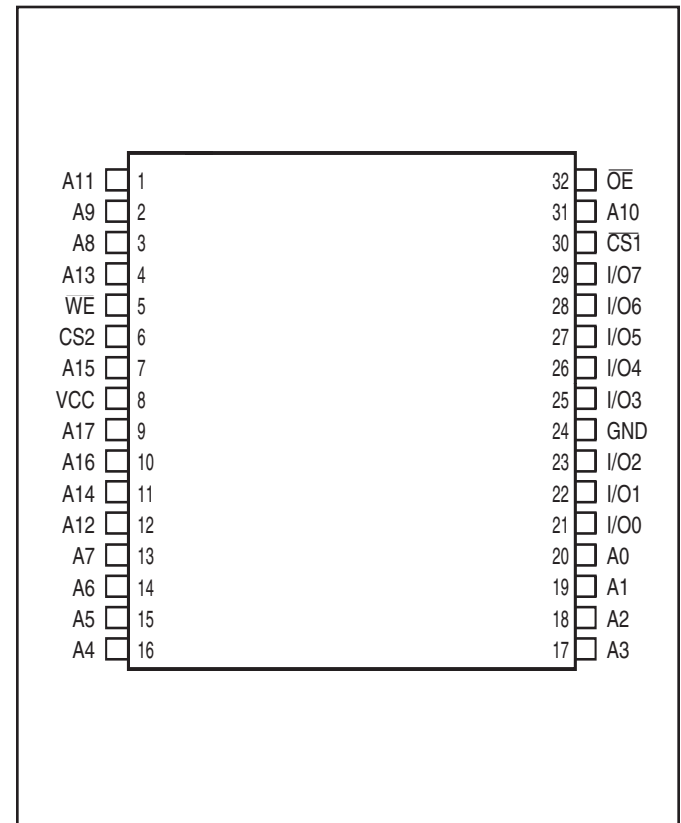
A0-A17	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
CS2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
Vcc	Power
GND	Ground

**PIN CONFIGURATION**

**36-pin mini BGA (B) (6mm x 8mm)**



**32-pin TSOP (TYPE I), sTSOP (TYPE I)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>CC</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE (V<sub>CC</sub>)**

Range	Ambient Temperature	IS62WV2568ALL	IS62WV2568BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
Industrial	-40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.65-2.2V	1.4	—	V
		I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.65-2.2V	—	0.2	V
		I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.65-2.2V	1.4	V <sub>CC</sub> + 0.2	V
			2.5-3.6V	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL<sup>(1)</sup></sub>	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Outputs Disabled		-1	1	μA

**Notes:**

1. Undershoot: -1.0V for pulse width less than 10ns. Not 100% tested.
2. Overshoot: V<sub>DD</sub> + 1.0V for pulse width less than 10ns. Not 100% tested.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

**AC TEST CONDITIONS**

Parameter	62WV2568ALL (Unit)	62WV2568BLL (Unit)
Input Pulse Level	0.4V to V <sub>CC</sub> -0.2V	0.4V to V <sub>CC</sub> -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V <sub>REF</sub>	V <sub>REF</sub>
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.65-2.2V	2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V <sub>REF</sub>	0.9V	1.5V
V <sub>TM</sub>	1.8V	2.8V

**AC TEST LOADS**

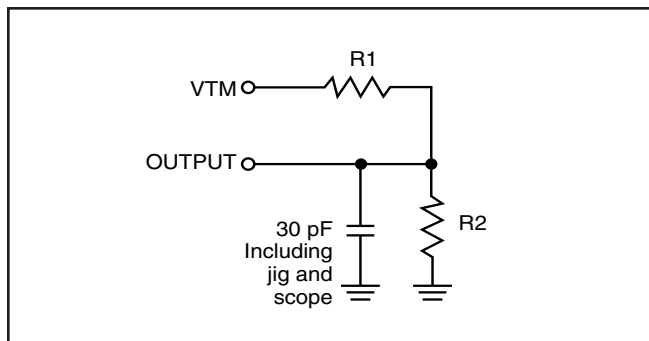


Figure 1

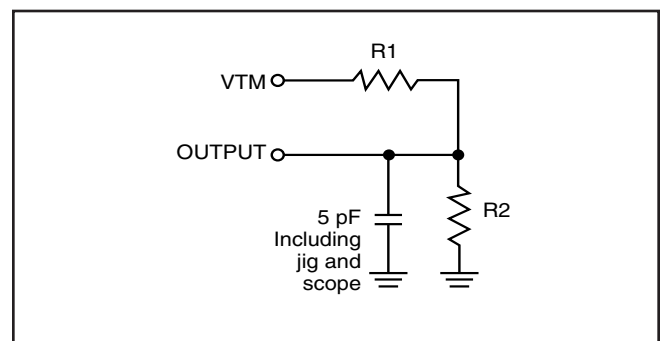


Figure 2

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

**62WV2568ALL** (1.65V - 2.2V)

Symbol	Parameter	Test Conditions		Max. 70ns	Unit
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	15 15	mA
I <sub>CC1</sub>	Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = 0	Com. Ind.	3 3	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz	Com. Ind.	0.3 0.3	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., $\overline{CS1} \geq V_{CC} - 0.2V$ , CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	5 10	μA

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

**62WV2568BLL** (2.5V - 3.6V)

Symbol	Parameter	Test Conditions		Max. 45ns	Max. 55ns	Max. 70ns	Unit
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	35 40	30 35	25 30	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz	Com. Ind.	0.3 0.3	0.3 0.3	0.3 0.3	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., $\overline{CS1} \geq V_{CC} - 0.2V$ , CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	10 10	10 10	10 10	μA

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

# IS62WV2568ALL, IS62WV2568BLL

## READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

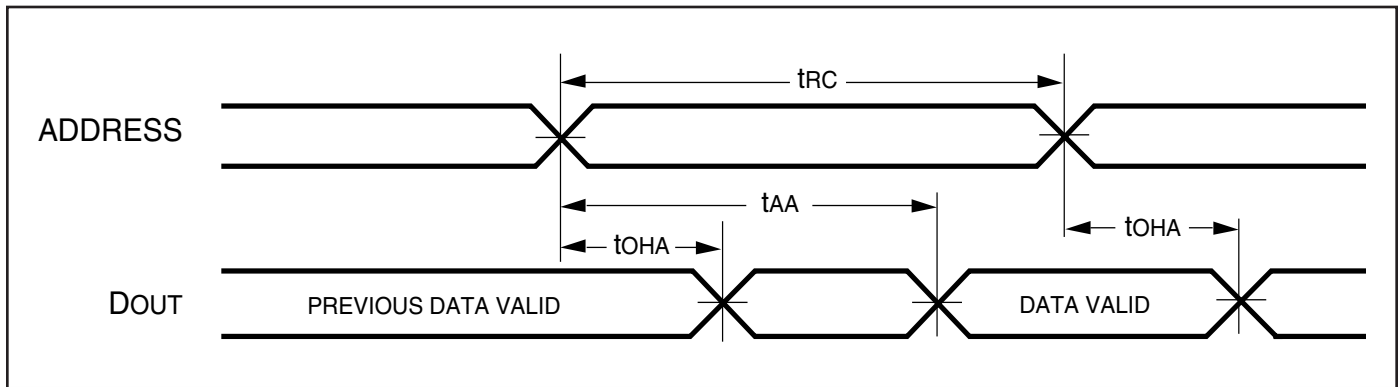
Symbol	Parameter	45ns		55ns		70ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	45	—	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	45	—	55	—	70	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	10	—	ns
t <sub>ACS1</sub> /t <sub>ACS2</sub>	$\overline{CS1}$ /CS2 Access Time	—	45	—	55	—	70	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	20	—	25	—	35	ns
t <sub>HZOE</sub> <sup>(2)</sup>	$\overline{OE}$ to High-Z Output	—	15	—	20	—	25	ns
t <sub>LZOE</sub> <sup>(2)</sup>	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t <sub>HZCS1</sub> /t <sub>HZCS2</sub> <sup>(2)</sup>	$\overline{CS1}$ /CS2 to High-Z Output	0	15	0	20	0	25	ns
t <sub>LZCS1</sub> /t <sub>LZCS2</sub> <sup>(2)</sup>	$\overline{CS1}$ /CS2 to Low-Z Output	10	—	10	—	10	—	ns

### Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

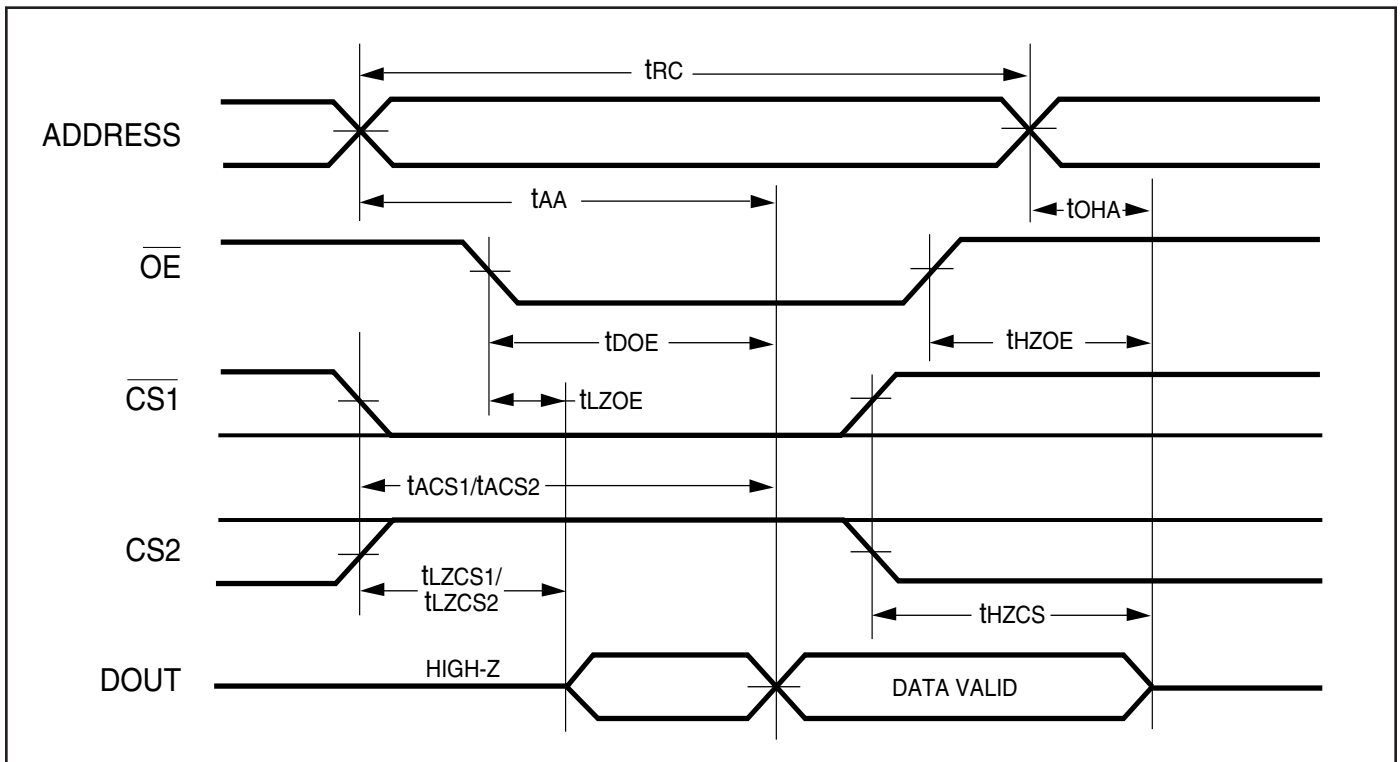
## AC WAVEFORMS

### READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ , $CS2 = \overline{WE} = V_{IH}$ )



**AC WAVEFORMS**

**READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{OE}$  Controlled)**



**Notes:**

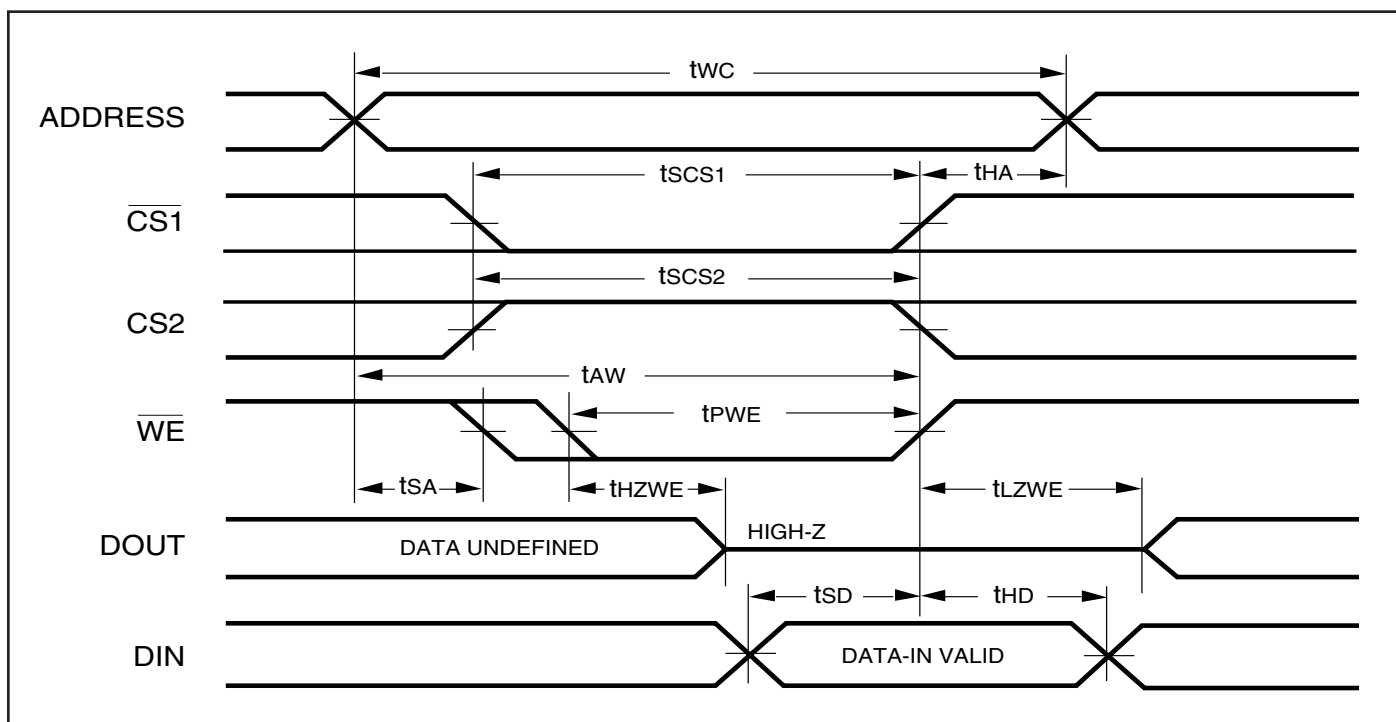
1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW and  $CS2$  HIGH transition.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

Symbol	Parameter	45ns		55ns		70ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	45	—	55	—	70	—	ns
t <sub>SCS1/tSCS2</sub>	$\overline{CS1}/CS2$ to Write End	35	—	45	—	60	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	35	—	45	—	60	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35	—	40	—	50	—	ns
t <sub>SD</sub>	Data Setup to Write End	20	—	25	—	30	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

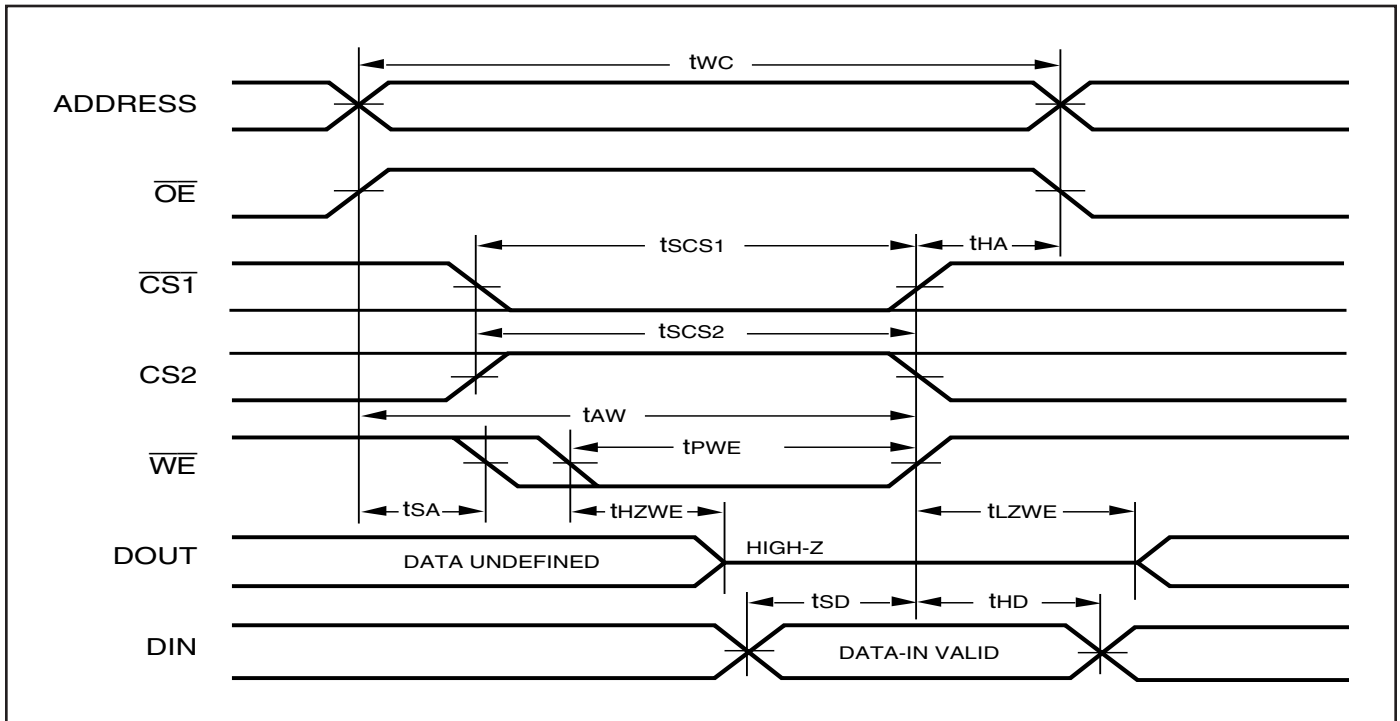
**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW, CS2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

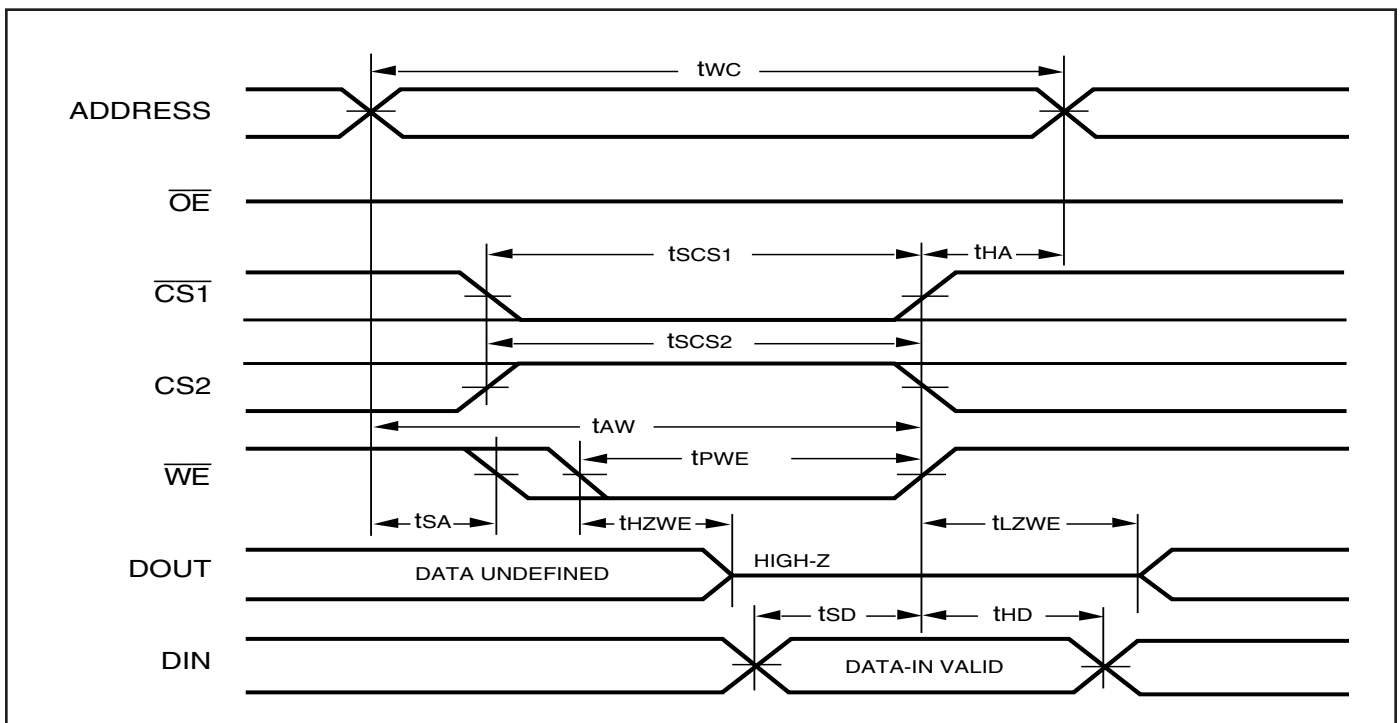
**AC WAVEFORMS**
**WRITE CYCLE NO. 1** ( $\overline{CS1}/CS2$  Controlled,  $\overline{OE} = \text{HIGH or LOW}$ )


**AC WAVEFORMS**

**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



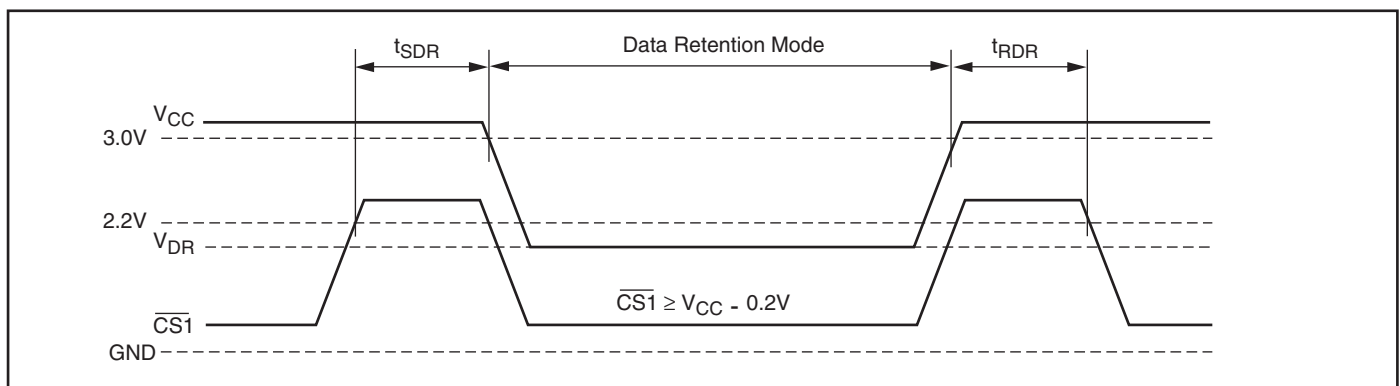
**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



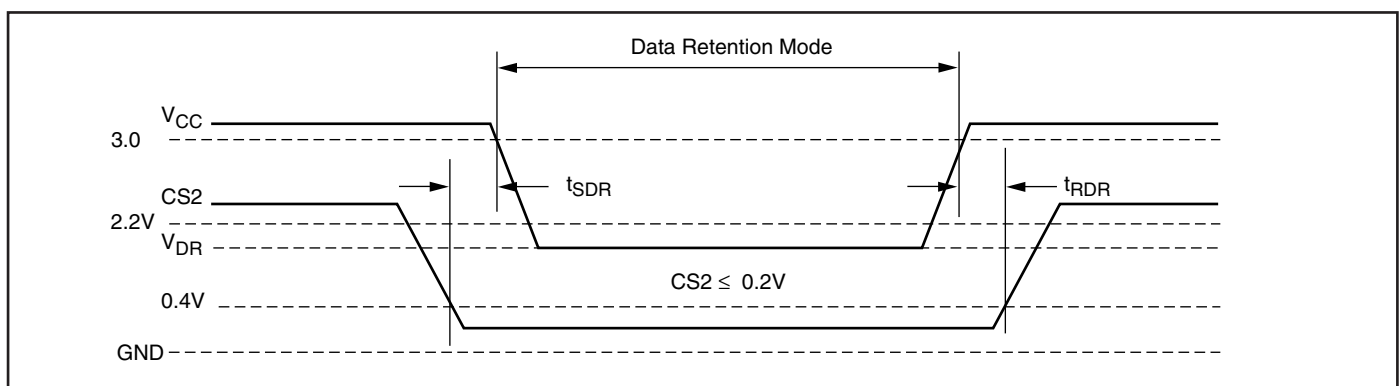
**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	See Data Retention Waveform	1.0	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V, $\overline{CS1} \geq V_{CC} - 0.2V$	—	10	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns

**DATA RETENTION WAVEFORM ( $\overline{CS1}$  Controlled)**



**DATA RETENTION WAVEFORM (CS2 Controlled)**



**ORDERING INFORMATION**
**IS62WV2568ALL (1.65V - 2.2V)**
**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
70	IS62WV2568ALL-70T	TSOP, TYPE I,

**Industrial Range: -40°C to +85°C**

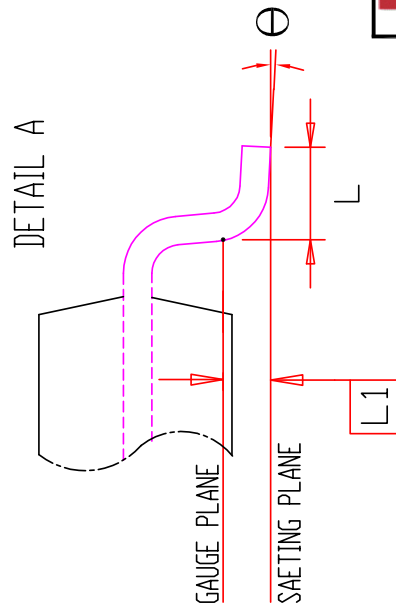
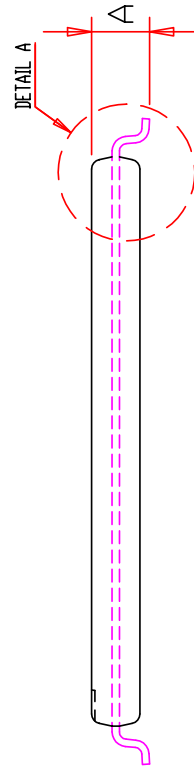
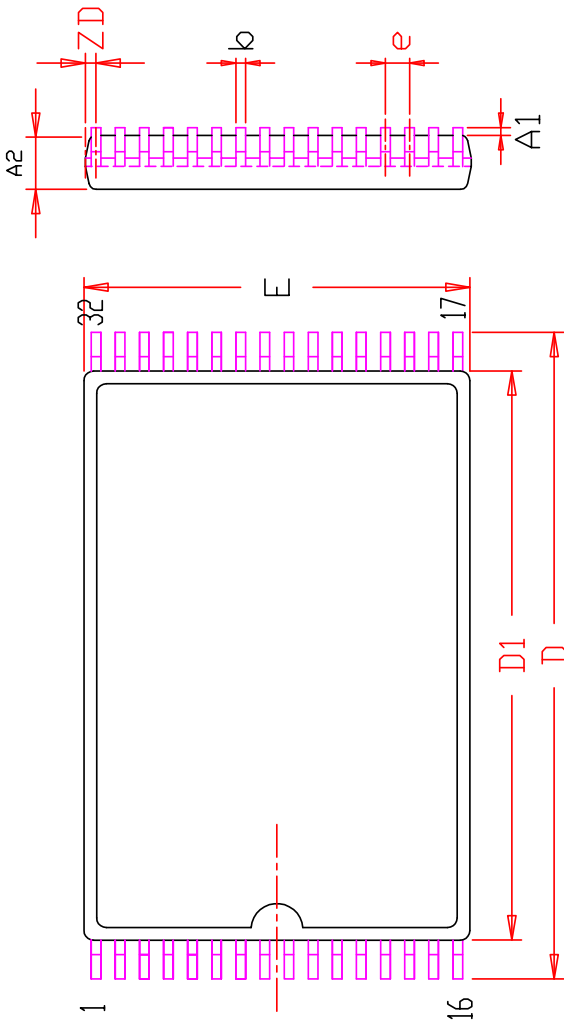
Speed (ns)	Order Part No.	Package
70	IS62WV2568ALL-70TI	TSOP, TYPE I
70	IS62WV2568ALL-70TLI	TSOP, TYPE I, Lead-free
70	IS62WV2568ALL-70BI	mini BGA (6mm x 8mm)
70	IS62WV2568ALL-70BLI	mini BGA (6mm x 8mm), Lead-free
70	IS62WV2568ALL-70HI	sTSOP, TYPE I
70	IS62WV2568ALL-70HLI	sTSOP, TYPE I, Lead-free

**IS62WV2568BLL (2.5V - 3.6V)**
**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
70	IS62WV2568BLL-70T	TSOP, TYPE I
70	IS62WV2568BLL-70B	mini BGA (6mm x 8mm)
70	IS62WV2568BLL-70H	sTSOP, TYPE I

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
45	IS62WV2568BLL-45TLI	TSOP, TYPE I, Lead-free
45	IS62WV2568BLL-45BLI	mini BGA (6mm x 8mm), Lead-free
45	IS62WV2568BLL-45HLI	sTSOP, TYPE I
55	IS62WV2568BLL-55TI	TSOP, TYPE I
55	IS62WV2568BLL-55TLI	TSOP, TYPE I, Lead-free
55	IS62WV2568BLL-55BI	mini BGA (6mm x 8mm)
55	IS62WV2568BLL-55BLI	mini BGA (6mm x 8mm), Lead-free
55	IS62WV2568BLL-55HI	sTSOP, TYPE I
55	IS62WV2568BLL-55HLI	sTSOP, TYPE I, Lead-free
70	IS62WV2568BLL-70TI	TSOP, TYPE I
70	IS62WV2568BLL-70BI	mini BGA (6mm x 8mm)
70	IS62WV2568BLL-70HI	sTSOP, TYPE I



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183



32L 8x13.4mm TSOP-1  
Package Outline

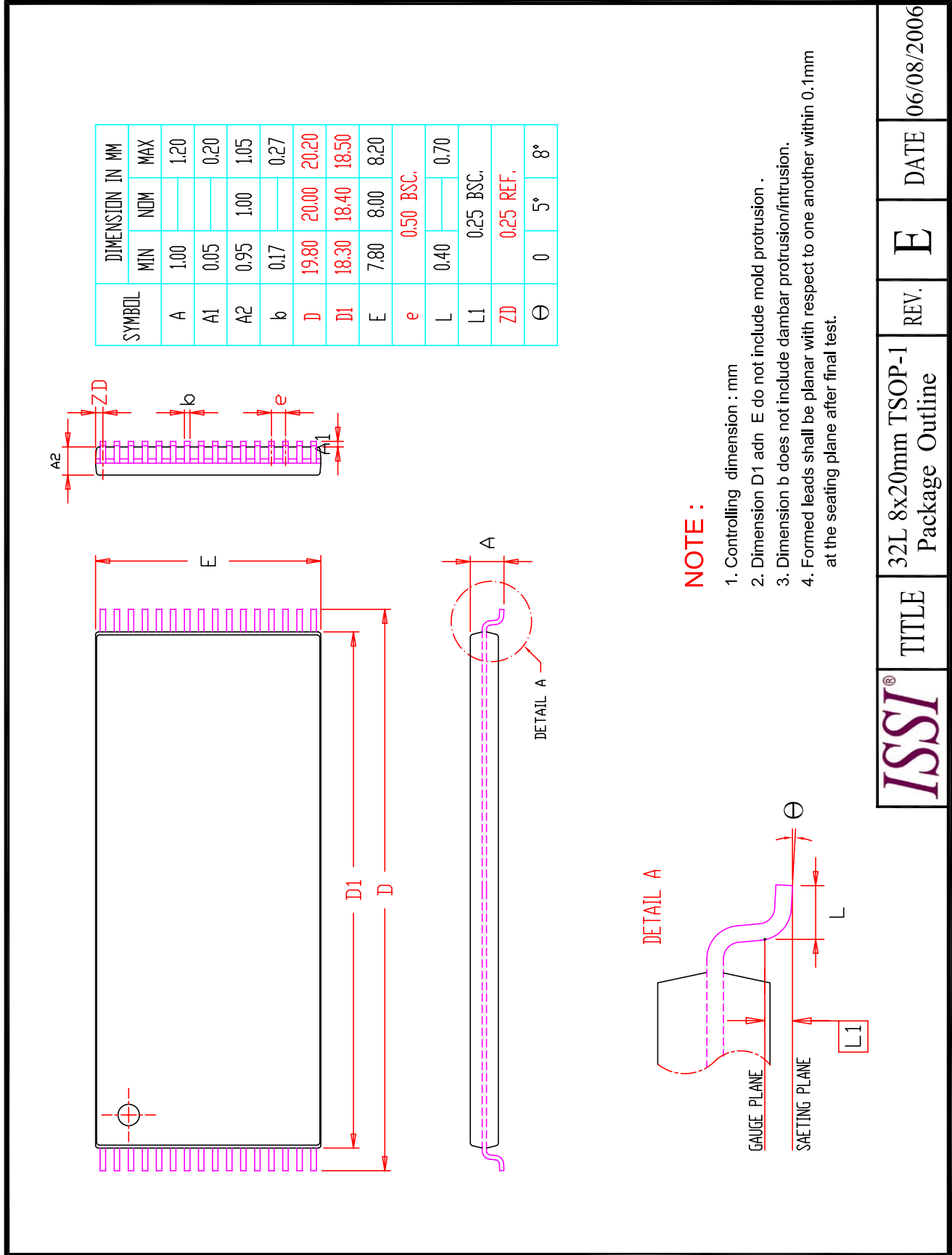
TITLE

REV.

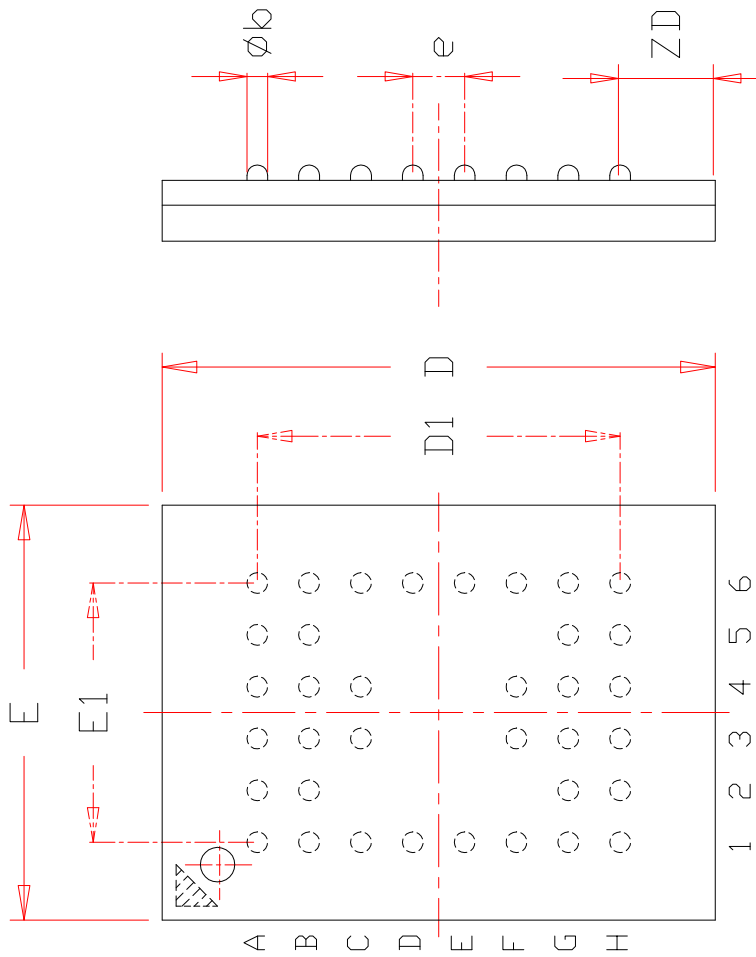
E

DATE

04/24/2009



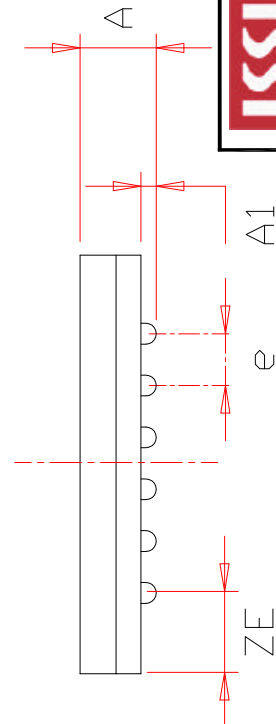
TOP VIEW



**NOTE :**

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	NOM.	MAX.	
A			1.20	0.047
A1	0.20		0.30	0.008
$\phi b$	0.30	0.35	0.40	0.012
D	7.90	8.00	8.10	0.311
D1	5.25	BSC.	0.207	BSC.
E	5.90	6.00	6.10	0.232
E1	3.75	BSC.	0.148	BSC.
e	0.75	BSC.	0.030	BSC.
ZD	1.375	REF.	0.054	REF.
ZE	1.125	REF.	0.044	REF.



	TITLE	36/48L 6x8mm TF-BGA Package Outline	REV.	E	DATE	08/12/2008
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- ✓ Excess Inventory Management