THE DATASHEET OF

IRS25411SPBF

IRS25411S

Synchronous buck LED driver

Features

- 600 V high side/low side gate drive outputs
- Switching frequency up to 500kHz
- 500mA source/700mA sink gate drive outputs
- Hysteretic or slave mode operation
- Logic level enable input
- PWM dimmable
- SO8 package

Potential applications

- High voltage current regulated synchronous buck LED drivers

Product validation

Qualified for applications listed above based on the test conditions in the relevant tests of JEDEC20/22

Description

The IRS25411 is a half-bridge driver for current regulated synchronous buck regulators typically used in high voltage output non-isolated LED drivers.

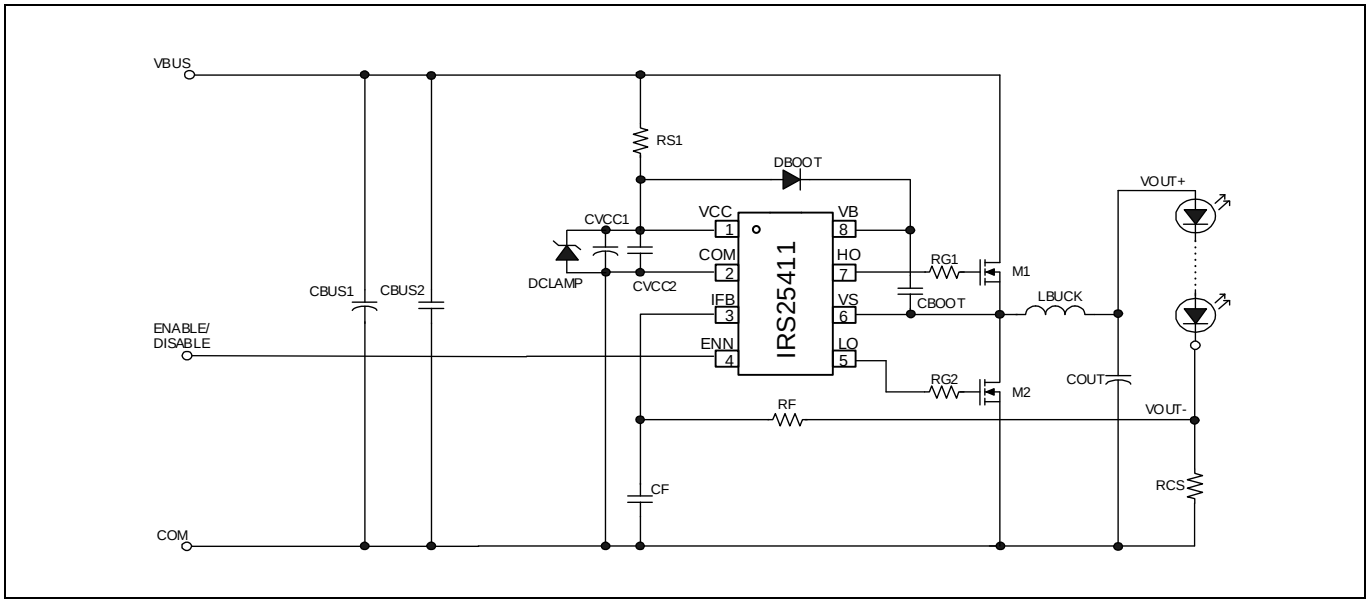

Figure 1 Typical schematic

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1 Maximum ratings

1.1 Absolute maximum ratings

Table 1 Maximum electrical ratings

Symbol	Definition	Minimum	Maximum	Units
V_B	Floating high side bias supply voltage	-0.3	625	V
V_S	Floating high side reference voltage	-0.3	V_B + 0.3V	V
V_{HO}	Floating gate drive output voltage	V_B - 0.3V	V_B + 0.3V	V
V_{LO}	Low side output voltage	-0.3	V_{CC}+0.3	V
V_{IFB}	Feedback input voltage	-0.3	V_{CC}+0.3	V
V_{ENN}	Enable input voltage	-0.3	V_{CC}+0.3	V
V_{CC}	Bias supply voltage	-0.3	V_{CLAMP}[1]	V
I_{CC}	Supply current	-20	20	mA
dV_S/dt	Half-bridge node slew rate	-50	50	V/ns

Table 2 Maximum thermal ratings

Symbol	Definition	Minimum	Maximum	Units
P_D	Package power dissipation at $T_A \leq 25°C$ (SO8) $P_D = (T_{JMAX} - T_A)/R_{THJA}$		0.625	W
$R_{\theta JA}$	Thermal resistance, junction to ambient (SO8)		200	°C/W
T_J	Junction temperature	-55	150	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temperature during soldering (10 seconds)		300	°C

1.2 Recommended operating conditions

Table 3 Recommended operating conditions

Symbol	Definition	Minimum	Maximum	Units
V_{BS}	High side floating supply voltage	V_{CC} – 0.7	V_{CLAMP}	V
V_S	Steady state floating high side offset voltage	-1	600	V
V_{CC}	Bias supply voltage	VCCUV+	VCLAMP	V
I_{CC}	Supply current		10	mA
f_S	Switching frequency	10	500	kHz
T_J	Junction temperature	-25	125	°C

[1] This IC contains an internal zener diode clamp from VCC to COM. The clamp voltage is referred to as V_{CLAMP}.

2 Electrical characteristics

V_{CC} = V_{BS} = 14 V +/- 0.25 V, C_{LO}=C_{HO}=1000 pF, C_{VCC}=C_{VBS}=0.1 µF, T_A=25 °C unless otherwise specified.

Table 4 Bias supply characteristics

Symbol	Definition	Minimum	Typical	Maximum	Units
V_{CLAMP}	V_{CC} clamp voltage	14.6	15.6	16.6	V
V_{CCUV+}	V_{CC} turn on threshold	8.0	9.0	10.0	V
V_{CCUV-}	V_{CC} turn off threshold	6.5	7.5	8.5	V
$V_{CCUVHYS}$	V_{CC} threshold hysteresis	1.0	1.5	2.0	V
I_{QCCUV}	Low V_{CC} bias current		50	150	µA
I_{QCCENN}	Disabled (sleep) mode bias current		1.0	2.0	mA
I_{QCC}	VCC quiescent current (no switching)		1.0	2.0	mA
I_{QCC50k}	Supply current at 50kHz switching		2.0	3.0	mA

Table 5 Floating bias supply characteristics

Symbol	Definition	Minimum	Typical	Maximum	Units
$V_{CLAMPHS}$	V_B-V_S clamp voltage	24.4	26.0	27.6	V
V_{BSUV+}	V_{BS} turn on threshold	6.5	7.5	8.5	V
V_{BSUV-}	V_{BS} turn off threshold	6.0	7.0	8.0	V
I_{QBS0}	V_{BS} supply current, V_{HO} low		0.05	1.0	mA
I_{QBS1}	V_{BS} supply current, V_{HO} high (V_{IFB} = 0 V)		1.0	2.0	mA
I_{LK}	Offset leakage current (V_B = V_S = 600 V)		1	50	µA

Table 6 Control characteristics

Symbol	Definition	Minimum	Typical	Maximum	Units
V_{ENNTH+}	Enable input positive threshold (disable)	2.5	2.7	3.0	V
V_{ENNTH-}	Enable input negative threshold (enable)	1.7	2.0	2.3	V
$V_{0.5}$	Internal voltage reference	490	500	510	mV
V_{IFBTH}	IFB input threshold	455	500	540	mV
t_{LO-ON}	Propagation delay, V_{IFB}>V_{IFBTH} to LO high		320		ns
t_{LO-OFF}	Propagation delay, V_{IFB}<V_{IFBTH} to LO low		180		ns
t_{HO-ON}	Propagation delay, V_{IFB}<V_{IFBTH} to HO high		320		ns
t_{HO-OFF}	Propagation delay, V_{IFB}>V_{IFBTH} to HO low		180		ns

Table 7 Gate drive output characteristics

Symbol	Definition	Minimum	Typical	Maximum	Units
V_{OL}	Low state gate drive voltage		0		V
V_{OH}	High state gate drive voltage		V_{CC}		V
I_{O+}	Gate drive source current		0.5		A
I_{O-}	Gate drive sink current		0.7		A
t_f	Turn off fall time		50	120	ns
t_r	Turn on rise time		30	50	ns
t_{DT}	Dead time (low to high/high to low)		140		ns

Table 8 Bootstrap re-charger[1] characteristics

Symbol	Definition	Minimum	Typical	Maximum	Units
t_{WD}	Bootstrap capacitor re-charge wait time (V_{IFB} = 1 V, LO output low)		20.0		µs
t_{WDCH}	Boot strap capacitor re-charge pulse time (V_{IFB} = 1 V, LO output high)		1.0		µs

[1] This circuit periodically re-charges the bootstrap capacitor (C_{BOOT}) when the output is in the low state for a period > t_{WD}. This ensures that the capacitor does not discharge, which would prevent the high side output from operating.

3 Functional description

3.1 Internal block diagram and pin functions

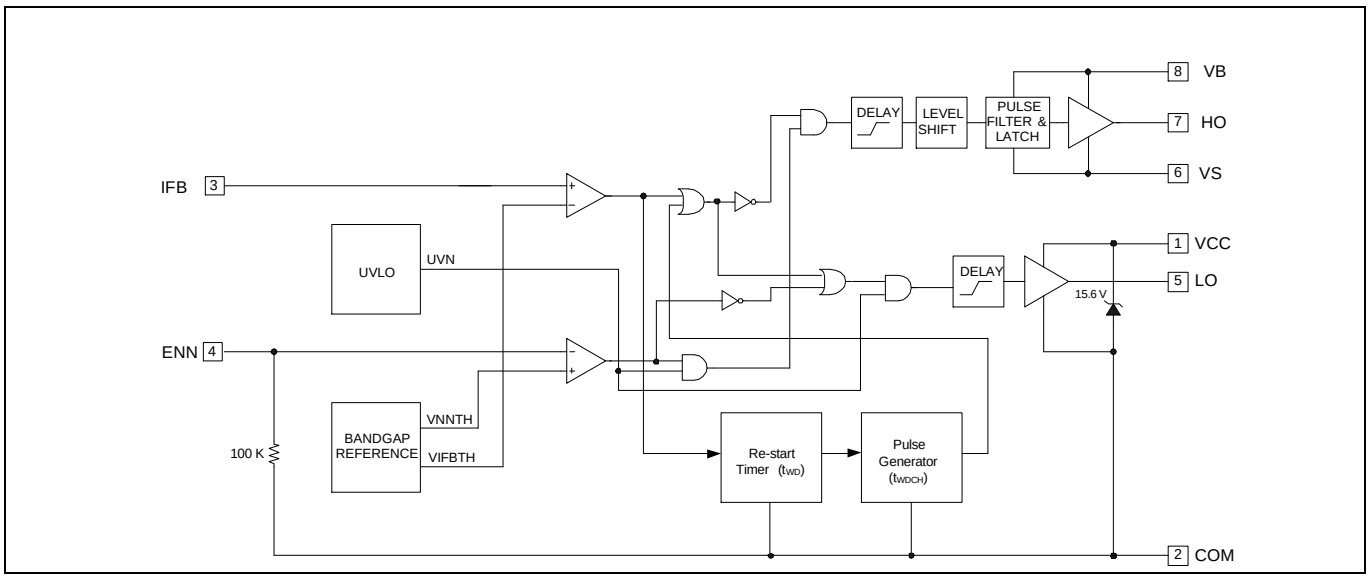


Figure 2 Internal block diagram

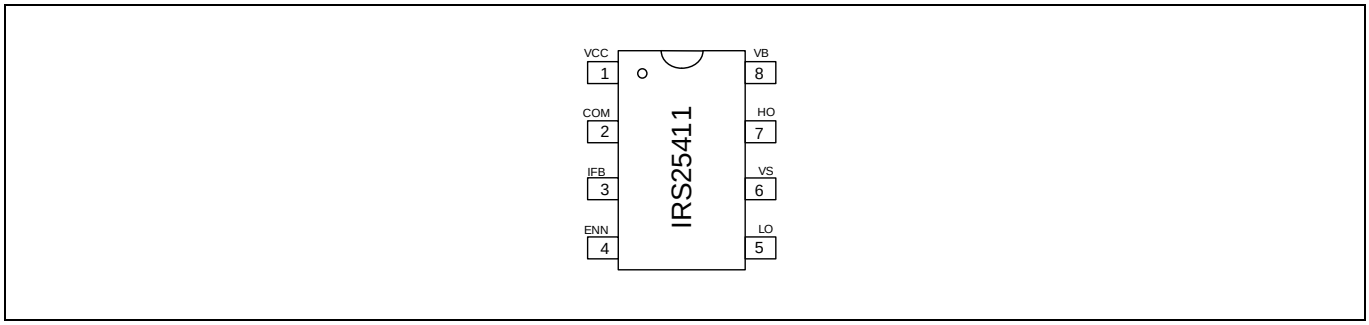


Figure 3 Pin assignments

Table 9 Pin functions

Pin	Symbol	Description
1	VCC	Supply voltage
2	COM	0 V return
3	IFB	Current feedback (hysteretic)
4	ENN	Enable/disable input (high to disable, LO=High and HO=Low)
5	LO	Low side gate drive output
6	VS	Half bridge node, floating high side return
7	HO	High side gate drive output
8	VB	High side gate drive floating supply

3.2 Operation

The IRS25411 is a time-delayed hysteretic current regulated synchronous[1] buck controller. The output current is sensed through a 0V referenced shunt resistor from which the voltage (V_{IFB}) is fed back to the IFB pin voltage and compared to an internal high precision bandgap voltage reference (V_{IFBTH}). The high and low side gate drive outputs (HO and LO) change state as V_{IFB} rises above and falls below V_{IFBTH}. A fixed dead time (t_{DT}) is provided to prevent shoot though due to overlapping switching transitions of the MOSFETs.

Once the V_{CC} supply to the IC rises above the under-voltage lockout positive threshold (V_{CCUV+}), the LO output transitions high while the HO output is low for a predetermined period of time to pre-charge the bootstrap capacitor (C_{BOOT}) connected externally between the VB and VS pins. This establishes the V_{BS} floating supply voltage required for the high-side gate driver, without which the buck regulator would never be able to start up. The recommended capacitor type for C_{BOOT} is a 0.1 µF at 25 V ceramic. The bootstrap diode D_{BOOT} must be rated at 600 V, 1 A and must be a fast recovery type, t_{rr} < 50 ns is recommended.

In this configuration the high side MOSFET (M1) in the on state delivers power from the input to the output via the buck inductor. The low side MOSFET (M2) is switched on when M1 is off to provide a low resistance path for the re-circulating inductor current thus eliminating the diode conduction losses that occur in a standard buck converter. C_{BOOT} is replenished every switching cycle while LO is high connecting VS to 0V/COM through M2.

It is not permissible for HO to be high continuously because if that were the case the charge on C_{BOOT} would eventually leak away and V_{BS} would fall below the minimum threshold required for high side gate drive operation. To prevent this from occurring the IRS25411 includes an internal re-charge timer that forces HO to switch off and LO to switch on for a short pulse after a period of t_{WD} despite V_{IFB} being below V_{IFBTH}. The length of this bootstrap re-charge pulse is t_{WDCH} after which HO and LO revert to their previous states. This process is repeated indefinitely thereby preventing the buck regulator to operate at 100% duty cycle.

3.2.1 Basic operation

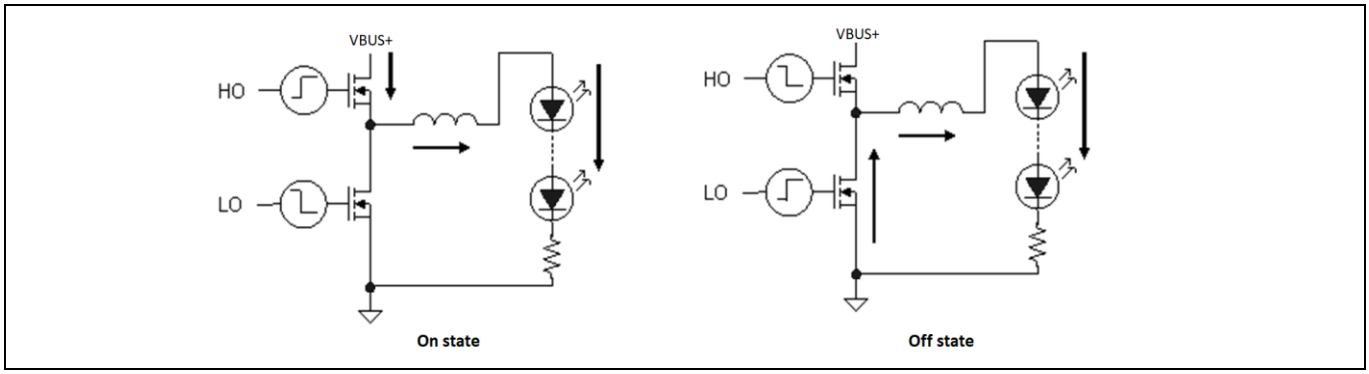


Figure 4 Synchronous buck operation

During normal operation V_{IFB} rises and falls above and below V_{IFBTH} to regulate the output current through the buck inductor. An RC filter (RF and CF) is required at the IFB input to avoid false triggering, which can occur due to noise coupling. This filter also introduces a delay (t_{RC}) that limits the switching frequency.

As V_{IFB} rises above V_{IFBTH}, HO switches high to low (M1 off) after a propagation delay of t_{HO-OFF} plus t_{RC}. When M1 switches off, LO switches low to high (M2 on) after the dead-time (DT). The buck inductor then releases stored energy into the load as the current falls and V_{IFB} decreases. When V_{IFB} drops below V_{IFBTH} again LO switches low

[1] A synchronous buck converter utilizes a second MOSFET in place of the buck diode in order to eliminate diode conduction losses.

after a delay of t_{HO-ON} plus t_{RC} and HO switches high after a delay of t_{HO-ON} plus t_{RC} plus t_{DT}. The hysteretic buck converter operates in continuous conduction mode (CCM). This hysteretic switching operation continues to regulate the average current as follows:

$$I_{OUT(AVG)} = \frac{V_{IFBTH}}{R_{CS}} \quad [1]$$

The high and low gate drive and feedback are illustrated below:

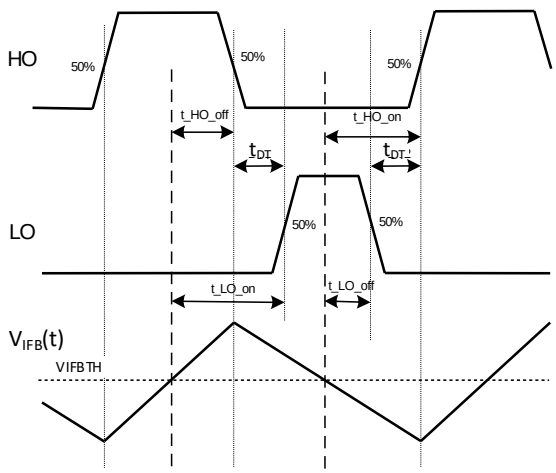


Figure 5 Hysteretic operation

3.2.1.1 Switching frequency and duty cycle

Since the IRS25411 operates hysteretically without a built in oscillator, the switching frequency and duty cycle will vary as the feedback signal $V_{IFB}(t)$ rises and falls across the threshold V_{IFBTH}. The rise and fall slopes of the sensed current depend on the input voltage, the output voltage and the inductor value (LBUCK). The IFB input RC filter delay t_{RC} combined with the internal propagation delays will determine the amount of overshoot and undershoot and therefore the peak to peak current ripple. Higher ripple occurs with lower inductor values since the effect of these delays increases. With higher ripple the average output current will vary more with line and load changes. Higher switching frequency offers better regulation accuracy but reduced efficiency.

The standard current sensing arrangement is shown in figure 1. In this case the current sensed is not equal to the inductor since some of the ripple bypasses the load through the output capacitor. It is also possible to locate RCS differently to also include the ripple component from the output capacitor effectively sensing the inductor current.

The switching frequency varies depending on input and voltages as well as inductance and load current. This is not easy to calculate accurately and therefore a design approach based on simulation and physical circuit optimization in a lab is required.

3.2.2 ZVS operation

In order to realize an efficient high voltage buck regulator, it becomes necessary to implement zero voltage switching of the MOSFETs (ZVS). Buck regulators operating in CCM exhibit hard switching during switch on of the MOSFETs. This results in switching losses that increase with bus voltage and frequency. In a back end

converter stage operating from a front end PFC DC bus voltage in the region of 400 V the efficiency is limited by switching losses, which can only be reduced so far by limiting the frequency. To get around this, it is possible to operate the converter in discontinuous mode, which can be done by reducing the inductor value and/or increasing the feedback RC filter delay so that the inductor current falls to zero during the off period. The downside is that, since the inductor ripple is now very high, it becomes necessary to add an electrolytic capacitor at the output to remove the ripple component from the output current driving the LED load.

3.2.3 Enable/disable input (ENN)

The ENN input when raised above the V_{ENNTH+} threshold forces the IRS25411 into the disabled/standby state where HO is low and LO is high regardless of the voltage level at V_{IFB}. LO remains high to ensure that C_{BOOT} remains fully charged ready for the controller to re-start when the ENN input is reduced below V_{ENNTH-}. The ENN input is internally pulled down to zero so that the controller remains enabled if the ENN pin is left floating.

3.2.3.1 PWM dimming through the ENN input

For PWM burst mode dimming operation a signal with constant frequency and adjustable duty cycle may be applied to the ENN input. An inverse linear relationship exists between the average load current and duty cycle of this input, i.e. if the ratio is 50% then 50% of the maximum set light output will be realized. A frequency of at least 2 kHz is recommended for the dimming control signal to avoid noticeable flicker/strobe effects and to meet flicker index limits. When utilizing the IRS25411 in this way a diode and optional series resistor should be connected from the ENN input to the IFB input (cathode to IFB) so that when ENN is high and the converter is disabled the IFB input is held above V_{IFBTH}. This is required to properly clear the re-charge timer and eliminate possible flicker at very low dimming levels.

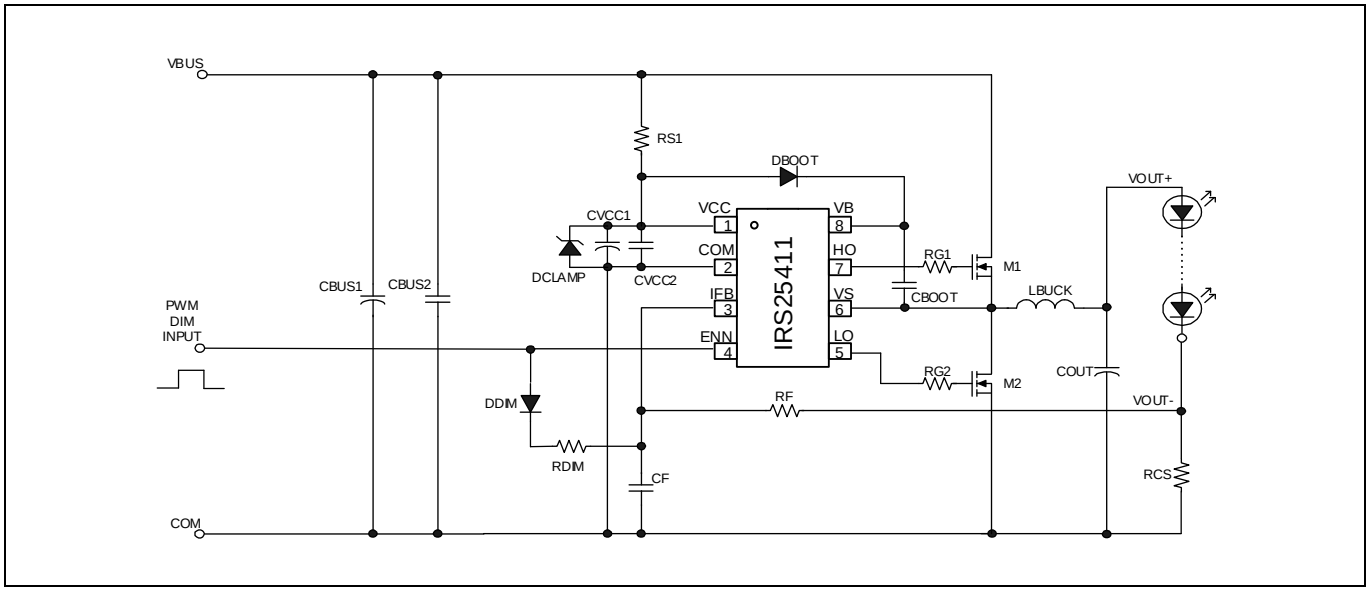


Figure 6 Burst mode/PWM dimming circuit configuration

In practice the minimum dimming level possible is limited by the length of the dimming burst in relation to the switching frequency. To prevent flicker there should be several switching cycles within the on burst at the minimum dimming level. This may require a PWM frequency below 2 kHz or a higher switching frequency than desired.

PWM dimming is further limited in designs with an electrolytic capacitor at the output because the hold up from this capacitor tends to limit the minimum possible dimming level.

For these reasons the IRS25411 is not recommended for dimming to very low levels except in low voltage applications where CCM operation is used.

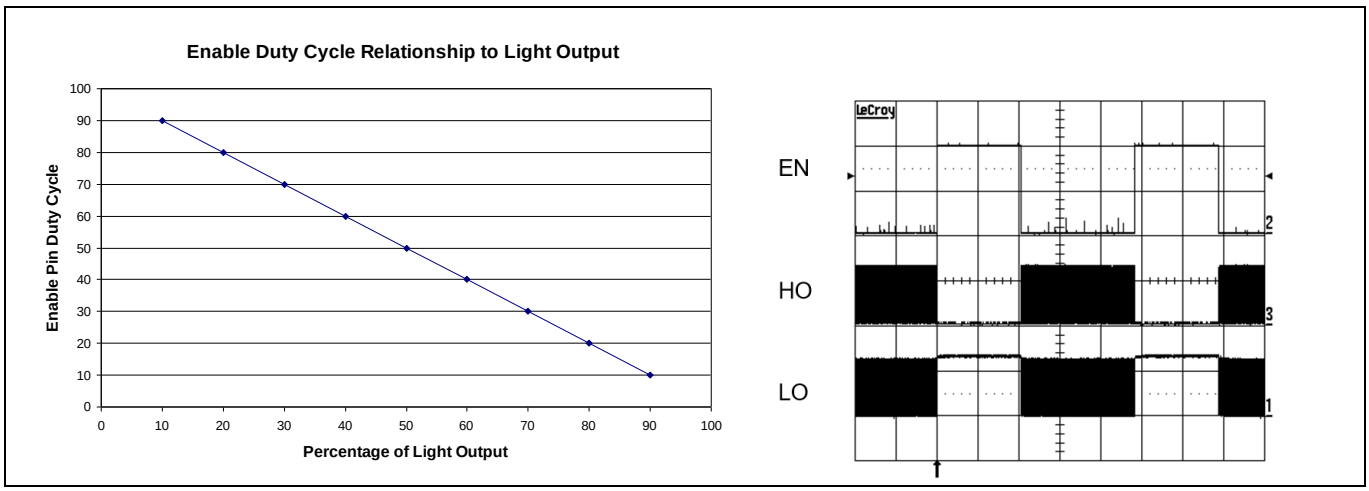


Figure 7 Light output vs ENN input duty cycle and waveforms

3.2.3.2 Adjustable output current

In applications where different values of output current are desired by external selection. The recommended method is to use various options for the current sense resistor (RCS), which can be connected as needed.

3.2.3.3 Linear current dimming

As an alternative to PWM/burst mode dimming, the IRS25411 may also be used in linear dimming mode. In this case the output current remains continuous with a level adjustable from an analog control voltage. The output current level is reduced as the voltage at the analog dimming input is increased. This provides a DC offset to the feedback signal, which is dependent on the ratio of RF and RDIM. A control voltage of 0V will allow the output current to regulate at maximum and when the voltage is increased to a certain level, will reduce the output current to zero. The output current will be linearly controlled according to the input current introduced into the RDIM/RFB (IFB) node. This analog dimming input may be used separately or in conjunction with the PWM dimming control in order to achieve wider dimming range. An input control voltage range of 0V to 3.3V would enable the output current to be controlled by a PWM output from an XMC microcontroller and converted to DC through an RC integrator.

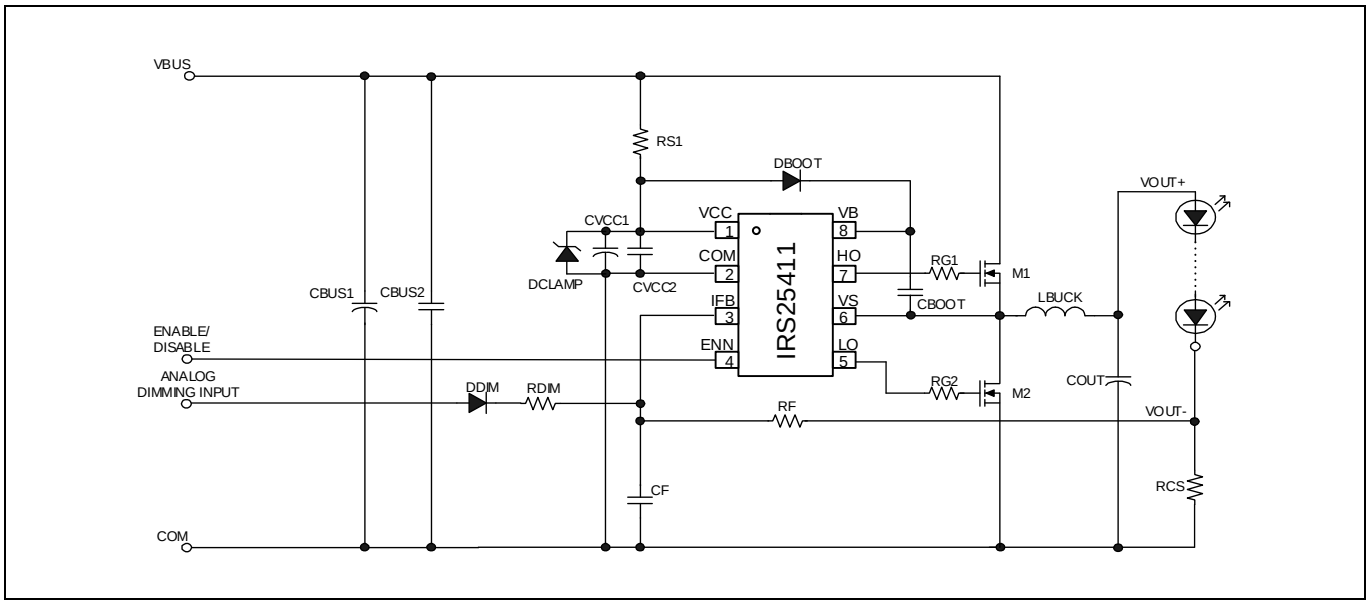


Figure 8 Linear dimming circuit

3.2.4 Slave mode operation

Should the application require more precise control of the switching frequency, the IRS25411 may also be used in slave mode. This is done by supplying the IFB input from an externally generated fixed frequency oscillating voltage signal with a DC offset. This signal may be triangular, sinusoidal or rectangular provided that it rises above and below V_{IFBTH}. As the DC offset is increased HO will become shorter and LO will become longer thus reducing the converter duty cycle while the frequency remains fixed. When the offset is reduced the opposite will occur increasing the converter duty cycle. The figure below illustrates a triangular waveform with a DC offset intersecting V_{IFBTH} to produce LO and HO gate drive outputs.

Slave mode operation may be used to more accurately regulate the output current or voltage by means of external control circuitry. In this configuration a feedback circuit produces an error voltage that can added to the oscillating signal that sets the switching frequency, which can be connected to the IFB input.

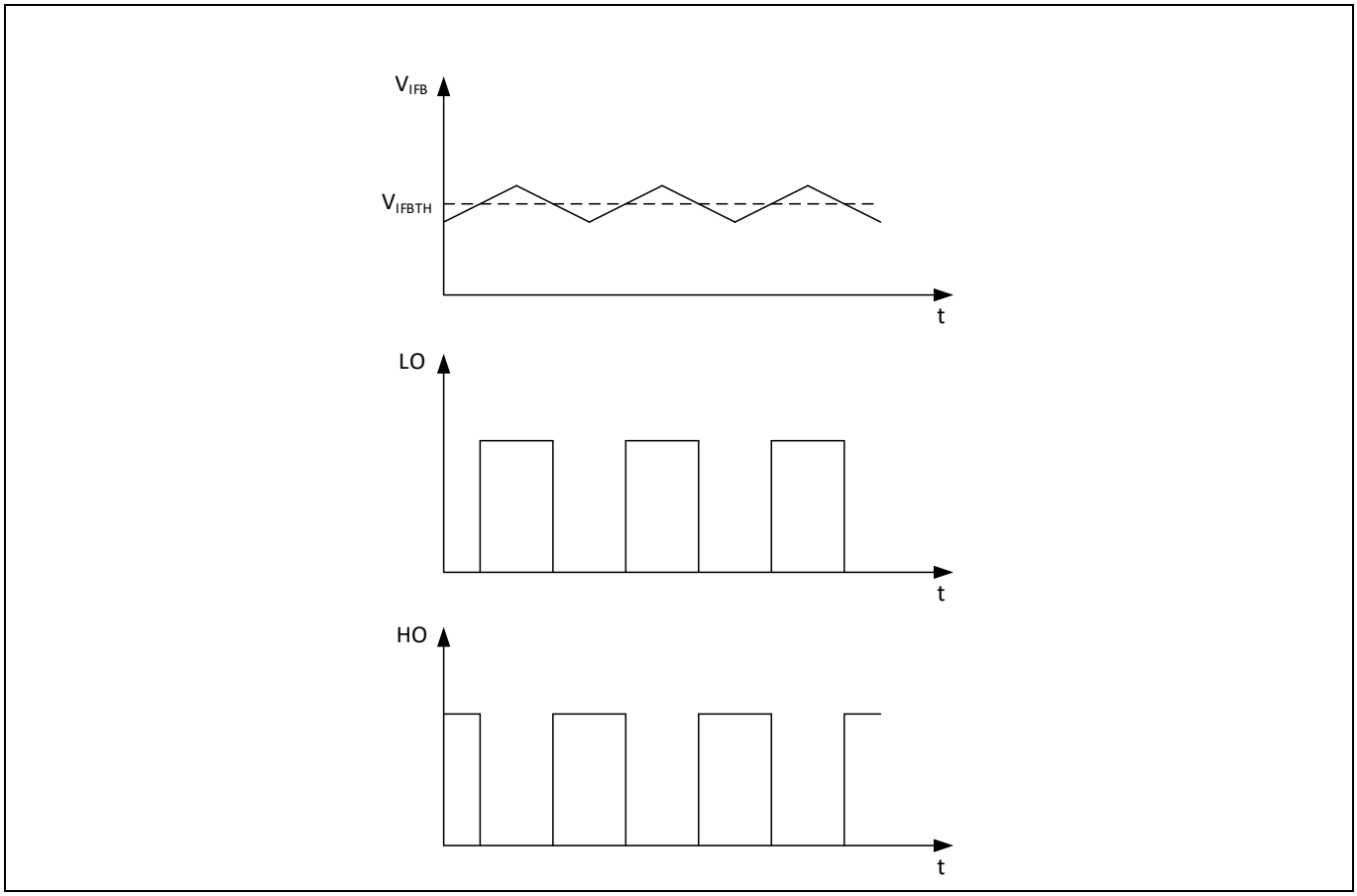


Figure 9 External switching control

3.2.5 IRS25411 state diagram

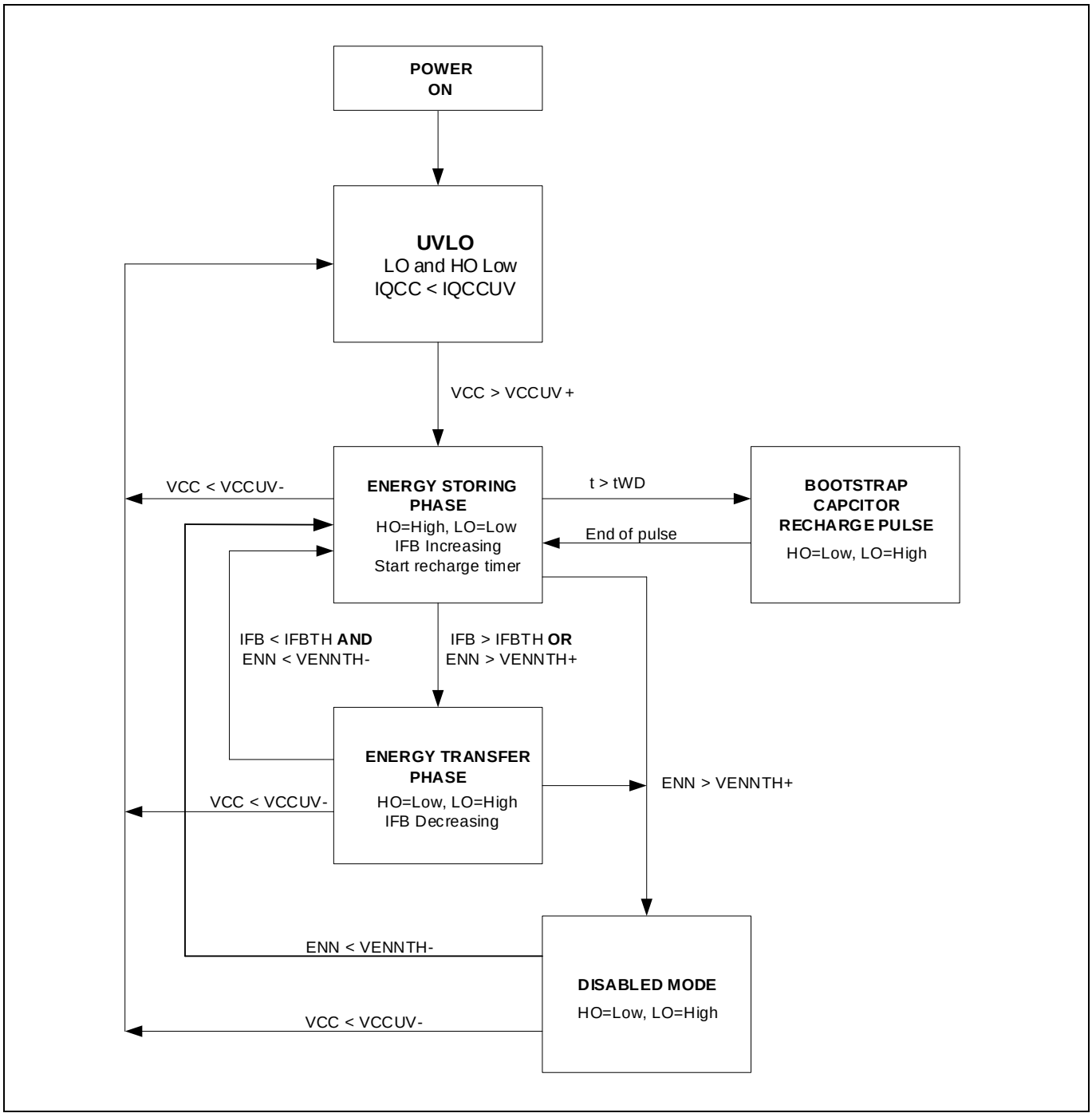


Figure 10 State diagram

3.3 PCB layout guidelines

To operate correctly the IRS25411 requires careful placement of components and layout of PCB traces. The following guidelines must be followed:

1. A decoupling capacitor (typically 0.1 µF, 25 V SMD ceramic) must be placed between the VCC and COM pins (1 and 2) as shown by CVCC in the layout example below.
2. The filter capacitor (CF) should be located as close as possible to the IFB input (pin 3) and COM (pin 2) with the shortest possible traces.
3. Traces connecting to the IFB pin must be kept as far as possible from the VS, HO and VB pins. It is recommended not to pass these traces under the IC.
4. The filter resistor (RF) should also be located close to the IFB pin if possible, however this is less critical.
5. The VS, HO and VB pins (6, 7 and 8) carry high voltage switching signals with fast rise and fall times, therefore traces connected to these pins need to be appropriately distanced from other circuit traces for clearance and to avoid noise propagation that could interfere with correct circuit operation.
6. Since the LO and VS pins are close together designers may choose to include extra HV isolation by routing a narrow slot in the PCB between these pins, adding coating or potting.
7. Under no circumstances should traces be routed between the VS, HO, VB and LO pins!
   This is also not recommended for the VCC, COM, IFB and ENN pins.
8. The bootstrap capacitor (CB) should be located close to the VB and VS pins allowing sufficient high voltage clearance from other circuit traces.
9. The bootstrap diode (DB) should be located close to the VCC and VB pins allowing sufficient high voltage clearance between the cathode and other circuit traces.
10. Traces should not be passed under DB as this reduces clearance distances.

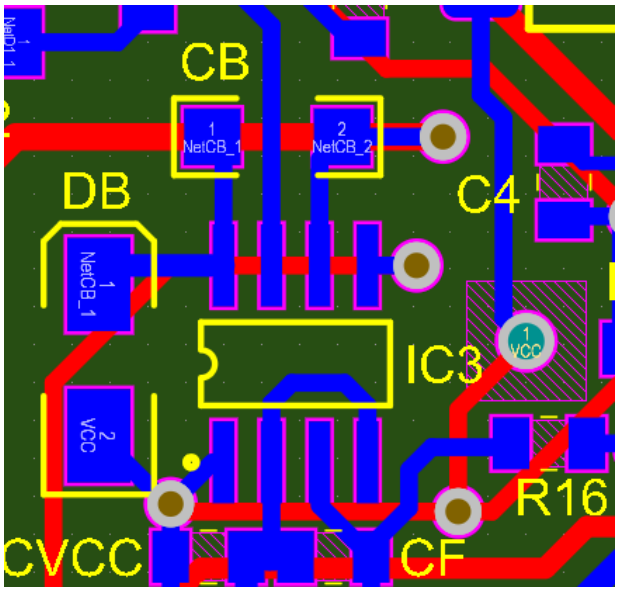
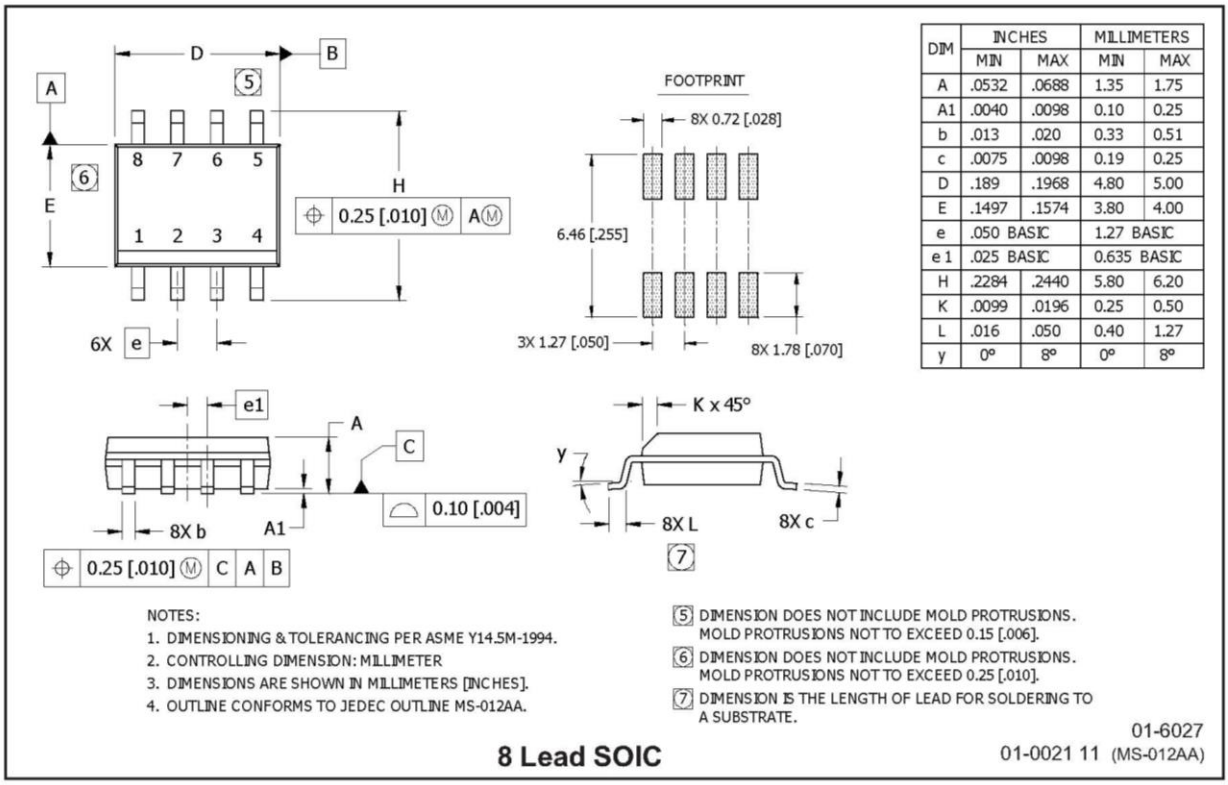


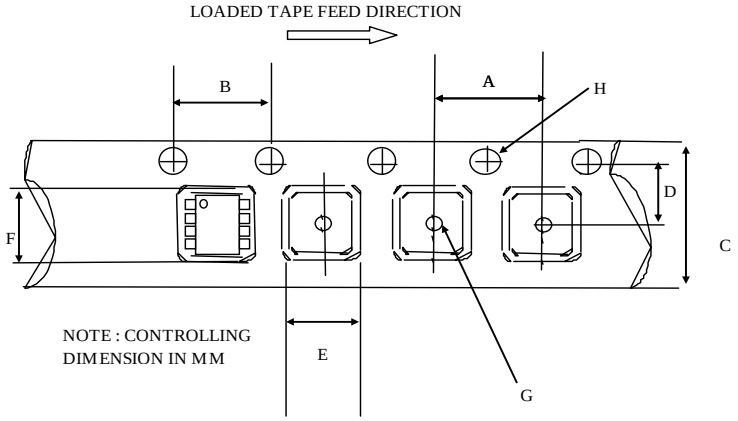
Figure 11 IRS25411 correct layout example

4 Package and marking



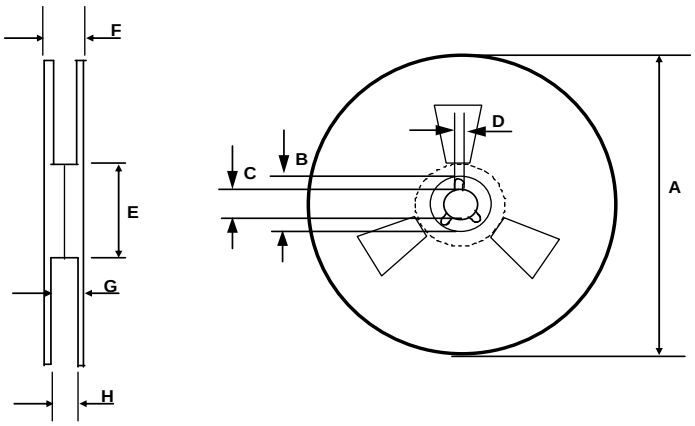
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

Figure 12 Package details



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 13 Tape and reel details

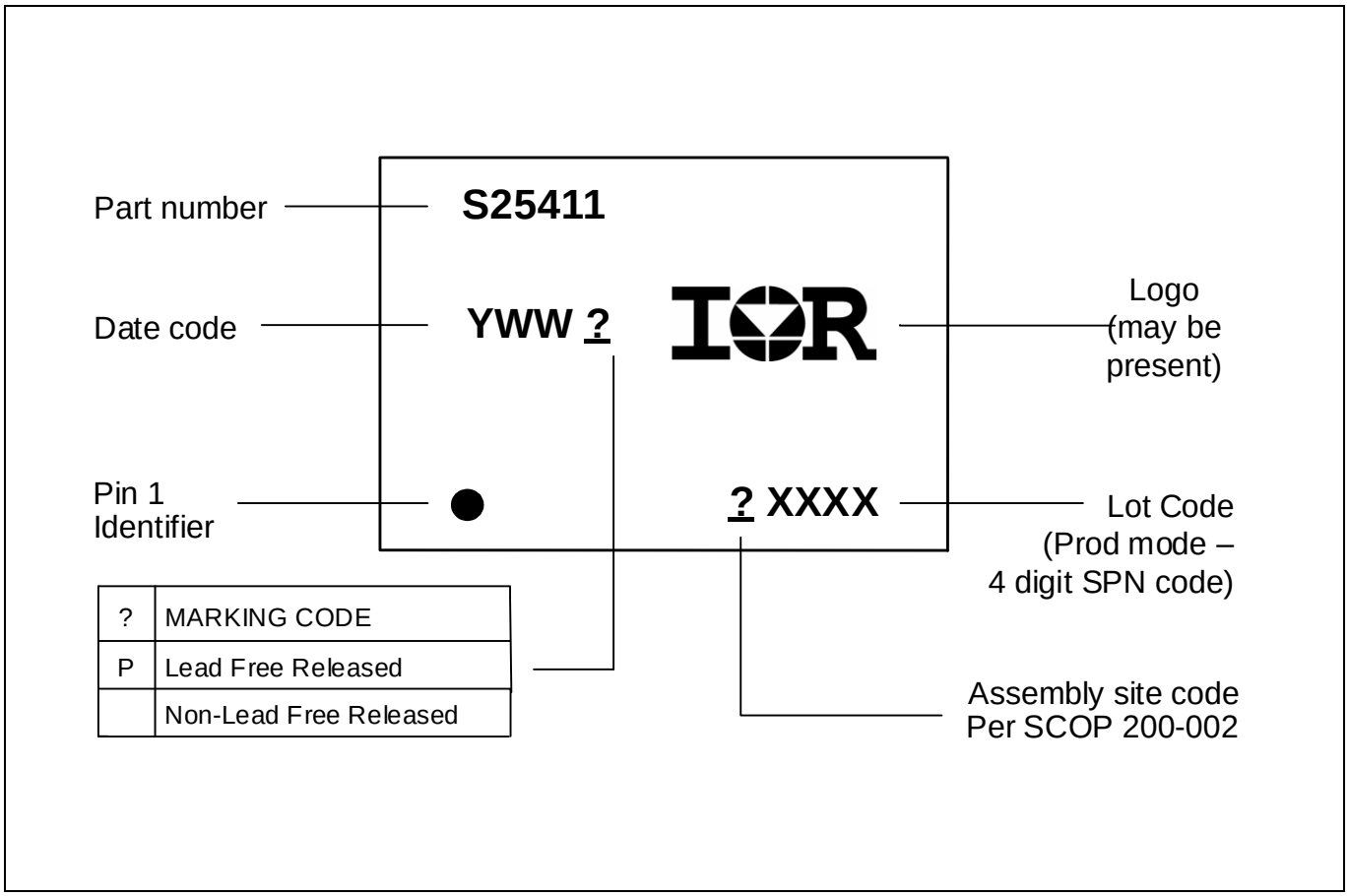


Figure 14 Part marking information

Revision history

Document version	Date of release	Description of changes
2.0.0	Feb 8, 2019	Updated datasheet replaces original IR version

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