THE DATASHEET OF

ISL6363IRTZ

ISL6363

Multiphase PWM Regulator for VR12™ Desktop CPUs

FN6898
Rev 1.00
Sep 5, 2013

Fully compliant with VR12™ specifications, the ISL6363 provides a complete solution for microprocessor core and graphics power supplies. It provides two Voltage Regulators (VRs) with three integrated gate drivers. The first output (VR1) can be configured as a 4, 3, 2 or 1-phase VR while the second output (VR2) is a 1-phase VR. The two VRs share a serial control bus to communicate with the CPU and achieve lower cost and smaller board area compared with a two-chip approach.

Based on Intersil's Robust Ripple Regulator R3 Technology™, the PWM modulator, compared to traditional modulators, has faster transient settling time, variable switching frequency during load transients and has improved light load efficiency with its ability to automatically change switching frequency.

The ISL6363 has several other key features. Both outputs support DCR current sensing with a single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. Both outputs come with remote voltage sensing, programmable V_{BOOT} voltage, serial bus address, IMAX, TMAX, adjustable switching frequency, OC protection and separate power-good indicators. To reduce output capacitors, the ISL6363 also has an additional compensation function for PS1/2 mode and high frequency load transient compensation.

Features

- Serial Data Bus (SVID)
- Dual Outputs:
  - Configurable 4, 3, 2 or 1-phase for the 1st Output with 2 Integrated Gate Drivers
  - 1-phase for the 2nd Output with Integrated Gate Driver
- Precision Core Voltage Regulation
  - 0.5% System Accuracy Over-Temperature
  - Enhanced Load Line Accuracy
- PS2 Compensation and High Frequency Load Transient Compensation
- Differential Remote Voltage Sensing
- Lossless Inductor DCR Current Sensing
- Programmable V_{BOOT} Voltage at Start-up
- Resistor Programmable Address, IMAX, TMAX for Both Outputs
- Adaptive Body Diode Conduction Time Reduction

Applications

- VR12 Desktop Computers

Related Literature

- ISL6363EVAL1Z User Guide

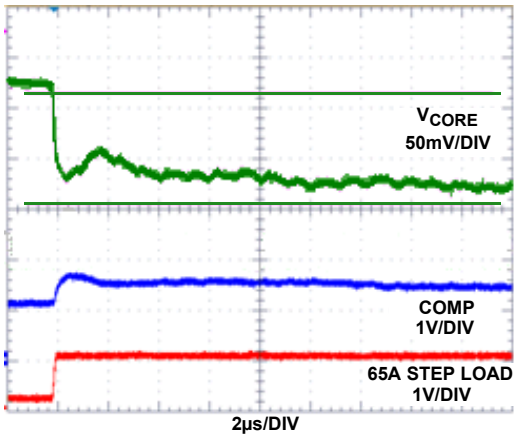


FIGURE 1. FAST TRANSIENT RESPONSE

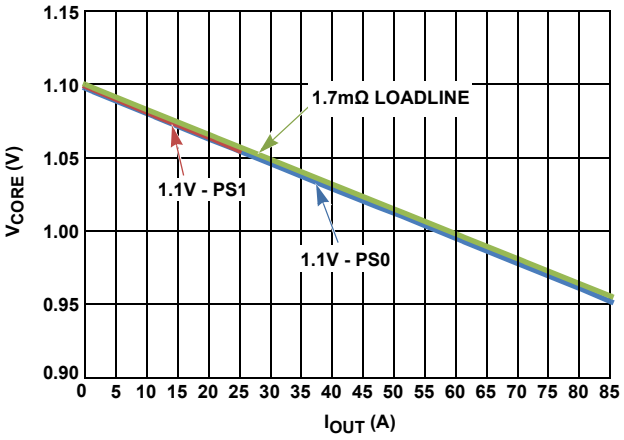


FIGURE 2. ACCURATE LOADLINE, V_{CORE} vs I_{OUT}

Ordering Information

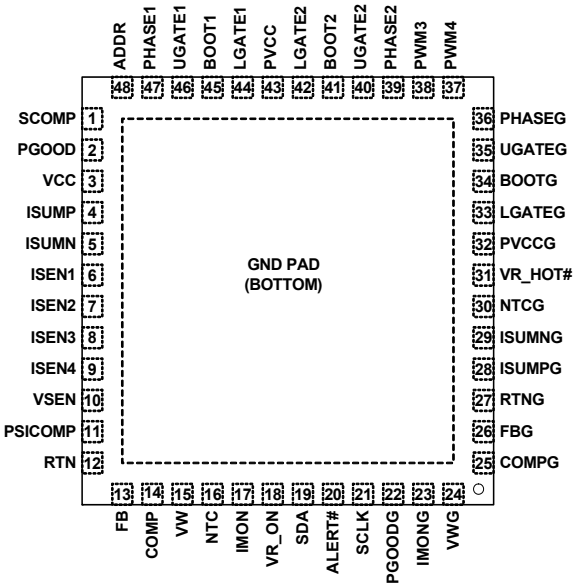
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6363CRTZ	ISL6363 CRTZ	0 to +70	48 Ld 6x6 TQFN	L48.6x6
ISL6363IRTZ	ISL6363 IRTZ	-40 to +85	48 Ld 6x6 TQFN	L48.6x6

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6363. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL6363
(48 LD TQFN)
TOP VIEW



Pin Descriptions

ISL6363	SYMBOL	DESCRIPTION
Bottom Pad	GND	Common ground signal of the IC. Unless otherwise stated, signals are referenced to the GND pin. The pad should also be used as the thermal pad for heat dissipation.
1	SCOMP	This pin is a placeholder for potential future functionality. This pin can be left floating.
2	PGOOD	Power-good open-drain output indicating when VR1 is able to supply a regulated voltage. Pull-up externally with a 680Ω resistor to +5V or 1kΩ to +3.3V.
3	VCC	+5V bias supply pin. Connect a high quality 0.1µF capacitor from this pin to GND and place it as close to the pin as possible. A small resistor (2.2Ω for example) between the +5V supply and the decoupling capacitor is recommended.
4, 5	ISUMP, ISUMN	VR1 current sense input pins for current monitoring, droop current and overcurrent detection.
6	ISEN1	VR1 phase 1 current sense input pin for phase current balancing.
7	ISEN2	VR1 phase 2 current sense input pin for phase current balancing.
8	ISEN3	VR1 phase 3 current sense input pin for phase current balancing.

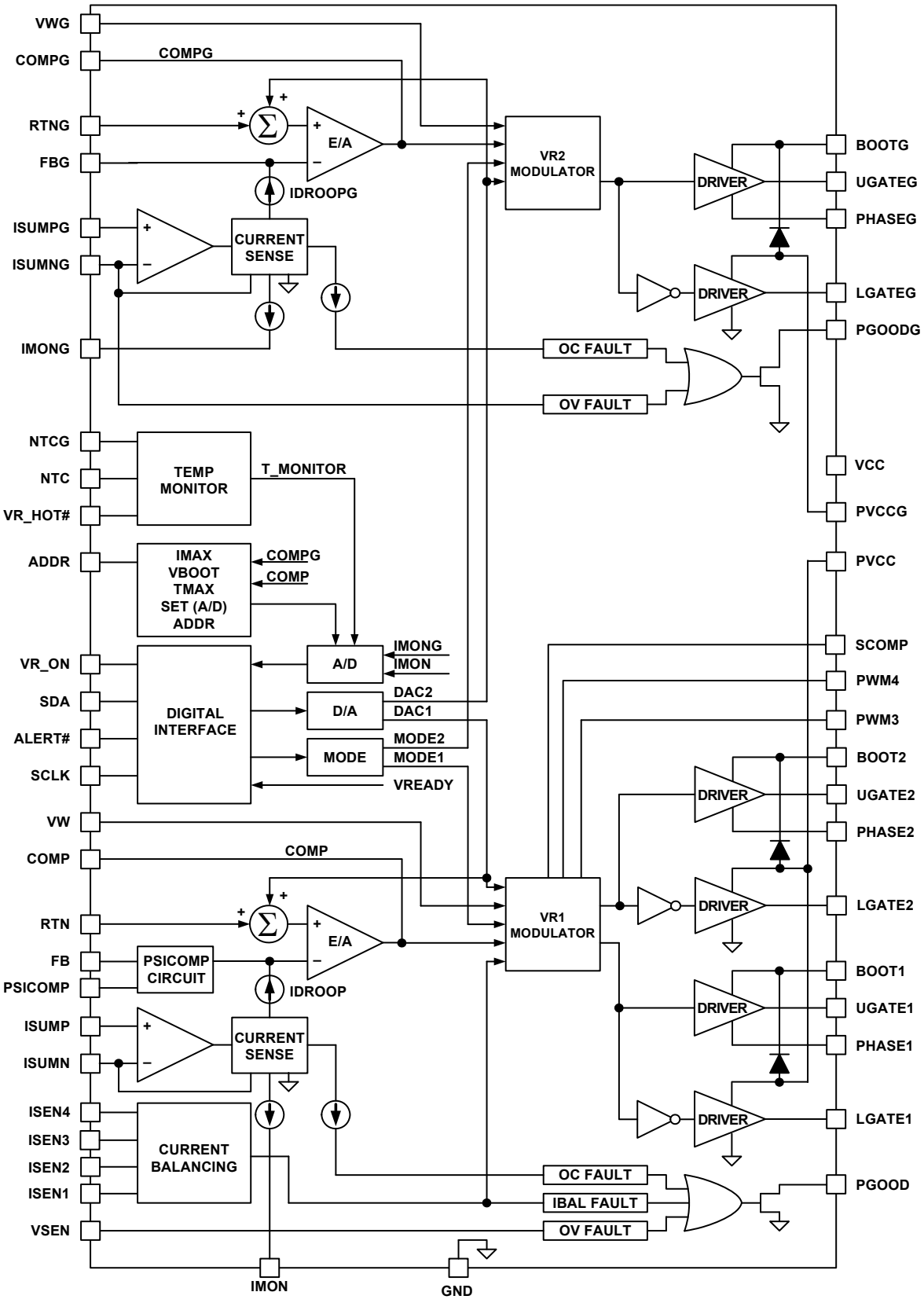
Pin Descriptions (Continued)

ISL6363	SYMBOL	DESCRIPTION
9	ISEN4	VR1 phase 4 current sense input pin for phase current balancing.
10	VSEN	VR1 remote core voltage sense input.
11	PSICOMP	This pin is used for improving transient response in PS2/3 mode of VR1 by switching in an additional type 3 compensation network to improve system gain and phase margin. Connect a resistor and capacitor from this pin to the output of VR1 near the feedback compensation network.
12	RTN	VR1 remote voltage sensing return input. Connect this pin to the remote ground sensing location.
13	FB	Inverting input of the error amplifier for VR1.
14	COMP	This is a dual function pin. This pin is the output of the error amplifier for VR1. A resistor connected from this pin to GND programs IMAX for VR1 and V_{BOOT} for both VR1 and VR2. Refer to Table 7 on page 28.
15	VW	A resistor from this pin to COMP programs the PWM switching frequency for VR1.
16	NTC	One of the thermistor network inputs to the thermal monitoring circuit used to control the VR_HOT# signal. Use this pin to monitor the temperature of VR1. Place the NTC close to the desired thermal detection point on the PCB.
17	IMON	Current monitoring output pin for VR1. The current sense signal from ISUMN and ISUMP is output on this pin to generate a voltage proportional to the output current of VR1.
18	VR_ON	Enable input signal for the controller. A high level logic signal on this pin enables the controller and initiates soft-start for VR1 and VR2.
19, 20, 21	SDA, ALERT#, SCLK	Data, alert and clock signal for the SVID communication bus between the CPU and VR1 and VR2.
22	PGOODG	Power-good open-drain output indicating when VR2 is able to supply a regulated voltage. Pull-up externally with a 680Ω resistor to +5V or 1.0kΩ to 3.3V.
23	IMONG	Current monitoring output pin for VR2. The current sense signal from ISUMNG and ISUMPG is output on this pin to generate a voltage proportional to the output current of VR2.
24	VWG	A resistor from this pin to COMPG programs the PWM switching frequency for VR1.
25	COMPG	This is a dual function pin. This pin is the output of the error amplifier for VR2. A resistor connected from this pin to GND programs IMAX for VR2 and TMAX for both VR1 and VR2. Refer to Table 8 on page 28.
26	FBG	Inverting input of the error amplifier for VR2.
27	RTNG	VR2 remote voltage sensing return input. Connect this pin to the remote ground sensing location.
28, 29	ISUMPG, ISUMNG	VR2 current sense input pin for current monitoring, droop current and overcurrent detection.
30	NTCG	One of the thermistor network inputs to the thermal monitoring circuit used to control the VR_HOT# signal. Use this pin to monitor the temperature of VR2. Place the NTC close to the desired thermal detection point on the PCB.
31	VR_HOT#	Open drain thermal overload output indicator.
32	PVCCG	Input voltage bias for the internal gate driver for VR2. Connect +12V to this pin. Decouple with at least a 1µF MLCC capacitor and place it as close to the pin as possible.
33	LGATEG	Output of the VR2 low-side MOSFET gate driver. Connect this pin to the gate of the VR2 low-side MOSFET.
34	BOOTG	Connect a MLCC capacitor from this pin to the PHASEG pin. The boot capacitor is charged through an internal boot diode connected from the PVCCG pin to the BOOTG pin.
35	UGATEG	Output of the VR2 high-side MOSFET gate drive. Connect this pin to the gate of the VR2 high-side MOSFET.
36	PHASEG	Current return path for the VR2 high-side MOSFET gate driver. Connect this pin to the node connecting the source of the high-side MOSFET, the drain of the low-side MOSFET and the output inductor of VR2.
37	PWM4	PWM output for phase 4 of VR1. When PWM4 is pulled to +5V VCC, the controller will disable phase 4 of VR1.
38	PWM3	PWM output for phase 3 of VR1. When PWM3 is pulled to +5V VCC, the controller will disable phase 3 of VR1.
39	PHASE2	Current return path for the VR1 phase 2 high-side MOSFET gate driver. Connect this pin to the node connecting the source of the high-side MOSFET, the drain of the low-side MOSFET and the output inductor of phase 2.
40	UGATE2	Output of the VR1 phase 2 high-side MOSFET gate drive. Connect this pin to the gate of the high-side MOSFET of phase 2.

Pin Descriptions (Continued)

ISL6363	SYMBOL	DESCRIPTION
41	BOOT2	Connect an MLCC capacitor from this pin to the PHASE2 pin. The boot capacitor is charged through an internal boot diode connected from the PVCCG pin to the BOOTG pin.
42	LGATE2	Output of the VR1 phase 2 low-side MOSFET gate driver. Connect this pin to the gate of the low-side MOSFET of phase 2.
43	PVCC	Input voltage bias for the internal gate drivers for VR1. Connect +12V to this pin. Decouple with at least a 1µF MLCC capacitor and place it as close to the pin as possible.
44	LGATE1	Output of the VR1 phase 1 low-side MOSFET gate driver. Connect this pin to the gate of the low-side MOSFET of phase 1.
45	BOOT1	Connect an MLCC capacitor from this pin to the PHASE1 pin. The boot capacitor is charged through an internal boot diode connected from the PVCC pin to the BOOT1 pin.
46	UGATE1	Output of the VR1 phase 1 high-side MOSFET gate drive. Connect this pin to the gate of the high-side MOSFET of phase 1.
47	PHASE1	Current return path for the VR1 phase 1 high-side MOSFET gate driver. Connect this pin to the node connecting the source of the high-side MOSFET, the drain of the low-side MOSFET and the output inductor of phase 1.
48	ADDR	A resistor from this pin to GND programs the SVID address for VR1 and VR2. Refer to Table 9 on page 28.

Block Diagram



Simplified Application Circuit

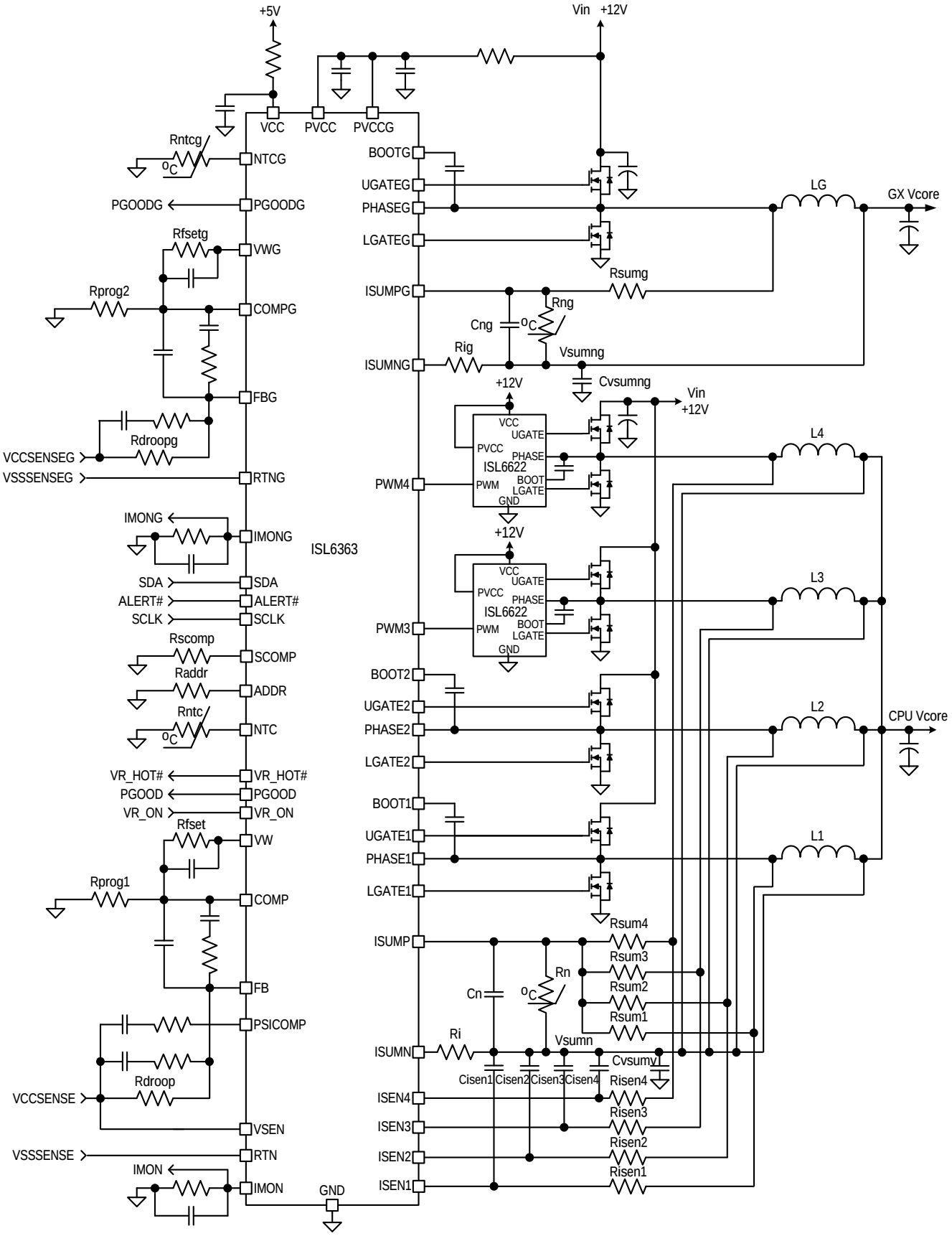


Table of Contents

Absolute Maximum Ratings

Supply Voltage, VCC . . . . . -0.3V to +7V
Supply Voltage, PVCC, PVCCG . . . . . -0.3V to 15V
Absolute Boot Voltage (BOOT) . . . . . -0.3V to +36V
Phase Voltage (PHASE) . . . . . -8V (<400ns, 20µJ) to +30V,
(<200ns, V_{BOOT} - VGND < +36V)
UGATE Voltage (UGATE) . . . . . PHASE-0.3V to BOOT + 0.3V
PHASE-3.5V (<100ns Pulse Width, 2µJ) to BOOT + 0.3V
LGATE Voltage . . . . . -3V (<20ns Pulse Width, 5µJ) to PVCC + 0.3V
-5V (<100ns Pulse Width, 2µJ) to PVCC + 0.3V
All Other Pins . . . . . -0.3V to (VCC + 0.3V)
Open Drain Outputs, PGOOD, VR_HOT#, ALERT# . . . . . -0.3V to +7V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2500V
Machine Model (Tested per JESD22-A115-A) 250V
Charged Device Model (Tested per JESD22-C101A) 1000V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld TQFN Package (Notes 4, 5)	27	1

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage, VCC . . . . . +5V ±5%
PVCC, PVCCG Voltage . . . . . +5V to 12V
Ambient Temperature
CRTZ (Commercial) . . . . . 0°C to +70°C
IRTZ (Industrial) . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V, PVCC = 12V, PVCCG = 12V, T_A = 0°C to +70°C, (Commercial) or -40°C to +85°C (Industrial), f_{SW} = 300kHz, unless otherwise noted.
Boldface limits apply over the operating temperature range, 0°C to +70°C (Commercial) or -40°C to +85°C (Industrial).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I_{VCC}	VR_ON = 1V		18	**20**	mA
		VR_ON = 0V		4.1	**5.5**	mA
PVCC Supply Current	I_{PVCC}	VR_ON = 1V		1	**2**	mA
		VR_ON = 0V			**1**	mA
PVCCG Supply Current	I_{PVCCG}	VR_ON = 1V		1	**2**	mA
		VR_ON = 0V			**1**	mA
VCC Power-On-Reset Threshold	POR_r	V_{CC} rising		4.35	**4.5**	V
	POR_f	V_{CC} falling	**4**	4.15		V
PVCC and PVCCG Power-On-Reset Threshold	$PPOR_r$	V_{CC} rising		4.35	**4.5**	V
	$PPOR_f$	V_{CC} falling	**4**	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	CRTZ	No load; closed loop, active mode range VID = 0.75V to 1.52V	**-0.5**		**+0.5**	%
		VID = 0.5V to 0.745V	**-8**		**+8**	mV
		VID = 0.25V to 0.495V	**-15**		**+15**	mV
	IRTZ	No load; closed loop, active mode range VID = 0.75V to 1.52V	**-0.8**		**+0.8**	%
		VID = 0.5V to 0.745V	**-10**		**+10**	mV
		VID = 0.25V to 0.495V	**-18**		**+18**	mV
Internal V_{BOOT}	CRTZ		**1.0945**	1.100	**1.1055**	V
	IRTZ		**1.0912**	1.1	**1.1088**	V

Electrical Specifications

Operating Conditions: VCC = 5V, PVCC = 12V, PVCCG = 12V, T_A = 0°C to +70°C, (Commercial) or -40°C to +85°C (Industrial), f_{SW} = 300kHz, unless otherwise noted.

Boldface limits apply over the operating temperature range, 0°C to +70°C (Commercial) or -40°C to +85°C (Industrial). (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Maximum Output Voltage	$V_{CC\_CORE(max)}$	VID = [11111111]		1.52		V
Minimum Output Voltage	$V_{CC\_CORE(min)}$	VID = [00000001]		0.25		V
Maximum Output Voltage with Offset	$V_{CC\_CORE(max)}$ + Offset	Register 33h = 7Fh, VID = FFh		2.155		V
CHANNEL FREQUENCY						
Nominal Channel Frequency	$f_{SW(nom)}$	R_{fset} = 8.06kΩ, 3-channel operation, V_{COMP} = 1.1V	**280**	300	**320**	kHz
Minimum Adjustment Range					**200**	kHz
Maximum Adjustment Range			**500**			
AMPLIFIERS						
Current-Sense Amplifier Input Offset		I_{FB} = 0A	**-0.313**		**+0.313**	mV
Error Amp DC Gain	A_{V0}			90		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		18		MHz
ISEN						
Imbalance Voltage		Maximum of ISENs - Minimum of ISENs			**1.1**	mV
Input Bias Current				20		nA
POWER-GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA		0.15	**0.4**	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V			**1**	µA
PGOOD Delay	tpgd			3.8		ms
ALERT# Low Resistance				7	**13**	Ω
VR_HOT# Low Resistance				7	**13**	Ω
ALERT# Leakage Current					**1**	µA
VR_HOT# Leakage Current					**1**	µA
GATE DRIVE SWITCHING TIME						
UGATE Rise Time		t_{RUGATE}; V_{PVCC} / V_{PVCCG} = 12V, 3nF load, 10% to 90%		26		ns
LGATE Rise Time		t_{RLGATE}; V_{PVCC} = 12V, 3nF load, 10% to 90%		18		ns
UGATE Fall Time		t_{FUGATE}; V_{PVCC} = 12V, 3nF load, 90% to 10%		18		ns
LGATE Fall Time		t_{FLGATE}; V_{PVCC} = 12V, 3nF load, 90% to 10%		12		ns
UGATE Turn-On Non-Overlap		$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF load, adaptive		10		ns
LGATE Turn-On Non-Overlap		$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF load, adaptive		10		ns
GATE DRIVE RESISTANCE						
Upper Drive Source Resistance		V_{PVCC} = 12V, 15mA source current		2.0		W
Upper Drive Sink Resistance		V_{PVCC} = 12V, 15mA sink current		1.35		W
Lower Drive Source Resistance		V_{PVCC} = 12V, 15mA source current		1.35		W
Lower Drive Sink Resistance		V_{PVCC} = 12V, 15mA sink current		0.90		W
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 12V, I_F = 2mA		0.58		V
Reverse Leakage	I_R	V_R = 25V		0.2		µA

Electrical Specifications

Operating Conditions: VCC = 5V, PVCC = 12V, PVCCG = 12V, T_A = 0°C to +70°C, (Commercial) or -40°C to +85°C (Industrial), f_{SW} = 300kHz, unless otherwise noted.

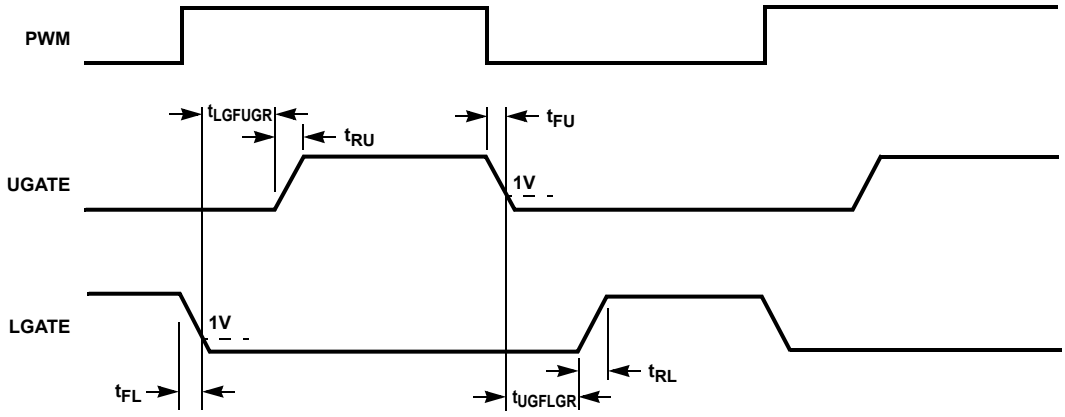
Boldface limits apply over the operating temperature range, 0°C to +70°C (Commercial) or -40°C to +85°C (Industrial). (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
PROTECTION						
Overvoltage Threshold	OV_H	VSEN rising above setpoint for >1µs	**116**		**232**	mV
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
VR1 Overcurrent Threshold		4, 3, 2, 1-Phase Configuration PS0 Mode	**50**	60	**71**	µA
		4-Phase Configuration, drop to 2-Phase in PS1 Mode		30		µA
		4-Phase Configuration, drop to 1-Phase in PS2/3 Mode	**16**	20	**26**	µA
		3-Phase Configuration, drop to 2-Phase in PS1		40		µA
		3-Phase Configuration, drop to 1-Phase in PS2/3	**16**	20	**26**	µA
		2-Phase Configuration, drop to 1-phase in PS1/2/3 Mode		30		µA
VR2 Overcurrent Threshold		All modes of operation	**50**	60	**71**	µA
LOGIC THRESHOLDS						
VR_ON Input Low	V_{IL}				**0.3**	V
VR_ON Input High	V_{IH}		0.7			V
PWM						
PWM Output Low	V_{OL}	Sinking 5mA			**1.0**	V
PWM Output High (Note 6)	V_{OH}	Sourcing 5mA	**3.5**	4.2		V
PWM Tri-State Leakage		PWM = 2.5V		2		µA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	**58**	60	**63**	µA
VR_HOT# Trip Voltage (VR1 and VR2)		Falling	**0.86**	0.873	**0.89**	V
VR_HOT# Reset Voltage (VR1 and VR2)		Rising	**0.905**	0.929	**0.935**	V
Therm_Alert Trip Voltage (VR1 and VR2)		Falling	**0.9**	0.913	**0.93**	V
Therm_Alert Reset Voltage (VR1 and VR2)		Rising	**0.945**	0.961	**0.975**	V
CURRENT MONITOR						
IMON Output Current (VR1 and VR2)		ISUM- pin current = 25µA	**147**	150	154	µA
ICCMAX_Alert Trip Voltage (VR1 and VR2)		Rising	2.61	2.66	**2.695**	V
ICCMAX_ALERT Reset Voltage (VR1 and VR2)		Falling	2.585	2.62	**2.650**	V
INPUTS						
VR_ON Leakage Current	I_{VR_ON}	VR_ON = 0V	**-1**	0		µA
		VR_ON = 1V		18	**35**	µA
SCLK, SDA Leakage		VR_ON = 0V, SCLK and SDA = 0V and 1V	-1		**1**	µA
		VR_ON = 1V, SCLK and SDA = 1V	-5		**1**	µA
		VR_ON = 1V, SCLK and SDA = 0V	-85	-60	**-30**	µA
SLEW RATE (For VID Change)						
Fast Slew Rate			**10**			mV/µs
Slow Slew Rate			**2.5**			mV/µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Gate Driver Timing Diagram



Theory of Operation

Multiphase R3 Modulator

The ISL6363 is a multiphase regulator implementing Intel's™ VR12™ protocol. It has two voltage regulators, VR1 and VR2, on one chip. VR1 can be programmed for 1, 2, 3, or 4-phase operation, and VR2 is dedicated for 1-phase operation. The following description is based on VR1, but also applies to VR2 because the same architecture is implemented.

The ISL6363 uses Intersil's patented R3 (Robust Ripple Regulator) modulator. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 3 conceptually shows the multiphase R3 modulator circuit, and Figure 4 shows the operation principles.

A current source flows from the VW pin to the COMP pin, creating a voltage window set by the resistor between the two pins. This voltage window is called VW window in the following discussion.

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to g_mV_o, where g_m is a gain factor. C_{rm} voltage V_{crm} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If VR1 is in 4-phase mode, the master clock signal will be distributed to the four phases, and the Clock1~4 signals will be 90° out-of-phase. If VR1 is in 3-phase mode, the master clock signal will be distributed to the three phases, and the Clock1~3 signals will be 120° out-of-phase. If VR1 is in 2-phase mode, the master clock signal will be distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If VR1 is in 1-phase mode, the master clock signal will be distributed to Phase 1 only and be the Clock1 signal.

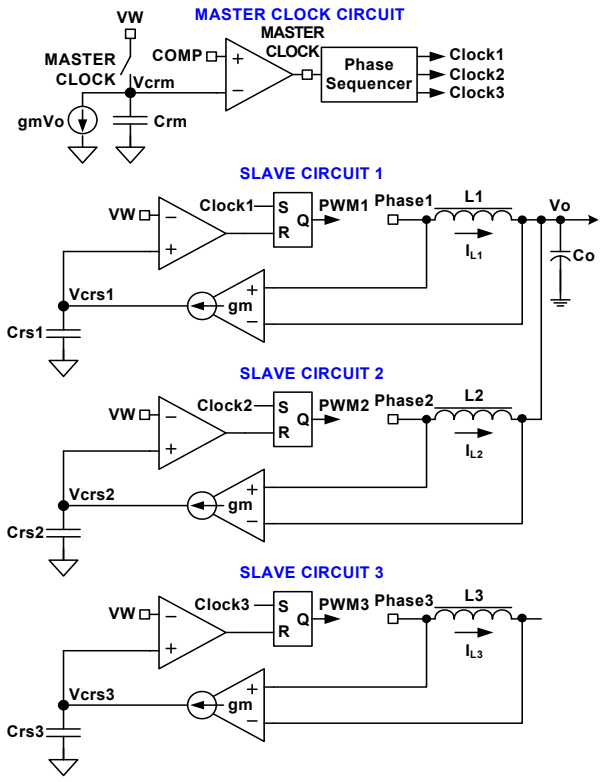


FIGURE 3. R3 MODULATOR CIRCUIT

Each slave circuit has its own ripple capacitor C_{rs}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{rs}. When C_{rs} voltage V_{Crs} hits VW, the slave circuit turns off the PWM pulse, and the current source discharges C_{rs}.

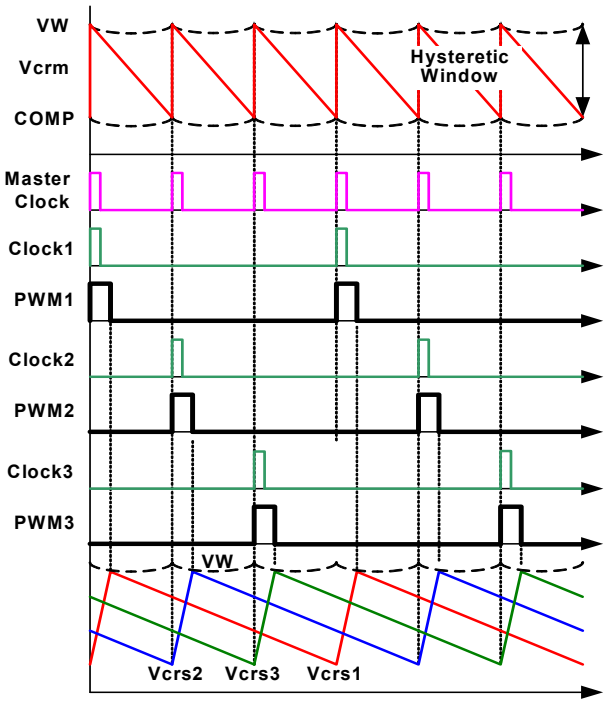


FIGURE 4. R3 MODULATOR OPERATION PRINCIPLES IN STEADY STATE

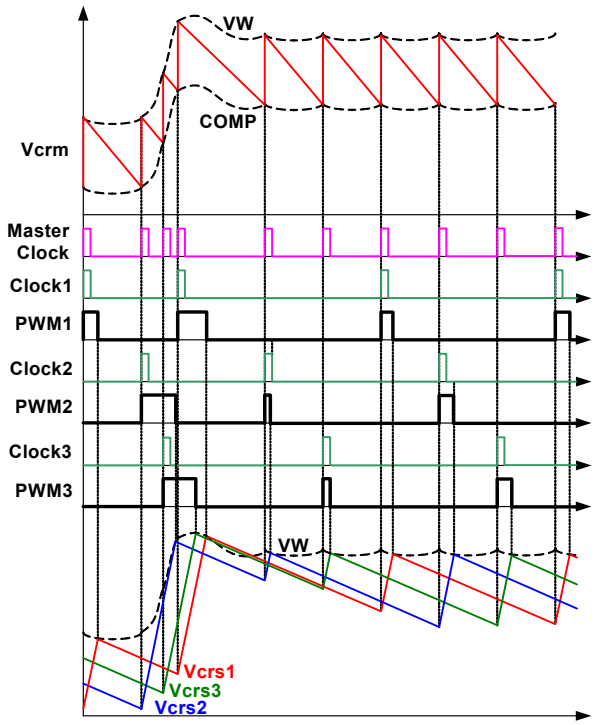


FIGURE 5. R3 MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

Since the controller works with V_{crs}, which are large-amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL6363 uses an error amplifier that allows the controller to maintain a 0.5% output voltage accuracy.

Figure 5 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency, which allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL6363 excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

Diode Emulation and Period Stretching of the ISL6363 can operate in diode emulation (DE) mode to improve light load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and does not allow reverse current, emulating a diode. As Figure 6 shows, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL6363 monitors the current through monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

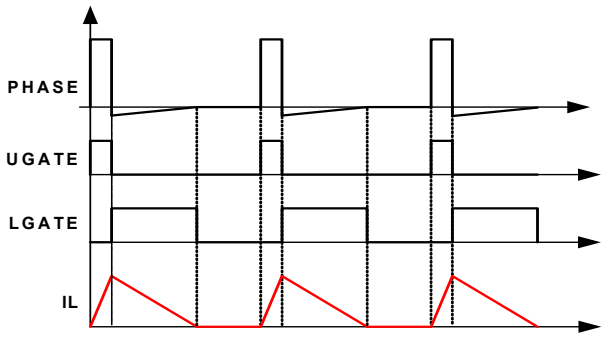


FIGURE 6. DIODE EMULATION

If the load current is light enough, as Figure 6 shows, the inductor current will reach and stay at zero before the next phase node pulse, and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator is in CCM although the controller is in DE mode.

Figure 7 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore is the same, making the inductor current triangle the same in the three cases. The ISL6363 clamps the ripple capacitor voltage V_{crs} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{crs}, naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light load efficiency.

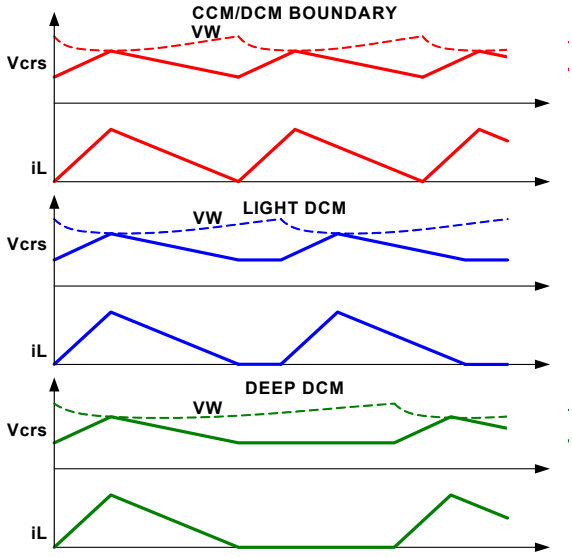


FIGURE 7. PERIOD STRETCHING

Start-up Timing

With the controller's V_{CC} voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the logic high threshold. Figure 8 shows the typical start-up timing of VR1 and VR2. The ISL6363 uses digital soft-start to ramp-up DAC to the voltage programmed by the SetVID command. PGOOD is asserted high and ALERT# is asserted low at the end of the ramp-up. Similar results occur if VR_ON is tied to VCC, with the soft-start sequence starting 800µs after VCC crosses the POR threshold.

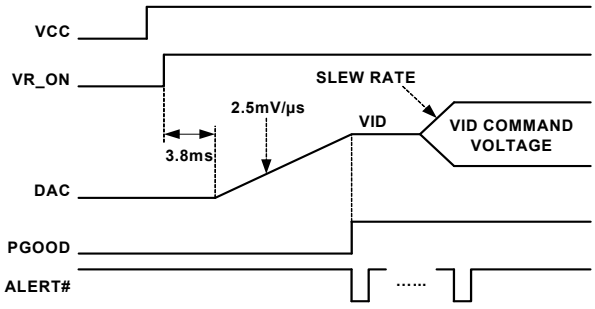


FIGURE 8. VR1 SOFT-START WAVEFORMS

Voltage Regulation and Load Line Implementation

After the start sequence, the ISL6363 regulates the output voltage to the value set by the VID information per Table 1. The ISL6363 will control the no-load output voltage to an accuracy of ±0.5% over the range of 0.75V to 1.52V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

TABLE 1. VID TABLE

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000
0	0	1	0	0	0	0	0	2	0	0.40500

TABLE 1. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500

TABLE 1. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000
0	1	0	1	0	1	1	0	5	6	0.67500
0	1	0	1	0	1	1	1	5	7	0.68000
0	1	0	1	1	0	0	0	5	8	0.68500
0	1	0	1	1	0	0	1	5	9	0.69000
0	1	0	1	1	0	1	0	5	A	0.69500
0	1	0	1	1	0	1	1	5	B	0.70000
0	1	0	1	1	1	0	0	5	C	0.70500
0	1	0	1	1	1	0	1	5	D	0.71000
0	1	0	1	1	1	1	0	5	E	0.71500
0	1	0	1	1	1	1	1	5	F	0.72000
0	1	1	0	0	0	0	0	6	0	0.72500
0	1	1	0	0	0	0	1	6	1	0.73000
0	1	1	0	0	0	1	0	6	2	0.73500
0	1	1	0	0	0	1	1	6	3	0.74000
0	1	1	0	0	1	0	0	6	4	0.74500
0	1	1	0	0	1	0	1	6	5	0.75000
0	1	1	0	0	1	1	0	6	6	0.75500
0	1	1	0	0	1	1	1	6	7	0.76000
0	1	1	0	1	0	0	0	6	8	0.76500
0	1	1	0	1	0	0	1	6	9	0.77000
0	1	1	0	1	0	1	0	6	A	0.77500
0	1	1	0	1	0	1	1	6	B	0.78000
0	1	1	0	1	1	0	0	6	C	0.78500
0	1	1	0	1	1	0	1	6	D	0.79000
0	1	1	0	1	1	1	0	6	E	0.79500
0	1	1	0	1	1	1	1	6	F	0.80000
0	1	1	1	0	0	0	0	7	0	0.80500

TABLE 1. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	1	1	1	0	0	0	1	7	1	0.81000
0	1	1	1	0	0	1	0	7	2	0.81500
0	1	1	1	0	0	1	1	7	3	0.82000
0	1	1	1	0	1	0	0	7	4	0.82500
0	1	1	1	0	1	0	1	7	5	0.83000
0	1	1	1	0	1	1	0	7	6	0.83500
0	1	1	1	0	1	1	1	7	7	0.84000
0	1	1	1	1	0	0	0	7	8	0.84500
0	1	1	1	1	0	0	1	7	9	0.85000
0	1	1	1	1	0	1	0	7	A	0.85500
0	1	1	1	1	0	1	1	7	B	0.86000
0	1	1	1	1	1	0	0	7	C	0.86500
0	1	1	1	1	1	0	1	7	D	0.87000
0	1	1	1	1	1	1	0	7	E	0.87500
0	1	1	1	1	1	1	1	7	F	0.88000
1	0	0	0	0	0	0	0	8	0	0.88500
1	0	0	0	0	0	0	1	8	1	0.89000
1	0	0	0	0	0	1	0	8	2	0.89500
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	1	0	0	0	0	9	0	0.96500
1	0	0	1	0	0	0	1	9	1	0.97000
1	0	0	1	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500

TABLE 1. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	0	0	0	0	0	A	0	1.04500
1	0	1	0	0	0	0	1	A	1	1.05000
1	0	1	0	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	1	0	0	0	0	B	0	1.12500
1	0	1	1	0	0	0	1	B	1	1.13000
1	0	1	1	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500

TABLE 1. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500
1	1	0	0	0	1	1	1	C	7	1.24000
1	1	0	0	1	0	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	1	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	0	0	0	D	0	1.28500
1	1	0	1	0	0	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000
1	1	0	1	0	1	0	0	D	4	1.30500
1	1	0	1	0	1	0	1	D	5	1.31000
1	1	0	1	0	1	1	0	D	6	1.31500
1	1	0	1	0	1	1	1	D	7	1.32000
1	1	0	1	1	0	0	0	D	8	1.32500
1	1	0	1	1	0	0	1	D	9	1.33000
1	1	0	1	1	0	1	0	D	A	1.33500
1	1	0	1	1	0	1	1	D	B	1.34000
1	1	0	1	1	1	0	0	D	C	1.34500
1	1	0	1	1	1	0	1	D	D	1.35000
1	1	0	1	1	1	1	0	D	E	1.35500
1	1	0	1	1	1	1	1	D	F	1.36000
1	1	1	0	0	0	0	0	E	0	1.36500
1	1	1	0	0	0	0	1	E	1	1.37000
1	1	1	0	0	0	1	0	E	2	1.37500
1	1	1	0	0	0	1	1	E	3	1.38000
1	1	1	0	0	1	0	0	E	4	1.38500
1	1	1	0	0	1	0	1	E	5	1.39000
1	1	1	0	0	1	1	0	E	6	1.39500
1	1	1	0	0	1	1	1	E	7	1.40000
1	1	1	0	1	0	0	0	E	8	1.40500

TABLE 1. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
1	1	1	0	1	0	0	1	E	9	1.41000
1	1	1	0	1	0	1	0	E	A	1.41500
1	1	1	0	1	0	1	1	E	B	1.42000
1	1	1	0	1	1	0	0	E	C	1.42500
1	1	1	0	1	1	0	1	E	D	1.43000
1	1	1	0	1	1	1	0	E	E	1.43500
1	1	1	0	1	1	1	1	E	F	1.44000
1	1	1	1	0	0	0	0	F	0	1.44500
1	1	1	1	0	0	0	1	F	1	1.45000
1	1	1	1	0	0	1	0	F	2	1.45500
1	1	1	1	0	0	1	1	F	3	1.46000
1	1	1	1	0	1	0	0	F	4	1.46500
1	1	1	1	0	1	0	1	F	5	1.47000
1	1	1	1	0	1	1	0	F	6	1.47500
1	1	1	1	0	1	1	1	F	7	1.48000
1	1	1	1	1	0	0	0	F	8	1.48500
1	1	1	1	1	0	0	1	F	9	1.49000
1	1	1	1	1	0	1	0	F	A	1.49500
1	1	1	1	1	0	1	1	F	B	1.50000
1	1	1	1	1	1	0	0	F	C	1.50500
1	1	1	1	1	1	0	1	F	D	1.51000
1	1	1	1	1	1	1	0	F	E	1.51500
1	1	1	1	1	1	1	1	F	F	1.52000

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to the load current to achieve the load line. The ISL6363 can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors as shown in Figure 16 or through resistors in series with the inductors as shown in Figure 22. In both methods, capacitor C_n voltage represents the inductor total currents. A droop amplifier converts C_n voltage into an internal current source with the gain set by resistor R_i. The current source is used for load line implementation, current monitor and overcurrent protection.

Figure 9 shows the load line implementation. The ISL6363 drives a current source I_{droop} out of the FB pin, described by Equation 1.

$$I_{droop} = \frac{2 \times V_{Cn}}{R_i} \quad \text{(EQ. 1)}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding, thus sustaining the load line accuracy with reduced cost.

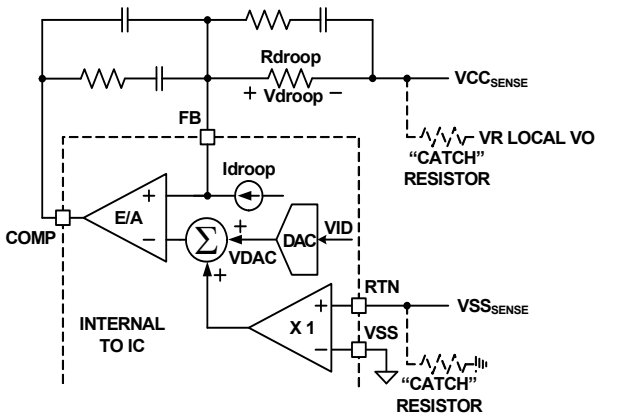


FIGURE 9. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 2.

$$V_{droop} = R_{droop} \times I_{droop} \quad \text{(EQ. 2)}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can both change the load line slope. Since I_{droop} also sets the overcurrent protection level, it is recommended to first scale I_{droop} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Voltage Sensing

Figure 9 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and add it to the DAC output. The error amplifier regulates the inverting and the non-inverting input voltages to be equal as shown in Equation 3:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 3)}$$

Rewriting Equation 3 and substitution of Equation 2 gives

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 4)}$$

Equation 4 is the exact equation required for load line implementation.

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback will be open circuit in the absence of the processor. As Figure 9 shows, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without a processor installed.

Phase Current Balancing

The ISL6363 monitors individual phase average current by monitoring the ISEN1, ISEN2, ISEN3, and ISEN4 voltages. Figure 10 shows the current balancing circuit recommended for ISL6363 for a 3-Phase configuration as an example. Each phase node voltage is averaged by a low-pass filter consisting of R_{isen} and C_{isen}, and presented to the corresponding ISEN pin. R_{isen} should be routed to the inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 5 through 7 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad \text{(EQ. 5)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad \text{(EQ. 6)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad \text{(EQ. 7)}$$

Where R_{dcr1}, R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2} and I_{L3} are inductor average currents.

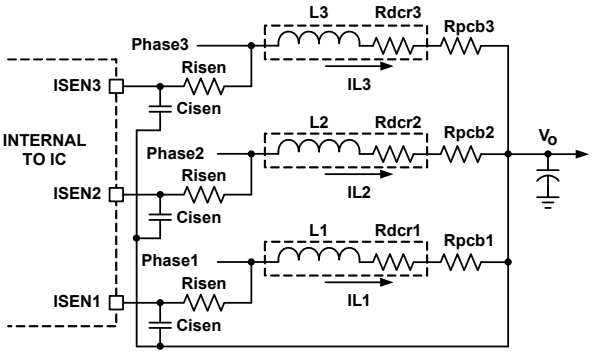


FIGURE 10. CURRENT BALANCING CIRCUIT

The ISL6363 will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus, to achieve $I_{L1} = I_{L2} = I_{L3}$, when there are $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using the same components for L1, L2 and L3 will provide a good match of R_{dcr1}, R_{dcr2} and R_{dcr3}. Board layout will determine R_{pcb1}, R_{pcb2} and R_{pcb3}. It is recommended to have symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

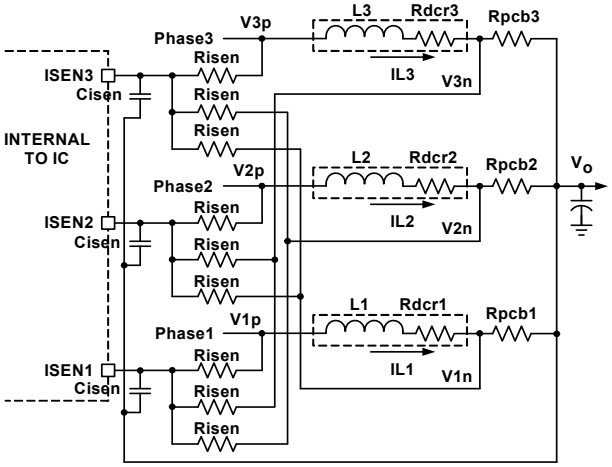


FIGURE 11. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes it is difficult to implement symmetrical layout. For the circuit shown in Figure 10, asymmetric layout causes different R_{pcb1}, R_{pcb2} and R_{pcb3}, thus current imbalance. Figure 11 shows a differential-sensing current balancing circuit recommended for the ISL6363. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of

three sources: its own phase inductor phase-node pad, and the other two phases inductor output side pads. Equations 8 thru 10 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad \text{(EQ. 8)}$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 9)}$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 10)}$$

The ISL6363 will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as shown in Equations 11 and 12:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 11)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 12)}$$

Rewriting Equation 11 gives Equation 13:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 13)}$$

and rewriting Equation 12 gives Equation 14:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 14)}$$

Combining Equations 13 and 14 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 15)}$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 16)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) will be achieved when there is $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2} and R_{pcb3} will not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, the R3 modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 12 shows current balancing performance of the evaluation board with a load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at low rep rate, but cannot keep up when the rep rate gets into the hundred-kHz range, where it's out of the control loop bandwidth. The controller achieves excellent current balancing in all cases installed.

CCM SWITCHING FREQUENCY

The R_{fset} resistor between the COMP and the VW pins sets the VW windows size, therefore sets the switching frequency. When the ISL6363 is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the R3 modulator. As explained in the Multiphase R3 Modulator section on page 11, the effective switching frequency will increase during load insertion and will decrease during load release to achieve fast response. On the other hand, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc., changes. The variation is usually less than 15% and doesn't have any significant effect on output voltage ripple magnitude. Equation 17 gives an estimate of the frequency-setting resistor R_{fset} value. 8kΩ R_{fset} gives approximately 300kHz switching frequency. Lower resistance gives higher switching frequency.

$$R_{fset}(k\Omega) = (Period(\mu s) - 0.29) \times 2.65 \quad \text{(EQ. 17)}$$

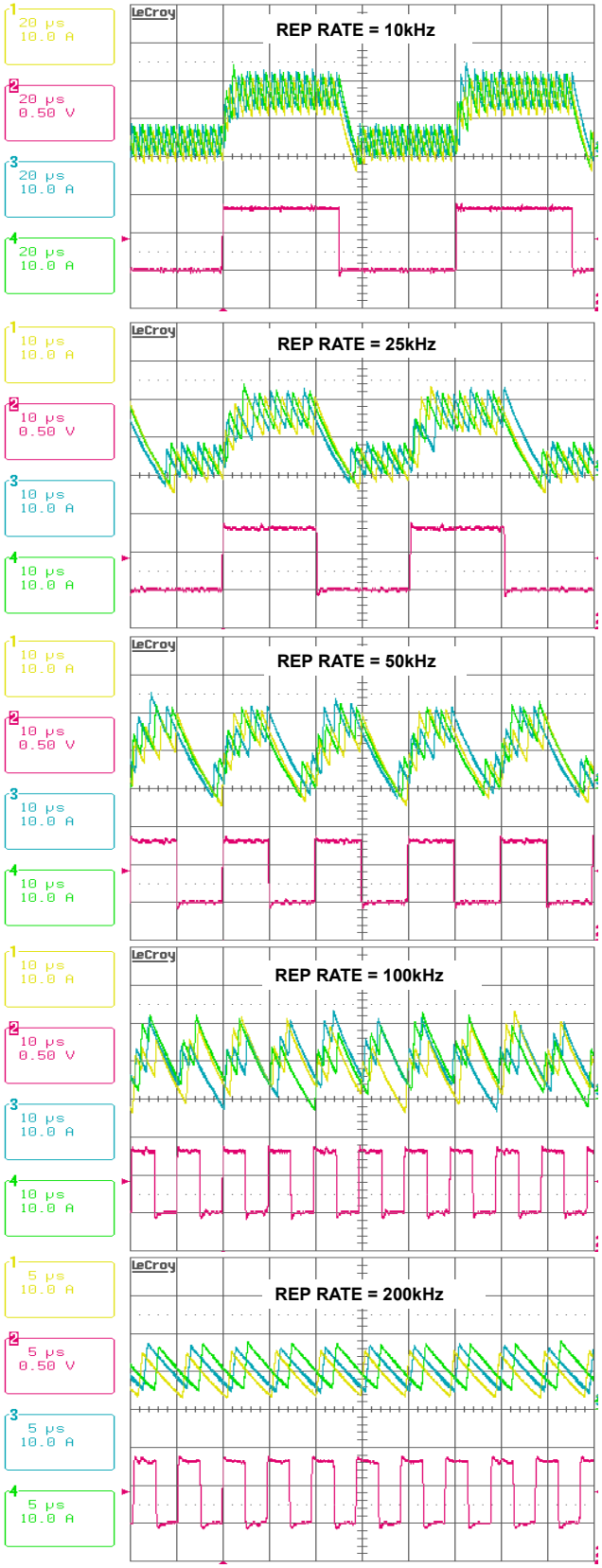


FIGURE 12. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: IL1, CH2: I_{LOAD}, CH3: IL2, CH4: IL3

Modes of Operation

TABLE 2. VR1 MODES OF OPERATION

PWM4	PWM3	ISEN2	CONFIG.	PS	MODE	OCP THRESHOLD (µA)
To Ext Driver	To Ext Driver	To Power Stage	4-phase CPU VR Config.	0	4-PH CCM	60
				1	2-PH CCM	30
				2	1-PH DE	20
				3		
Tie to 5V VCC			3-phase CPU VR Config.	0	3-PH CCM	60
				1	2-PH CCM	40
				2	1-PH DE	20
				3		
	Tie to 5V VCC		2-phase CPU VR Config.	0	2-PH CCM	60
				1	2-PH CCM	60
				2	1-PH DE	30
				3		
		Tie to 5V VCC	1-phase CPU VR Config.	0	1-PH CCM	60
				1		
				2	1-PH DE	
				3		

VR1 can be configured for 4, 3, 2 or 1-phase operation. Table 2 shows VR1 configurations and operational modes, programmed by the PWM4, PWM3 pins and the ISEN2 pin status, and the PS command. For 3-phase configuration, tie the PWM4 pin to 5V. In this configuration, phases 1, 2 and 3 are active. For 2-phase configuration, tie the PWM4 and PWM3 pin to 5V. In this configuration, phases 1 and 2 are active. For 1-phase configuration, tie the PWM4, PWM3 and the ISEN2 pin to 5V. In this configuration, only phase 1 is active.

In 4-phase configuration, VR1 operates in 4-phase CCM in PS0 mode. It enters 2-phase CCM operation in PS1 mode. It enters 1-phase DE operation in PS2 and PS3 modes.

In 3-phase configuration, VR1 operates in 3-phase CCM in PS0 mode. It enters 2-phase CCM operation in PS1 mode. It enters 1-phase DE operation in PS2 and PS3 modes.

In 2-phase configuration, VR1 operates in 2-phase CCM in PS0 and PS1 mode. It enters 1-phase DE mode in PS2 and PS3 modes.

In 1-phase configuration, VR1 operates in 1-phase CCM in PS0 and PS1, and enters 1-phase DE mode in PS2 and PS3.

TABLE 3. VR2 MODES OF OPERATION

PS	MODE	OCP THRESHOLD
0	1-phase CCM	60µA
1		
2	1-phase DE	
3		

Table 3 shows VR2 operational modes, programmed by the PS command. VR2 operates in 1-phase CCM in PS0 and PS1, and enters 1-phase DE mode in PS2 and PS3 mode.

VR2 can be disabled completely by tying ISUMNG to 5V, and all communication to VR2 will be blocked.

Dynamic Operation

VR1 and VR2 behave the same during dynamic operation. The controller responds to VID changes by slewing to the new voltage at a slew rate indicated in the SetVID command. There are three SetVID slew rates, namely SetVID_fast, SetVID_slow and SetVID_decay.

SetVID_fast command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 10mV/µs slew rate.

SetVID_slow command prompts the controller to enter CCM and to actively drive the output voltage to the new VID value at a minimum 2.5mV/µs slew rate.

SetVID_decay command prompts the controller to enter DE mode. The output voltage will decay down to the new VID value at a slew rate determined by the load. If the voltage decay rate is too fast, the controller will limit the voltage slew rate at SetVID_slow slew rate.

ALERT# will be asserted low at the end of SetVID_fast and SetVID_slow VID transitions.

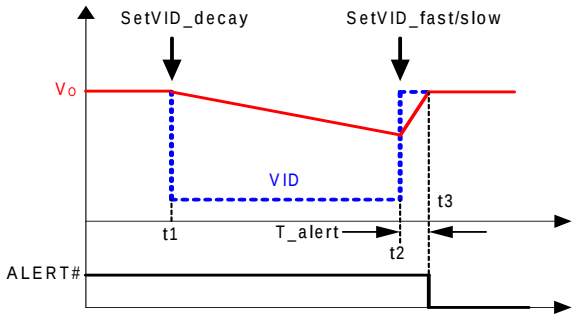


FIGURE 13. SETVID DECAY PRE-EMPTIVE BEHAVIOR

Figure 13 shows SetVID Decay Pre-Emptive behavior. The controller receives a SetVID_decay command at t1. The VR enters DE mode and the output voltage V_O decays down slowly. At t2, before V_O reaches the intended VID target of the SetVID_decay command, the controller receives a SetVID_fast (or SetVID_slow) command to go to a voltage higher than the actual V_O. The controller will turn around immediately and slew V_O to the new target voltage at the slew rate specified by the SetVID command. At t3, V_O reaches the new target voltage and the controller asserts the ALERT# signal.

The R3 modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

VR_HOT#/ALERT# Behavior

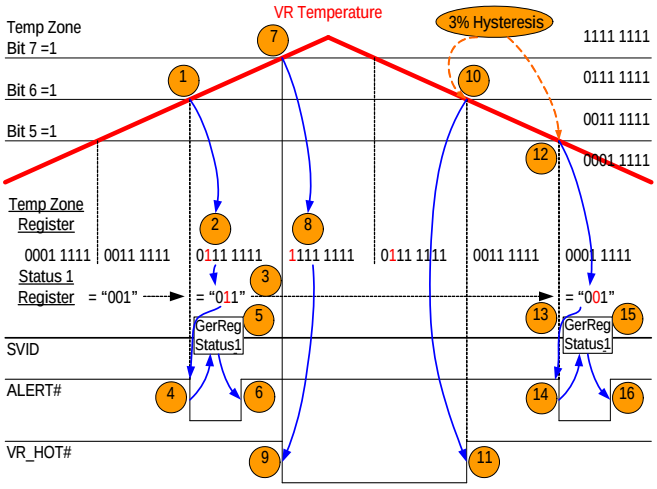


FIGURE 14. VR_HOT#/ALERT# BEHAVIOR

The controller drives 60µA current source out of the NTC pin and the NTCG pin alternatively at 1kHz frequency with 50% duty cycle. The current source flows through the respective NTC resistor networks on the pins and creates voltages that are monitored by the controller through an A/D converter (ADC) to generate the TZONE value. Table 4 shows the programming table for TZONE. The user needs to scale the NTC and the NTCG network resistance such that it generates the NTC (and NTCG) pin voltage that corresponds to the left-most column. Do not use any capacitor to filter the voltage.

TABLE 4. TZONE TABLE

VNTC (V)	TMAX (%)	TZONE
0.84	>100	FFh
0.88	100	FFh
0.92	97	7Fh
0.96	94	3Fh
1.00	91	1Fh
1.04	88	0Fh
1.08	85	07h
1.12	82	03h
1.16	79	01h
1.2	76	01h
>1.2	<76	00h

Figure 14 shows how the NTC and the NTCG network should be designed to get correct VR_HOT#/ALERT# behavior when the system temperature rises and falls, manifested as the NTC and the NTCG pin voltage falls and rises. The series of events are:

1. The temperature rises so the NTC pin (or the NTCG pin) voltage drops. TZONE value changes accordingly.
2. The temperature crosses the threshold where the TZONE register Bit 6 changes from 0 to 1.
3. The controller changes Status_1 register bit 1 from 0 to 1.
4. The controller asserts ALERT#.
5. The CPU reads Status_1 register value to know that the alert assertion is due to TZONE register bit 6 flipping.
6. The controller clears ALERT#.
7. The temperature continues rising.
8. The temperature crosses the threshold where the TZONE register Bit 7 changes from 0 to 1.
9. The controller asserts the VR_HOT# signal. The CPU throttles back and the system temperature starts dropping eventually.
10. The temperature crosses the threshold where the TZONE register bit 6 changes from 1 to 0. This threshold is 1 ADC step lower than the one when VR_HOT# gets asserted, to provide 3% hysteresis.
11. The controllers de-assert the VR_HOT# signal.
12. The temperature crosses the threshold where the TZONE register bit 5 changes from 1 to 0. This threshold is 1 ADC step lower than the one when ALERT# gets asserted during the temperature rise to provide 3% hysteresis.
13. The controller changes Status_1 register bit 1 from 1 to 0.
14. The controller asserts ALERT#.
15. The CPU reads Status_1 register value to know that the alert assertion is due to TZONE register bit 5 flipping.
16. The controller clears ALERT#.

Protection Functions

VR1 and VR2 both provide overcurrent, current-balance and overvoltage fault protections. The controller also provides over-temperature protection. The following discussion is based on VR1 and also applies to VR2.

The controller determines overcurrent protection (OCP) by comparing the average value of the droop current I_{droop} with an internal current source threshold as Table 2 shows. It declares OCP when I_{droop} is above the threshold for 120µs.

For overcurrent conditions above 1.5x the OCP level, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection. This protection is also referred to as way-overcurrent protection or fast-overcurrent protection, for short-circuit protections.

The controller monitors the ISEN pin voltages to determine current-balance protection. If the ISEN pin voltage difference is greater than 9mV for 1ms, the controller will declare a fault and latch off.

The controller takes the same actions for all of the above fault protections: de-assertion of PGOOD and turn-off of the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes.

The controller will declare an overvoltage fault and de-assert PGOOD if the output voltage exceeds the VID set value by +200mV. The ISL6363 will immediately declare an OV fault, de-assert PGOOD, and turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value when all power MOSFETs are turned off. If the output voltage rises above the VID set value +200mV again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground.

All the above fault conditions can be reset by bringing VR_ON low or by bringing VCC below the POR threshold. When VR_ON and VCC return to their high operating levels, a soft-start will occur

Table 5 summarizes the fault protections.

TABLE 5. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VCC toggle
Phase Current Unbalance	1ms		
Way-Overcurrent (1.5xOC)	Immediately		
Overvoltage +200mV		PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-state.	

CURRENT MONITOR

The ISL6363 provides the current monitor function for both VRs. IMON pin reports VR1 inductor current and IMONG pins reports VR2 inductor current. Since they are designed following the same principle, the following discussion will be only based on the IMON pin but also applies to the IMONG pin.

The IMON pin outputs a high-speed analog current source that is 3 times of the droop current flowing out of the FB pin. Thus becoming Equation 18:

$$I_{IMON} = 3 \times I_{droop} \quad \text{(EQ. 18)}$$

As the “Simplified Application Circuit” on page 6 shows, a resistor R_{imon} is connected to the IMON pin to convert the IMON pin current to voltage. A capacitor can be paralleled with R_{imon} to filter the voltage information.

The IMON pin voltage range is 0V to 2.7V. The controller monitors the IMON pin voltage and considers that VR1 has reached ICCMAX on IMON pin voltage is 2.7V.

PSICOMP Function

Figure 15 shows the PSICOMP function. A switch turns on to short the FB and the PSICOMP pins when the controller is in PS2 mode. The RC network C2.2 and R3.2 is connected in parallel with R1 and C2/R3 compensation network in PS2/3 mode. This additional RC network increases the high frequency content of the signal passing from the output voltage to the COMP pin which will improve transient response in PS2/3 mode of operation.

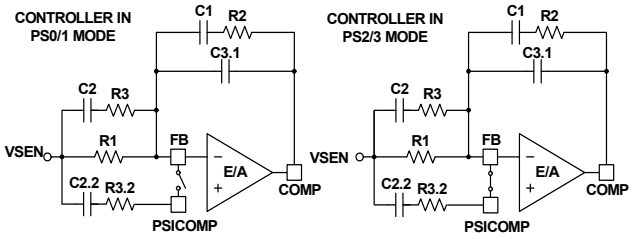


FIGURE 15. PSICOMP FUNCTION

When the PSICOMP switch is off, C2.2 and R3.2 are disconnected from the FB pin. However, the controller still actively drives the PSICOMP pin to allow for smooth transitions between modes of operation.

The PSICOMP function ensures excellent transient response in both PS0, PS1 and PS2/3 modes of operation. If the PSICOMP function is not needed C2.2 and R3.2 can be disconnected.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero-crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it will flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it will flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase comparator threshold voltage accordingly in iterative steps, such that the low-side MOSFET body diode conducts for approximately 40ns to minimize the body diode-related loss.

Supported Data and Configuration Registers

The controller supports the following data and configuration registers.

TABLE 6. SUPPORTED DATA AND CONFIGURATION REGISTERS

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
00h	Vendor ID	Uniquely identifies the VR vendor. Assigned by Intel.	12h
01h	Product ID	Uniquely identifies the VR product. Intersil assigns this number.	1Fh
02h	Product Revision	Uniquely identifies the revision of the VR control IC. Intersil assigns this data.	
05h	Protocol ID	Identifies what revision of SVID protocol the controller supports.	01h

TABLE 6. SUPPORTED DATA AND CONFIGURATION REGISTERS (Continued)

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
06h	Capability	Identifies the SVID VR capabilities and which of the optional telemetry registers are supported.	81h
10h	Status_1	Data register read after ALERT# signal. Indicating if a VR rail has settled, has reached VRHOT condition or has reached ICC max.	00h
11h	Status_2	Data register showing status_2 communication.	00h
12h	Temperature Zone	Data register showing temperature zones that have been entered.	00h
1Ch	Status_2_ LastRead	This register contains a copy of the Status_2 data that was last read with the GetReg (Status_2) command.	00h
21h	ICC max	Data register containing the ICC max the platform supports, set at start-up by resistors Rprog1 and Rprog2. The platform design engineer programs this value during the design process. Binary format in amps, i.e., 100A = 64h	Refer to Table 7
22h	Temp max	Data register containing the temperature max the platform support, set at startup by resistor Rprog2. The platform design engineer programs this value during the design process. Binary format in °C, i.e., +100°C = 64h	Refer to Table 8
24h	SR-fast	Slew Rate Normal. The fastest slew rate the platform VR can sustain. Binary format in mV/µs. i.e., 0Ah = 10mV/µs.	0Ah
25h	SR-slow	Is 4x slower than normal. Binary format in mV/µs. i.e., 02h = 2.5mV/µs	02h
26h	V_{BOOT}	If programmed by the platform, the VR supports V_{BOOT} voltage during start-up ramp. The VR will ramp to V_{BOOT} and hold at V_{BOOT} until it receives a new SetVID command to move to a different voltage.	00h
30h	Vout max	This register is programmed by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR will respond with “not supported” acknowledge.	FBh
31h	VID Setting	Data register containing currently programmed VID voltage. VID data format.	00h
32h	Power State	Register containing the current programmed power state.	00h
33h	Voltage Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is a sign bit, 0 = positive margin, 1 = negative margin. Remaining 7 bits are # VID steps for the margin. 00h = no margin, 01h = +1 VID step 02h = +2 VID steps	00h
34h	Multi VR Config	Data register that configures multiple VRs behavior on the same SVID bus.	VR1: 00h VR2: 01h

Key Component Selection

Inductor DCR Current-Sensing Network

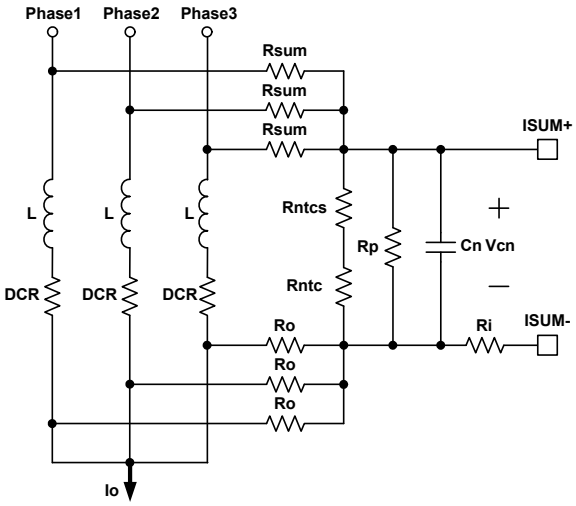


FIGURE 16. DCR CURRENT-SENSING NETWORK

Figure 16 shows the inductor DCR current-sensing network for a 3-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown, and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to temperature-compensate the inductor DCR change.

The inductor output side pads are electrically shorted in the schematic, but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the

current-sensing summing network. It is recommended to use 1Ω~10Ω R_o to create quality signals. Since R_o value is much smaller than the rest of the current sensing circuit, the following analysis will ignore it for simplicity.

The summed inductor current information is presented to the capacitor C_n. Equations 19 thru 23 describe the frequency-domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 19)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 20)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 21)}$$

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 22)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 23)}$$

Where N is the number of phases.

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC R_{ntc} values decreases as its temperature decreases. Proper selections of R_{sum}, R_{ntcs}, R_p and R_{ntc} parameters ensure that V_{Cn} represent the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of V_{cn} to the inductor DCR voltage, so the droop circuit has higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current-sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole w_{sns} and a zero w_L. One needs to match w_L and w_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing w_L equal to w_{sns} and solving for the solution, Equation 24 gives Cn value.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 24)}$$

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ and L = 0.36µH, Equation 24 gives C_n = 0.406µF.

Assuming the compensator design is correct, Figure 17 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{CORE} also has a square response.

If C_n value is too large or too small, $V_{Cn}(s)$ will not accurately represent real-time $I_o(s)$ and will worsen the transient response. Figure 18 shows the load transient response when C_n is too small. V_{CORE} will sag excessively upon load insertion and may create a system failure. Figure 19 shows the transient response when C_n is too large. V_{CORE} is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.

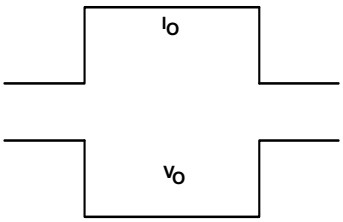


FIGURE 17. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

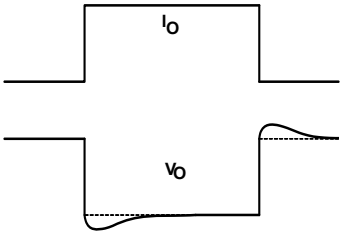


FIGURE 18. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

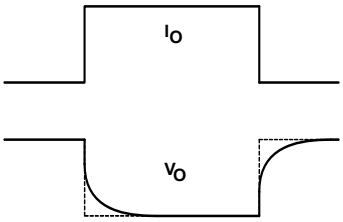


FIGURE 19. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

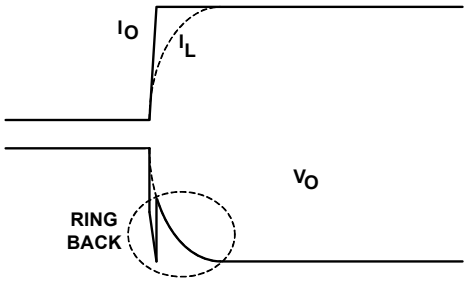


FIGURE 20. OUTPUT VOLTAGE RING BACK PROBLEM

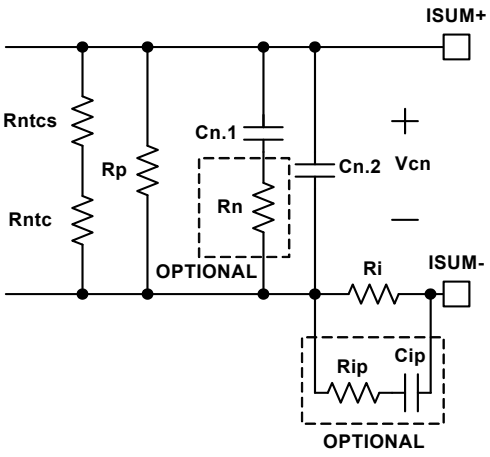


FIGURE 21. OPTIONAL CIRCUITS FOR RING BACK REDUCTION

Figure 20 shows the output voltage ring back problem during load transient response. The load current i_o has a fast step change, but the inductor current I_L cannot accurately follow. Instead, I_L responds in first order system fashion due to the nature of current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_O dip quickly upon load current change. However, the controller regulates V_O according to the droop current I_{droop}, which is a real-time representation of I_L; therefore it pulls V_O back to the level dictated by I_L, causing the ring back problem. This phenomenon is not observed when the output capacitor have very low ESR and ESL, such as all ceramic capacitors.

Figure 21 shows two optional circuits for reduction of the ring back.

C_n is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 21 shows that two capacitors $C_{n.1}$ and $C_{n.2}$ are in parallel. Resistor R_n is an optional component to reduce the V_O ring back. At steady state, $C_{n.1} + C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 18 explains, V_O tends to dip when C_n is too small, and this effect will reduce the V_O ring back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. R_n value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and R_n values should be determined through tuning the load transient response waveforms on an actual board.

R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of i_o change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L, and V_O will not ring back. The recommended value for R_{ip} is 100Ω. C_{ip} should be determined through tuning the load transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF. However, it should be noted that the R_{ip} -C_{ip} branch may distort the i_{droop} waveform. Instead of being triangular as the real inductor current, i_{droop} may have sharp spikes, which may adversely affect i_{droop} average value detection and therefore may affect OCP accuracy. User discretion is advised.

Resistor Current-Sensing Network

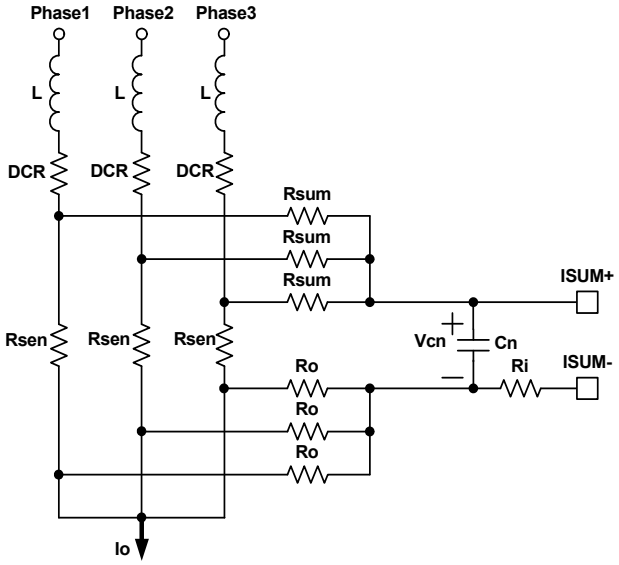


FIGURE 22. RESISTOR CURRENT-SENSING NETWORK

Figure 22 shows the resistor current-sensing network for a 2-phase solution. Each inductor has a series current-sensing resistor R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a filter for noise attenuation. Equations 25 thru 27 give $V_{Cn}(s)$ expression

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 25)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 26)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 27)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current-sensing resistor R_{sen} value will not have significant variation over-temperature, so there is no need for the NTC network.

The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

Overcurrent Protection

Refer to Equation 1 on page 16 and Figures 16, 20 and 22; resistor R_i sets the droop current I_{droop}. Tables 2 (page 19) and 3 (page 19) show the internal OCP threshold. It is recommended to design I_{droop} without using the R_{comp} resistor.

For example, the OCP threshold is 60µA for 3-phase solution. We will design I_{droop} to be 40.9µA at full load, so the OCP trip level is 1.5x of the full load current.

For inductor DCR sensing, Equation 28 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 28)}$$

Substitution of Equation 28 into Equation 1 gives Equation 29:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 29)}$$

Therefore:

$$R_i = \frac{2R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{droop}} \quad \text{(EQ. 30)}$$

Substitution of Equation 20 and application of the OCP condition in Equation 30 gives Equation 31:

$$R_i = \frac{2 \times \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{droopmax}} \quad \text{(EQ. 31)}$$

Where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ, I_{omax} = 51A and $I_{droopmax}$ = 40.9µA, Equation 31 gives R_i = 606Ω.

For resistor sensing, Equation 32 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 32)}$$

Substitution of Equation 32 into Equation 1 gives Equation 33:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 33)}$$

Therefore

$$R_i = \frac{2R_{sen} \times I_o}{N \times I_{droop}} \quad \text{(EQ. 34)}$$

Substitution of Equation 34 and application of the OCP condition in Equation 30 gives Equation 35:

$$R_i = \frac{2R_{sen} \times I_{omax}}{N \times I_{droopmax}} \quad \text{(EQ. 35)}$$

Where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given N = 3, R_{sen} = 1mΩ, I_{omax} = 53A and $I_{droopmax}$ = 40.9µA, Equation 35 gives R_i = 863Ω.

LOAD LINE SLOPE

Refer to Figure 9.

For inductor DCR sensing, substitution of Equation 29 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \quad \text{(EQ. 36)}$$

For resistor sensing, substitution of Equation 33 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{sen} \times R_{droop}}{N \times R_i} \quad \text{(EQ. 37)}$$

Substitution of Equation 30 and rewriting Equation 36, or substitution of Equation 34 and rewriting Equation 37 give the same result in Equation 38:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad \text{(EQ. 38)}$$

One can use the full load condition to calculate R_{droop}. For example, given I_{omax} = 51A, $I_{droopmax}$ = 40.9µA and LL = 1.9mΩ, Equation 38 gives R_{droop} = 2.37kΩ.

It is recommended to start with the R_{droop} value calculated by Equation 38, and fine tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Compensator

Figure 17 shows the desired load transient response waveforms. Figure 23 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e., constant output impedance, in the entire frequency range, V_O will have square response when I_o has a square change.

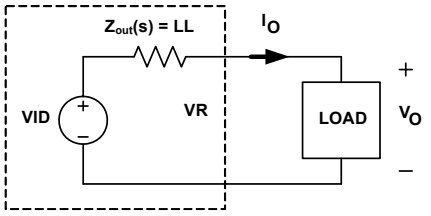


FIGURE 23. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network, so the VR achieves constant output impedance as a stable system. Figure 26 shows a screenshot of the spreadsheet.

A VR with an active droop function is a dual-loop system consisting of a voltage loop and a droop loop which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 24 conceptually shows T1(s) measurement set-up and Figure 25

conceptually shows T2(s) measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. T(1) is measured after the summing node, and T2(s) is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can be actually measured on an ISL6363 regulator.

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s) and has more meaning of system stability.

T2(s) is the voltage loop gain with closed droop loop. It has more meaning of output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin, and output impedance equal or smaller than the load line slope.

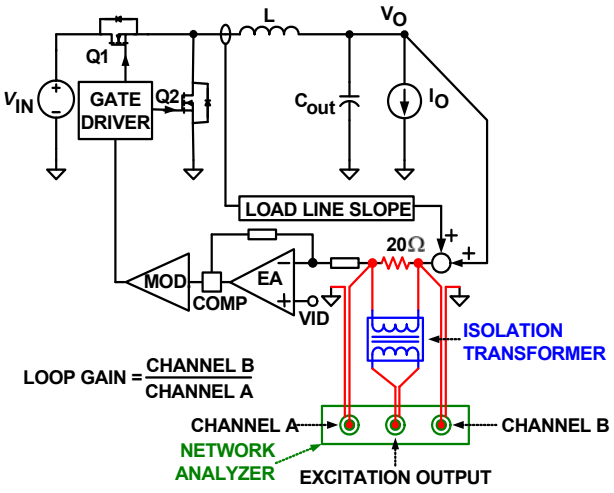


FIGURE 24. LOOP GAIN T1(s) MEASUREMENT SET-UP

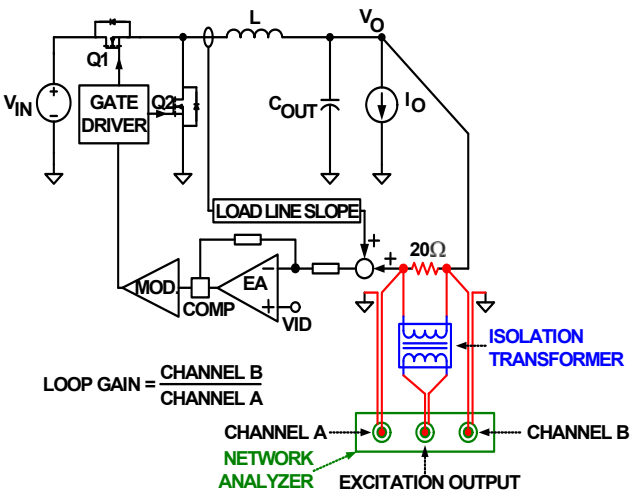


FIGURE 25. LOOP GAIN T2(s) MEASUREMENT SET-UP

Compensation & Current Sensing Network Design for Intersil Multiphase R^3 Regulators.

Revision 9.0

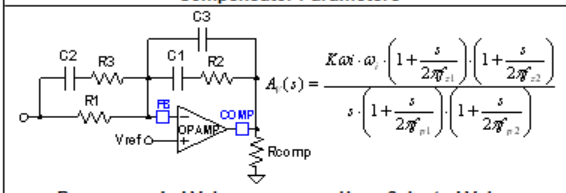
Attention: 1. "Analysis ToolPak" Add-in is required. (To turn it on in MS Excel 2003, go to Tools--Add-Ins, and check "Analysis ToolPak").

2. Green cells require user input

Operation Parameters

Controller Part Number:	ISL6363	
Phase Number:	4	
Vin:	12	volts
Vo:	1.1	volts
Full Load Current:	112	Amps
Estimated Full-Load Efficiency:	85	%
Number of Output Bulk Capacitors:	4	
Capacitance of Each Output Bulk Capacitor:	720	uF
ESR of Each Output Bulk Capacitor:	6	mΩ
ESL of Each Output Bulk Capacitor:	1	nH
Number of Output Ceramic Capacitors:	20	
Capacitance of Each Output Ceramic Capacitor:	19	uF
ESR of Each Output Ceramic Capacitor:	3	mΩ
ESL of Each Output Ceramic Capacitor:	3	nH
Switching Frequency:	350	kHz
Inductance Per Phase:	0.23	uH
CPU Socket Resistance:	0.9	mΩ
Desired Load-Line Slope:	1.7	mΩ
Desired Idroop Current at Full Load:	46	uA
(This sets the over-current protection level)		

Compensator Parameters



$$A_i(s) = \frac{K\omega i \cdot \omega_i \cdot \left(1+\frac{s}{2\pi f_{z1}}\right)\cdot\left(1+\frac{s}{2\pi f_{z2}}\right)}{s\cdot\left(1+\frac{s}{2\pi f_{p1}}\right)\cdot\left(1+\frac{s}{2\pi f_{p2}}\right)}$$

	Recommended Value		User-Selected Value	
R1	4.139	kΩ	4.14	kΩ
R2	147.303	kΩ	249	kΩ
R3	0.544	kΩ	0.1	kΩ
C1	403.756	pF	270	pF
C2	556.844	pF	390	pF
C3	88.239	pF	82	pF
Rcomp			200	kΩ

Use User-Selected Value (Y/N)? Y

Disable Droop Function (Y/N)? N

Performance and Stability

T1 Bandwidth:	164kHz	T2 Bandwidth:	39kHz
T1 Phase Margin:	82.9°	T2 Phase Margin:	108.3°

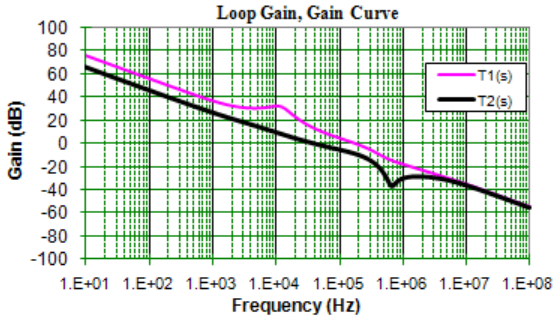
Changing the settings in red requires deep understanding of control loop design

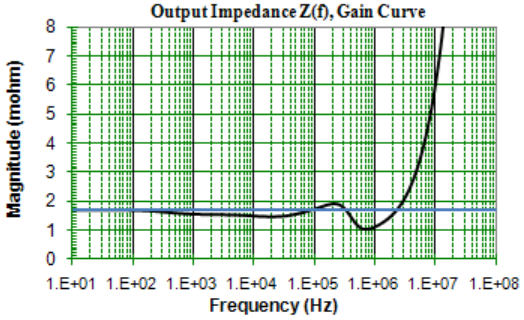
Place the 2nd compensator pole fp2 at: 1.5 xfs (Switching Frequency)

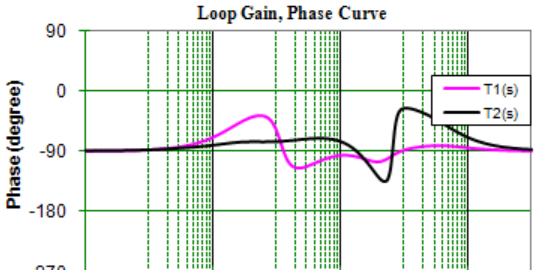
Tune Kωi to get the desired loop gain bandwidth

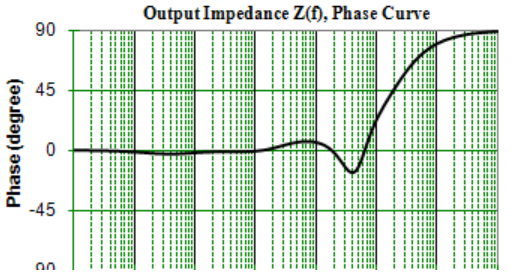
Tune the compensator gain factor Kωi: 1.3

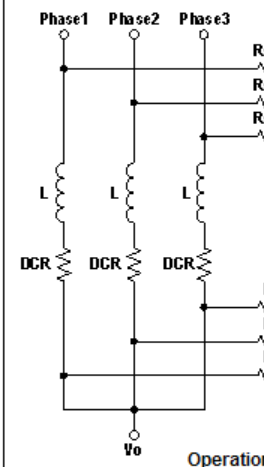
(Recommended Kωi range is 0.8~2)











Current Sensing M

Operatio

Inductor DCR

Rsum

Rntc

Rntcs

Rp

Recommended Val

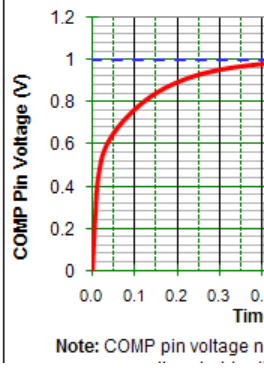
Cn 0.485 uF

Ri 632.237 Ω

These Rsum and Cn values a
so it can calculate for r
They should not be use

COMP Pin Voltage Duri

(Only On Controllers With CO



Note: COMP pin voltage n

FIGURE 26. SCREENSHOT OF THE COMPENSATOR DESIGN SPREADSHEET

Programming Resistors

There are three programming resistors: R_{prog1}, R_{prog2} and R_{addr}. Table 7 shows how to select R_{prog1} based on V_{BOOT} and IMAX_CR register settings. VR1 can power to 0V V_{BOOT} or an internally-set V_{BOOT} based on R_{prog1} value. When the controller works with an actual CPU, select R_{prog1} such that VR1 powers up to V_{BOOT} = 0V as required by the SVID command. In the absence of a CPU, such as testing of the only the VR, select R_{prog1} such that VR1 powers up to the internally-set V_{BOOT}, which by default is 1.1V. Determine the maximum current VR1 can support and set the IMAX_CR register value accordingly by selecting the appropriate R_{prog1} value. The CPU will read the IMAX_CR register and ensures that the CPU CORE current doesn't exceed the value specified by IMAX_CR.

Table 8 shows how to select R_{prog2} based on TMAX and IMAX_GR register settings. There are four TMAX temperatures to choose from: +120°C, +110°C, +105°C, and +95°C. There are also four IMAX_GR values to choose from: 35A, 30A, 25A and 20A.

TABLE 7. RPROG1 PROGRAMMING TABLE

RPROG1 (kΩ)	BOOT (V)	IMAX CORE Nph = 4 (A)	IMAX CORE Nph = 3 (A)	IMAX CORE Nph = 2 (A)	IMAX CORE Nph = 1 (A)
7.15	1.1	100	75	50	25
13.0	1.1	108	81	54	27
20.5	1.1	116	87	58	29
27.4	1.1	124	93	62	31
38.3	1.1	132	99	66	33
52.3	1.1	140	105	70	35
66.5	1.1	148	111	74	37
80.6	0	148	111	74	37
95.3	0	140	105	70	35
113	0	132	99	66	33
137	0	124	93	62	31
165	0	116	87	58	29
196	0	108	81	54	27
226	0	100	75	50	25
Open Circuit	0	92	69	46	23

TABLE 8. RPROG2 PROGRAMMING TABLE

RPROG2 (kΩ)	TMAX (°C)	IMAX_GR (A)
7.15	120	30
13.0	120	25
20.5	120	20
27.4	110	20
38.3	110	25
52.3	110	30
66.5	110	35
80.6	105	35
95.3	105	30
113	105	25
137	105	20
165	95	20
196	95	25
226	95	30
Open Circuit	95	35

Table 9 shows how to select R_{prog2} based on TMAX and IMAX_GR register settings. There are four TMAX temperatures to choose from: +120°C, +110°C, +105°C, and +95°C. There are also four IMAX_GR values to choose from: 35A, 30A, 25A and 20A.

TABLE 9. RADDR PROGRAMMING TABLE

RADDR (kΩ)	VR1 AND VR1 SVID ADDRESS
0	0,1
7.15	0,1
13	2,3
20.5	2,3
27.4	4,5
38.3	4,5
52.3	6,7
66.5	6,7
80.6	8,9
95.3	8,9
113	A,B
137	A,B
165	C,D
196	C,D
226	0,1
Open Circuit	0,1

NTC Network on the NTC and the NTCG pins

The controller drives 60µA current source out of the NTC pin and the NTCG pin alternatively at 1kHz frequency with 50% duty cycle. The current source flows through the respective NTC resistor networks on the pins and creates voltages that are monitored by the controller through an A/D converter to generate the TZONE value. Table 10 shows the programming table for TZONE. The user needs to scale the NTC (and NTCG) network resistance such that it generates the NTC (and NTCG) pin voltage that corresponds to the left-most column. Do not use any capacitor to filter the voltage. On ADC Output = 7, the controller issues thermal alert to the CPU, on ADC Output <7, the controller asserts the VR_HOT# signal.

TABLE 10. TZONE PROGRAMMING TABLE

VNTC (V)	ADC OUTPUT	%TMAX	TZONE
0.64	0	>100%	FFh
0.68	1	>100%	FFh
0.72	2	>100%	FFh
0.76	3	>100%	FFh
0.80	4	>100%	FFh
0.84	5	>100%	FFh
0.88	6	100%	FFh
0.92	7	97%	7Fh
0.96	8	94%	3Fh
1.00	9	91%	1Fh
1.04	A	88%	0Fh
1.08	B	85%	07h
1.12	C	82%	03h
1.16	D	79%	01h
1.2	E	76%	01h
>1.2	F	<76%	00h

Current Monitor

Refer to Equation 18 for the IMON pin current expression.

Referencing the “Simplified Application Circuit” on page 6, the IMON pin current flows through R_{imon}. The voltage across R_{imon} is expressed in Equation 39:

$$V_{Rimon} = 3 \times I_{droop} \times R_{imon} \quad \text{(EQ. 39)}$$

Rewriting Equation 38 gives Equation 40:

$$I_{droop} = \frac{I_o}{R_{droop}} \times LL \quad \text{(EQ. 40)}$$

Substitution of Equation 40 into Equation 39 gives Equation 41:

$$V_{Rimon} = \frac{3I_o \times LL}{R_{droop}} \times R_{imon} \quad \text{(EQ. 41)}$$

Rewriting Equation 41 and application of full load condition gives Equation 42:

$$R_{imon} = \frac{V_{Rimon} \times R_{droop}}{3I_o \times LL} \quad \text{(EQ. 42)}$$

For example, given LL = 1.9mΩ, R_{droop} = 2.825kΩ, V_{Rimon} = 2.7V at I_{omax} = 53A, Equation 42 gives R_{imon} = 25.2kΩ.

A capacitor C_{imon} can be paralleled with R_{imon} to filter the IMON pin voltage. The $R_{imon}C_{imon}$ time constant is the user’s choice. It is recommended to have a time constant long enough such that switching frequency ripples are removed.

Current Balancing

The ISL6363 achieves current balancing through matching the ISEN pin voltages. R_{isen} and C_{isen} form filters to remove the switching ripple of the phase node voltages. It is recommended to use a rather long $R_{isen}C_{isen}$ time constant such that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are R_s = 10kΩ and C_s = 0.22µF.

Optional Slew Rate Compensation Circuit for 1-Tick VID Transition

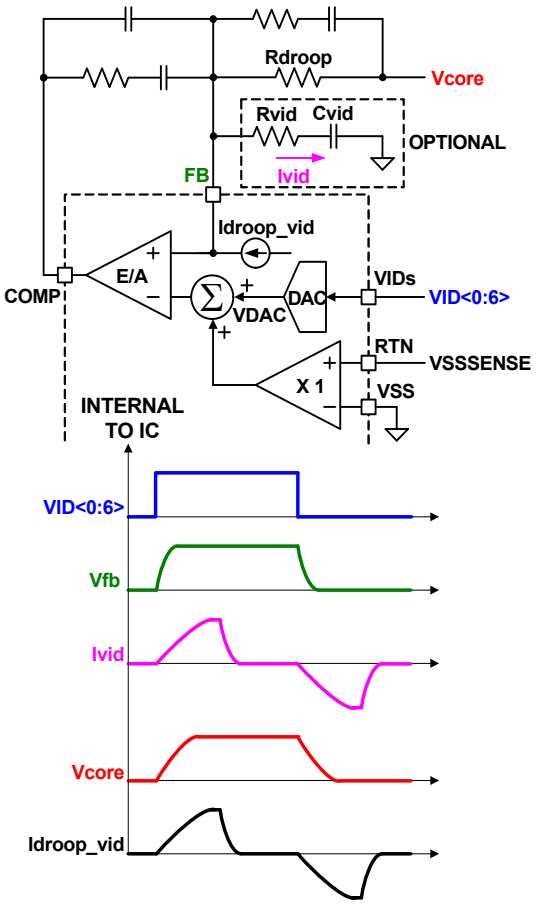


FIGURE 27. OPTIONAL SLEW RATE COMPENSATION CIRCUIT FOR 1-TICK VID TRANSITION

During a large VID transition, the DAC steps through the VIDs at a controlled slew rate. For example, the DAC may change a tick (5mV) per 0.5µs, controlling output voltage V_{CORE} slew rate at 10mV/µs.

Figure 27 shows the waveforms of 1-tick VID transition. During 1-tick VID transition, the DAC output changes at approximately 15mV/µs slew rate, but the DAC cannot step through multiple VIDs to control the slew rate. Instead, the control loop response speed determines V_{CORE} slew rate. Ideally, V_{CORE} will follow the FB pin voltage slew rate. However, the controller senses the inductor current increase during the up transition, as the I_{droop_vid} waveform shows, and will droop the output voltage V_{CORE} accordingly, making V_{CORE} slew rate slow. Similar behavior occurs during the down transition.

To control V_{CORE} slew rate during 1-tick VID transition, one can add the R_{vid}-C_{vid} branch, whose current I_{vid} cancels I_{droop_vid}.

When V_{CORE} increases, the time domain expression of the induced I_{droop} change is:

$$I_{droop}(t) = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \times \left(1 - e^{\frac{-t}{C_{out} \times LL}}\right) \quad \text{(EQ. 43)}$$

Where C_{out} is the total output capacitance.

In the mean time, the R_{vid}-C_{vid} branch current I_{vid} time domain expression is:

$$I_{vid}(t) = C_{vid} \times \frac{dV_{fb}}{dt} \times \left(1 - e^{\frac{-t}{R_{vid} \times C_{vid}}}\right) \quad \text{(EQ. 44)}$$

It is desired to let $I_{vid}(t)$ cancel $I_{droop\_vid}(t)$. So there are:

$$C_{vid} \times \frac{dV_{fb}}{dt} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \quad \text{(EQ. 45)}$$

and:

$$R_{vid} \times C_{vid} = C_{out} \times LL \quad \text{(EQ. 46)}$$

The result is expressed in Equation 47:

$$R_{vid} = R_{droop} \quad \text{(EQ. 47)}$$

and:

$$C_{vid} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{\frac{dV_{core}}{dt}}{\frac{dV_{fb}}{dt}} \quad \text{(EQ. 48)}$$

For example: given LL = 1.9mΩ, R_{droop} = 2.37kΩ, C_{out} = 1320µF, dV_{CORE}/dt = 10mV/µs and dV_{fb}/dt = 15mV/µs, Equation 47 gives R_{vid} = 2.37kΩ and Equation 48 gives C_{vid} = 700pF.

It is recommended to select the calculated R_{vid} value and start with the calculated C_{vid} value and tweak it on the actual board to get the best performance.

During normal transient response, the FB pin voltage is held constant, therefore is virtual ground in small signal sense. The R_{vid} - C_{vid} network is between the virtual ground and the real ground, and hence has no effect on transient response.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not guaranteed. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
September 5, 2013	FN6898.1	Stamped Not Recommend For New Designs No Recommended Replacement. Changed Products information verbiage to About Intersil verbiage. Updated Copyright on page 1 from Americas Inc to Americas LLC
September 29, 2011	FN6898.0	Initial Release.

About Intersil

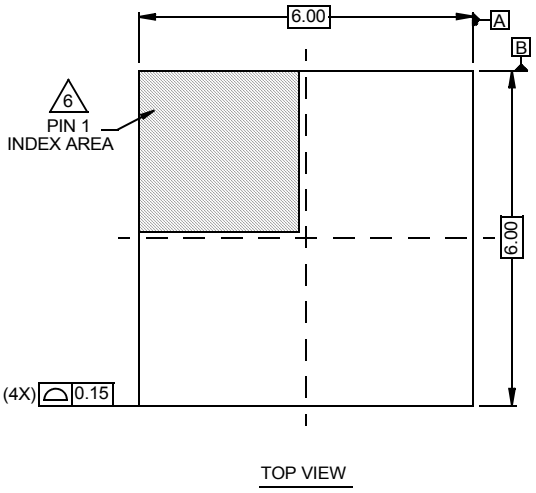
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

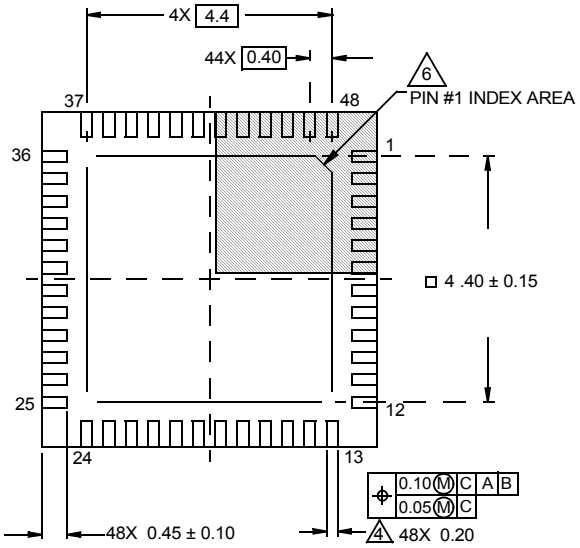
Package Outline Drawing

L48.6x6

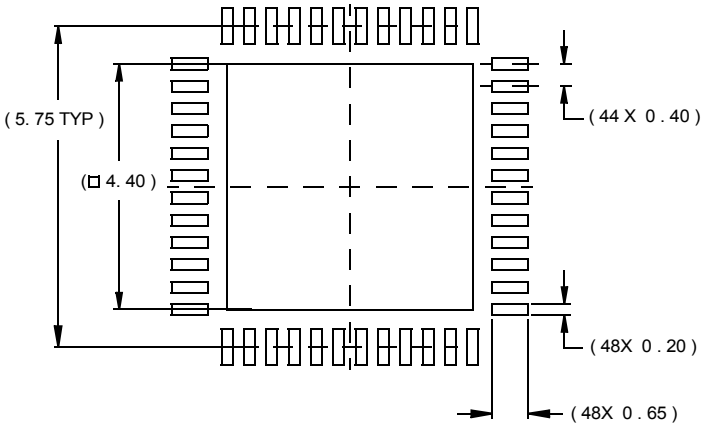
48 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 4/07



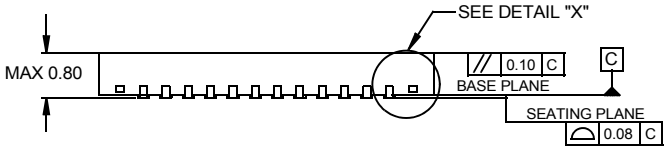
TOP VIEW



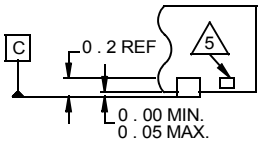
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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