THE DATASHEET OF

IR3088AMTRPBF

International
IOR Rectifier

IR3088APbF

DATA SHEET

XPHASE™ PHASE IC WITH FAULT AND OVERTEMP DETECT

DESCRIPTION

The IR3088A Phase IC combined with an IR *XPhase*™ Control IC provides a full featured and flexible way to implement power solutions for the latest high performance CPUs and ASICs. The "Control" IC provides overall system control and interfaces with any number of "Phase" ICs which each drive and monitor a single phase of a multiphase converter. The *XPhase*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

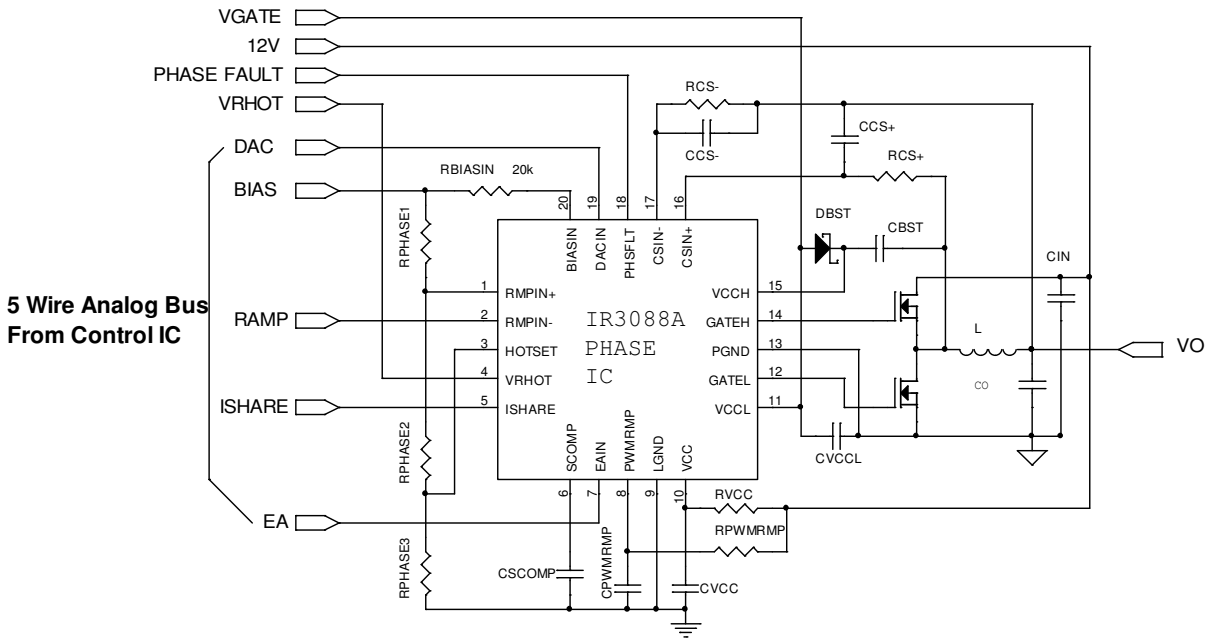
The IR3088A is intended for the following application conditions;

- Excessive impedance between converter and load
- Output voltage exceeding the control IC reference/VID voltage is desired

FEATURES

- 2.5A Average Gate Drive Current
- Loss-Less Inductor Current Sense
- Internal Inductor DCR Temperature Compensation
- Programmable Phase Delay
- Programmable Feed-Forward Voltage Mode PWM Ramp
- Sub 100ns Minimum Pulse Width supports 1MHz per-phase operation
- Current Sense Amplifier drives a single wire Average Current Share Bus
- Current Share Amplifier reduces PWM Ramp slope to ensure sharing between phases
- *Body Braking*™ disables Synchronous MOSFET for improved transient response and prevents negative output voltage at converter turn-off
- Phase Fault Detection
- Programmable Phase Over-Temperature Detection
- Control FET driver's 25V input voltage capability simplifies boot-strap supply design
- Small thermally enhanced 20L MLPQ package

APPLICATION CIRCUIT



ORDERING INFORMATION

Device	Order Quantity
IR3088AMTR	3000
* IR3088AM	100 piece strips

* Samples only

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……..150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC standard

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	RMPIN+	20V	-0.3V	1mA	1mA
2	RMPIN-	20V	-0.3V	1mA	1mA
3	HOTSET	20V	-0.3V	1mA	1mA
4	VRHOT	20V	-0.3V	1mA	30mA
5	ISHARE	20V	-0.3V	5mA	5mA
6	SCOMP	20V	-0.3V	1mA	1mA
7	EAIN	20V	-0.3V	1mA	1mA
8	PWMRMP	20V	-0.3V	1mA	20mA
9	LGND	n/a	n/a	50mA	n/a
10	VCC	24V	-0.3V	n/a	50mA
11	VCCL	27V	-0.3V	n/a	3A for 100ns, 200mA DC
12	GATEL	27V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
13	PGND	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
14	GATEH	27V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
15	VCCH	27V	-0.3V	n/a	3A for 100ns, 200mA DC
16	CSIN+	20V	-0.3V	1mA	1mA
17	CSIN-	20V	-0.3V	1mA	1mA
18	PHSFLT	20V	-0.3V	1mA	20mA
19	DACIN	20V	-0.3V	1mA	1mA
20	BIASIN	20V	-0.3V	1mA	1mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 8.4V ≤ V_{CC} ≤ 14V, 6V ≤ V_{CCH} ≤ 25V, 6V ≤ V_{CCL} ≤ 14V, 0 °C ≤ T_J ≤ 125 °C, C_{GATEH} = 3.3nF, C_{GATEL} = 6.8nF

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Gate Drivers					
GATEH Rise Time	VCCH = 12V, Measure 2V to 9V transition time		22	50	ns
GATEH Fall Time	VCCH = 12V, Measure 9V to 2V transition time		22	50	ns
GATEL Rise Time	VCCL = 12V, Measure 2V to 9V transition time		50	75	ns
GATEL Fall Time	VCCL = 12V, Measure 9V to 2V transition time		50	75	ns
GATEL low to GATEH high delay	VCCH = VCCL = 12V, Measure the time from GATEL falling to 1V to GATEH rising to 1V	10	25	50	ns
GATEH low to GATEL high delay	VCCH = VCCL = 12V, Measure the time from GATEH falling to 1V to GATEL rising to 1V	10	25	50	ns
Disable Pull-Down Current	Force GATEH or GATEL = 2V with BIASIN = 0V	15	25	40	µA
Current Sense Amplifier					
CSIN+ Bias Current		-0.5	-0.25	0	µA
CSIN- Bias Current		-0.5	-0.25	0	µA
Input Offset Voltage	CSIN+ = CSIN- = DACIN. Measure input referred offset from DACIN	-3	0.5	5	mV
Gain at T_J = 25 °C		32	34	36	V/V
Gain at T_J = 125 °C		27	29	31	V/V
Slew Rate	Current Sense Amplifier output is an internal node. Slew rate at the ISHARE pin will be set by the internal 10kΩ resistor and any stray external capacitance		12.5		V/µs
Differential Input Range		-20		100	mV
Common Mode Input Range		0		4	V
Rout at T_J = 25 °C		7.9	10.5	13.1	kΩ
Rout at T_J = 125 °C		9.3	12.4	15.5	kΩ
Ramp Discharge Clamp					
Clamp Voltage	Force I(PWMRMP) = 500µA. Measure V(PWMRMP) – V(DACIN)	-10	5	20	mV
Clamp Discharge Current		4	8		mA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Ramp Comparator					
Input Offset Voltage		20	40	80	mV
Hysteresis	Note 1	-10	0	10	mV
RMPIN+, RMPIN- Bias Current		-1	-0.5	1	µA
Propagation Delay	VCCH = 12V. Measure time from RMPIN input (50mV overdrive) to GATEL transition to <11V.	100	150	240	ns
PWM Comparator					
PWM Comparator Input Offset Voltage		-5	5	15	mV
EAIN & PWMRMP Bias Current	Clamp and Current Share Adjust OFF	-1	-0.4	1	µA
Propagation Delay	VCCH = 12V. Measure time from PWMRMP input (50mV overdrive) to GATEH transition to < 11V.		70	150	ns
Common Mode Input Range	Exceeding the Common Mode input range results in 100% duty cycle			5	V
Share Adjust Error Amplifier					
Input Offset Voltage		10	20	30	mV
Input Voltage Range	EAIN – PWMRMP, Note 1	-3.5		3.5	V
PWMRMP Adjust Current		4	8		mA
Transconductance	I(PWMRMP) = 3.5mA, Note 1	0.9	1.6	2.3	A/V
SCOMP Source/Sink Current	Note 1	20	30	40	µA
SCOMP Activation Voltage	Amount SCOMP must increase from its minimum voltage until the Ramp Slope Adjust current equals = 10µA	60	150	300	mV
PWMRMP Min Voltage	I(PWMRMP) = 500µA	150	225	350	mV
0% Duty Cycle Comparator					
Threshold Voltage	Compare to V(DACIN)	88	91	94	%
Propagation Delay	VCCL = 12V. Measure time from EAIN < 0.9 x V(DACIN) (200mV overdrive) to GATEL transition to < 11V. Note 1.		100	150	ns
Phase Fault Comparator					
Threshold Voltage	Compare to V(DACIN)	88	91	94	%
Output Voltage	I(PHSFLT) = 4mA		300	400	mV
PHSFLT Leakage Current	V(PHSFLT) = 5.5V		0	10	µA
VRHOT Comparator					
HOTSET Bias Current		-2	-0.5	1	µA
Output Voltage	I(VRHOT) = 29mA		150	400	mV
VRHOT Leakage Current	V(VRHOT) = 5.5V		0	10	µA
Threshold Hysteresis	$T_J \geq 85\,^{\circ}C$	3.0	7.0	9.0	°C

		MIN	TYP	MAX	
Threshold Voltage	$T_J \geq 85\,^{\circ}C$	4.73mV/°C x T_J + 1.176V	4.73mV/°C x T_J + 1.241V	4.73mV/°C x T_J + 1.356V	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
General					
VCC Supply Current			10	14	mA
VCCL Supply Current			2.5	5	mA
VCCH Supply Current	$6V \leq V_{CCH} \leq 14V$		5.5	8	mA
	$14V \leq V_{CCH} \leq 25V$		6.5	10	mA
BIASIN Bias Current		-5	-2.5	2	µA
DACIN Bias Current		-2	-0.5	1	µA

Note 1: Guaranteed by design, but not tested in production

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	RMPIN+	Non-inverting input to Ramp Comparator
2	RMPIN-	Inverting input to Ramp Comparator
3	HOTSET	Inverting input to VRHOT comparator. Connect resistor divider from VBIAS to LGND to program VRHOT threshold. Diode or thermistor may be substituted for lower resistor for enhanced/remote temperature sensing.
4	VRHOT	Open Collector output of the VRHOT comparator which drives low if IC junction temperature exceeds the user programmable limit. Connect external pull-up.
5	ISHARE	Output of the Current Sense Amplifier and input to the Share Adjust Error Amplifier. Voltage on this pin is equal to V(DACIN) + 34 * [V(CSIN+) – V(CSIN-)]. Connecting ISHARE pins together creates a Share Bus enabling current sharing between Phase ICs. The Share bus is also used by the Control IC for voltage positioning and Over-Current protection.
6	SCOMP	Compensation for the Current Share control loop. Connect a capacitor to ground to set the control loop's bandwidth.
7	EAIN	PWM comparator input from the error amplifier output of Control IC. Both Gate Driver outputs drive low if the voltage on this pin is less than 91% of V(DACIN).
8	PWMRMP	PWM comparator ramp input. Connect a resistor from this pin to the converter input voltage and a capacitor to LGND to program the PWM ramp.
9	LGND	Signal ground and IC substrate connection
10	VCC	Power for internal circuitry
11	VCCL	Power for Low-Side Gate Driver
12	GATEL	Low-Side Gate Driver Output and input to GATEH non-overlap comparator
13	PGND	Return for Gate Drivers
14	GATEH	High-Side Gate Driver Output and input to GATEL non-overlap comparator
15	VCCH	Power for High-Side Gate Driver
16	CSIN+	Non-inverting input to the Current Sense Amplifier
17	CSIN-	Inverting input to the Current Sense
18	PHSFLT	Open Collector output of the Phase Fault comparator. Drives low if Phase current is unable to match the level of the SHARE bus due to an external fault. Connect external pull-up.
19	DACIN	Reference voltage input from the Control IC. Current sensing and PWM operation referenced to this pin.
20	BIASIN	System reference voltage for internal circuitry

SYSTEM THEORY OF OPERATION

XPhase™ Architecture

The *XPhase*™ architecture is designed for multiphase interleaved buck converters which are used in applications requiring small size, design flexibility, low voltage, high current and fast transient response. The architecture can control converters of any phase number where flexibility facilitates the design trade-off of multiphase converters. The scalable architecture can be applied to other applications which require high current or multiple output voltages.

As shown in Figure 1, the *XPhase*™ architecture consists of a Control IC and a scalable array of phase converters each using a single Phase IC. The Control IC communicates with the Phase ICs through a 5-wire analog bus, i.e. bias voltage, phase timing, average current, error amplifier output, and VID voltage. The Control IC incorporates all the system functions, i.e. VID, PWM ramp oscillator, error amplifier, bias voltage, and fault protections etc. The Phase IC implements the functions required by the converter of each phase, i.e. the gate drivers, PWM comparator and latch, over-voltage protection, and current sensing and sharing.

There is no unused or redundant silicon with the *XPhase*™ architecture compared to others such as a 4 phase controller that can be configured for 2, 3, or 4 phase operation. PCB Layout is easier since the 5 wire bus eliminates the need for point-to-point wiring between the Control IC and each Phase. The critical gate drive and current sense connections are short and local to the Phase ICs. This improves the PCB layout by lowering the parasitic inductance of the gate drive circuits and reducing the noise of the current sense signal.

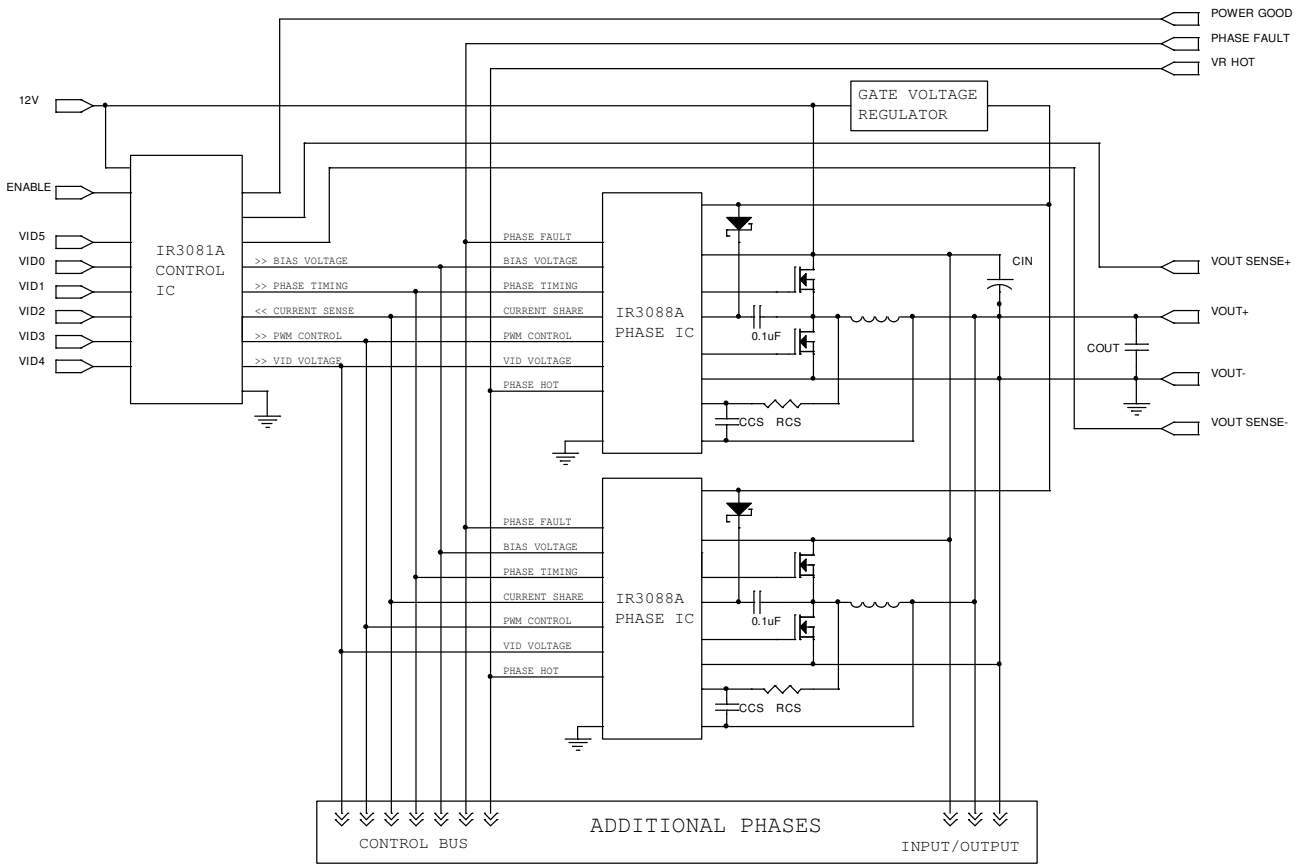


Figure 1. System Block Diagram

PWM Control Method

The PWM block diagram of the *XPhase*™ architecture is shown in Figure 2. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed-forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

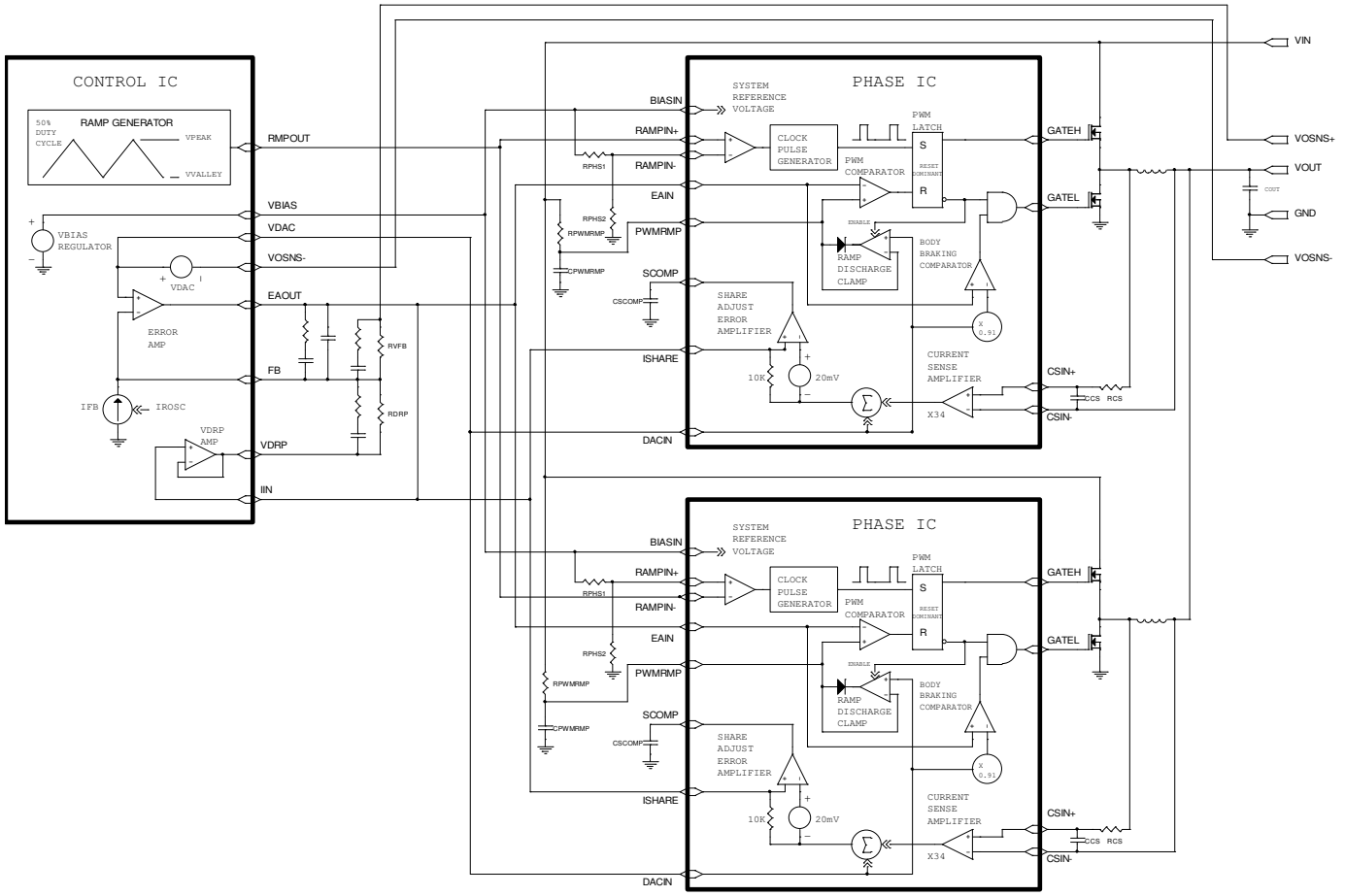


Figure 2. PWM Block Diagram

Frequency and Phase Timing Control

An oscillator with programmable frequency is located in the Control IC. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 5V and 1V respectively. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider R_{PHS1} and R_{PHS2} connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform over the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 3 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for phase timing by swapping the RMPIN+ and RMPIN– pins, as shown in Figure 2.

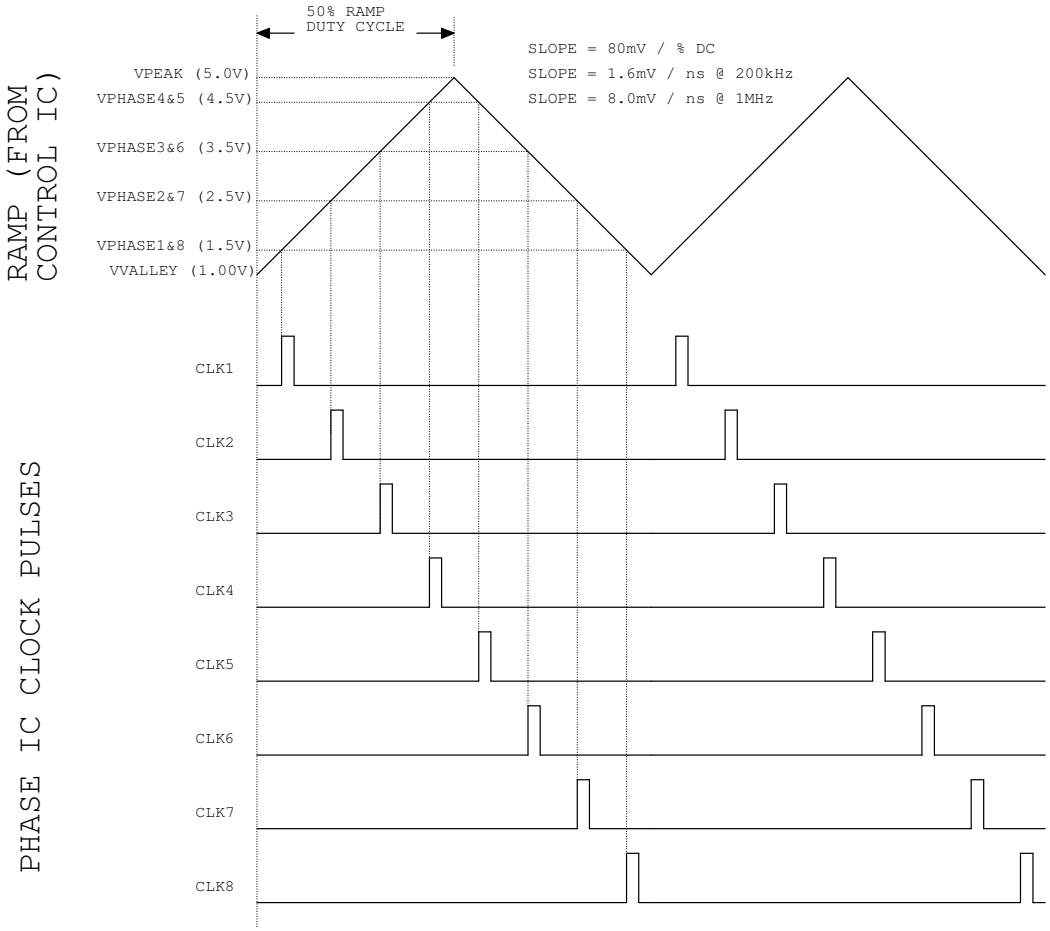


Figure 3. 8 Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set; the PWMRMP voltage begins to increase; the low side driver is turned off, and the high side driver is then turned on after the non-overlap time. When the PWMRMP voltage exceeds the Error Amplifier's output voltage, the PWM latch is reset. This turns off the high side driver and then turns on the low side driver after the non-overlap time; it activates the Ramp Discharge Clamp, which quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 4 depicts PWM operating waveforms under various conditions.

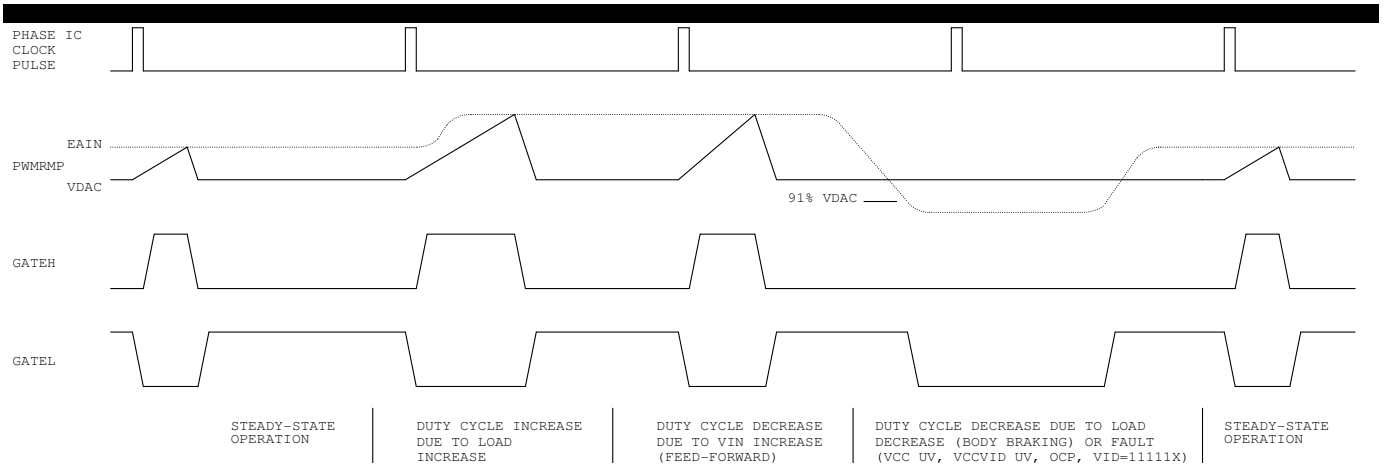


Figure 4. PWM Operating Waveforms

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "0% Duty Cycle Comparator" located in the Phase IC. If the Error Amplifier's output voltage drops below 91% of the VDAC voltage this comparator turns off the low side gate driver.

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a resistor and a capacitor in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 5. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

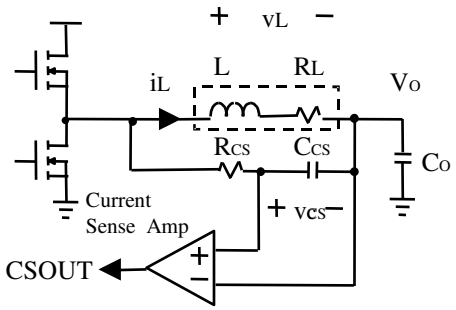


Figure 5. Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

This is a high speed differential current sense amplifier, as shown in Figure 5. Its gain decreases with increasing temperature and is nominally 34 at 25ºC and 29 at 125ºC (-1470 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to -20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current being delivered to the load and is used by the Control IC for voltage positioning and current limit protection.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each Phase IC. The output of the current sense amplifier is compared with the share bus less a 20mV offset. If current in a phase is smaller than the average current, the share adjust error amplifier of the phase will activate a current source that reduces the slope of its PWM ramp thereby increasing its duty cycle and output current. The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop.

IR3088A THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3088A is shown in figure 6, and specific features are discussed in the following sections.

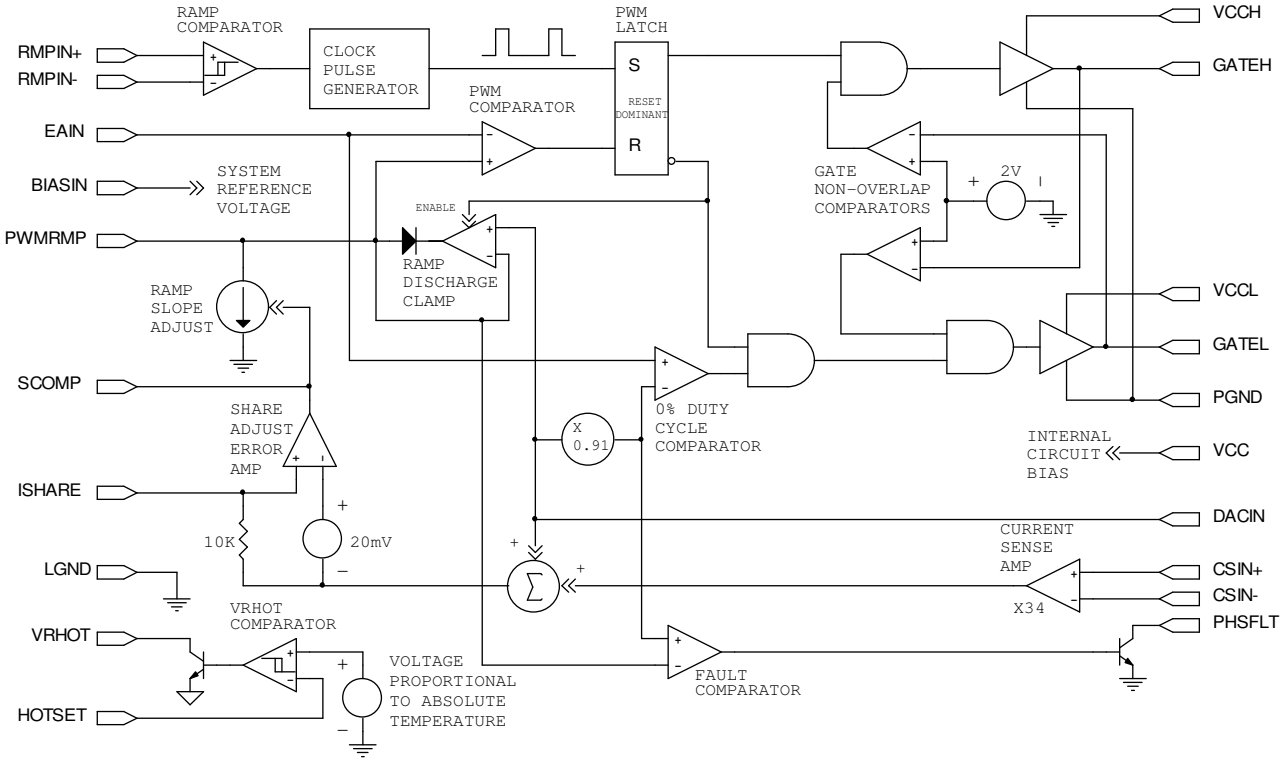


Figure 6. IR3088A Block Diagram

Tri-State Gate Drivers

The gate drivers can deliver up to 3A peak current. An adaptive non-overlap circuit monitors the voltage on the GATEH and GATEL pins to prevent MOSFET shoot-through current while minimizing body diode conduction.

An Enable signal is provided by the Control IC to the Phase IC without the addition of a dedicated signal line. The Error Amplifier output of the Control IC drives low in response to any fault condition such as input under voltage or output overload. The IR3088A 0% duty cycle comparator detects this and drives both gate outputs low. This tri-state operation prevents negative inductor current and negative output voltage during power-down.

The Gate Drivers revert to a high impedance “off” state if VCCL and VCCH supply voltages are below the normal operating range. An 80kΩ resistor is connected across the GATEH/GATEL and PGND pins to prevent the GATEH/GATEL voltage from rising due to leakage or other cause under these conditions.

Thermal Monitoring (VRHOT)

The IR3088A senses its own die temperature and produces a voltage at the input of the VRHOT comparator that is proportional to temperature. An external resistor divider connected from VBIAS to the HOTSET pin and ground can be used to program the thermal trip point of the VRHOT comparator. The VRHOT pin is an open-collector output and should be pulled up to a voltage source through a resistor. If the thermal trip point is reached the VRHOT output drives low.

Phase Fault

It is possible for multiphase converters to appear to be working correctly with one or more phases not functioning. The output voltage can still be regulated and the full load current may still be delivered. However, the remaining phase(s) will be stressed far beyond their intended design limits and are likely to fail. Loss of a phase can occur due to poor solder connections or mounting during the manufacturing process, or can occur in the field. The most common failure mode of a buck converter is failure of the high side MOSFET. The IR3088A has the ability to detect if a phase stops switching and can provide this information to the system through the PHSFLT output pin. If a phase stops switching its output current will drop to zero and the output of its IR3088A current sense amplifier will be the DACIN voltage. The Share Adjust Amplifier reacts to this by increasing the Ramp Slope Adjust current until it exceeds the externally programmable PWM Ramp bias current. This will cause the voltage at the PWMRMP pin to drop below its normal operating range. The Fault Comparator trips and drives the PHSFLT output to ground when the voltage on the PWMRMP pin falls below 91% of the DACIN voltage. PHSFLT is an open-collector output and should be pulled up to a voltage source through a resistor.

APPLICATIONS INFORMATION

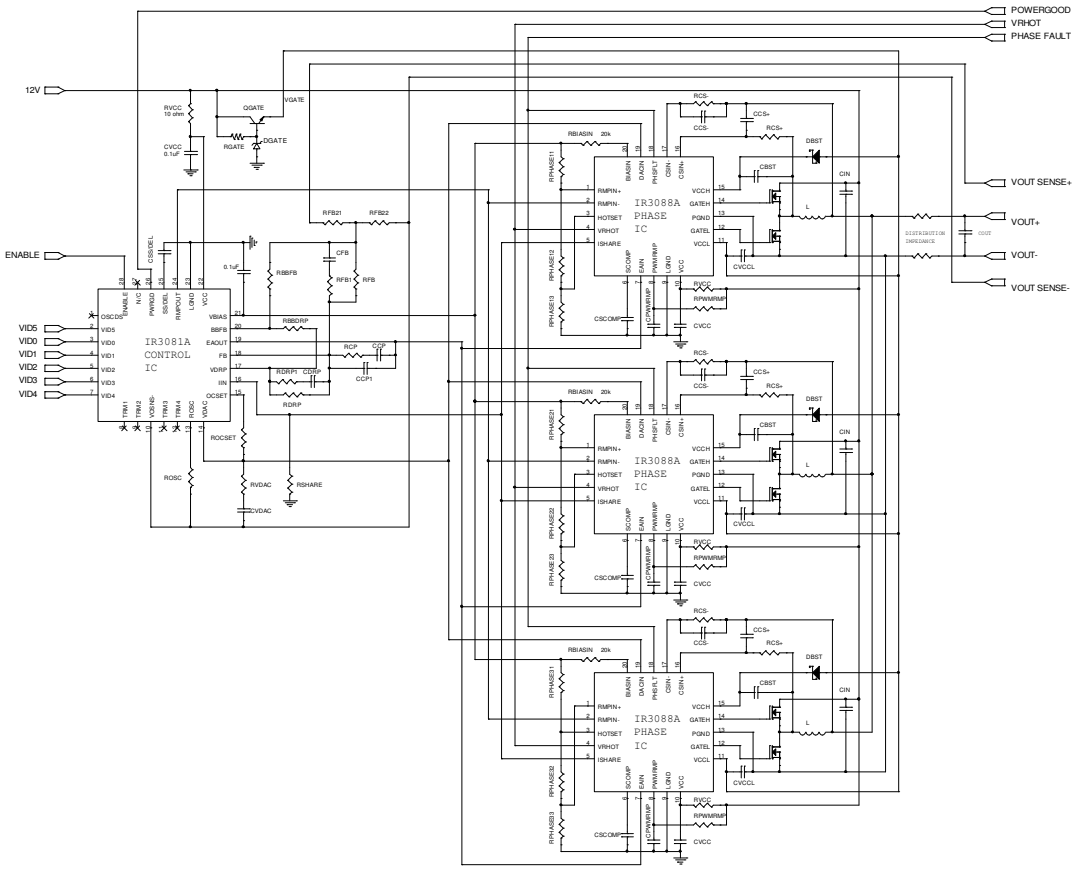


Figure 7. IR3081A/3088A 12V to 2.5V 3 Phase Converter

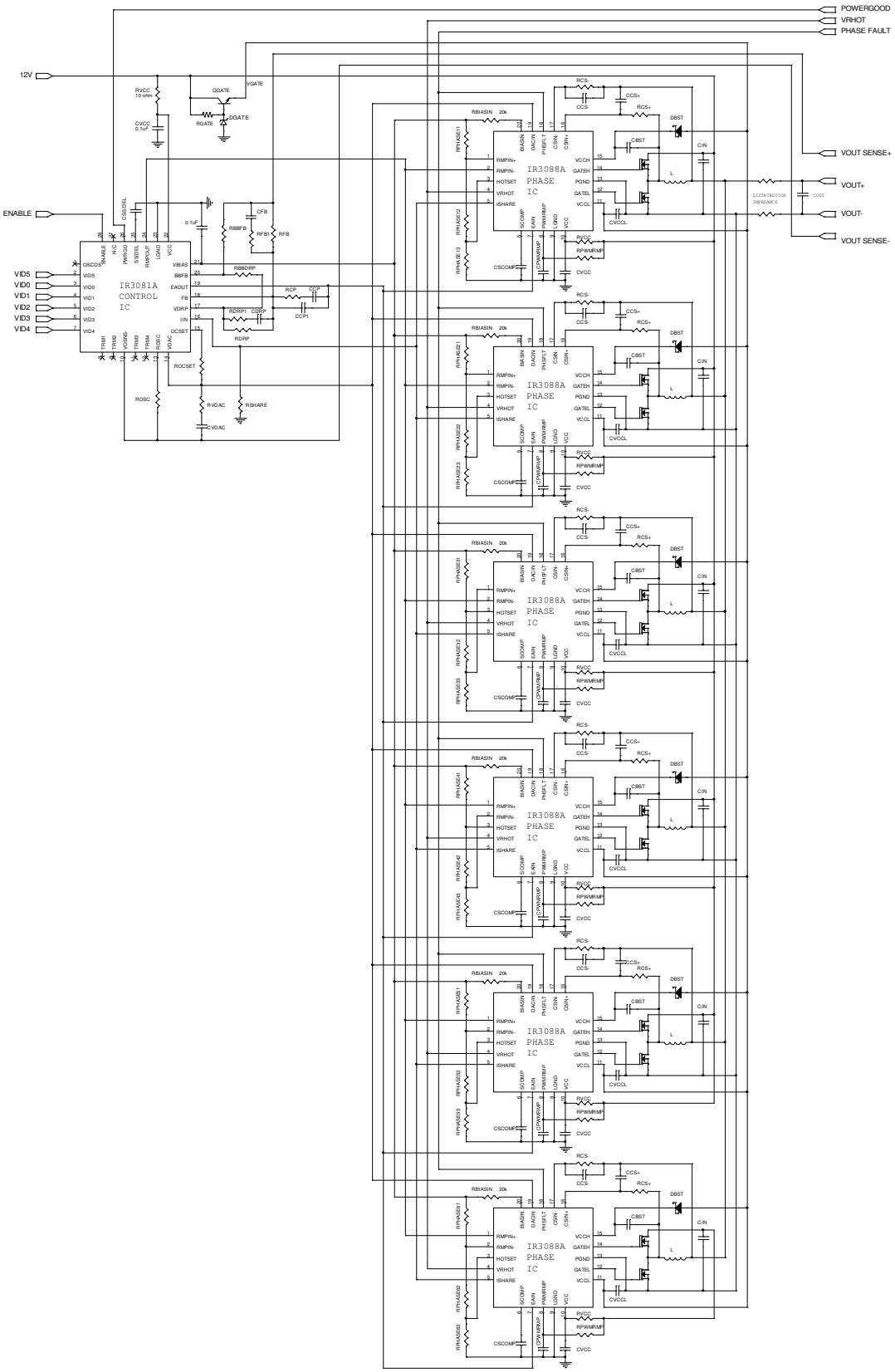


Figure 8. 6 Phase IR3081A/3088A VRM/EVRD10 Converter

DESIGN PROCEDURES - IR3081A AND IR3088A CHIPSET

IR3081A EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

The oscillator of IR3081A generates a triangle waveform to synchronize the phase ICs, and the switching frequency of the each phase converter equals the oscillator frequency, which is set by the external resistor ROSC according to the curve in Figure 13 of IR3081A Data Sheet.

Soft Start Capacitor *CSS/DEL*

Because the capacitor CSS/DEL programs four different time parameters, i.e. soft start delay time, soft start time, over-current latch delay time, and power good delay time, they should be considered together while choosing CSS/DEL.

The SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 10 of IR3081A data sheet. After the ENABLE pin voltage rises above 0.6V, there is a soft-start delay time tSSDEL, after which the error amplifier output is released to allow the soft start. The soft start time tSS represents the time during which converter voltage rises from zero to VO. tSS can be programmed by an external capacitor, which is determined by Equation (1).

$$C_{SS/DEL} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{70 * 10^{-6} * t_{SS}}{V_O} \quad (1)$$

Once CSS/DEL is chosen, the soft start delay time tSSDEL, the over-current fault latch delay time tOCDEL, and the delay time tVccPG from output voltage (VO) in regulation to Power Good are fixed and shown in Equations (2), (3) and (4) respectively.

$$t_{SSDEL} = \frac{C_{SS/DEL} * 1.3}{I_{CHG}} = \frac{C_{SS/DEL} * 1.3}{70 * 10^{-6}} \quad (2)$$

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.115}{I_{OCDISCHG}} = \frac{C_{SS/DEL} * 0.115}{40 * 10^{-6}} \quad (3)$$

$$t_{VccPG} = \frac{C_{SS/DEL} * (3.8 - 0.065 - V_O - 1.3)}{I_{CHG}} = \frac{C_{SS/DEL} * (3.735 - V_O - 1.3)}{70 * 10^{-6}} \quad (4)$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VDAC down-slope SRDOWN can be programmed by the external capacitor CVDAC as defined in Equation(5), where ISINK is the sink current of VDAC pin as shown in Figure 15 of IR3081A Data Sheet. The resistor RVDAC is used to compensate VDAC circuit and is determined by Equation (6). The slew rate of VDAC up-slope SRUP is proportional to that of VDAC down-slope and is given by Equation (7), where ISOURCE is the source current of VDAC pin as shown in Figure15 of IR3081A Data Sheet.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} \quad (5)$$

$$R_{VDAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VDAC}^{\ 2}} \quad (6)$$

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} \quad (7)$$

Over Current Setting Resistor *ROCSET*

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 ppm/℃, and therefore the maximum inductor DCR can be calculated from Equation (8), where R_{L_MAX} and R_{L_ROOM} are the inductor DCR at maximum temperature T_{L_MAX} and room temperature $T_{\_ROOM}$ respectively.

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})] \quad (8)$$

The current sense amplifier gain of IR3088A decreases with temperature at the rate of 1470 ppm/℃, which compensates part of the inductor DCR increase. The phase IC die temperature is only a couple of degrees Celsius higher than the PCB temperature due to the low thermal impedance of MLPQ package. The minimum current sense amplifier gain at the maximum phase IC temperature T_{IC_MAX} is calculated from Equation (9).

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470 * 10^{-6} * (T_{IC\_MAX} - T_{ROOM})] \quad (9)$$

The total input offset voltage (V_{CS_TOFST}) of current sense amplifier in phase ICs is the sum of input offset (V_{CS_OFST}) of the amplifier itself and that created by the amplifier input bias currents flowing through the current sense resistors R_{CS+} and R_{CS-}.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS+} - I_{CSIN-} * R_{CS-} \quad (10)$$

The over current limit is set by the external resistor R_{OCSET} as defined in Equation (11), where I_{LIMIT} is the required over current limit. I_{OCSET}, the bias current of OCSET pin, changes with switching frequency setting resistor R_{OSC} and is determined by the curve in Figure 14 of IR3081A Data Sheet. K_P is the ratio of inductor peak current over average current in each phase and is calculated from Equation (12).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS\_MIN} / I_{OCSET} \quad (11)$$

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_O / n} \quad (12)$$

No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP*

A resistor between FB pin and the converter output is used to create output voltage offset V_{O_NLOFST}, which is the difference between V_{DAC} voltage and output voltage at no load condition. Adaptive voltage positioning further lowers the converter voltage by R_O*I_O, where R_O is the required output impedance of the converter.

R_{FB} is not only determined by I_{FB}, the current flowing out of FB pin as shown in Figure 14 of IR3081A Data Sheet, but also affected by the adaptive voltage positioning resistor R_{DRP} and total input offset voltage of current sense amplifiers. R_{FB} and R_{DRP} are determined by (13) and (14) respectively.

$$R_{FB} = \frac{R_{L\_MAX} * V_{O\_NLOFST} - V_{CS\_TOFST} * n * R_O}{I_{FB} * R_{L\_MAX}} \quad (13)$$

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS\_MIN}}{n * R_O} \quad (14)$$

Body Braking™ Related Resistors *RBBFB* and *RBBDRP*

The body braking™ during Dynamic VID can be disabled by connecting BBFB pin to ground. If the feature is enabled, Resistors R_{BBFB} and R_{BBDRP} are needed to restore the feedback voltage of the error amplifier after Dynamic VID step down. Usually R_{BBFB} and R_{BBDRP} are chosen to match R_{FB} and R_{DRP} respectively.

IR3088A EXTERNAL COMPONENTS

PWM Ramp Resistor *RPWMRMP* and Capacitor C*PWMRMP*

PWM ramp is generated by connecting the resistor RPWMRMP between a voltage source and PWMRMP pin as well as the capacitor CPWMRMP between PWMRMP and LGND. Choose the desired PWM ramp magnitude VRAMP and the capacitor CPWMRMP in the range of 100pF and 470pF, and then calculate the resistor RPWMRMP from Equation (15). To achieve feed-forward voltage mode control, the resistor RPWMRMP should be connected to the input of the converter.

$$R_{PWMRMP} = \frac{V_O}{V_{IN} * f_{SW} * C_{PWMRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]} \quad (15)$$

Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor RCS+ and capacitor CCS+ in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor CCS+ represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affect the current signal ISHARE as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.
Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor CCS+ and calculate RCS+ as follows.

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} \quad (16)$$

The bias current flowing out of the non-inverting input of the current sense amplifier creates a voltage drop across RCS+, which is equivalent to an input offset voltage of the current sense amplifier. The offset affects the accuracy of converter current signal ISHARE as well as the accuracy of the converter output voltage if adaptive voltage positioning is adopted. To reduce the offset voltage, a resistor RCS- should be added between the amplifier inverting input and the converter output.

$$R_{CS-} = R_{CS+} \quad (17)$$

If RCS- is not used, RCS+ should be chosen so that the offset voltage is small enough. Usually RCS+ should be less than 2 kΩ and therefore a larger CCS+ value is needed.

Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

The threshold voltage of VRHOT comparator is proportional to the die temperature TJ (ºC) of phase IC. Determine the relationship between the die temperature of phase IC and the temperature of the power converter according to the power loss, PCB layout and airflow etc, and then calculate HOTSET threshold voltage corresponding to the allowed maximum temperature from Equation (18).

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 \quad (18)$$

There are two ways to set the over temperature threshold, central setting and local setting. In the central setting, only one resistor divider is used, and the setting voltage is connected to HOTSET pins of all the phase ICs. To reduce the influence of noise on the accuracy of over temperature setting, a 0.1uF capacitor should be placed next to HOTSET pin of each phase IC. In the local setting, a resistor divider per phase is needed, and the setting voltage is connected to HOTSET pin of each phase. The 0.1uF decoupling capacitor is not necessary. Use VBIAS as the reference voltage. If RHOTSET1 is pre-selected, RHOTSET2 can be calculated as follows.

$$R_{HOTSET2} = \frac{R_{HOTSET1} * V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} \quad (19)$$

Phase Delay Timing Resistors *RPHASE1* and *RPHASE2*

The phase delay of the interleaved multiphase converter is programmed by the resistor divider connected at RMPIN+ or RMPIN- depending on which slope of the oscillator ramp is used for the phase delay programming of phase IC, as shown in Figure 3.

If the upslope is used, RMPIN+ pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN- pin should be connected to the resistor divider. When RMPOUT voltage is above the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

If down slope is used, RMPIN- pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN+ pin should be connected to the resistor divider. When RMPOUT voltage is below the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

Use VBIAS voltage as the reference for the resistor divider since the oscillator ramp magnitude from control IC tracks VBIAS voltage. Try to avoid both edges of the oscillator ramp for better noise immunity. Determine the ratio of the programming resistors corresponding to the desired switching frequencies and phase numbers. If the resistor $R_{PHASEx1}$ is pre-selected, the resistor $R_{PHASEx2}$ is determined as:

$$R_{PHASEx2} = \frac{RA_{PHASEx} * R_{PHASEx1}}{1 - RA_{PHASEx}} \quad (20)$$

Combined Over Temperature and Phase Delay Setting Resistors *RPHASE1*, *RPHASE2* and *RPHASE3*

The over temperature setting resistor divider can be combined with the phase delay resistor divider to save one resistor per phase.

Calculate the HOTSET threshold voltage V_{HOTSET} corresponding to the allowed maximum temperature from Equation (18). If the over temperature setting voltage is lower than the phase delay setting voltage, VBIAS*RA_{PHASEx}, connect RMPIN+ or RMPIN- pin between $R_{PHASEx1}$ and $R_{PHASEx2}$, and connect HOTSET pin between $R_{PHASEx2}$ and $R_{PHASEx3}$. Pre-select $R_{PHASEx1}$,

$$R_{PHASEx2} = \frac{(RA_{PHASEx} * V_{BIAS} - V_{HOTSET}) * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} \quad (21)$$

$$R_{PHASEx3} = \frac{V_{HOTSET} * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} \quad (22)$$

If the over temperature setting voltage is higher than the phase delay setting voltage, VBIAS*RA_{PHASEx}, connect HOTSET pin between $R_{PHASEx1}$ and $R_{PHASEx2}$, and connect RMPIN+ or RMPIN- between $R_{PHASEx2}$ and $R_{PHASEx3}$. Pre-select $R_{PHASEx1}$,

$$R_{PHASEx2} = \frac{(V_{HOTSET} - RA_{PHASEx} * V_{BIAS}) * R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (23)$$

$$R_{PHASEx3} = \frac{RA_{PHASEx} * V_{BIAS} * R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (24)$$

Bootstrap Capacitor *CBST*

Depending on the duty cycle and gate drive current of the phase IC, a 0.1uF to 1uF capacitor is needed for the bootstrap circuit.

Decoupling Capacitors for Phase IC

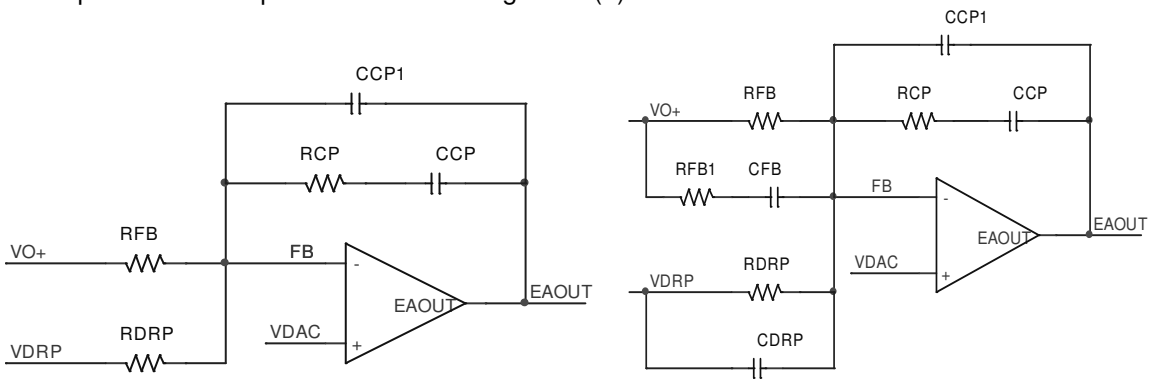
0.1uF-1uF decoupling capacitors are required at VCC and VCCL pins of phase ICs.

VOLTAGE LOOP COMPENSATION

The adaptive voltage positioning (AVP) is usually adopted in the computer applications to improve the transient response and reduce the power loss at heavy load. Like current mode control, the adaptive voltage positioning loop introduces extra zero to the voltage loop and splits the double poles of the power stage, which make the voltage loop compensation much easier.

Resistors R_{FB} and R_{DRP} are chosen according to Equations (13) and (14), and the selection of compensation types depends on the output capacitors used in the converter. For the applications using Electrolytic, Polymer or AL-Polymer capacitors and running at lower frequency, type II compensation shown in Figure 12(a) is usually enough. While for the applications using only ceramic capacitors and running at higher frequency, type III compensation shown in Figure 12(b) is preferred.

For applications where AVP is not required, the compensation is the same as for the regular voltage mode control. For converter using Polymer, AL-Polymer, and ceramic capacitors, which have much higher ESR zero frequency, type III compensation is required as shown in Figure 12(b) with R_{DRP} and C_{DRP} removed.



(a) Type II compensation (b) Type III compensation

Figure 12. Voltage loop compensation network

Type II Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, and determine R_{CP} and C_{CP} from Equations (25) and (26), where L_E and C_E are the equivalent inductance of output inductors and the equivalent capacitance of output capacitors respectively.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{PWMRMP}}{V_O * \sqrt{1 + (2\pi * f_C * C * R_C)^2}} \quad (25)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (26)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for AVP Applications

Determine the compensation at no load, the worst case condition. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, the crossover frequency and phase margin of the voltage loop can be estimated by Equations (27) and (28), where R_{LE} is the equivalent resistance of inductor DCR.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} \quad (27)$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} \quad (28)$$

Choose the desired crossover frequency fc around fc1 estimated by Equation (27) or choose fc between 1/10 and 1/5 of the switching frequency per phase, and select the components to ensure the slope of close loop gain is -20dB /Dec around the crossover frequency. Choose resistor R_{FB1} according to Equation (29), and determine C_{FB} and R_{DRP} from Equations (30) and (31).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \quad (29)$$

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} \quad (30)$$

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} \quad (31)$$

R_{CP} and C_{CP} have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Determine R_{CP} and C_{CP} from Equations (32) and (33).

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{PWMRMP}}{V_O} \quad (32)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (33)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for Non-AVP Applications

Resistor R_{FB} is chosen according to Equations (13), and resistor R_{DRP} and capacitor C_{DRP} are not needed. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase and select the desired phase margin θc. Calculate K factor from Equation (34), and determine the component values based on Equations (35) to (39),

$$K = \tan[\frac{\pi}{4} * (\frac{\theta_C}{180} + 1.5)] \quad (34)$$

$$R_{CP} = R_{FB} * \frac{(2\pi * \sqrt{L_E * C_E} * f_C)^2 * V_{PWMRMP}}{V_O * K} \quad (35)$$

$$C_{CP} = \frac{K}{2\pi * f_C * R_{CP}} \quad (36)$$

$$C_{CP1} = \frac{1}{2\pi * f_C * K * R_{CP}} \quad (37)$$

$$C_{FB} = \frac{K}{2\pi * f_C * R_{FB}} \quad (38)$$

$$R_{FB1} = \frac{1}{2\pi * f_C * K * C_{FB}} \quad (39)$$

CURRENT SHARE LOOP COMPENSATION

The crossover frequency of the current share loop should be at least one decade lower than that of the voltage loop in order to eliminate the interaction between the two loops. A capacitor from SCOMP to ground is usually enough for the share loop compensation. Choose the crossover frequency of current share loop (f_{CI}) based on the crossover frequency of voltage loop (f_C), and determine the C_{SCOMP},

$$C_{SCOMP} = \frac{0.65 * R_{PWMRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6} \quad (40)$$

Where F_{MI} is the PWM gain in the current share loop,

$$F_{MI} = \frac{R_{PWMRMP} * C_{PWMRMP} * f_{SW} * V_{PWMRMP}}{(V_I - V_{PWMRMP} - V_{DAC}) * (V_I - V_{DAC})} \quad (41)$$

DESIGN EXAMPLE 1 - VRM 10 2U CONVERTER

SPECIFICATIONS

Input Voltage: V_I=12 V
DAC Voltage: V_{DAC}=1.35 V
No Load Output Voltage Offset: V_{O_NLOFST}=20 mV
Output Current: I_O=105 ADC
Maximum Output Current: I_{OMAX}=120 ADC
Output Impedance: R_O=0.91 mΩ
VCC Ready to VCC Power Good Delay: t_{VccPG}=0-10mS
Soft Start Time: t_{SS}=2 mS
Over Current Delay: t_{OCDEL}=0.5mS
Dynamic VID Down-Slope Slew Rate: SR_{DOWN}=2.5mV/uS
Over Temperature Threshold: T_{PCB}=115 ºC

POWER STAGE

Phase Number: n=6
Switching Frequency: f_{SW}=400 kHz
Output Inductors: L=220 nH, R_L=0.47 mΩ
Output Capacitors: AL-Polymer, C=560uF, R_C= 7mΩ, Number Cn=10

IR3081A EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

Once the switching frequency is chosen, R_{OSC} can be determined from the curve in Figure 13 of IR3081A Data Sheet. For switching frequency of 400kHz per phase, choose R_{OSC}=30.1kΩ

Soft Start Capacitor *CSS/DEL*

Determine the soft start capacitor from the required soft start time.

$$C_{SS/DEL} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{70*10^{-6} * 2*10^{-3}}{1.35 - 20*10^{-3}} = 0.1uF$$

The soft start delay time is

$$t_{SSDEL} = \frac{C_{SS/DEL} * 1.3}{I_{CHG}} = \frac{0.1*10^{-6} * 1.3}{70*10^{-6}} = 1.86mS$$

The power good delay time is

$$t_{VccPG} = \frac{C_{SS/DEL} * (3.735 - V_O - 1.3)}{I_{CHG}} = \frac{0.1*10^{-6} * (3.735 - 1.33 - 1.3)}{70*10^{-6}} = 1.58ms$$

Over current delay time is

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.115}{I_{OCDISCHG}} = \frac{0.1*10^{-6} * 0.115}{40*10^{-6}} = 0.29ms$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

From Figure 15 of IR3081A Data Sheet, the sink current of VDAC pin corresponding to 400kHz (ROSC=30.1kΩ) is 76uA. Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{76*10^{-6}}{2.5*10^{-3}/10^{-6}} = 30.4nF$$, Choose CVDAC=33nF

Calculate the programming resistor.

$$R_{VDAC} = 0.5 + \frac{3.2*10^{-15}}{C_{VDAC}{}^2} = 0.5 + \frac{3.2*10^{-15}}{(33*10^{-9})^2} = 3.5\Omega$$

From Figure 15 of IR3081A Data Sheet, the source current of VDAC pin is 110uA. The VDAC up-slope slew rate is

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} = \frac{110*10^{-6}}{33*10^{-9}} = 3.3mV/uS$$

Over Current Setting Resistor *ROCSET*

The room temperature is 25ºC and the target PCB temperature is 100 ºC. The phase IC die temperature is about 1 ºC higher than that of phase IC, and the inductor temperature is close to PCB temperature.

Calculate Inductor DC resistance at 100 ºC,

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850*10^{-6} * (T_{L\_MAX} - T_{ROOM})] = 0.47*10^{-3} * [1 + 3850*10^{-6} * (100 - 25)] = 0.61m\Omega$$

The current sense amplifier gain is 34 at 25ºC, and its gain at 101ºC is calculated as,

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470*10^{-6} * (T_{IC\_MAX} - T_{ROOM})] = 34 * [1 - 1470*10^{-6} * (101 - 25)] = 30.2$$

Set the over current limit at 135A. From Figure 14 of IR3081A Data Sheet, the bias current of OCSET pin (IOCSET) is 41uA with ROSC=30.1kΩ. The total current sense amplifier input offset voltage is 0.55mV, which includes the offset created by the current sense amplifier input resistor mismatch.
Calculate constant KP, the ratio of inductor peak current over average current in each phase,

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_{LIMIT} / n} = \frac{(12 - 1.33) * 1.33 / (220*10^{-9} * 12 * 400*10^3 * 2)}{135/6} = 0.3$$

$$R_{OCSET} = [\frac{R_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS\_MIN} / I_{OCSET}$$

$$= (\frac{135}{6} * 0.61*10^{-3} * 1.3 + 0.55*10^{-3}) * 30.2 / (41*10^{-6}) = 13.3k\Omega$$

No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP*

From Figure 14 of IR3081A Data, the bias current of FB pin is 41uA with ROSC=30.1kΩ.

$$R_{FB} = \frac{R_{L\_MAX} * V_{O\_NLOFST} - V_{CS\_TOFST} * n * R_O}{I_{FB} * R_{L\_MAX}} = \frac{0.61*10^{-3} * 20*10^{-3} - 0.55*10^{-3} * 6 * 0.91*10^{-3}}{41*10^{-6} * 0.61*10^{-3}} = 365\Omega$$

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS\_MIN}}{n * R_O} = \frac{365 * 0.61*10^{-3} * 30.2}{6 * 0.91*10^{-3}} = 1.21k\Omega$$

Body Braking Related Resistors *RBBFB* and *RBBDRP*

N/A. The body braking during Dynamic VID is disabled.

IR3088A EXTERNAL COMPONENTS

PWM Ramp Resistor *RPWMRMP* and Capacitor C*PWMRMP*

Set PWM ramp magnitude VPWMRMP=0.8V. Choose 220pF for PWM ramp capacitor CPWMRMP, and calculate the resistor RPWMRMP,

$$R_{PWMRMP} = \frac{V_O}{V_{IN} * f_{SW} * C_{PWMRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]}$$

$$= \frac{1.33}{12 * 400 * 10^3 * 220 * 10^{-12} * [\ln(12 - 1.35) - \ln(12 - 1.35 - 0.8)]} = 16.1k\Omega$$, choose RPWMRMP=16.2kΩ

Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-*

Choose CCS+=47nF, and calculate RCS+,

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} = \frac{220 * 10^{-9} / (0.47 * 10^{-3})}{47 * 10^{-9}} = 10.0k\Omega$$

The bias currents of CSIN+ and CSIN- are 0.25uA and 0.4uA respectively. Calculate resistor RCS-,

$$R_{CS-} = R_{CS+} = 10.0k\Omega$$

Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2*

Use central over-temperature setting and set the temperature threshold at 115 ºC, which corresponds to the IC die temperature of 116 ºC. Calculate the HOTSET threshold voltage corresponding to the temperature thresholds.

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 = 4.73 * 10^{-3} * 116 + 1.241 = 1.79V$$

Pre-select RHOTSET1=10.0kΩ,

$$R_{HOTSET2} = \frac{R_{HOTSET1} * V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} = \frac{10 * 10^3 * 1.79}{6.8 - 1.79} = 3.57k\Omega$$

Phase Delay Timing Resistors *RPHASE1* and *RPHASE2*

Use central over temperature setting and set the temperature threshold at 115 ºC, which corresponds to the IC die temperature of 116 ºC. Calculate the HOTSET threshold voltage corresponding to the temperature thresholds.

The phase delay resistor ratios for phases 1 to 6 at 400kHz of switching frequencies are RAPHASE1=0.628, RAPHASE2=0.415, RAPHASE3=0.202, RAPHASE4=0.246, RAPHASE5=0.441 and RAPHASE6=0.637 starting from down-slope. Pre-select RPHASE11=RPHASE21=RPHASE31=RPHASE41=RPHASE51= RPHASE61=10kΩ,

$$R_{PHASE12} = \frac{RA_{PHASE1}}{1 - RA_{PHASE1}} * R_{PHASE11} = \frac{0.628}{1 - 0.628} * 10 * 10^3 = 16.9k\Omega$$

RPHASE22=7.15kΩ, RPHASE32=2.55kΩ, RPHASE42=3.24kΩ, PPHASE52=7.87kΩ, RPHASE62=17.4kΩ

Bootstrap Capacitor CBST

Choose CBST=0.1uF

Decoupling Capacitors for Phase IC and Power Stage

Choose CVCC=0.1uF, CVCCL=0.1uF

VOLTAGE LOOP COMPENSATION

Type II compensation is used for the converter with AL-Polymer output capacitors. Choose the crossover frequency fc=40kHz, which is 1/10 of the switching frequency per phase, and determine Rcp and CCP.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{RAMP}}{V_O * \sqrt{1+(2\pi * f_C * C * R_C)^2}} = \frac{(2\pi * 40 * 10^3)^2 * (220 * 10^{-9}/6) * (560 * 10^{-6} * 10) * 365 * 0.8}{(1.35 - 20 * 10^{-3}) * \sqrt{1+(2\pi * 40 * 10^3 * 560 * 10^{-6} * 7 * 10^{-3})^2}} = 2.0k\Omega$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} = \frac{10 * \sqrt{(220 * 10^{-9}/6) * (560 * 10^{-6} * 10)}}{2.0 * 10^3} = 71nF$$, Choose CCP=68nF

Choose CCP1=47pF to reduce high frequency noise.

CURRENT SHARE LOOP COMPENSATION

The crossover frequency of the current share loop fCI should be at least one decade lower than that of the voltage loop fC. Choose the crossover frequency of current share loop fCI=4kHz, and calculate CSCOMP,

$$F_{MI} = \frac{R_{PWMRMP} * C_{PWMRMP} * f_{SW} * V_{PWMRMP}}{(V_I - V_{PWMRMP} - V_{DAC}) * (V_I - V_{DAC})} = \frac{16.2 * 10^3 * 220 * 10^{-12} * 400 * 10^3 * 0.8}{(12 - 0.8 - 1.35) * (12 - 1.35)} = 0.011$$

$$C_{SCOMP} = \frac{0.65 * R_{PWMRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6}$$

$$= \frac{0.65 * 16.2 * 10^3 * 12 * 105 * 34 * (0.47 * 10^{-3}/6) * [1 + 2\pi * 4 * 10^3 * 560 * 10^{-6} * 10 * (1.33 - 105 * 9.1 * 10^{-4})/105] * 0.011}{(1.33 - 105 * 9.1 * 10^{-4}) * 2\pi * 4 * 10^3 * 1.05 * 10^6}$$

$$= 31.4nF$$

Choose CSCOMP=33nF

DESIGN EXAMPLE 2 - EVRD 10 HIGH FREQUENCY ALL-CERAMIC CONVERTER

SPECIFICATIONS

Input Voltage: V_I=12 V
DAC Voltage: V_{DAC}=1.3 V
No Load Output Voltage Offset: V_{O_NLOFST}=20 mV
Output Current: I_O=105 ADC
Maximum Output Current: I_{OMAX}=120 ADC
Output Impedance: R_O=0.91 mΩ
VCC Ready to VCC Power Good Delay: t_{VccPG}=0-10mS
Soft Start Time: t_{SS}=2.9mS
Over Current Delay: t_{OCDEL}=2.1mS
Dynamic VID Down-Slope Slew Rate: SR_{DOWN}=2.5mV/uS
Over Temperature Threshold: T_{PCB}=115 ºC

POWER STAGE

Phase Number: n=6
Switching Frequency: f_{SW}=800 kHz
Output Inductors: L=100 nH, R_L=0.5 mΩ
Output Capacitors: Ceramic, C=22uF, R_C= 2mΩ, Number Cn=62

IR3081A EXTERNAL COMPONENTS

Oscillator Resistor *Rosc*

Once the switching frequency is chosen, R_{OSC} can be determined from the curve in Figure 13 of IR3081A Data Sheet. For switching frequency of 800kHz per phase, choose R_{OSC}=13.3kΩ

Soft Start Capacitor *$C_{SS/DEL}$*

Determine the soft start capacitor from the required soft start time.

$$C_{SS/DEL} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{70*10^{-6} * 3*10^{-3}}{1.3 - 20*10^{-3}} = 0.16uF$$, choose $C_{SS/DEL}$=0.15uF

The soft start delay time is

$$t_{SSDEL} = \frac{C_{SS/DEL} * 1.3}{I_{CHG}} = \frac{0.15*10^{-6} * 1.3}{70*10^{-6}} = 2.8mS$$

The power good delay time is

$$t_{VccPG} = \frac{C_{SS/DEL} * (3.735 - V_O - 1.3)}{I_{CHG}} = \frac{0.15*10^{-6} * (3.735 - 1.33 - 1.3)}{70*10^{-6}} = 2.4ms$$

Over current delay time is

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.115}{I_{OCDISCHG}} = \frac{0.15*10^{-6} * 0.115}{40*10^{-6}} = 0.43ms$$

VDAC Slew Rate Programming Capacitor *C_{VDAC}* and Resistor *R_{VDAC}*

From Figure 15 of IR3081A Data Sheet, the sink current of VDAC pin corresponding to 800kHz (R_{OSC}=13.3kΩ) is 170uA. Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{170*10^{-6}}{2.5*10^{-3}/10^{-6}} = 68nF$$

Calculate the programming resistor.

$$R_{VDAC} = 0.5 + \frac{3.2*10^{-15}}{C_{VDAC}{}^2} = 0.5 + \frac{3.2*10^{-15}}{(68*10^{-9})^2} = 1.2\Omega$$

From Figure 15 of IR3081A Data Sheet, the source current of VDAC pin is 250uA. The VDAC up-slope slew rate is

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} = \frac{250*10^{-6}}{68*10^{-9}} = 3.7mV/uS$$

Over Current Setting Resistor *ROCSET*

The room temperature is 25ºC and the target PCB temperature is 100 ºC. The phase IC die temperature is about 1 ºC higher than that of phase IC, and the inductor temperature is close to PCB temperature.

Calculate Inductor DC resistance at 100 ºC,

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850*10^{-6} * (T_{L\_MAX} - T_{ROOM})] = 0.5*10^{-3} * [1 + 3850*10^{-6} * (100 - 25)] = 0.64m\Omega$$

The current sense amplifier gain is 34 at 25ºC, and its gain at 101ºC is calculated as,

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470*10^{-6} * (T_{IC\_MAX} - T_{ROOM})] = 34 * [1 - 1470*10^{-6} * (101 - 25)] = 30.2$$

Set the over current limit at 135A. From Figure 14 of IR3081A Data Sheet, the bias current of OCSET pin (I_{OCSET}) is 90uA with R_{OSC}=13.3kΩ. The total current sense amplifier input offset voltage is 0.55mV, which includes the offset created by the current sense amplifier input resistor mismatch.

Calculate constant K_P, the ratio of inductor peak current over average current in each phase,

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_{LIMIT} / n} = \frac{(12 - 1.28) * 1.28 / (100*10^{-9} * 12 * 800*10^3 * 2)}{135/6} = 0.32$$

$$R_{OCSET} = [\frac{R_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS\_MIN} / I_{OCSET}$$

$$= (\frac{135}{6} * 0.64*10^{-3} * 1.32 + 0.55*10^{-3}) * 30.2 / (90*10^{-6}) = 6.34k\Omega$$

No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP*

From Figure 14 of IR3081A Data Sheet, the bias current of FB pin is 90uA with R_{OSC}=13.3kΩ.

$$R_{FB} = \frac{R_{L\_MAX} * V_{O\_NLOFST} - V_{CS\_TOFST} * n * R_O}{I_{FB} * R_{L\_MAX}} = \frac{0.64*10^{-3} * 20*10^{-3} - 0.55*10^{-3} * 6 * 0.91*10^{-3}}{90*10^{-6} * 0.64*10^{-3}} = 162\Omega$$

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS\_MIN}}{n * R_O} = \frac{162 * 0.64*10^{-3} * 30.2}{6 * 0.91*10^{-3}} = 576\Omega$$

Body Braking Related Resistors *RBBFB* and *RBBDRP*

N/A. The body braking during Dynamic VID is disabled.

IR3088A EXTERNAL COMPONENTS

PWM Ramp Resistor *RPWMRMP* and Capacitor C*PWMRMP*

Set PWM ramp magnitude VPWMRMP=0.75V. Choose 100pF for PWM ramp capacitor CPWMRMP, and calculate the resistor RPWMRMP,

$$R_{PWMRMP} = \frac{V_O}{V_{IN} * f_{SW} * C_{PWMRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]}$$

$$= \frac{1.28}{12 * 800 * 10^3 * 100 * 10^{-12} * [\ln(12 - 1.3) - \ln(12 - 1.3 - 0.75)]} = 18.2k\Omega$$

Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-*

Choose 47nF for capacitor CCS+, and calculate RCS+,

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} = \frac{100 * 10^{-9} / (0.5 * 10^{-3})}{47 * 10^{-9}} = 4.22k\Omega$$

The bias currents of CSIN+ and CSIN- are 0.25uA and 0.4uA respectively. Calculate resistor RCS-,

$$R_{CS-} = R_{CS+} = 4.22k\Omega$$

Combined Over Temperature and Phase Delay Setting Resistors *RPHASEx1*, *RPHASEx2* and *RPHASEx3*

The over temperature setting resistor divider is combined with the phase delay resistor divider. Set the temperature threshold at 115 ºC, which corresponds to the IC die temperature of 116 ºC, and calculate the HOTSET threshold voltage corresponding to the temperature thresholds.

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 = 4.73 * 10^{-3} * 116 + 1.241 = 1.79V$$

The phase delay resistor ratios for phases 1 to 6 at 800kHz of switching frequencies are RAPHASE1=0.665, RAPHASE2=0.432, RAPHASE3=0.198, RAPHASE4=0.206, RAPHASE5=0.401 and RAPHASE6=0.597 starting from down-slope.

The over temperature setting voltage of phases 1, 2, 5, and 6 is lower than the phase delay setting voltage, VBIAS*RAPHASEx. Pre-select RPHASE11=10kΩ,

$$R_{PHASEx2} = \frac{(RA_{PHASEx} * V_{BIAS} - V_{HOTSET}) * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} = \frac{(0.665 * 6.8 - 1.79) * 10 * 10^3}{6.8 * (1 - 0.665)} = 12.1k\Omega$$

$$R_{PHASEx3} = \frac{V_{HOTSET} * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} = \frac{1.79 * 12.1 * 10^3}{6.8 * (1 - 0.665)} = 7.87k\Omega$$

RPHASE21=10kΩ, RPHASE22=2.94kΩ, RPHASE23=4.64kΩ

RPHASE51=10kΩ, RPHASE52=2.32kΩ, RPHASE53=4.42kΩ

RPHASE61=10kΩ, RPHASE62=8.25kΩ, RPHASE63=6.49kΩ

The over temperature setting voltage of Phases 3 and 4 is higher than the phase delay setting voltage, VBIAS*RAPHASEx. Pre-select RPHASEX1=10kΩ,

$$R_{PHASE32} = \frac{(V_{HOTSET} - RA_{PHASE3} * V_{BIAS}) * R_{PHASE31}}{V_{BIAS} - V_{HOTSET}} = \frac{(1.79 - 0.198 * 6.8) * 10 * 10^3}{6.8 - 1.79} = 887\Omega$$

$$R_{PHASE33} = \frac{RA_{PHASE3} * V_{BIAS} * R_{PHASE31}}{V_{BIAS} - V_{HOTSET}} = \frac{0.198 * 6.8 * 10 * 10^3}{6.8 - 1.79} = 2.67k\Omega$$

$R_{PHASE41}$=10kΩ, $R_{PHASE42}$=768Ω, $R_{PHASE43}$=2.80kΩ

Bootstrap Capacitor *C_{BST}*

Choose C_{BST}=0.1uF

Decoupling Capacitors for Phase IC and Power Stage

Choose C_{VCC}=0.1uF, C_{VCCL}=0.1uF

VOLTAGE LOOP COMPENSATION

Type III compensation is used for the converter with only ceramic output capacitors. The crossover frequency and phase margin of the voltage loop can be estimated as follows.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} = \frac{576}{2\pi * (62 * 22 * 10^{-6}) * 34 * 162 * (0.5 * 10^{-3} / 6)} = 146kHz$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} = 63°$$

Choose $R_{FB1} = \frac{2}{3} * R_{FB} = \frac{2}{3} * 162 = 110\Omega$

Choose the desired crossover frequency fc (=140kHz) around fc1 estimated above, and calculate

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} = \frac{1}{4\pi * 140 * 10^3 * 110} = 5.2nF$$, choose C_{FB}=5.6nF

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} = \frac{(162 + 110) * 5.6 * 10^{-9}}{576} = 2.7nF$$

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{RAMP}}{V_O} = \frac{(2\pi * 140 * 10^3)^2 * (100 * 10^{-9} / 6) * (22 * 10^{-6} * 62) * 162 * 0.75}{1.3 - 20 * 10^{-3}} = 1.65k\Omega$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} = \frac{10 * \sqrt{(100 * 10^{-9} / 6) * (22 * 10^{-6} * 62)}}{1.65 * 10^3} = 27nF$$

Choose C_{CP1}=47pF to reduce high frequency noise.

CURRENT SHARE LOOP COMPENSATION

The crossover frequency of the current share loop f_{CI} should be at least one decade lower than that of the voltage loop f_C. Choose the crossover frequency of current share loop f_{CI}=3.5kHz, and calculate C_{SCOMP},

$$F_{MI} = \frac{R_{PWMRMP} * C_{PWMRMP} * f_{SW} * V_{PWMRMP}}{(V_I - V_{PWMRMP} - V_{DAC}) * (V_I - V_{DAC})} = \frac{18.2 * 10^3 * 100 * 10^{-12} * 800 * 10^3 * 0.75}{(12 - 0.75 - 1.3) * (12 - 1.3)} = 0.011$$

$$C_{SCOMP} = \frac{0.65 * R_{PWMRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6}$$

$$= \frac{0.65 * 18.2 * 10^3 * 12 * 105 * 34 * (0.5 * 10^{-3} / 6) * [1 + 2\pi * 3500 * 22 * 10^{-6} * 62 * (1.33 - 105 * 9.1 * 10^{-4}) / 105] * 0.011}{(1.33 - 105 * 9.1 * 10^{-4}) * 2\pi * 3500 * 1.05 * 10^6}$$

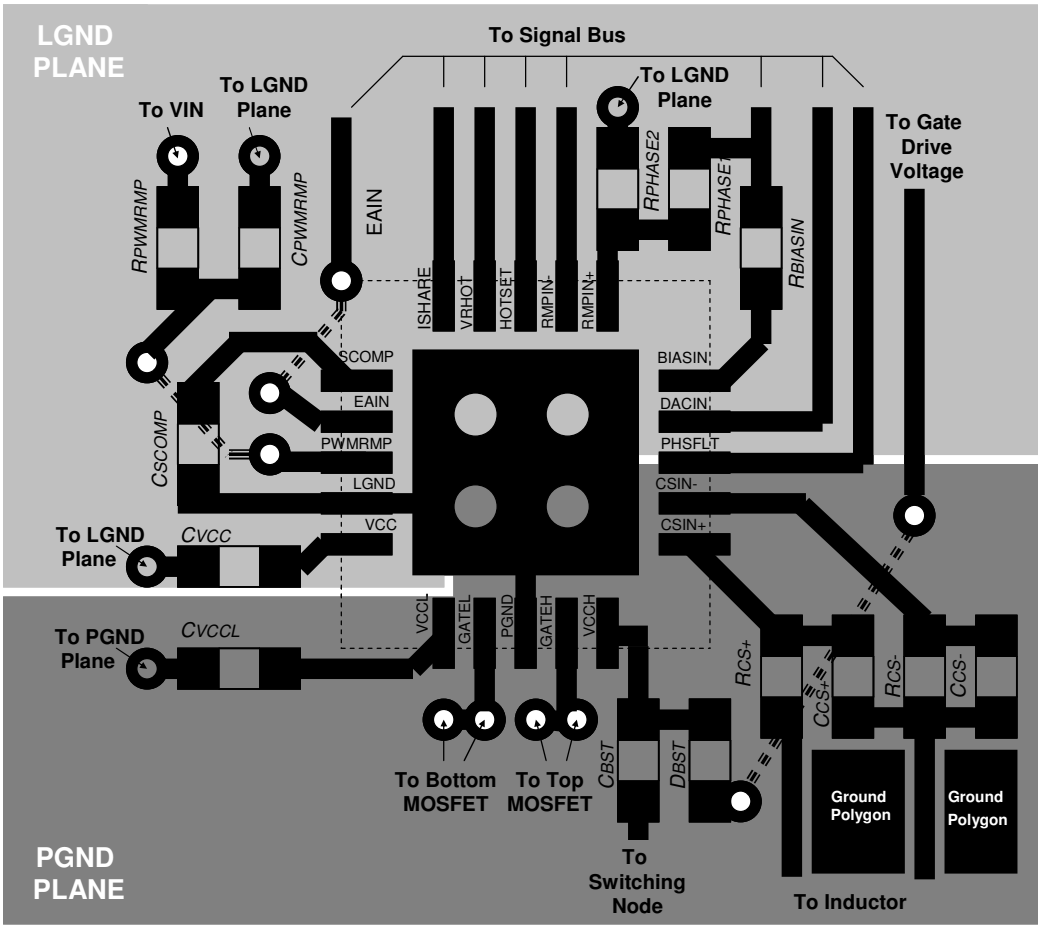
$$= 20.6nF$$

Choose C_{SCOMP}=22nF

LAYOUT GUIDELINES

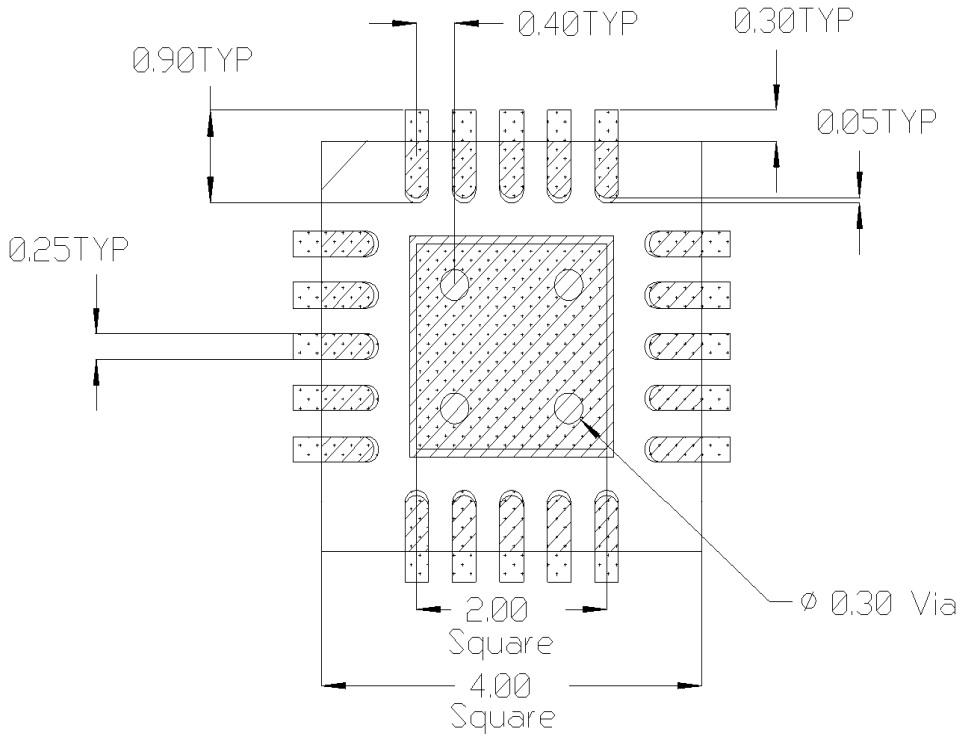
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane, which is then split into signal ground plane (LGND) and power ground plane (PGND).
- Connect PGND to LGND pins of each phase IC to the ground tab, which is tied to LGND and PGND planes respectively through vias.
- In order to reduce the noise coupled to SCOMP pin of phase IC, use a dedicated wire to connect the capacitor C_{SCOMP} directly to LGND pin. However, connect PWM ramp capacitor C_{PWMRMP}, phase delay programming resistor R_{PHASE2} or R_{PHASE3}, decoupling capacitor C_{VCC} to LGND plane through vias.
- Place current sense resistors and capacitors (R_{CS+}, R_{CS-}, C_{CS+}, and C_{CS-}) close to phase IC. Use Kelvin connection for the inductor current sense wires, but separate the two wires by ground polygon. The wire from the inductor terminal to RCS- should not cross over the fast transition nodes, i.e. switching nodes, gate drive outputs and bootstrap nodes.
- Place the decoupling capacitors C_{VCC} and C_{VCCL} as close as possible to VCC and VCCL pins of the phase IC respectively.
- Place the phase IC as close as possible to the MOSFETs to reduce the parasitic resistance and inductance of the gate drive paths.
- Place the input ceramic capacitors close to the drain of top MOSFET and the source of bottom MOSFET. Use combination of different packages of ceramic capacitors.
- There are two switching power loops. One loop includes the input capacitors, top MOSFET, inductor, output capacitors and the load; another loop consists of bottom MOSFET, inductor, output capacitors and the load. Route the switching power paths using wide and short traces or polygons; use multiple vias for connections between layers.



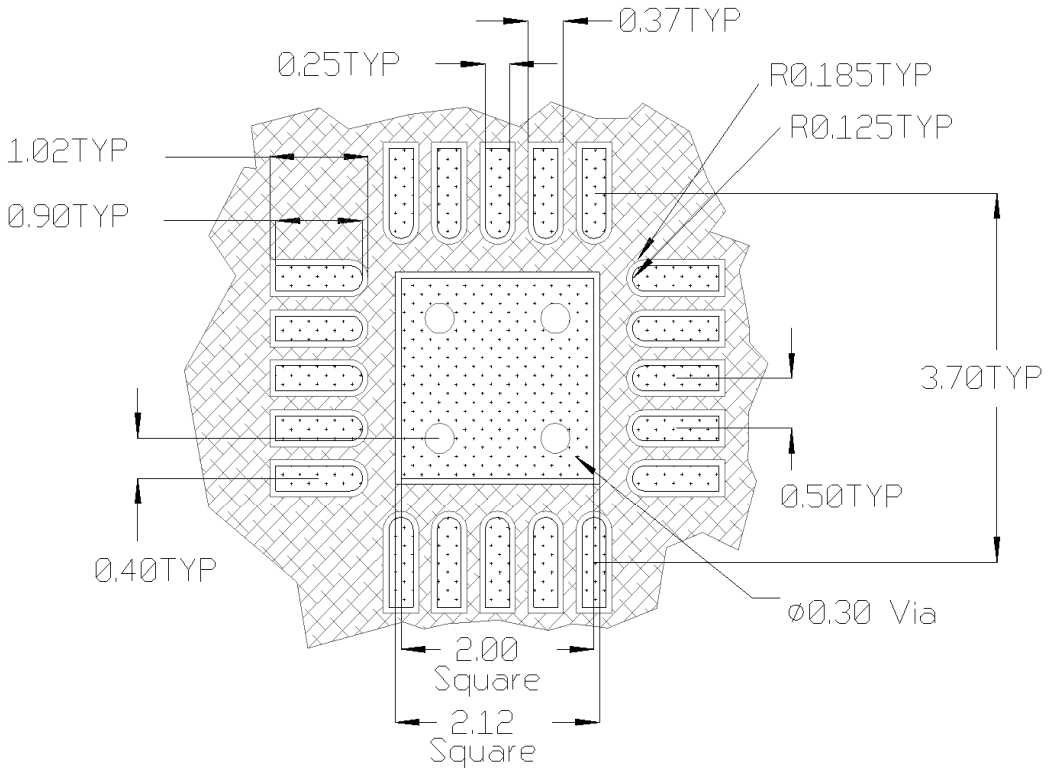
PCB Metal and Component Placement

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.3mm diameter vias shall be placed in the pad land spaced at 1.2mm, and connected to ground to minimize the noise effect on the IC and to transfer heat to the PCB.
- No PCB traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the PCB resulting in poor solder joints to the IC leads.



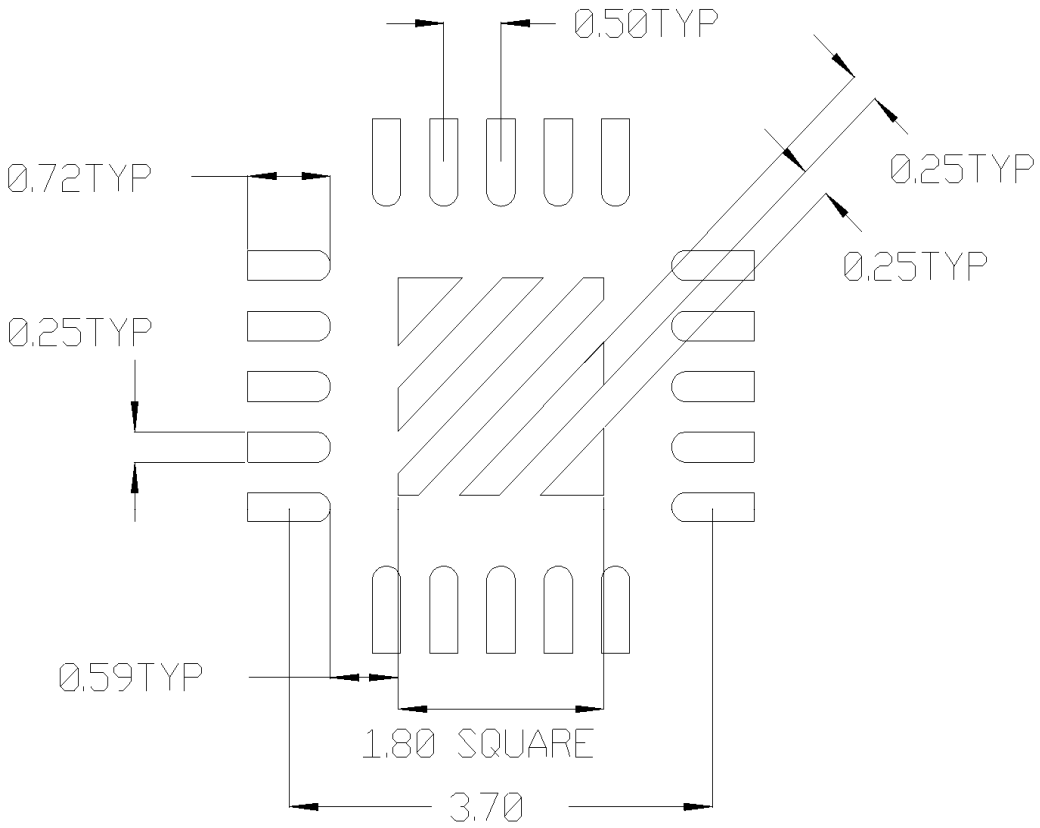
Solder Resist

- The solder resist should be pulled away from the metal lead lands and center pad by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore, pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm. At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The 4 vias in the land pad should be tented with solder resist 0.4mm diameter, or 0.1mm larger than the diameter of the via.



Stencil Design

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

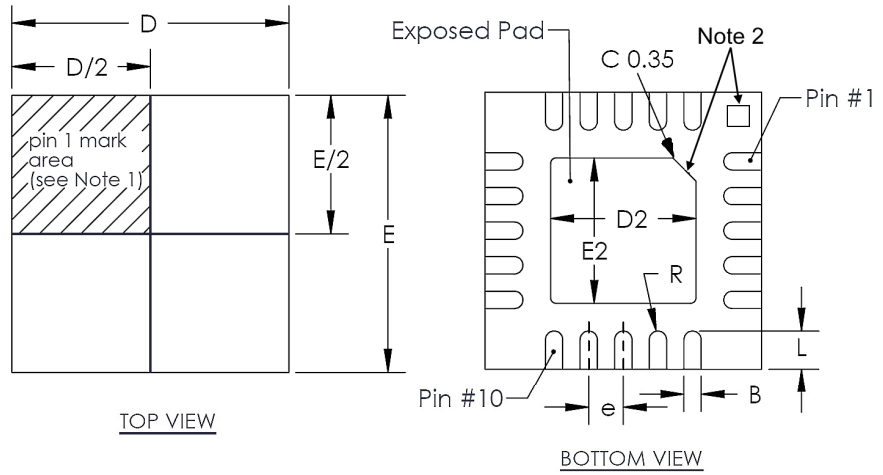


Stencil Aperture

All Dimensions in mm

PACKAGE INFORMATION

20L MLPQ (4 x 4 mm Body) – θ_{JA} = 32°C/W, θ_{JC} = 3°C/W



Note 1: Top details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

Note 2: Pin #1 will be indicated on the bottom by either a chamfer or a square island.

20L-4X4 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.20 REF	
B	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.00	2.10	2.20
E	3.90	4.00	4.10
E2	2.00	2.10	2.20
e		0.50 REF	
L	0.45	0.55	0.65
R		0.125 TYP	

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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