





## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating absolute voltage	-0.3	625	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage	-0.3	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(8 Lead DIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 Lead DIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High side floating supply offset voltage	Note 1	600	
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

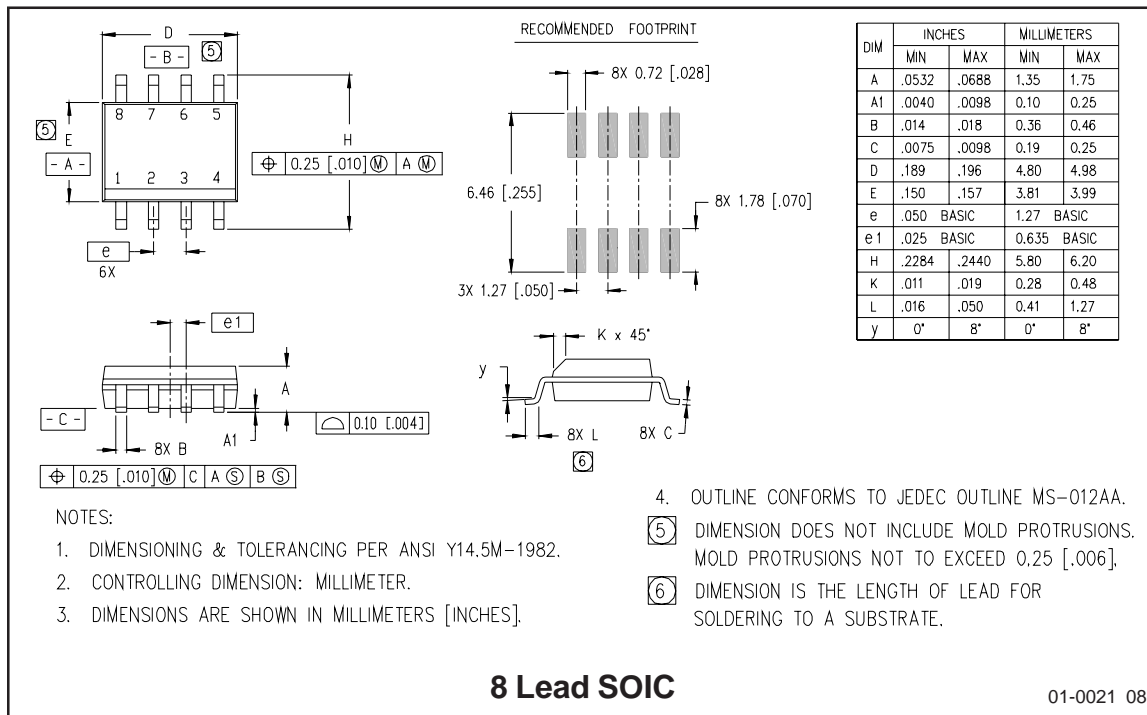
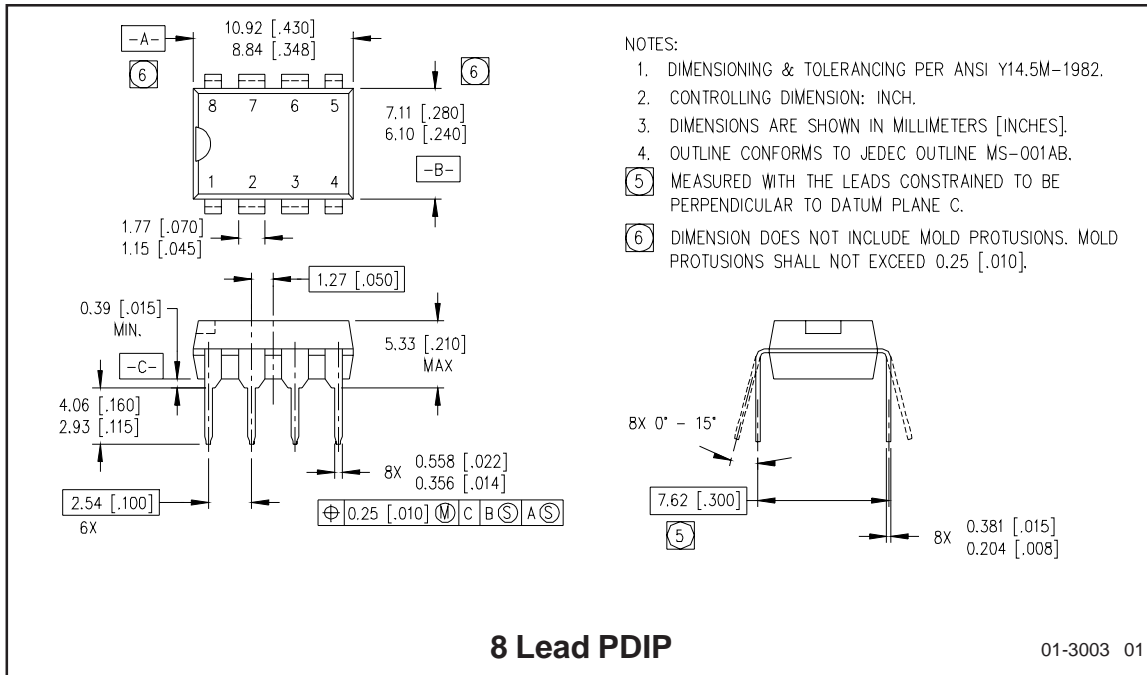
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	680	820	ns	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	150	220		$V_S = 600V$
$t_r$	Turn-on rise time	—	100	170		
$t_f$	Turn-off fall time	—	50	90		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" (HO) & Logic "0" (LO) Input Voltage	3	—	—	V	$V_{CC} = 10V$ to 20V
$V_{IL}$	Logic "0" (HO) & Logic "1" (LO) Input Voltage	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low Level Output Voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset Supply Leakage Current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	—	30	55		$V_{IN} = 0V$ or 5V
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	150	270		$V_{IN} = 0V$ or 5V
$I_{IN+}$	Logic "1" Input Bias Current	—	3	10		$V_{IN} = 5V$
$I_{IN-}$	Logic "0" Input Bias Current	—	—	1		$V_{IN} = 0V$
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold	8	8.9	9.8	V	
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	7.4	8.2	9		
$I_{O+}$	Output High Short Circuit Pulsed Current	130	210	—	mA	$V_O = 0V$ $PW \leq 10 \mu s$
$I_{O-}$	Output Low Short Circuit Pulsed Current	270	360	—		$V_O = 15V$ $PW \leq 10 \mu s$





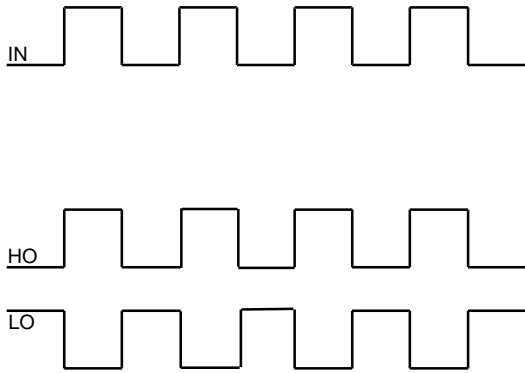


Figure 1. Input/Output Timing Diagram

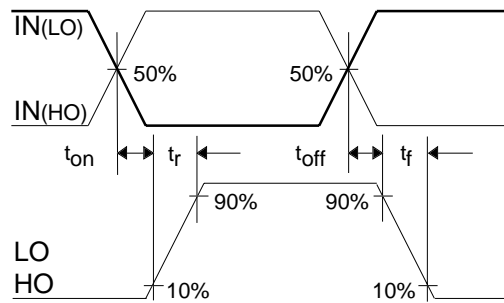


Figure 2. Switching Time Waveform Definitions

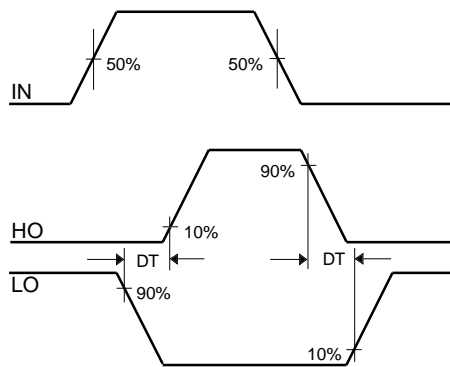


Figure 3. Deadtime Waveform Definitions

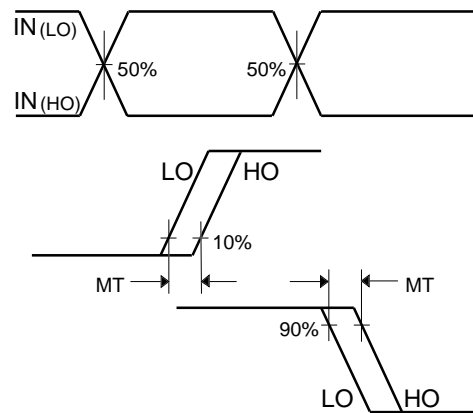


Figure 4. Delay Matching Waveform Definitions

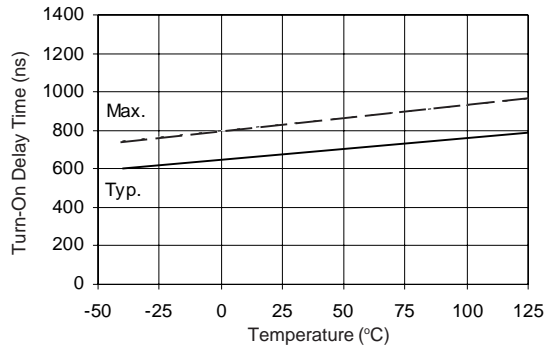


Figure 6A. Turn-On Time vs Temperature

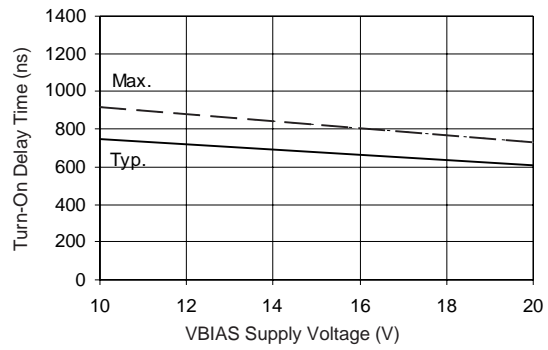


Figure 6B. Turn-On Time vs Voltage

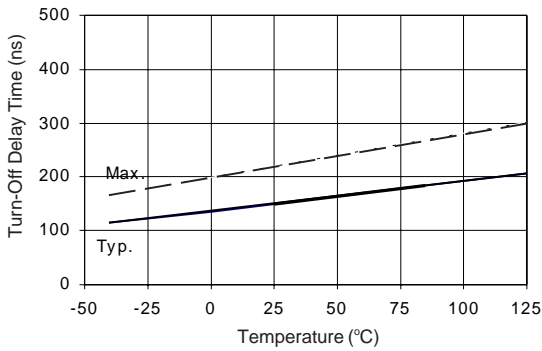


Figure 7A. Turn-Off Time vs Temperature

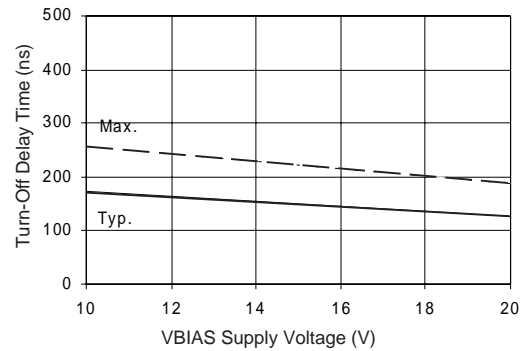


Figure 7B. Turn-Off Time vs Voltage

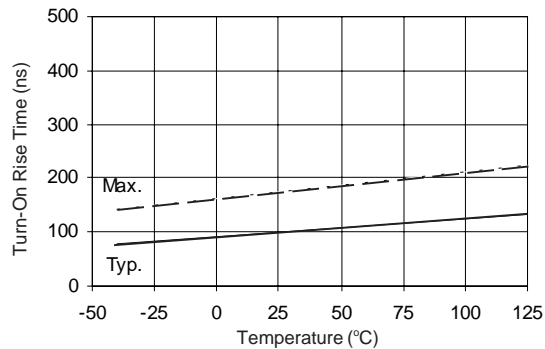


Figure 9A. Turn-On Rise Time vs Temperature

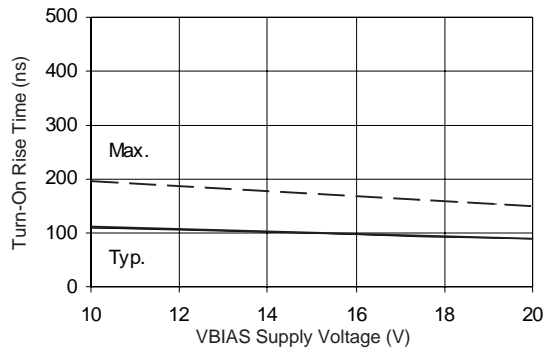
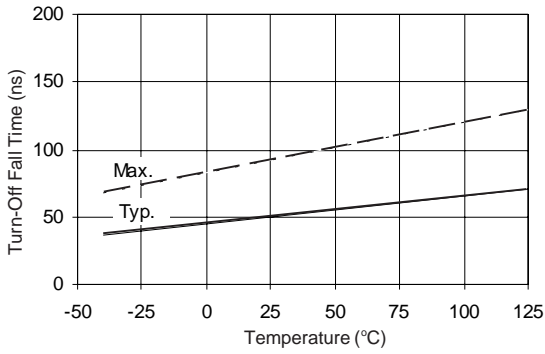
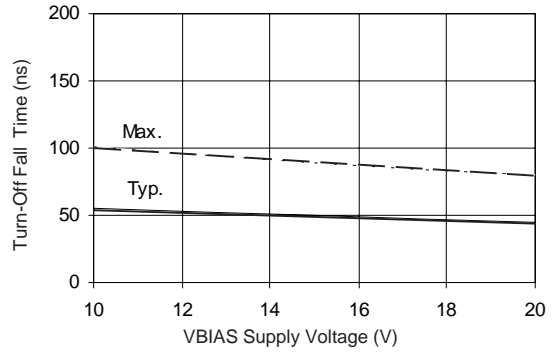


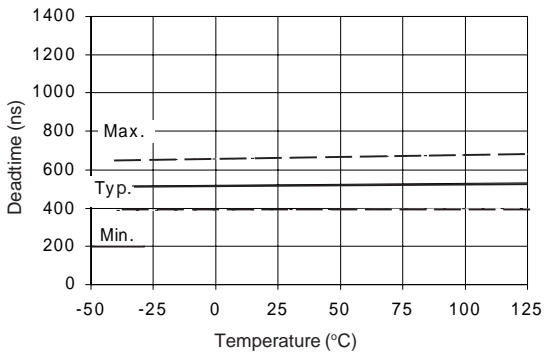
Figure 9B. Turn-On Rise Time vs Voltage



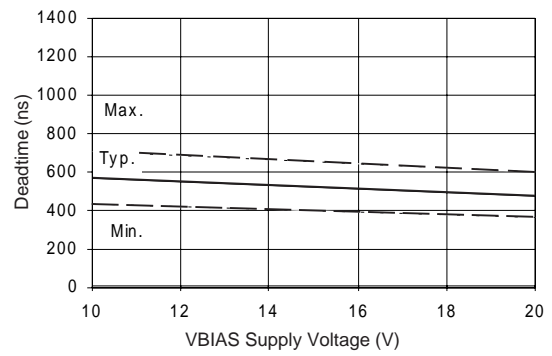
**Figure 10A. Turn Off Fall Time vs Temperature**



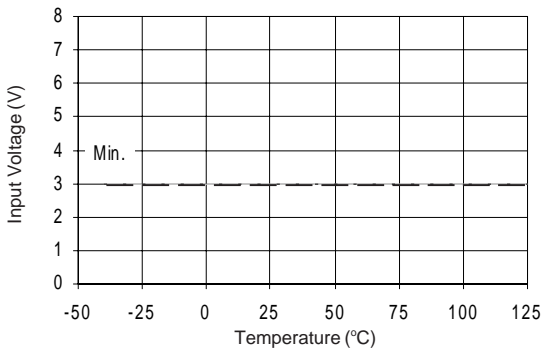
**Figure 10B. Turn Off Fall Time vs Voltage**



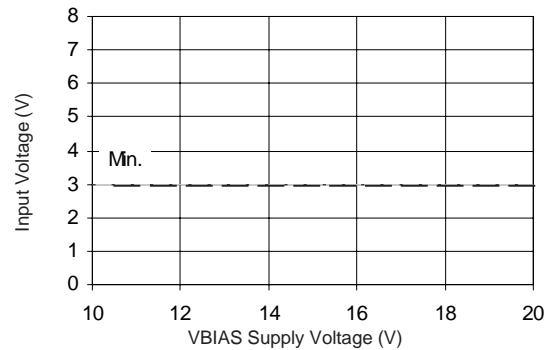
**Figure 11A. Deadtime vs Temperature**



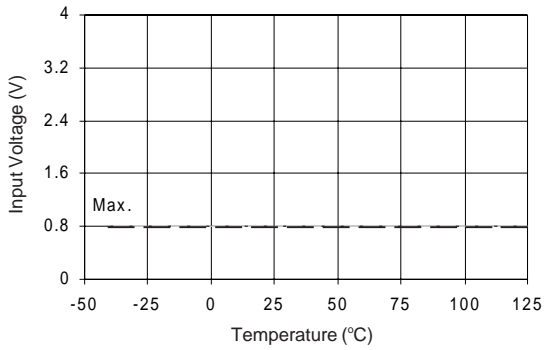
**Figure 11B. Deadtime vs Voltage**



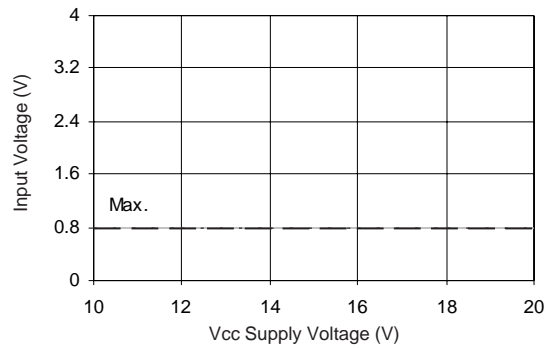
**Figure 12A. Logic "1" (HO) & Logic "0" (LO) Input Voltage vs Temperature**



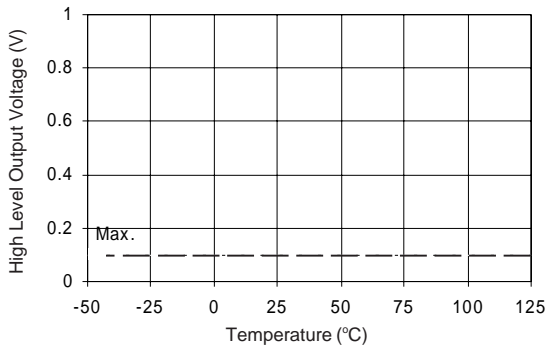
**Figure 12B. Logic "1" (HO) & Logic "0" (LO) Input Voltage vs Voltage**



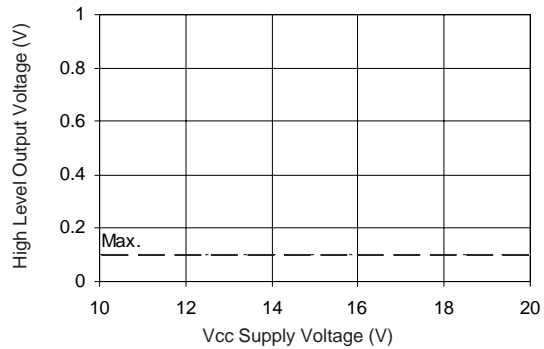
**Figure 13A. Logic "0"(HO) & Logic "1"(LO) Input Voltage vs Temperature**



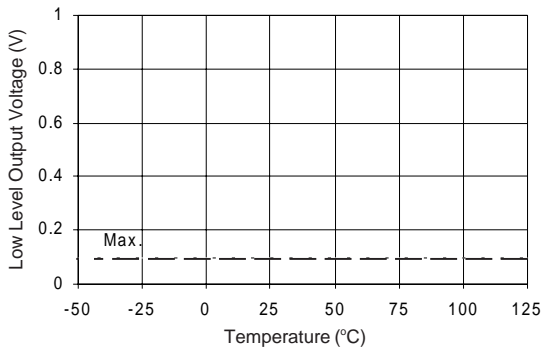
**Figure 13B. Logic "0"(HO) & Logic "1"(LO) Input Voltage vs Voltage**



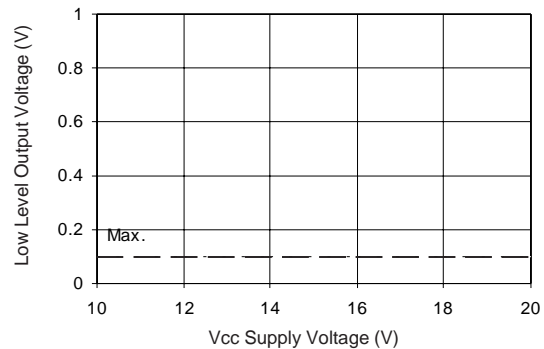
**Figure 14A. High Level Output vs Temperature**



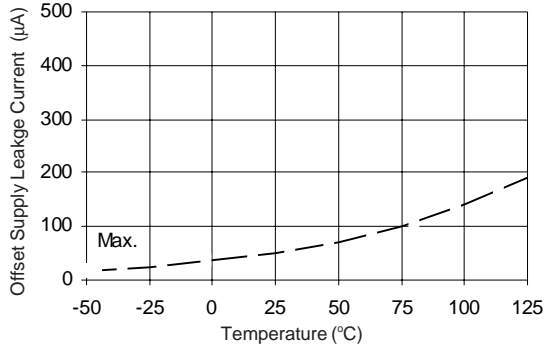
**Figure 14B. High Level Output vs Voltage**



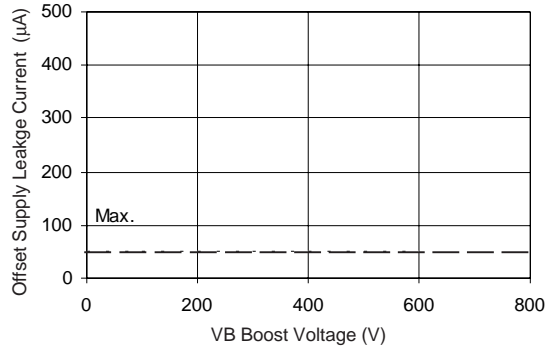
**Figure 15A. Low Level Output vs Temperature**



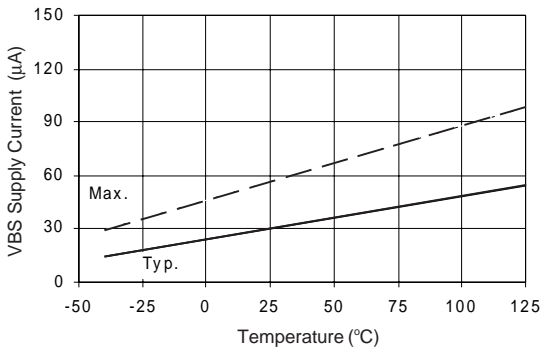
**Figure 15B. Low Level Output vs Voltage**



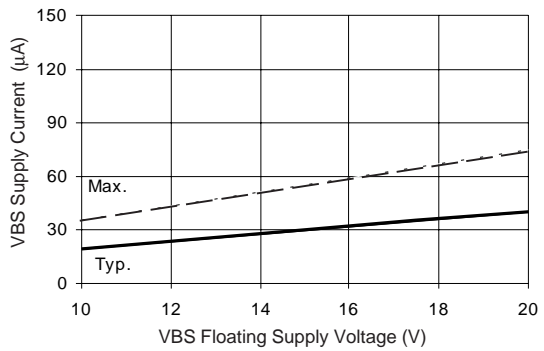
**Figure 16A. Offset Supply Current vs Temperature**



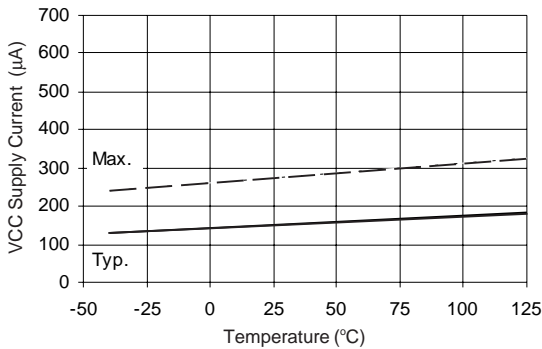
**Figure 16B. Offset Supply Current vs Voltage**



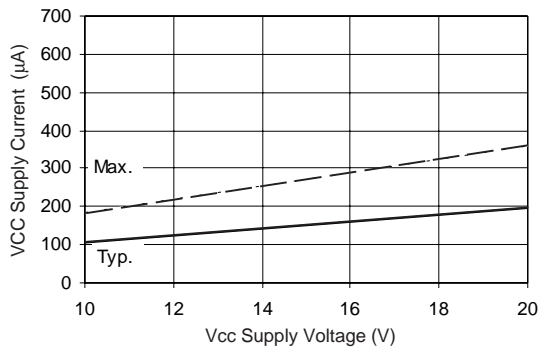
**Figure 17A. VBS Supply Current vs Temperature**



**Figure 17B. VBS Supply Current vs Voltage**



**Figure 18A. VCC Supply Current vs Temperature**



**Figure 18B. VCC Supply Current vs Voltage**

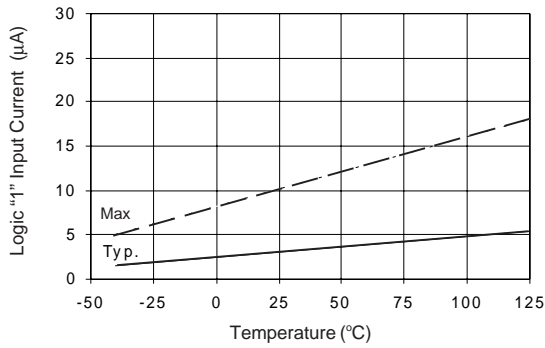


Figure 19A. Logic "1" Input Current vs Temperature

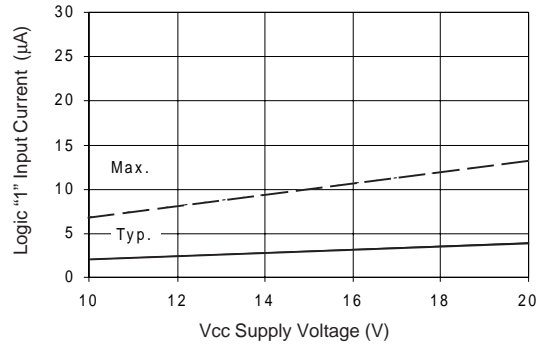


Figure 19B. Logic "1" Input Current vs Voltage

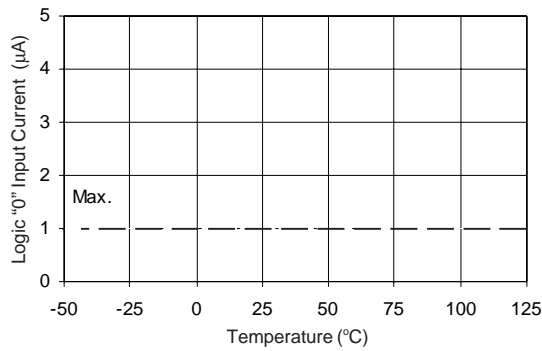


Figure 20A. Logic "0" Input Current vs Temperature

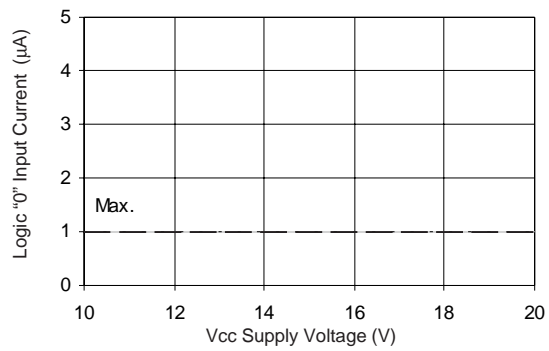


Figure 20B. Logic "0" Input Current vs Voltage

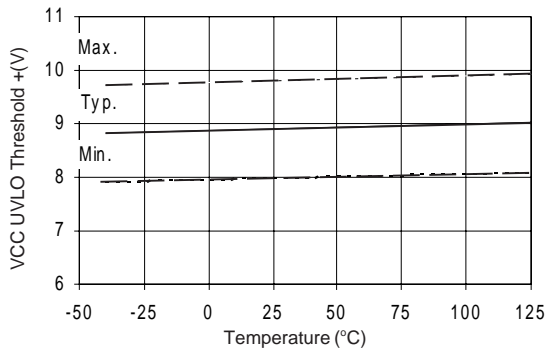


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

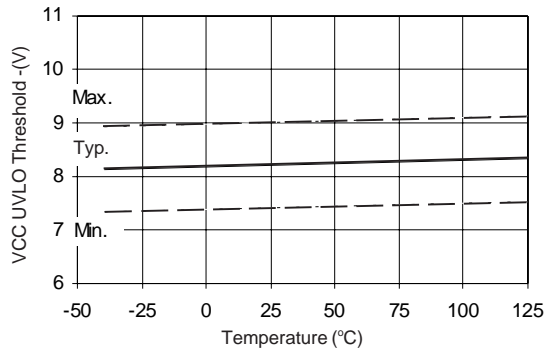
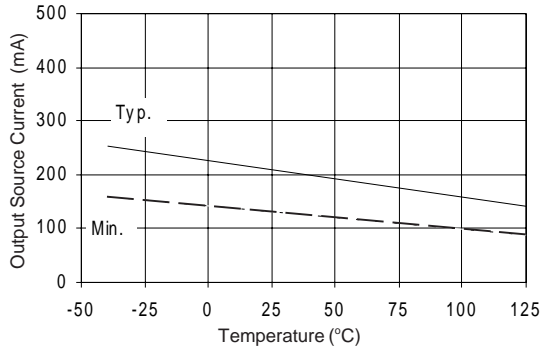
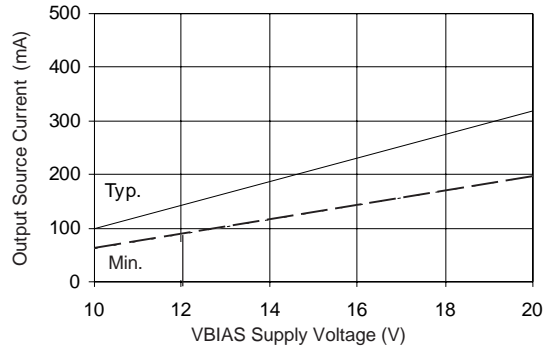


Figure 21B. Vcc Undervoltage Threshold (-) vs Temperature

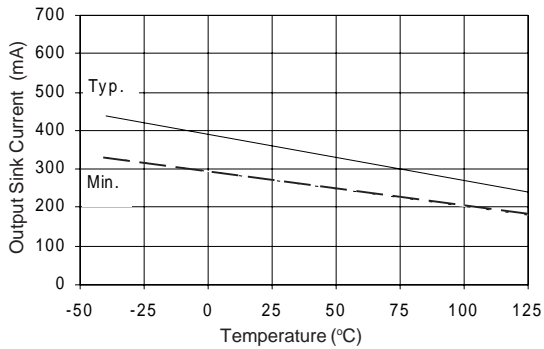
# IR2105



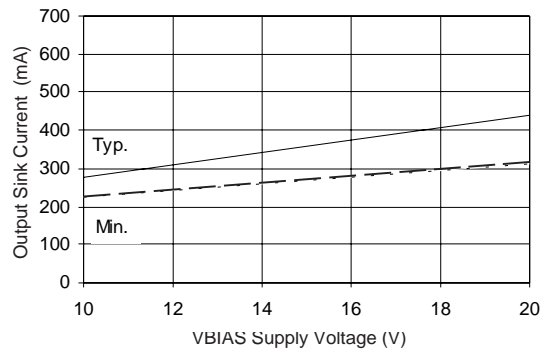
**Figure 22A. Output Source Current vs Temperature**



**Figure 22B. Output Source Current vs Voltage**





**Figure 23A. Output Sink Current vs Temperature**



**Figure 23B. Output Sink Current vs Voltage**

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