



**THE DATASHEET OF  
IR2103SPBF**



**Half-Bridge Driver**

**Features**

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High side output in phase with HIN input
- Low side output out of phase with LIN input

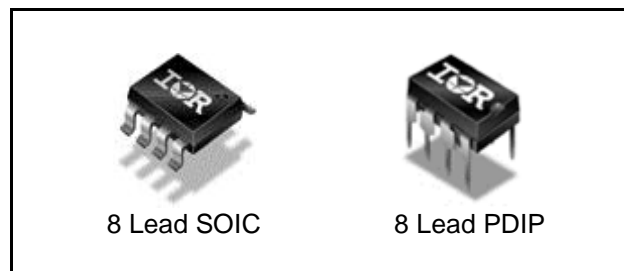
**Product Summary**

$V_{\text{OFFSET}}$ (max)	600V
$I_{\text{O+/-}}$	130mA / 270mA
$V_{\text{OUT}}$	10V – 20V
ton/off (typ.)	680 & 150 ns
Deadtime (typ.)	520 ns

**Description**

The IR2103(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

**Package Options**

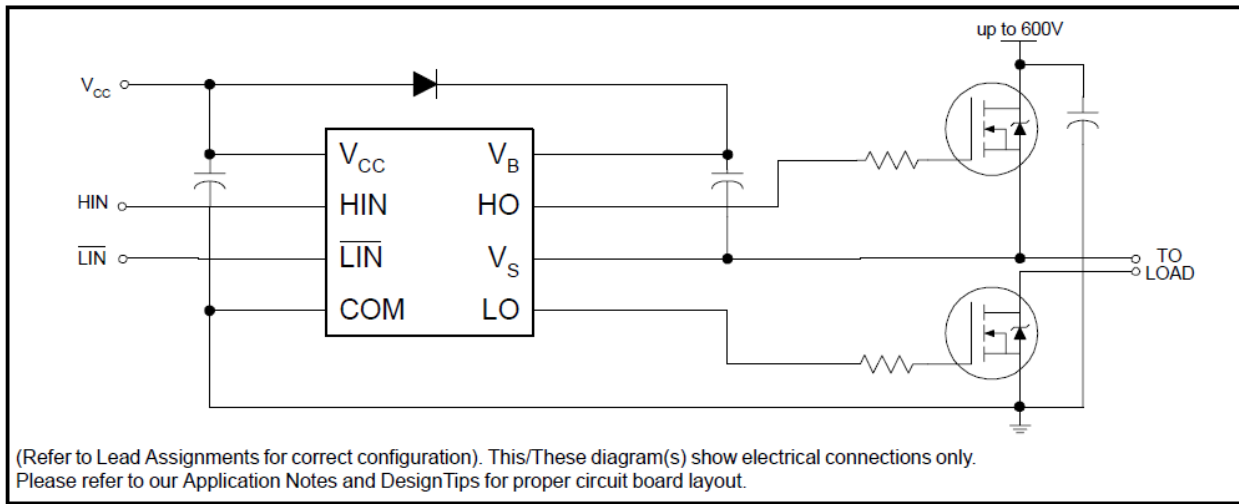


**Ordering Information**

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR2103SPBF	SO8N	Tube	95	IR2103SPBF
IR2103SPBF	SO8N	Tape and Reel	2500	IR2103STRPBF
IR2103PBF	PDIP8	Tube	50	IR2103PBF

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**Typical Connection Diagram**



### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
$V_B$	High side floating absolute voltage	-0.3	625	V	
$V_S$	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$		
$V_{HO}$	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$		
$V_{CC}$	Low side and logic fixed supply voltage	-0.3	25		
$V_{LO}$	Low side output voltage	-0.3	$V_{CC} + 0.3$		
$V_{IN}$	Logic input voltage (HIN & LIN)	-0.3	$V_{CC} + 0.3$		
$dV_S/dt$	Allowable offset supply voltage transient	—	50	V/ns	
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	8 lead PDIP	—	1	W
		8 lead SOIC	—	0.625	
$R_{thJA}$	Thermal resistance, junction to ambient	8 lead PDIP	—	125	$^\circ\text{C/W}$
		8 lead SOIC	—	200	
$T_J$	Junction temperature	—	150	$^\circ\text{C}$	
$T_S$	Storage temperature	-55	150		
$T_L$	Lead temperature (soldering, 10 seconds)	—	300		

### Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High side floating supply offset voltage	†	600	
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low side and logic fixed supply voltage	10	20	
$V_{LO}$	Low side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage (HIN & LIN)	0	$V_{CC}$	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

† Logic operational for  $V_S$  of -5 to +600V. Logic state held for  $V_S$  of -5V to  $-V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified.

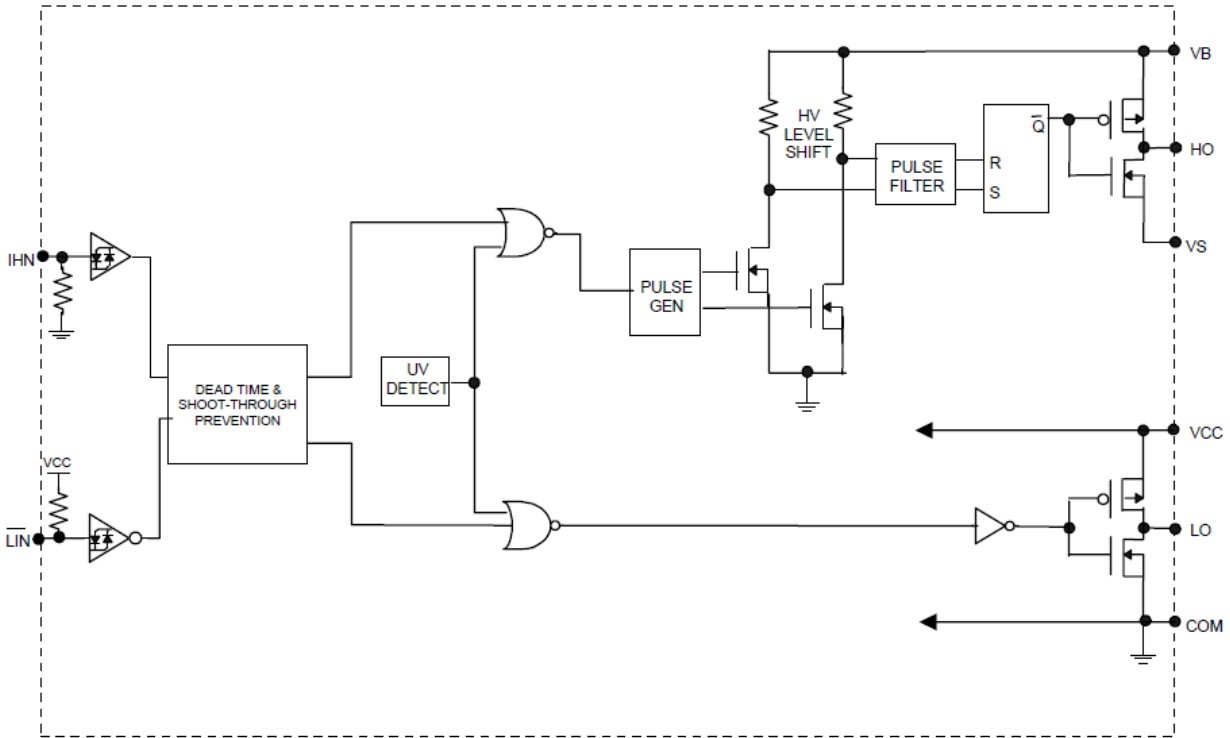
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	680	820	ns	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	150	220		$V_S = 600V$
$t_r$	Turn-on rise time	—	100	170		
$t_f$	Turn-off fall time	—	50	60		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650		
MT	Delay matching, HS & LS turn on/off	—	—	60		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" (HIN) & Logic "0" (LIN) input voltage	3	—	—	V	$V_{CC} = 10V$ to 20V
$V_{IL}$	Logic "0" (HIN) & Logic "1" (LIN) input voltage	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{OH}$	High level output voltage $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low level output voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	30	55		$V_{IN} = 0V$ or 5V
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	150	270		$V_{IN} = 0V$ or 5V
$I_{IN+}$	Logic "1" input bias current	—	3	10		$H_{IN} = 5V$ , $L_{IN} = 0V$
$I_{IN-}$	Logic "0" input bias current	—	—	1		$H_{IN} = 0V$ , $L_{IN} = 5V$
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	8	8.9	9.8	V	
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.2	9		
$I_{O+}$	Output high short circuit pulsed current	130	210	—	mA	$V_O = 0V$ , $V_{IN} = V_{IH}$ $PW \leq 10 \mu s$
$I_{O-}$	Output low short circuit pulsed current	270	360	—		$V_O = 15V$ , $V_{IN} = V_{IL}$ $PW \leq 10 \mu s$

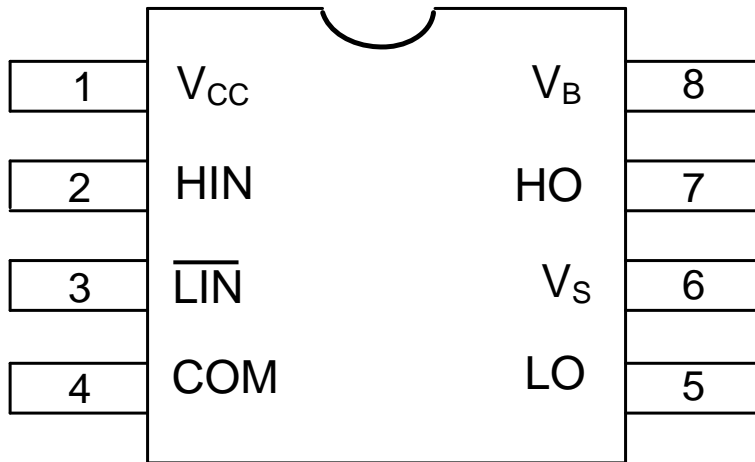
**Functional Block Diagram**



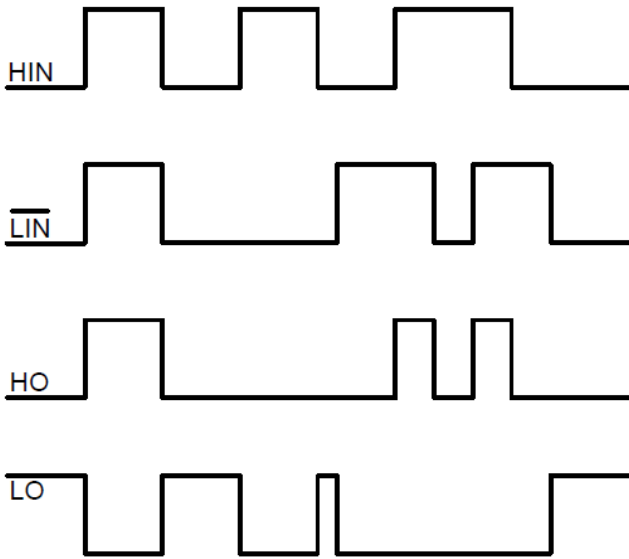
**Lead Definitions**

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), out of phase
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

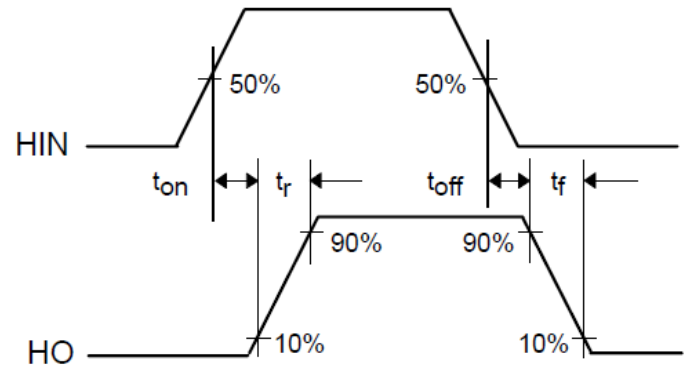
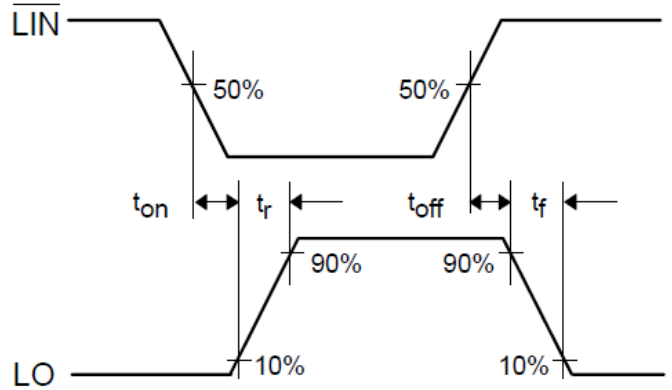
**Lead Assignments**



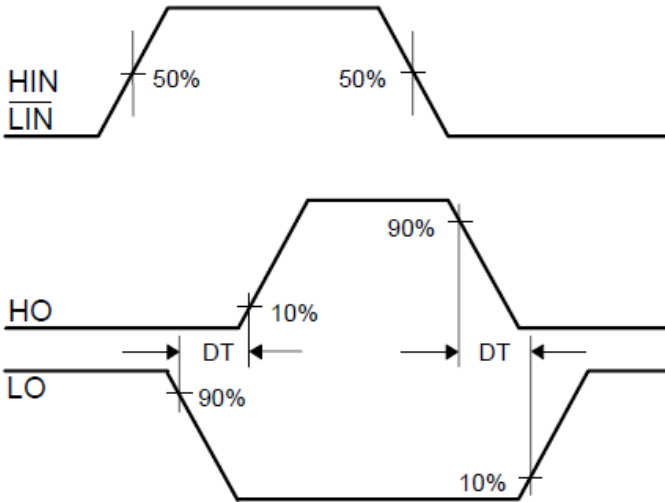
**Application Information and Additional Details**



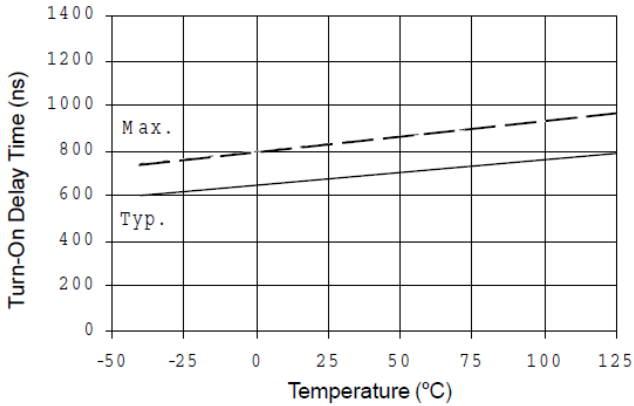
**Figure 1. Input/Output Timing Diagram**



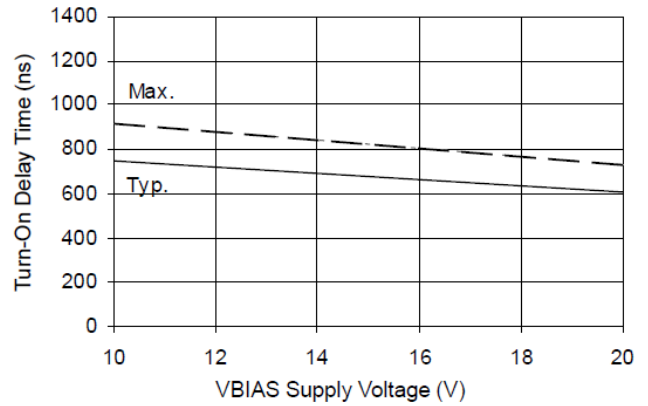
**Figure 2. Switching Time Waveform Definitions**



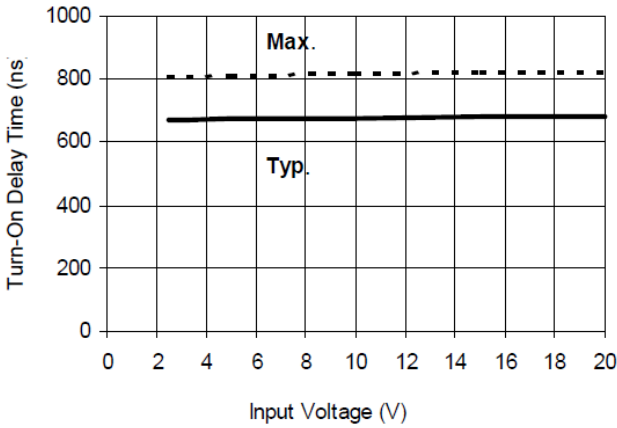
**Figure 3. Deadtime Waveform Definitions**



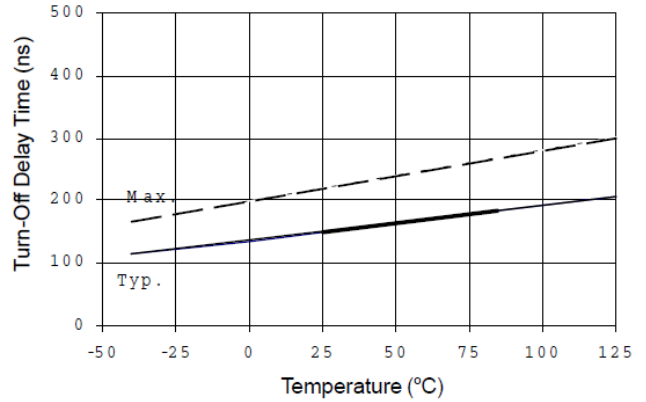
**Figure 4A. Turn-On Time vs. Temperature**



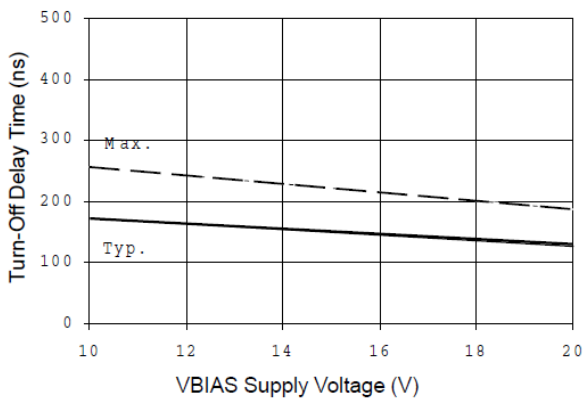
**Figure 4B. Turn-On Time vs. Supply Voltage**



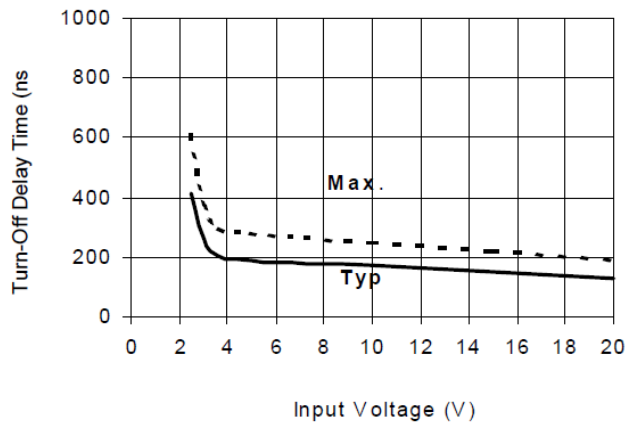
**Figure 4C. Turn-On Time vs. Input Voltage**



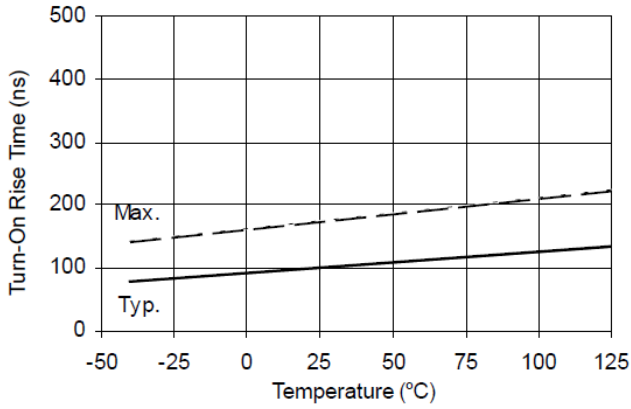
**Figure 5A. Turn-Off Time vs. Temperature**



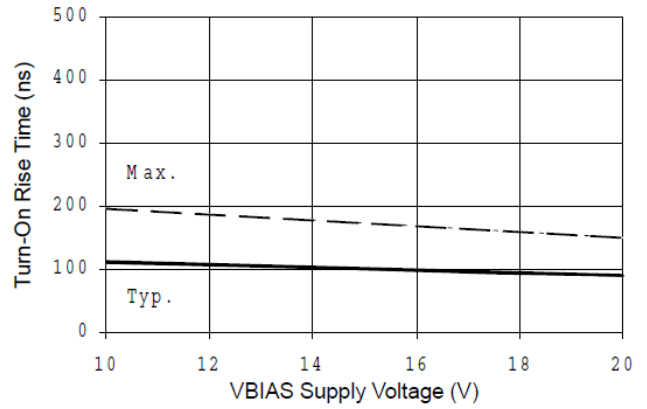
**Figure 5B. Turn-Off Time vs. Supply Voltage**



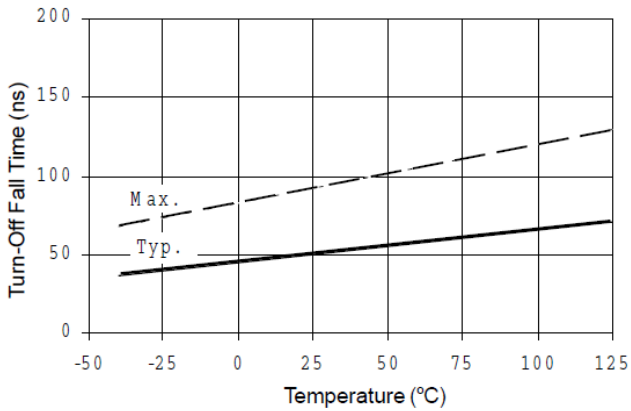
**Figure 5C. Turn-Off Time vs. Input Voltage**



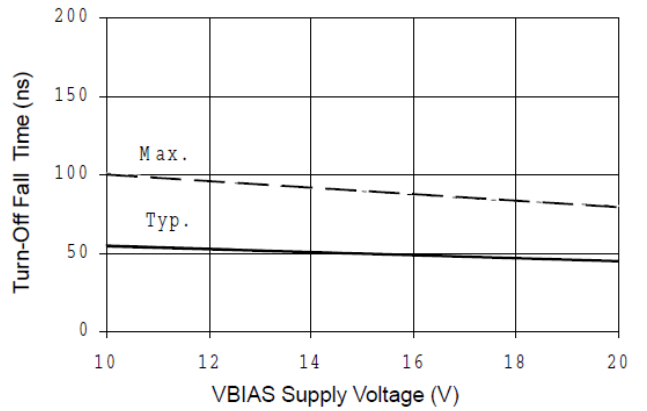
**Figure 6A. Turn-On Rise Time vs. Temperature**



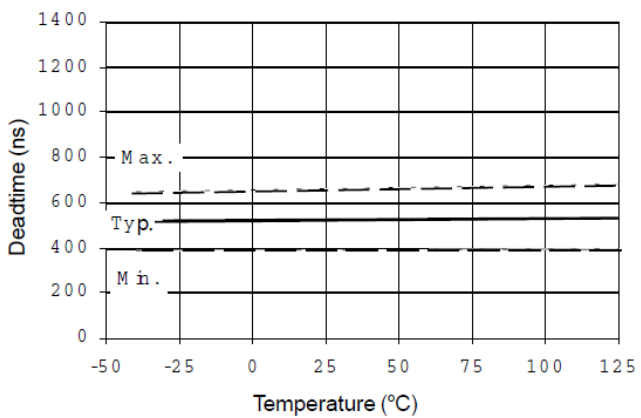
**Figure 6B. Turn-On Rise Time vs. Voltage**



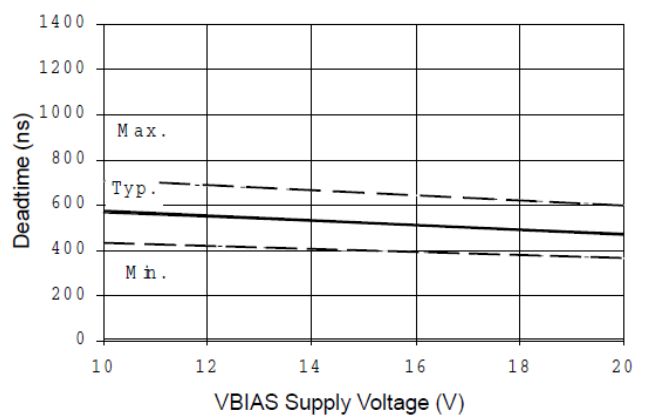
**Figure 7A. Turn Off Fall Time vs. Temperature**



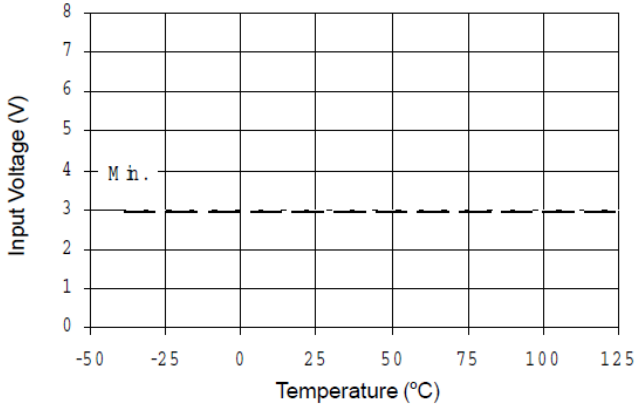
**Figure 7B. Turn Off Fall Time vs. Voltage**



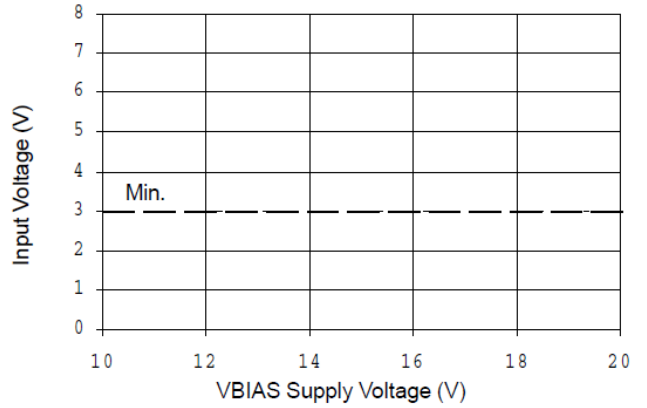
**Figure 8A. Deadtime vs. Temperature**



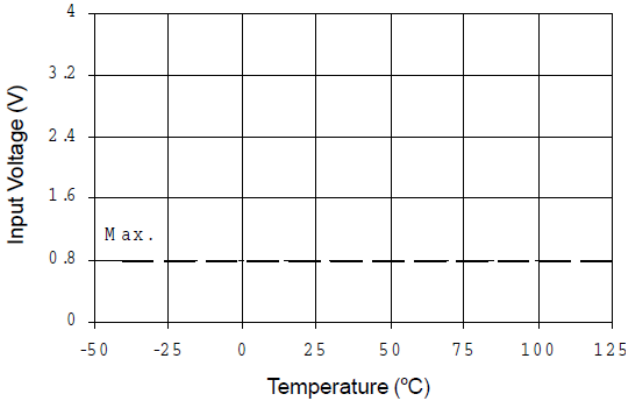
**Figure 8B. Deadtime vs. Voltage**



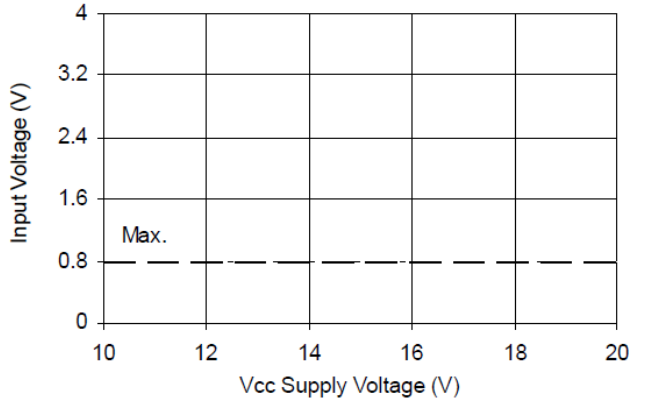
**Figure 9A. Logic "1" ( HIN) & Logic "0" ( LIN) Input Voltage vs. Temperature**



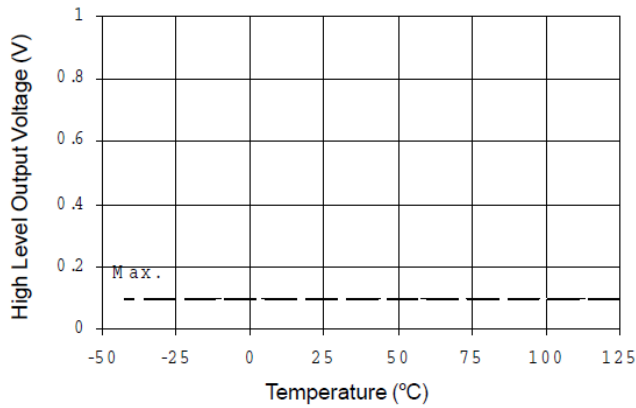
**Figure 9B. Logic "1" ( HIN) & Logic "0" ( LIN) Input Voltage vs. Voltage**



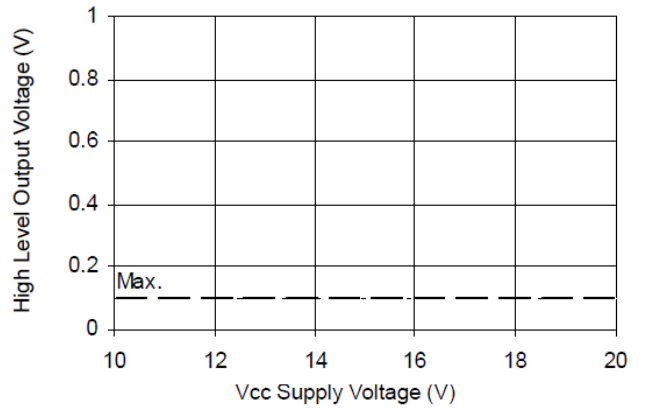
**Figure 10A. Logic "0" ( HIN) & Logic "1" ( LIN) Input Voltage vs. Temperature**



**Figure 10B. Logic "0" ( HIN) & Logic "1" ( LIN) Input Voltage vs. Voltage**



**Figure 11A. High Level Output vs. Temperature**



**Figure 11B. High Level Output vs. Voltage**

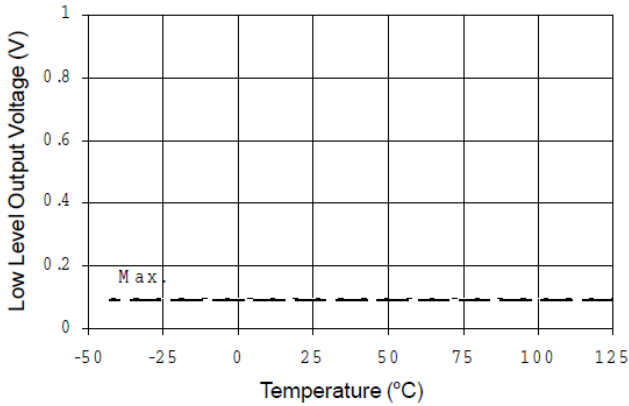


Figure 12A. Low Level Output vs. Temperature

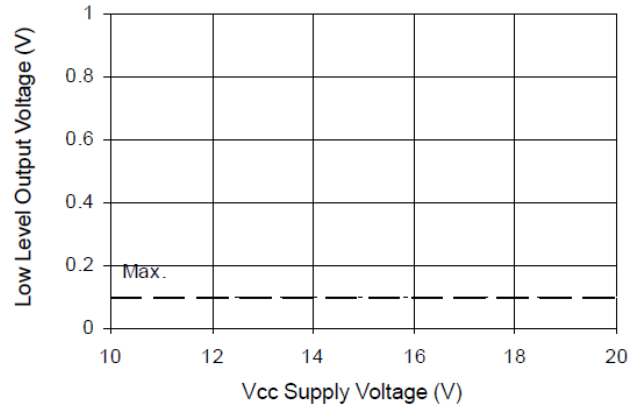


Figure 12B. Low Level Output vs. Voltage

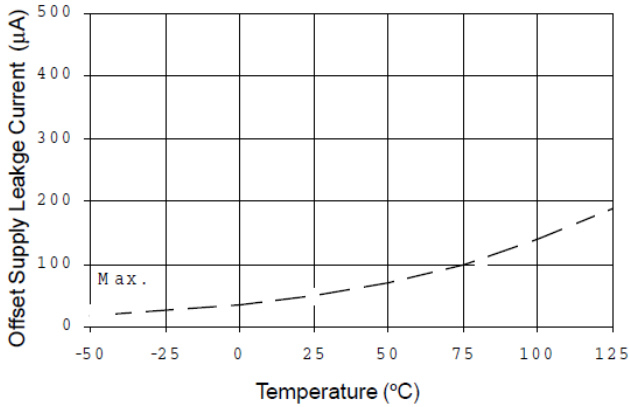


Figure 13A. Offset Supply Current vs. Temperature

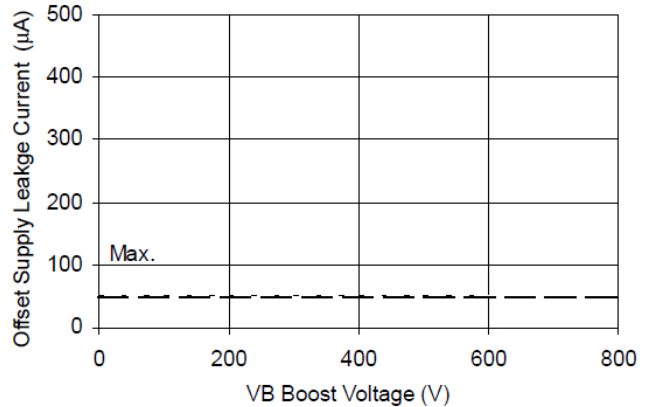


Figure 13B. Offset Supply Current vs. Voltage

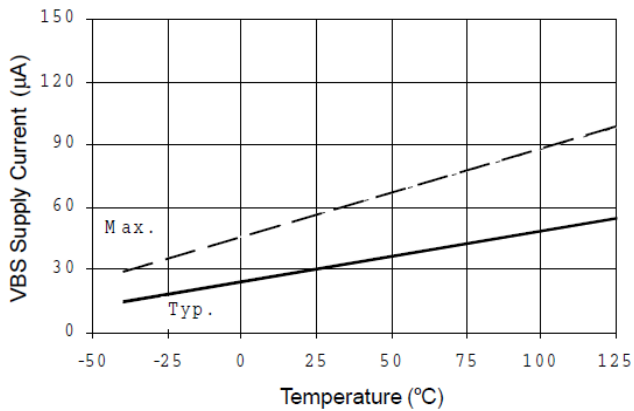


Figure 14A.  $V_{BS}$  Supply Current vs. Temperature

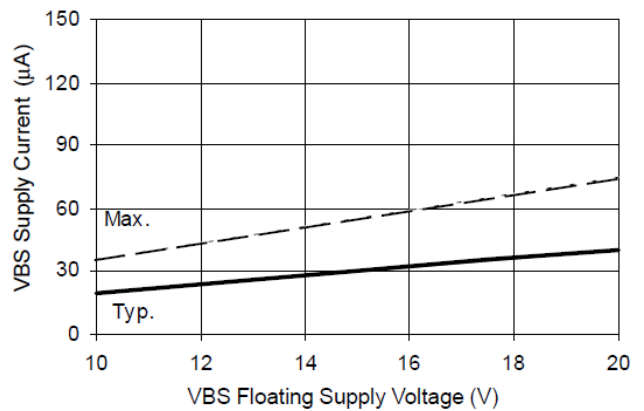
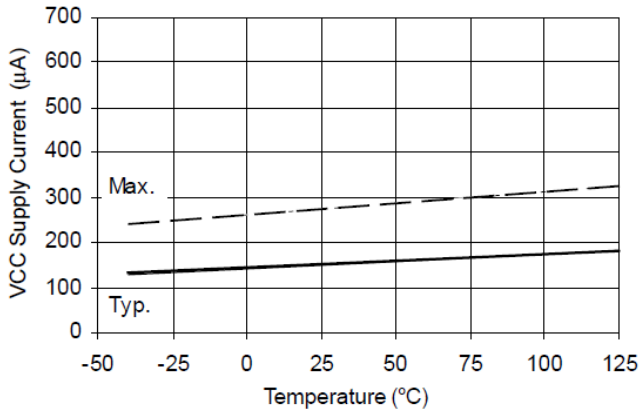
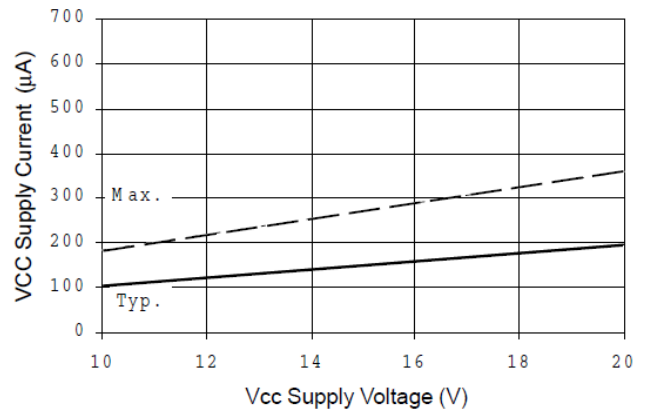


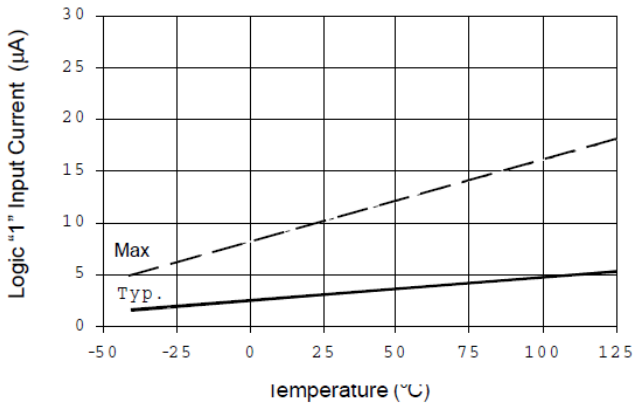
Figure 14B.  $V_{BS}$  Supply Current vs. Voltage



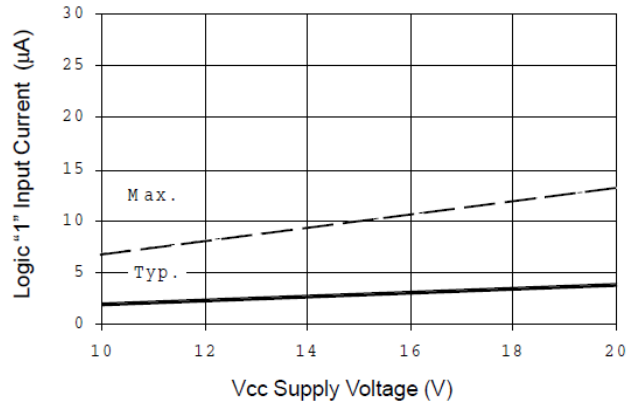
**Figure 15A. V<sub>CC</sub> Supply Current vs. Temperature**



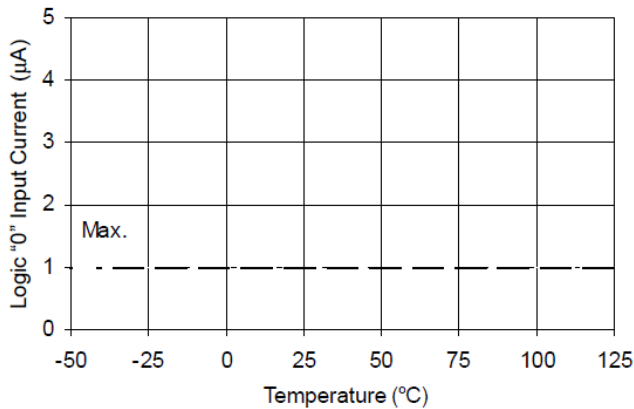
**Figure 15B. V<sub>CC</sub> Supply Current vs. Voltage**



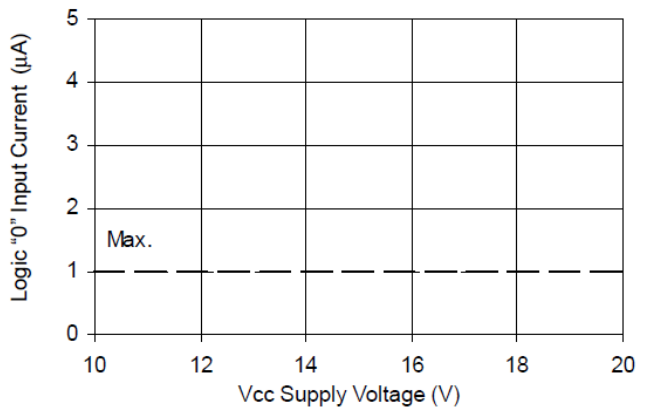
**Figure 16A. Logic "1" Input Current vs. Temperature**



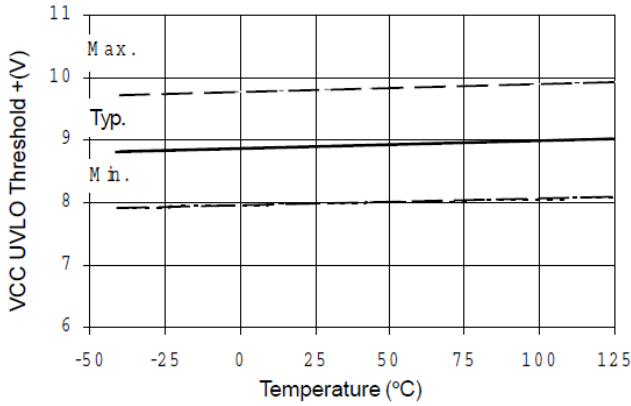
**Figure 16B. Logic "1" Input Current vs. Voltage**



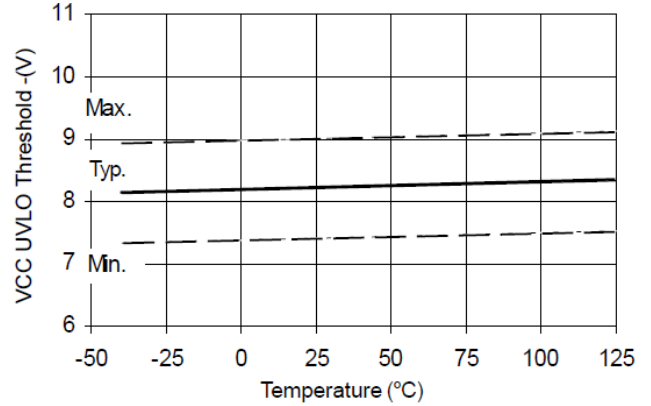
**Figure 17A. Logic "0" Input Current vs. Temperature**



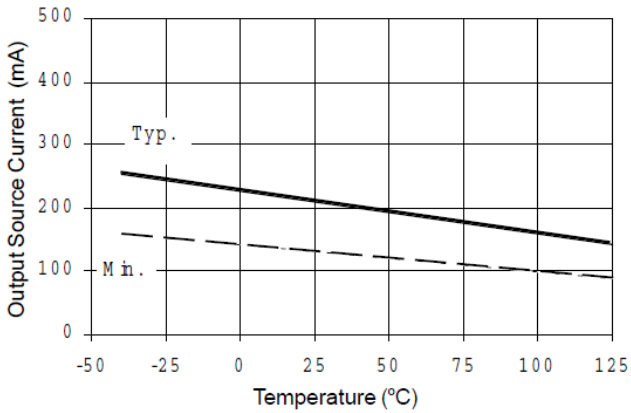
**Figure 17B. Logic "0" Input Current vs. Voltage**



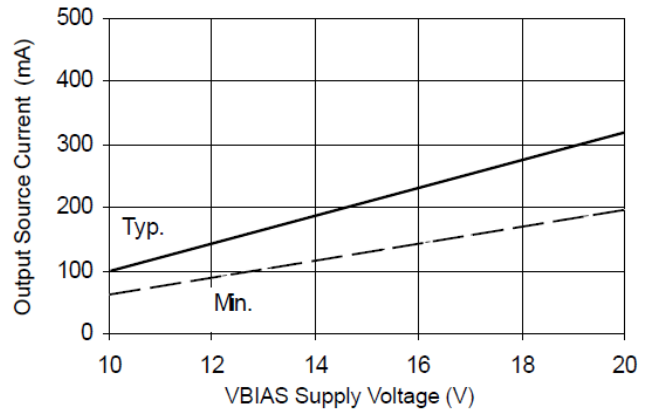
**Figure 18A. V<sub>CC</sub> Undervoltage Threshold (+) vs. Temperature**



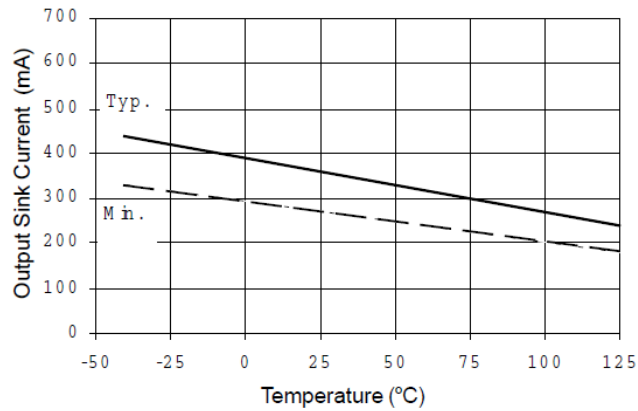
**Figure 18B. V<sub>CC</sub> Undervoltage Threshold (-) vs. Temperature**



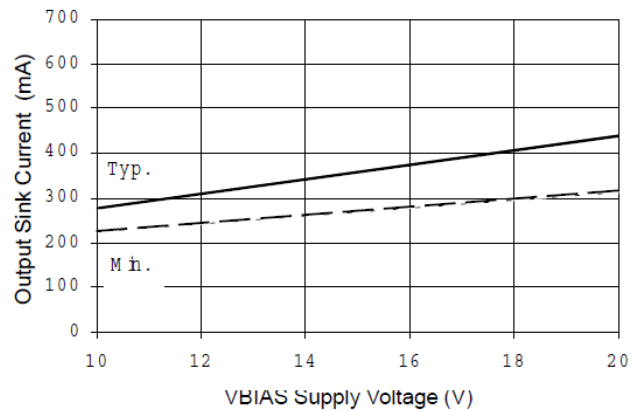
**Figure 19A. Output Source Current vs. Temperature**



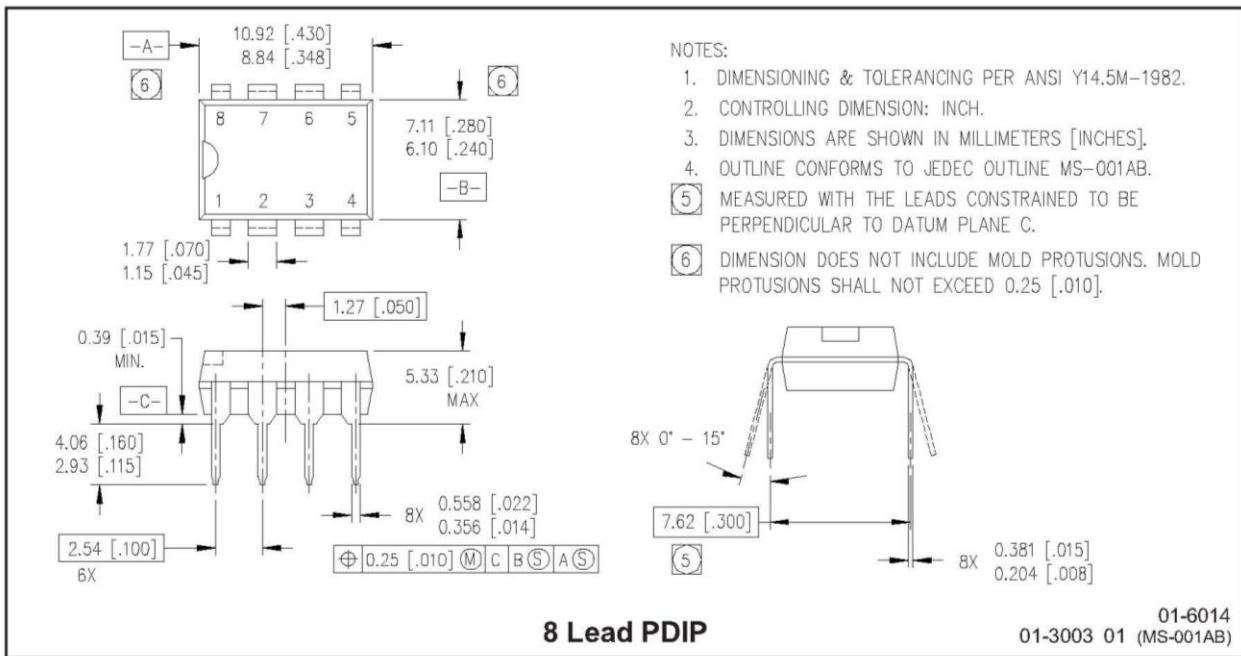
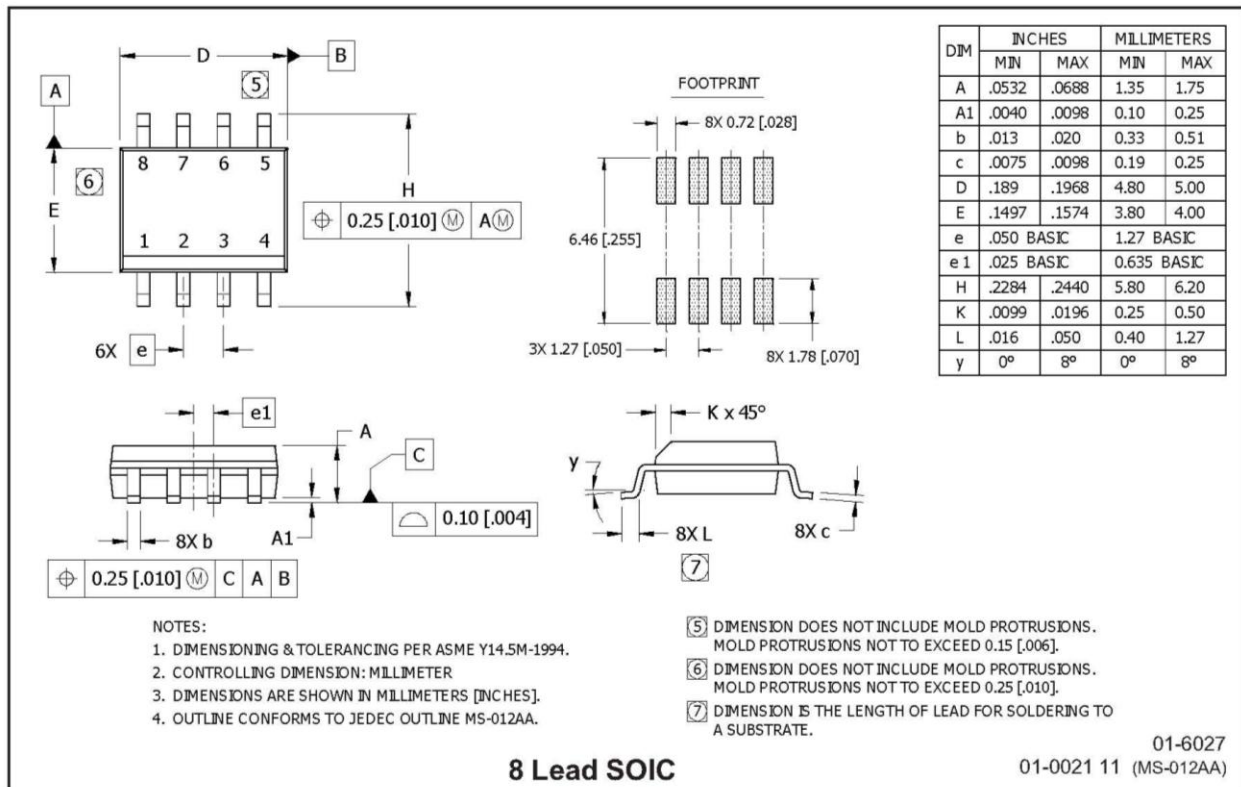
**Figure 19B. Output Source Current vs. Voltage**



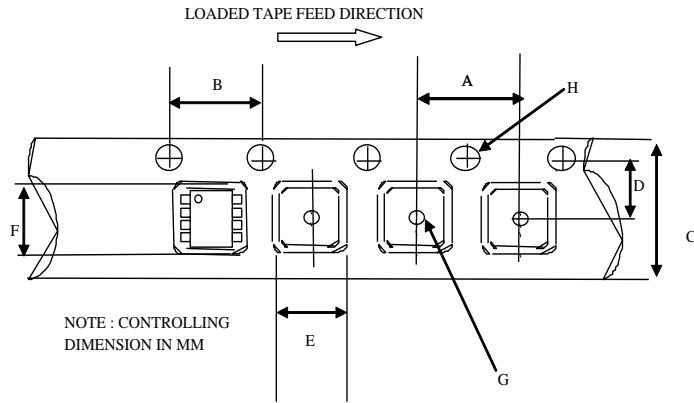
**Figure 20A. Output Sink Current vs. Temperature**



**Figure 20B. Output Sink Current vs. Voltage**

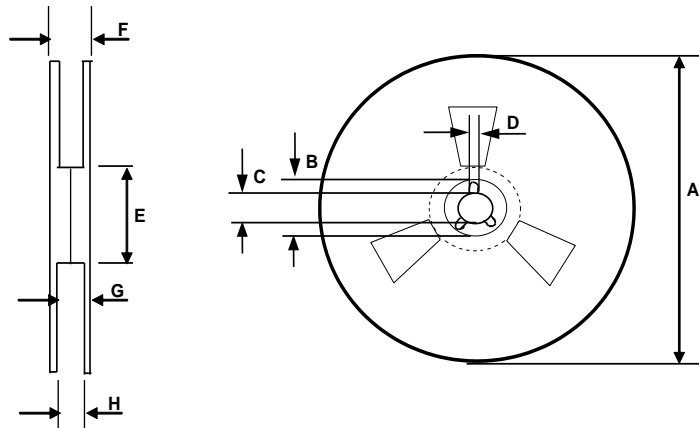
**Package Details: PDIP8, SO8N**

**8 Lead PDIP**

**8 Lead SOIC**

## Tape and Reel Details: SO8N



CARRIER TAPE DIMENSION FOR 8SOICN

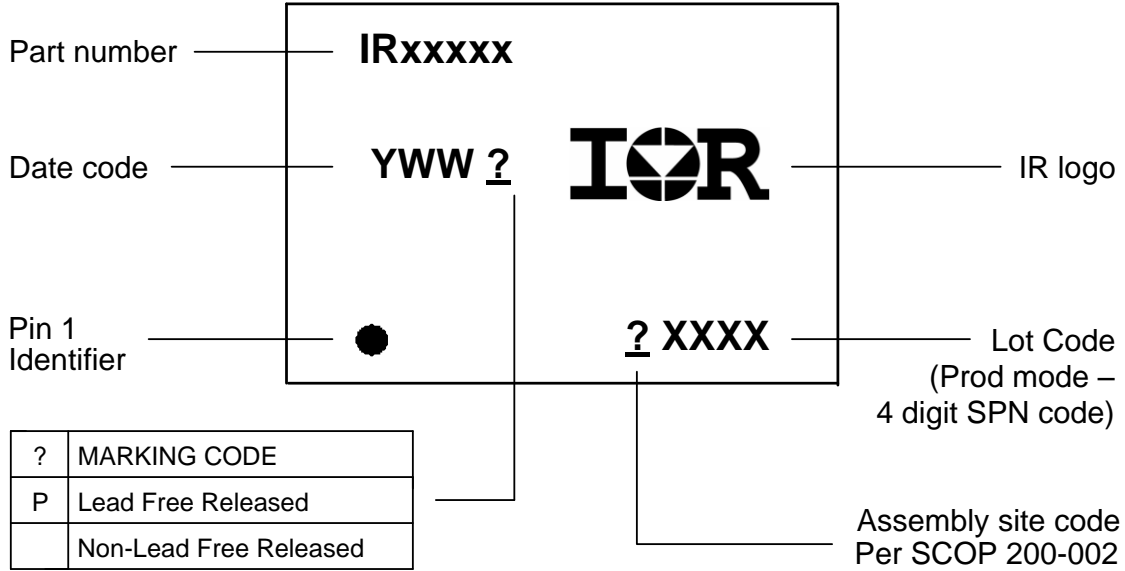
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**



**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial <sup>††</sup> (per JEDEC JESD 47)	
	Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>	SOIC8N	MSL2 <sup>†††</sup> (per IPC/JEDEC J-STD 020)
	PDIP8	Not applicable (non-surface mount package style)
<b>RoHS Compliant</b>	Yes	

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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