THE DATASHEET OF

GPY241B0BC

GPY241

Ethernet Network Connection

4-Port 2.5 Gigabit Ethernet PHY

GPY241 (GPY241B0BC)

Data Sheet

Revision 1.7, 2024-04-18
Reference ID 619982

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Table of Contents

Table of Contents . . . 5
List of Figures . . . 8
List of Tables . . . 9
Preface . . . 11
Document Conventions . . . 11
Document Information . . . 11
1 Product Overview . . . 12
1.1 Features . . . 13
1.2 Block Diagram . . . 15
2 External Signals . . . 16
2.1 Overview . . . 16
2.2 External Signal Description . . . 17
2.2.1 Ball Diagram Overview . . . 17
2.2.2 Ball Diagram . . . 17
2.2.3 Abbreviations . . . 19
2.2.4 Input/Output Signals . . . 20
2.2.4.1 Ethernet Media Interface . . . 20
2.2.4.2 SGMII Interface . . . 22
2.2.4.3 USXGMII Interface . . . 23
2.2.4.4 MDIO Interface . . . 24
2.2.4.5 SPI Interface . . . 24
2.2.4.6 Reset Interface . . . 24
2.2.4.7 LED/UART/JTAG Interface . . . 25
2.2.4.8 Miscellaneous Signals . . . 27
2.2.4.9 Power Supply for GPHY . . . 28
2.2.4.10 Power Supply for SGMIIs and USXGMII . . . 30
2.2.4.11 Power Supply for Twisted Pair Interface (TPI) Analog Front End (AFE) . . . 30
2.2.4.12 Ground . . . 31
3 Functional Description . . . 32
3.1 Power Supply, Clock and Reset . . . 32
3.1.1 Power Supply . . . 32
3.1.2 Clock . . . 32
3.1.3 Reset Generation . . . 32
3.1.4 Power-On Sequence . . . 32
3.1.5 Configuration by Pin Strapping . . . 32
3.2 Configuration via MDIO Management Interface . . . 33
3.3 Ethernet PHY Interface . . . 34
3.3.1 Twisted Pair Interface . . . 34
3.3.2 Transformerless Ethernet (TLE) . . . 34
3.3.3 Auto-Negotiation (ANEG) . . . 35
3.3.4 Auto-Downspeed (ADS) . . . 35
3.3.5 Polarity Reversal Correction . . . 36
3.3.6 Auto-Crossover Correction . . . 36
3.3.7 Wake-on-LAN (WoL) . . . 37
3.4 SGMII Interface . . . 38
3.4.1 Selection of Gigabit PHY . . . 38

3.4.2 SGMII Control and Status Registers . . . 38
3.4.3 Operation Procedure . . . 39
3.4.4 SGMII Configuration at Power Up . . . 40
3.4.5 SGMII PHY-Side Setup According to TPI Setup . . . 40
3.4.6 SGMII PHY-Side Setup Fixed Irrespective of TPI Setup . . . 40
3.4.7 SGMII MAC-Side Setup by MAC SoC . . . 40
3.4.8 SGMII Link Monitoring by MAC SoC . . . 40
3.4.8.1 Actions on TPI Link Down / Link Up Status Change . . . 41
3.4.8.2 New TPI Link Up at Same Speed . . . 41
3.4.8.3 Change of Speed After a New Link Up on TPI . . . 41
3.4.9 Auto-Negotiation Modes Supported by SGMII . . . 42
3.4.9.1 Enabling SGMII Auto-Negotiation Mode . . . 42
3.5 USXGMII Interface . . . 43
3.5.1 USXGMII Configuration at Power Up . . . 43
3.6 LED Interface . . . 44
3.6.1 LED . . . 44
3.6.2 LED Configuration . . . 44
3.6.3 LED Brightness Control . . . 46
3.7 Precision Time Protocol Feature . . . 46
3.7.1 PTP Feature Purpose . . . 46
3.7.2 PTP Feature Configuration . . . 47
3.8 Pulse Per Second Feature . . . 48
3.8.1 PPS Feature Purpose . . . 48
3.8.2 PPS Feature Configuration . . . 48
3.9 Smart-AZ Feature . . . 48
3.10 Power Management . . . 49
3.10.1 Power States . . . 49
3.10.2 RESET Power Up . . . 49
3.10.3 POWER DOWN State . . . 49
3.10.4 SCAN State . . . 50
3.10.5 PING State . . . 50
3.10.6 LP State . . . 50
3.10.7 NORMAL State . . . 54
3.10.8 Low Power IDLE State: Energy-Efficient Ethernet . . . 54
3.11 Firmware Upgrade . . . 55

4 MDIO and MMD Register Interface Description . . . 56
4.1 MDIO-Specific Terminology . . . 56
4.2 Register Naming and Numbering . . . 57
4.2.1 Register Numbering . . . 57
4.2.2 Register Naming . . . 57
4.2.3 Examples . . . 57
4.3 MMD Devices Present in GPY241 . . . 58
4.4 Responsibilities of the STA . . . 58
4.5 MDIO Access Protocols to Read / Write Registers . . . 58

5 MDIO Registers Detailed Description . . . 59
5.1 Standard Management Registers . . . 60
5.1.1 Standard Management Registers . . . 60
5.2 GPY-specific Management Registers . . . 77
5.2.1 GPY-specific Management Registers . . . 77

6 MMD Registers Detailed Description . . . 91

6.1 Standard PMAPMD Registers for MMD=0x01 . . . 92
6.1.1 Standard PMAPMD Registers for MMD=0x01 . . . 93
6.2 Standard PCS Registers for MMD=0x03 . . . 116
6.2.1 Standard PCS Registers for MMD=0x03 . . . 116
6.3 Standard Auto-Negotiation Registers for MMD=0x07 . . . 130
6.3.1 Standard Auto-Negotiation Registers for MMD=0x07 . . . 131
6.4 Vendor Specific 1 Device for MMD=0x1E . . . 150
6.4.1 Vendor Specific 1 Device for MMD=0x1E . . . 150
6.5 Vendor Specific 2 Device for MMD=0x1F . . . 163
6.5.1 Vendor Specific 2 Device for MMD=0x1F . . . 163

7 Chip Electrical Characteristics . . . 167
7.1 Absolute Maximum Ratings . . . 167
7.2 Operating Range . . . 169
7.3 Typical Power Consumption . . . 170
7.4 Maximum Thermal Design Power . . . 171
7.5 Peak Current . . . 172
7.6 DC Characteristics . . . 173
7.6.1 Digital Interfaces . . . 173
7.6.2 Twisted Pair Interface . . . 173
7.6.3 Built-in Temperature Sensor . . . 173
7.7 AC Characteristics . . . 174
7.7.1 Power Up and Power Down Sequence . . . 175
7.7.2 Input Clock . . . 177
7.7.3 Power Supply Rail Requirements . . . 177
7.7.4 MDIO Interface . . . 178
7.7.5 Serial Peripheral Interface (SPI) . . . 179
7.7.6 JTAG Interface . . . 180
7.7.7 SGMII Interface Timing . . . 181
7.7.7.1 SGMII Transmit Timing Characteristics . . . 181
7.7.7.2 SGMII Receive Timing Characteristics . . . 182
7.7.8 UXSGMII Interface Timing . . . 183
7.7.8.1 UXSGMII Transmit Timing Characteristics . . . 183
7.7.8.2 UXSGMII Receive Timing Characteristics . . . 183
7.7.9 Crystal Specification . . . 184
7.8 External Circuitry . . . 185
7.8.1 Twisted-Pair Common-Mode Rejection and Termination Circuitry . . . 185
7.8.2 Transformer (Magnetics) . . . 186
7.8.3 RJ45 Plug . . . 187
7.8.4 Calibration Resistors . . . 187
7.9 Power Supply . . . 187

8 Package Outline . . . 188
8.1 Ordering Information . . . 190

Literature References . . . 191

Standards References . . . 191

Terminology . . . 192

List of Figures

Figure 1 Ethernet Network Connection GPY241 Block Diagram . . . 15
Figure 2 Ethernet Network Connection GPY241 External Signal Overview . . . 16
Figure 3 Ball Diagram for PG-VF2BGA-260 (Top View) . . . 18
Figure 4 MDIO Access Timing . . . 33
Figure 5 Twisted-Pair Interface of GPY241 Including Transformer and RJ45 Plug . . . 34
Figure 6 External Circuitry for the Transformerless Ethernet Application . . . 35
Figure 7 Block Diagram of WoL Application . . . 37
Figure 8 GPY241 SGMII Configuration and Status Registers . . . 38
Figure 9 LED Connection Options to Ground or Power Supply . . . 44
Figure 10 Connection of a Dual Color LED and Configuring Pin Strap Value . . . 45
Figure 11 Connection of a Single Color LED and Configuring Pin Strap Value . . . 45
Figure 12 LED Brightness Control by Controlling LED Output Enable/Disable . . . 46
Figure 13 State Diagram for Power Down State Management . . . 49
Figure 14 LP Sequence . . . 51
Figure 15 EEE Low Power Idle Sequence . . . 54
Figure 16 Input/Output Waveform for AC Tests . . . 174
Figure 17 Timing Diagram for the Reset Sequence in SGMII Mode . . . 175
Figure 18 Timing Diagram for the Reset Sequence in USXGMII Mode . . . 176
Figure 19 Timing Diagram for the MDIO Interface . . . 178
Figure 20 SPI Master Interface Timing . . . 179
Figure 21 Test Interface Timing . . . 180
Figure 22 Transmit Timing Diagram of the SGMII (shows alternating data sequence) . . . 181
Figure 23 Receive Timing Diagram of the SGMII (alternating data input sequence) . . . 182
Figure 24 Twisted Pair Common-Mode Rejection and Termination Circuitry . . . 185
Figure 25 Schematic of an Ethernet Transformer Device . . . 186
Figure 26 PG-VF2BGA-260 12 mm x 12 mm Package Outline . . . 189

List of Tables

Table 1 Ball Diagram Color Codes . . . 17
Table 2 Abbreviations for Pin Type . . . 19
Table 3 Abbreviations for Buffer Type . . . 19
Table 4 Ethernet Media Interface Signals . . . 20
Table 5 SGMII Interface Signals . . . 22
Table 6 USXGMII Interface Signals . . . 23
Table 7 Management Interface Signals . . . 24
Table 8 Management Interface Signals . . . 24
Table 9 Reset Signals . . . 24
Table 10 LED and Debug Interface Signals . . . 25
Table 11 Miscellaneous Signals . . . 27
Table 12 Power Supply Pins . . . 28
Table 13 Power Supply Pins . . . 30
Table 14 Power Supply Pins . . . 30
Table 15 Power Supply Pins . . . 31
Table 16 Pin Names Used for Pin Strapping . . . 33
Table 17 Pin Strapping Configuration Description . . . 33
Table 18 Supported Twisted Pair Mappings on a CAT5 or Better Cable . . . 36
Table 19 Programming Sequence for the Wake-on-LAN Functionality . . . 37
Table 20 XPCS Feature List . . . 43
Table 21 LP State Entry and Exit Sequence . . . 52
Table 22 MDIO / MMD Devices Present in GPY241 . . . 58
Table 23 Register Access Type . . . 59
Table 24 Registers Overview . . . 60
Table 25 Registers Overview . . . 77
Table 26 Register Access Type . . . 91
Table 27 Registers Overview . . . 92
Table 28 Registers Overview . . . 116
Table 29 Registers Overview . . . 130
Table 30 Registers Overview . . . 150
Table 31 Registers Overview . . . 163
Table 32 Absolute Maximum Ratings . . . 167
Table 33 Operating Range . . . 169
Table 34 Typical Power Consumption in SGMII Configuration . . . 170
Table 35 Typical Power Consumption in USXGMII Configuration . . . 170
Table 36 Maximum Power Consumption . . . 171
Table 37 Peak Current Per Rail . . . 172
Table 38 DC Characteristics of the GPIO Interfaces (VDDP=3.3 V) . . . 173
Table 39 Temperature Sensor Characteristics . . . 173
Table 40 Power Supply Timings . . . 176
Table 41 AC Characteristics of Input Clock on XTAL1 Pin . . . 177
Table 42 AC Characteristics of the Power Supply . . . 177
Table 43 Timing Characteristics of the MDIO Interface . . . 178
Table 44 SPI Interface Timing Parameters . . . 179
Table 45 Test Interface Clock . . . 180
Table 46 JTAG Timing . . . 180
Table 47 Transmit Timing Characteristics of the SGMII . . . 181
Table 48 Receive Timing Characteristics of the SGMII . . . 182
Table 49 Transmit Timing Characteristics of the UXSGMII . . . 183

List of Tables

Table 50 Receive Timing Characteristics of the UXSGMII 183
Table 51 Specification of the Crystal 184
Table 52 Electrical Characteristics for Common-Mode Rejection and Termination Circuitry 185
Table 53 Electrical Characteristics for Supported Transformers (Magnetics) 186
Table 54 Electrical Characteristics for Supported RJ45 Plugs 187
Table 55 Calibration Resistors Values. 187
Table 56 JEDEC Thermal Resistance Package Parameter - Still air conditions at 85°C 188
Table 57 JEDEC Thermal Resistance Package Parameter - Still air conditions at 70°C 188
Table 58 JEDEC Thermal Resistance Package Parameter - With Thermal Solution Environment 188
Table 59 JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network 188
Table 60 Product Naming 190

Preface

This Data Sheet describes the features and architecture of the Ethernet Network Connection EASY GPY241.

Document Conventions

In the interest of brevity, this document uses short names to represent full MaxLinear product names.

GPY241	Ethernet Network Connection EASY GPY241

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Organization of this Document

- **Chapter 1**, **Product Overview**
  This chapter provides an overview.
- **Chapter 2**, **External Signals**
  This chapter provides the external signals.
- **Chapter 3**, **Functional Description**
  This chapter provides the function description.
- **Chapter 4**, **MDIO and MMD Register Interface Description**
  This chapter describes the MDIO and MMD register format.
- **Chapter 5**, **MDIO Registers Detailed Description**
  This chapter details the MDIO registers.
- **Chapter 6**, **MMD Registers Detailed Description**
  This chapter details the MDD registers.
- **Chapter 7**, **Chip Electrical Characteristics**
  This chapter provides the electrical specifications.
- **Chapter 8**, **Package Outline**
  This chapter provides information about the package.
- **Literature References** and **Standards References**
- **Terminology**

1 Product Overview

The Ethernet Network Connection GPY241 is a low power Quad - Ethernet PHY transceiver integrated circuit. It offers a cost-optimized solution well-suited for routers, switches, and home gateways. GPY241 supports four data rates: 2500, 1000, 100, and 10 Mbps.

On the Ethernet twisted pair interface, the GPY241 is compliant with these IEEE 802.3 standards referenced in **[5]** and **[6]**: 2.5GBASE-T (IEEE 802.3bz, NBASE-T), 1000BASE-T (IEEE 802.3 Clause 40), 100BASE-TX (IEEE 802.3 Clause 25), and 10BASE-Te (IEEE 802.3 Clause 14). This interface supports the Energy-Efficient Ethernet feature to reduce idle mode power consumption. Power saving at the system level is also possible with the wake-on-LAN feature. A low-EMI line driver with integrated termination facilitates the PCB design.

With reference to the Open System Interconnection (OSI) model, GPY241 implements a layer 1 physical media access device, and is connected to a layer 2 MAC using a SerDes data interface and an MDIO management interface.

GPY241 provides two options for the SerDes data interface:

- A USXGMII single-lane interface with 10.3125 GHz bit clock to connect to a MAC processor with a single Rx / Tx lane
- A quad-lane SGMII interface with a clock of up to 3.125 GHz or 1.25 GHz bit to connect to legacy switches that only support SGMII and not USXGMII.

The chip operates in one of the two SerDes modes, which are mutually exclusive.

On the SerDes interface, connecting to another chip implementing a MAC layer, the GPY241 supports these standards: IEEE802.3 Clause 36 and 27 **[5]**, and Cisco SGMII **[8]**. This interface also operates at these data rates: 2500, 1000, 100, and 10 Mbps.

The GPY241 supports a standard MDIO management interface as defined in IEEE 802.3 Clause 22 and Clause 45 **[5]**, **[6]**. The MDIO serial interface is operable with a clock running up to 25 MHz. It allows a management entity (the external chip implementing the MAC) to access standard MDIO / MMD registers to control the GPY241 behavior, or to read the link status. In addition, two vendor specific register banks (VSPEC1 and VSPEC2) allow GPY241 specific configuration of LED, SGMII, and wake-on-LAN features. The MDIO and MMD registers are documented in **Chapter 5**. The GPY241 is also configurable via pin strapping.

The GPY241 is capable of driving up to twelve LEDs (3 per BASE-T port). Each LED is independently programmable to indicate the link speed and traffic activities. Several indication schemes are selectable.

External supplies of 0.95 V and 3.3 V are required to power the GPY241. When USXGMII is used, an additional external supply of 1.8 V is required for the USXGMII SerDes and Low Jitter PLL.

The GPY241 uses a ball grid array package (type BGA 18 x18 matrix, size 12 mm x 12 mm).

1.1 Features

This section provides an overview of the features supported by the GPY241.

Communication Interfaces

- The multiple speed, four-port Ethernet PHY interfaces to the twisted pair cables support:
  - Ethernet modes and standards: 2.5GBASE-T (IEEE 802.3bz, NBASE-T), 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3) and 10BASE-Te (IEEE 802.3)
  - Ethernet twisted pair copper cable of category CAT5 or higher
  - Low EMI voltage mode line driver with integrated termination resistors
  - Transformerless Ethernet for backplane applications
  - Auto-negotiation (ANEG) with extended next page support
  - Auto-MDIX and polarity correction
  - Auto-downspeed (ADS)
  - Energy-Efficient Ethernet (EEE) and Power Down (PD) mode
  - Cable diagnostics: cable open/short detection and cable length estimation
  - Wake-on-LAN (WoL)
  - Power-over-Ethernet (POE)
  - Precise time stamping, implementing standard IEEE 1588v2
  - Jumbo frames of up to 10 KB

- The four SGMII SerDes interfaces support:
  - Cisco Serial-GMII Specification [8] operating at 1.25 Gbaud/s; extensions to achieve 3.125 GBaud/s by overclocking the SerDes
  - 2.5 Gbps (one lane of XAUI conforming per 802.3, part 4, clause 47: 10 Gigabit Attachment Unit Interface (XAUI) full duplex)
  - Clock and Data Recovery (CDR), no clock forwarding required
  - SGMII power saving when a Low Power Indication (LPI) is active

- The four SGMII PCS interfaces support:
  - IEEE 802.3 clause 36 and 37 compliant PCS component
  - Cisco Serial-GMII Specification [8] operating at 1.25 Gbaud/s; extensions to achieve 3.125 GBaud/s by overclocking the SGMII PCS
  - IEEE 802.3 clause 35 compliant GMII and MII interface (GMII compliant except for transmit clock direction); extensions to achieve operation at 2.5 Gbps by overclocking
  - 2.5 Gbps full duplex, 1 Gbps full duplex, 100 Mbps full/half duplex, and 10 Mbps full/half duplex
  - Minimum IPG of 4 bytes and minimum preamble of 0 bytes (before considering clock deviation factor)

- The USXGMII SerDes interface supports:
  - IEEE 802.3-2012, IEEE 10GBASE-KR (10.3125 Gbps) and Energy Efficient Ethernet (EEE) Physical Layer electrical specifications
  - Back channel adaptation, auto-negotiation, forward error correction (FEC), and Energy-Efficient Ethernet (EEE)
  - Clock and Data Recovery (CDR), no clock forwarding required
  - Power saving when a Low Power Indication (LPI) is active

- The quad mode XPCS supports:
  - Clause 73 auto-negotiation per Ethernet PCS
  - USXGMII with clause 37 auto-negotiation per Ethernet XPCS
  - Clause 72 for 10G-base (K)R training
  - PCH preamble

  - EEE mode

- The management interface supports the communication between the Station Management (STA), per the IEEE 802.3, and the GPY241 using:
  - An MDIO slave interface that provides access to the standard registers in the MMD as described in IEEE 802.3 Clause 22 and Clause 45 **[4]** and **Chapter 5**.
  - An MDIO interface clock of up to 25 MHz
  - 3 MDIO message frame types as described in IEEE 802.3: Clause 22, Clause 22 Extended, Clause 45 **[4]**

- The SPI master interface connecting to serial external E2PROM memory supports:
  - Programmable interface clocks: maximum 100 MHz
  - Internal PHY firmware code access from external E2PROM memory
  - Write access to the E2PROM memory
  - Different E2PROM sizes from 512 Kbit to 128 Mbit
  - Secure firmware upgrade of the flash memory

- The JTAG boundary scan, test and debug interface supports:
  - Shared pins with GPIO functions

- The LED interface supports:
  - Up to 3 LEDs per port
  - Single and dual color LEDs
  - Connection of LED to ground or 3.3 V
  - Several LED indication schemes (link/activity, duplex/collision, link speed)
  - Configuration of LED indication via MDIO registers
  - Control of LED brightness via software driver API
  - Alternative configuration of LED pins as GPIO for custom indication

- Supports two external interrupts:
  - Configurable as output to an external controller
  - Configurable as input from external device(s)
  - Configurable edge, level, and polarity

Clocking, Timing and Time Stamping Features

- 25 MHz crystal operation
- Precise time stamping (PTP) according to standard IEEE 1588v2
- Three general purpose clock pins GPC1, GPC2, and GPC3 shared with GPIO for several usage options, configurable by GPY API:
  - to input or output the precise time stamping signals (PTP)
  - to output the pulse per second signal (PPS)

Other Features

- Temperature Sensor (warning, interrupt and auto-downspeed)
-

Power Supply

- 3.3 V and 0.95 V external power sources
- When operated in USXGMII mode instead of SGMII mode, an additional external supply of 1.8 V is required.

1.2 Block Diagram

Figure 1 shows the block diagram of the GPY241. The main interfaces are:

- Data interface to a MAC processor, using SGMII/USXGMII
- Slave control interface driven by a MAC processor, using MDIO slave
- Interrupt signal MDINT allowing the GPY241 to notify the MAC processor about a change of status
- LED control
- Twisted pair interface
- Master SPI interface to download the firmware

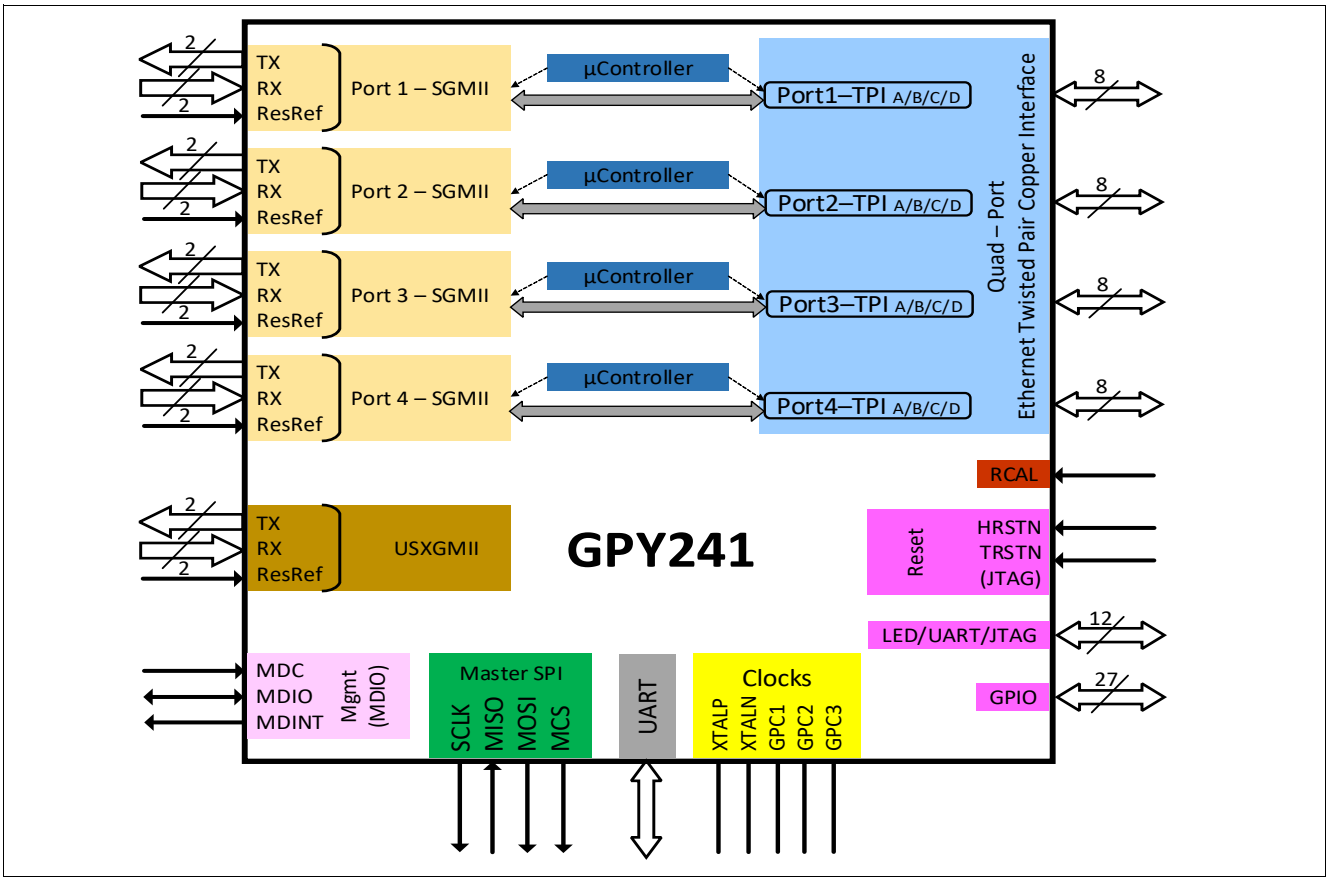


Figure 1 Ethernet Network Connection GPY241 Block Diagram

2 External Signals

This chapter describes the signal mapping to the package.

2.1 Overview

Figure 2 provides an overview of the external interfaces of the GPY241.

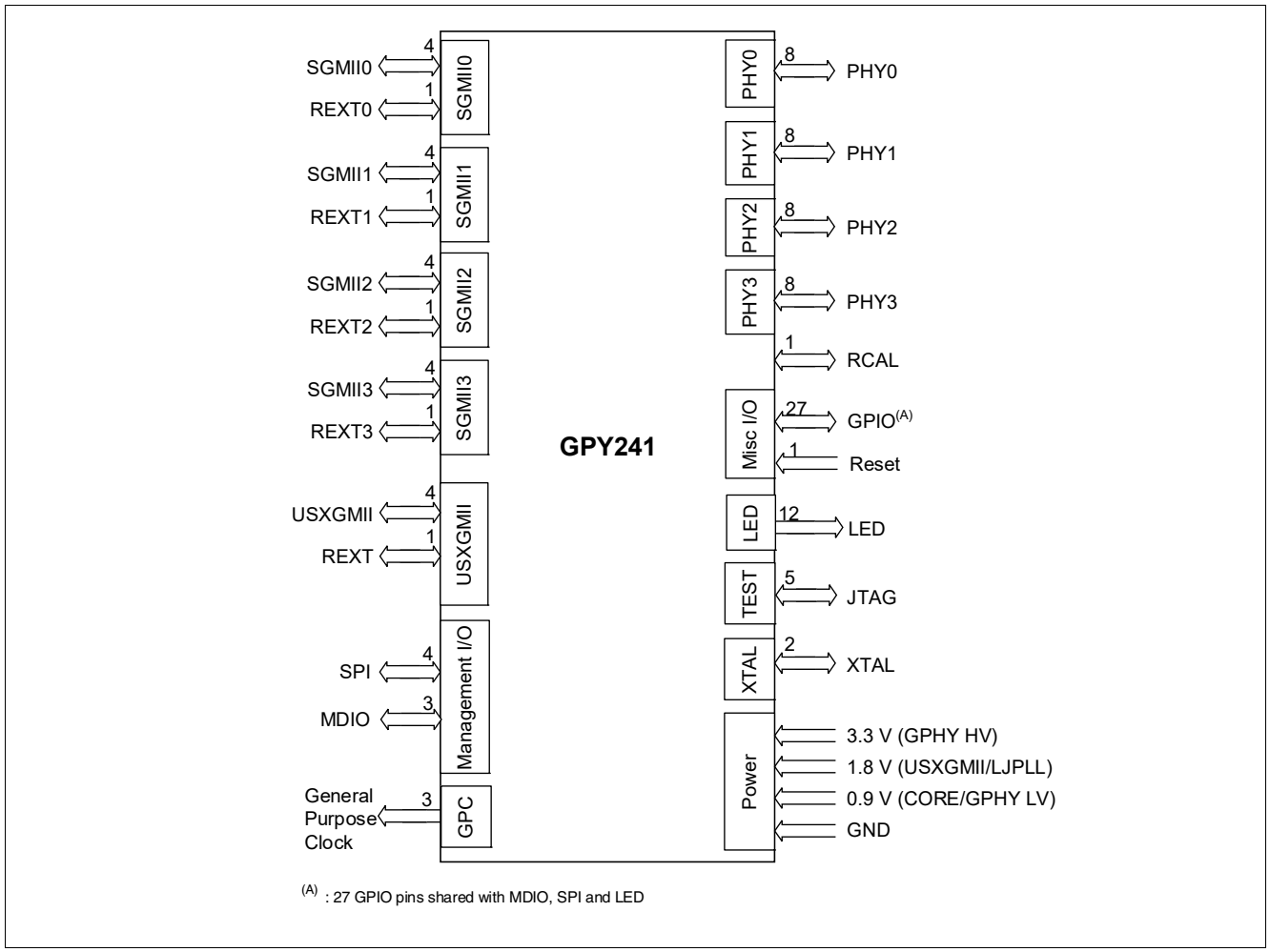


Figure 2 Ethernet Network Connection GPY241 External Signal Overview

2.2 External Signal Description

This section provides in detail the ball diagram, abbreviations for pin types and buffer types, and the table of input and output signals.

2.2.1 Ball Diagram Overview

Figure 3 describes the positions of the balls on the GPY241 package.

2.2.2 Ball Diagram

Figure 3 shows the ball diagram. **Table 1** lists the ball diagram color codes.

Table 1 Ball Diagram Color Codes

Color	Description
White in outer ring	Unpopulated Balls
Orange	Power
Grey	Ground
Red	GPHY Signals
Pink	SGMII Signals
Green	USXGMI Signals
Yellow	GPIO, JTAG Interface
Blue	MDIO, SPI, Reset Signals
White	NC

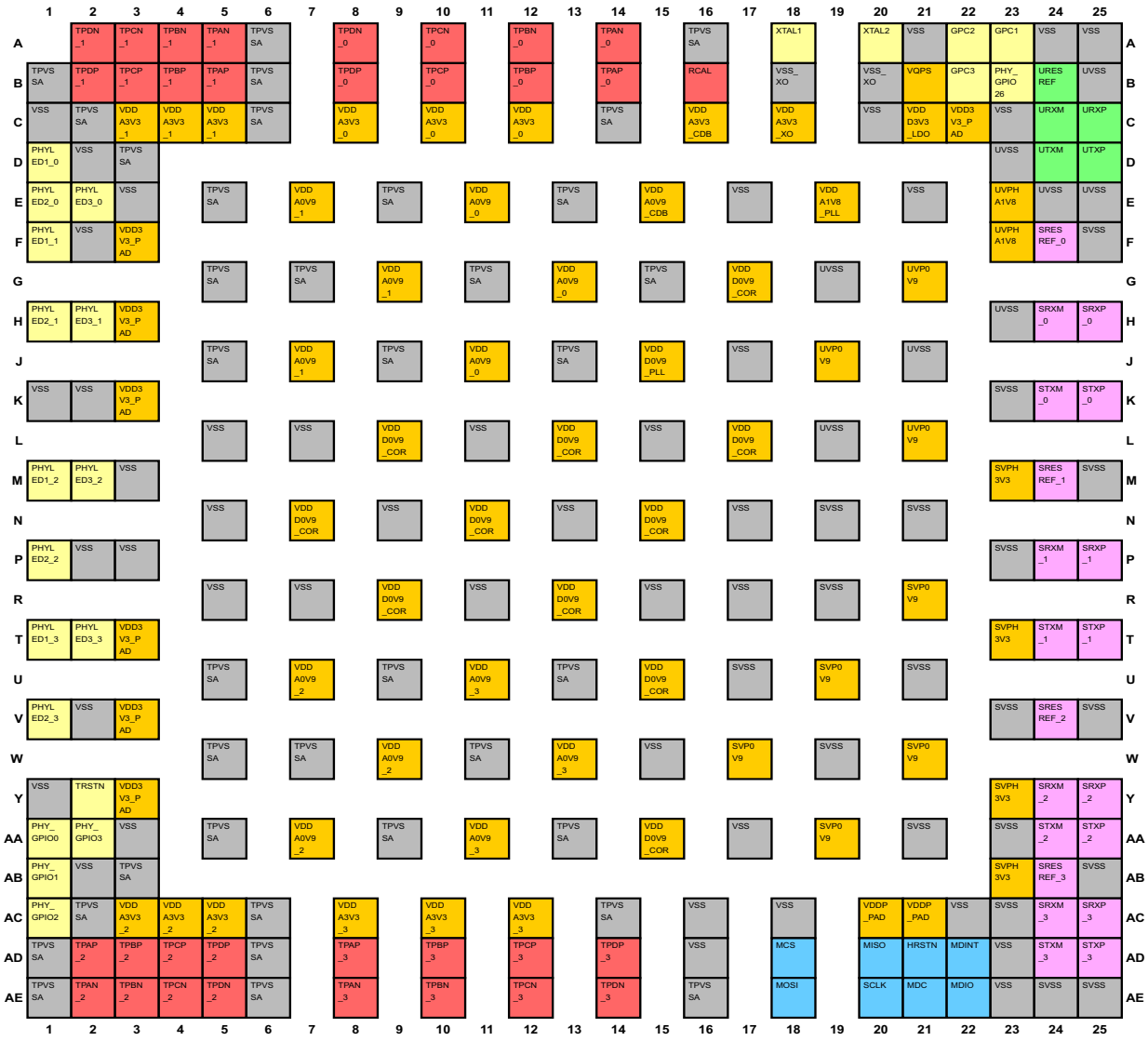


Figure 3 Ball Diagram for PG-VF2BGA-260 (Top View)

2.2.3 Abbreviations

Table 2 and Table 3 summarize the abbreviations used in the signal tables.

Table 2 Abbreviations for Pin Type

Abbreviations	Description
I	Input only, digital levels
O	Output only, digital levels
I/O	Bidirectional input/output signal, digital levels
Prg	Bidirectional pad, programmable to operate either as input or output, digital levels
AI	Input only, analog levels
AO	Output only, analog levels
AI/O	Bidirectional, analog levels
PWR	Power
GND	Ground

Table 3 Abbreviations for Buffer Type

Abbreviations	Description
LVTTL n	LVTTL characteristics, n = A, B, or C (driver strength)
LVTTL n PU m	LVTTL characteristics with weak pull-up device; n = A, B, or C (driver strength); m = A, B, or C (pull-up strength)
LVTTL n PD m	LVTTL characteristics with weak pull-down device; n = A, B, or C (driver strength); m = A, B, or C (pull-down strength)
LVTTL n OD	LVTTL characteristics with open-drain characteristic, n = A, B, or C (driver strength)
LVTTL n PP	LVTTL characteristics with push-pull characteristic, n = A, B, or C (driver strength)
A	Analog characteristics, refer to the AC/DC specification for more detail.

2.2.4 Input/Output Signals

Table 4 to Table 15 provide a detailed description of all the pins.

2.2.4.1 Ethernet Media Interface

Table 4 Ethernet Media Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Ethernet Port 0 Ethernet Media Interface				
B14	**TPAP_0**	AI/AO	A	**Port 0 Transmit/Receive Positive/Negative**
A14	**TPAN_0**	AI/AO	A	
B12	**TPBP_0**	AI/AO	A	
A12	**TPBN_0**	AI/AO	A	
B10	**TPCP_0**	AI/AO	A	
A10	**TPCN_0**	AI/AO	A	
B8	**TPDP_0**	AI/AO	A	
A8	**TPDN_0**	AI/AO	A	
B5	**TPAP_1**	AI/AO	A	**Port 1 Transmit/Receive Positive/Negative**
A5	**TPAN_1**	AI/AO	A	
B4	**TPBP_1**	AI/AO	A	
A4	**TPBN_1**	AI/AO	A	
B3	**TPCP_1**	AI/AO	A	
A3	**TPCN_1**	AI/AO	A	
B2	**TPDP_1**	AI/AO	A	
A2	**TPDN_1**	AI/AO	A	
AD2	**TPAP_2**	AI/AO	A	**Port 2 Transmit/Receive Positive/Negative**
AE2	**TPAN_2**	AI/AO	A	
AD3	**TPBP_2**	AI/AO	A	
AE3	**TPBN_2**	AI/AO	A	
AD4	**TPCP_2**	AI/AO	A	
AE4	**TPCN_2**	AI/AO	A	
AD5	**TPDP_2**	AI/AO	A	
AE5	**TPDN_2**	AI/AO	A	

Table 4 Ethernet Media Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
AD8	**TPAP_3**	AI/AO	A	**Port 3 Transmit/Receive Positive/Negative**
AE8	**TPAN_3**	AI/AO	A	
AD10	**TPBP_3**	AI/AO	A	
AE10	**TPBN_3**	AI/AO	A	
AD12	**TPCP_3**	AI/AO	A	
AE12	**TPCN_3**	AI/AO	A	
AD14	**TPDP_3**	AI/AO	A	
AE14	**TPDN_3**	AI/AO	A	
Ethernet Port Calibration				
B16	**RCAL**	AI/AO	A	**Calibration for all GPHY Ethernet Ports**

2.2.4.2 SGMII Interface

Table 5 SGMII Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
H25	**SRXP_0**	AI	HD	**Differential SGMII Data Input Pair/Lane 0** These are the negative and positive signals, respectively, of the differential input pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
H24	**SRXM_0**	AI	HD	
K25	**STXP_0**	AO	HD	**Differential SGMII Data Output Pair/Lane 0** These are the negative and positive signals, respectively, of the differential output pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
K24	**STXM_0**	AO	HD	
F24	**SRESREF_0**	AI/O	A	**Connection for External Tuning Resistor/Lane 0**
P25	**SRXP_1**	AI	HD	**Differential SGMII Data Input Pair/Lane 1** These are the negative and positive signals, respectively, of the differential input pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
P24	**SRXM_1**	AI	HD	
T25	**STXP_1**	AO	HD	**Differential SGMII Data Output Pair/Lane 1** These are the negative and positive signals, respectively, of the differential output pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
T24	**STXM_1**	AO	HD	
M24	**SRESREF_1**	AI/O	A	**Connection for External Tuning Resistor/Lane 1**
Y25	**SRXP_2**	AI	HD	**Differential SGMII Data Input Pair/Lane 2** These are the negative and positive signals, respectively, of the differential input pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
Y24	**SRXM_2**	AI	HD	
AA25	**STXP_2**	AO	HD	**Differential SGMII Data Output Pair/Lane 2** These are the negative and positive signals, respectively, of the differential output pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
AA24	**STXM_2**	AO	HD	
V24	**SRESREF_2**	AI/O	A	**Connection for External Tuning Resistor/Lane 2**

Table 5 SGMII Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
AC25	**SRXP_3**	AI	HD	**Differential SGMII Data Input Pair/Lane 3** These are the negative and positive signals, respectively, of the differential input pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
AC24	**SRXM_3**	AI	HD	
AD25	**STXP_3**	AO	HD	**Differential SGMII Data Output Pair/Lane 3** These are the negative and positive signals, respectively, of the differential output pair of the SGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for SGMII. These pins must be AC-coupled.
AD24	**STXM_3**	AO	HD	
AB24	**SRESREF_3**	AI/O	A	**Connection for External Tuning Resistor/Lane 3**

2.2.4.3 USXGMII Interface

Table 6 USXGMII Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
C25	**URXP**	AI	HD	**Differential USXGMII Data Input Pair** These are the negative and positive signals, respectively, of the differential input pair of the USXGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for USXGMII. These pins must be AC-coupled.
C24	**URXM**	AI	HD	
D25	**UTXP**	AO	HD	**Differential USXGMII Data Output Pair** These are the negative and positive signals, respectively, of the differential output pair of the USXGMII SerDes interface. Due to the integrated CDR, no external transmission peer source-synchronous clock is required for USXGMII. These pins must be AC-coupled.
D24	**UTXM**	AO	HD	
B24	**URESREF**	AI	A	**Connection for External USXGMII Tuning Resistor**

2.2.4.4 MDIO Interface

There are two types of serial management interfaces provided:

- SPI master interface
- MDIO slave interface

Attention: The pin functionality in Table 7 highlighted in bold indicates the pin name.

Table 7 Management Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
MDIO Slave Interface				
AD22	**MDINT**	O		**MDIO Interrupt from Any GPHY** The MDIO interrupt is used to interrupt an external block, such as a higher-level management entity or a device controller of an SoC, on detection of certain events and states inside the GPHY device.
AE21	**MDC**	I		**MDIO Slave Clock** The external controller provides the serial clock of up to 25 MHz on this input.
AE22	**MDIO**	I/O		**MDIO Slave Data Input/Output** The external controller uses this signal to address internal registers and to transfer data to and from the internal registers.

2.2.4.5 SPI Interface

Table 8 Management Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
AD20	**MISO**	I		**SPI Data Input** SPI interface data input
AE18	**MOSI**	O		**SPI Data Output** SPI interface data output
AE20	**SCLK**	O		**SPI Clock** SPI interface clock
AD18	**MCS**	O		**SPI Chip Select** SPI interface chip select. Active low signal.

2.2.4.6 Reset Interface

Table 9 Reset Signals

Pin No.	Name	Pin Type	Buffer Type	Function
AD21	**HRSTN**	I	PU	**Hardware Reset** Asynchronous active low device reset

2.2.4.7 LED/UART/JTAG Interface

The LED interface is used to connect external LEDs to indicate the status of the the Ethernet PHY interfaces. Single and dual color LEDs are supported.

Attention: The pin functionality highlighted in bold in Table 10 indicates the pin name.

Table 10 LED and Debug Interface Signals

Pin No.	Name	Pin Type	Buffer Type	Function
LED Signals				
D1	**PHYLED1_0**	O		**GPHY LED1 for Port 0** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
	FW_UTXD	O		**Firmware UART Data Output** Firmware UART interface data output
E1	**PHYLED2_0**	O		**GPHY LED2 for Port 0** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
	FW_URXD	I		**Firmware UART Data Input** Firmware UART interface data input
E2	**PHYLED3_0**	I/O		**GPHY LED3 for Port 0** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs. This pin is also used for the brightness control switch input.
F1	**PHYLED1_1**	O		**GPHY LED1 for Port 1** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
	FW_UTXD	O		**Firmware UART Data Output** Firmware UART interface data output
H1	**PHYLED2_1**	O		**GPHY LED2 for Port 1** This signal controls the LED output. It is freely configurable and drives either drives single color or dual color LEDs.
H2	**PHYLED3_1**	O		**GPHY LED3 for Port 1** This signal controls the LED output. It is freely configurable and drives either drives single color or dual color LEDs.
M1	**PHYLED1_2**	O		**GPHY LED1 for Port 2** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
	FW_UTXD	O		**Firmware UART Data Output** Firmware UART interface data output
	TDI	I		**JTAG Serial Test Data Input**
P1	**PHYLED2_2**	O		**GPHY LED2 for Port 2** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
	TMS	I		**JTAG Test Mode Select**

Table 10 LED and Debug Interface Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
M2	**PHYLED3_2**	O		**GPHY LED3 for Port 2** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
	TDO	O		**JTAG Serial Test Data Output** JTAG test data output
T1	**PHYLED1_3**	O		**GPHY LED1 for Port 3** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
	FW_UTXD	O		**Firmware UART Data Output** Firmware UART interface data output
	TCK	I		**JTAG Test Clock** The signals TDI, TDO and TMS are synchronous to this JTAG test clock. *Note: When the JTAG Controller is held in the reset state, i.e. GPY241 operates in normal mode, this clock pin does not need to be clocked.*
V1	**PHYLED2_3**	O		**GPHY LED2 for Port 3** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
T2	**PHYLED3_3**	O		**GPHY LED3 for Port 3** This signal controls the LED output. It is freely configurable and drives either single color or dual color LEDs.
Y2	TRSTN	I	PD	**JTAG Test Enabling** 1_B **JTAG** The GPIO pins are used as the JTAG interface (TCK, TDI, TDO, TMS). 0_B **GPIO** The GPIO pins are in their normal application mode. *Note: The integrated pull-down resistor holds the TAP controller in its reset state when this pin is left open. This is different to the JTAG specification given by IEEE 1149.1.*

2.2.4.8 Miscellaneous Signals

Attention: The pin functionality highlighted in bold in Table 11 indicates the pin name.

Table 11 Miscellaneous Signals

Pin No.	Name	Pin Type	Buffer Type	Function
Reset and Clocking				
A18	**XTAL1**	AI	A	**Crystal: Oscillator Input** A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must tie both pins to GND. **Crystal Oscillator: Clock Input** A clock must be connected to XTAL1. See **Section 7.7.2** for the clock details.
A20	**XTAL2**	AO	A	**Crystal: Oscillator Output** A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must tie both pins to GND.
A22	**GPC2**	Prg		**General Purpose Clock 2** General purpose clock for SyncE or external devices. Selectable as input or output.
A23	**GPC1**	Prg		**General Purpose Clock 1** General purpose clock for SyncE or external devices. Selectable as input or output.
B22	**GPC3**	Prg		**General Purpose Clock 2** General purpose clock for SyncE or external devices. Selectable as input or output.
AA1	**PHY_GPIO0**	Prg	Prg	**General Purpose IO 1** Selectable as input or output. The output characteristic is configurable as open drain or push-pull.
	EXTINT0	Prg	Prg	**External Interrupt 0**
	HW_UTXD	Prg	Prg	
AB1	**PHY_GPIO1**	Prg	Prg	**General Purpose IO 1** Selectable as input or output. The output characteristic is configurable as open drain or push-pull.
	EXTINT1	Prg	Prg	**External Interrupt 1**
	HW_URXD	Prg	Prg	
AC1	**PHY_GPIO2**	Prg	Prg	**General Purpose IO 2** Selectable as input or output. The output characteristic is selected as open drain or push-pull.
	OBS_CLK	O		**Clock Observation Output (Alternate to GPIO2)**

Table 11 Miscellaneous Signals (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
AA2	**PHY_GPIO3**	Prg	Prg	**General Purpose IO 3** Selectable as input or output. The output characteristic is configurable as open drain or push-pull.
B23	**PHY_GPIO26**	Prg		**General Purpose IO 26** Selectable as input or output. The output characteristic is configurable as open drain or push-pull.

2.2.4.9 Power Supply for GPHY

This section specifies the power supply pins for GPHY.

Table 12 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
C8, C10, C12	**VDDA3V3_0**	PWR		**GPHY0 High Voltage Domain Supply** This is the group of supply pins for the high voltage domain. It supplies the Analog Front End (AFE) of the Gigabit Ethernet PHY.
E11, G13, J11	**VDDA0V9_0**	PWR		**GPHY0 Low Voltage Domain Supply** This is the group of supply pins for the low voltage domain. It supplies mixed signal blocks in the AFE and CDB of the Gigabit Ethernet PHY.
C3, C4, C5	**VDDA3V3_1**	PWR		**GPHY1 High Voltage Domain Supply** This is the group of supply pins for the high voltage domain. It supplies the AFE of the Gigabit Ethernet PHY.
E7, G9, J7	**VDDA0V9_1**	PWR		**GPHY1 Low Voltage Domain Supply** This is the group of supply pins for the low voltage domain. It supplies mixed signal blocks in the AFE and CDB of the Gigabit Ethernet PHY.
AC3, AC4, AC5	**VDDA3V3_2**	PWR		**GPHY2 High Voltage Domain Supply** This is the group of supply pins for the high voltage domain. It supplies the AFE of the Gigabit Ethernet PHY.
U7, W9, AA7	**VDDA0V9_2**	PWR		**GPHY2 Low Voltage Domain Supply** This is the group of supply pins for the low voltage domain. It supplies mixed signal blocks in the AFE and CDB of the Gigabit Ethernet PHY.
AC8, AC10, AC12	**VDDA3V3_3**	PWR		**GPHY3 High Voltage Domain Supply** This is the group of supply pins for the high voltage domain. It supplies the AFE of the Gigabit Ethernet PHY.
U11, W13, AA11	**VDDA0V9_3**	PWR		**GPHY3 Low Voltage Domain Supply** This is the group of supply pins for the low voltage domain. It supplies mixed signal blocks in the AFE and CDB of the Gigabit Ethernet PHY.

Table 12 Power Supply Pins (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
C22, F3, H3, K3, T3, V3, Y3	**VDD3V3_PAD**	PWR		**Power Supply Digital Domain 3.3 V** 3.3 V pad voltage digital power supply
AC20, AC21	**VDDP_PAD**	PWR		**Power Supply** 3.3 V pad voltage digital power supply.
G17, L9, L13, L17, N7, N11, N15, R9, R13, U15, AA15	**VDDD0V9_COR**	PWR		**Power Supply Digital Domain 0.9 V** 0.95 V core voltage digital power supply
C18	**VDDA3V3_XO**	PWR		**Power Supply Digital Domain 3.3 V** 3.3 V XO voltage digital power supply
C16	**VDDA3V3_CDB**	PWR		**Power Supply Digital Domain 3.3 V** 3.3 V CDB voltage digital power supply
E15	**VDDA0V9_CDB**	PWR		**Power Supply Digital Domain 0.9 V** 0.9 V CDB voltage digital power supply
C21	**VDDD3V3_LDO**	PWR		**Power Supply Digital Domain 3.3 V** 3.3 V LDO voltage digital power supply
E19	**VDDA1V8_PLL**	PWR		**Power Supply Digital Domain 1.8 V** 1.8 V LJPLL voltage digital power supply
J15	**VDDD0V9_PLL**	PWR		**Power Supply Digital Domain 0.9 V** 0.9 V LJPLL voltage digital power supply
B21	**VQPS**	PWR		**OTP fusing Supply** Tie to ground

2.2.4.10 Power Supply for SGMIIs and USXGMII

This section specifies the power supply pins for SGMIIs and USXGMII.

Table 13 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
R21, U19, W17, W21, AA19	**SVP0V9**	PWR		**SGMII Port 0, 0.9 V Domain Supply**
M23, T23, Y23, AB23	**SVPH3V3**	PWR		**SGMII Port 0, 3.3 V Domain Supply**
G21, J19, L21	**UVP0V9**	PWR		**USXGMII 0.9 V Analog Domain Supply**
E23, F23	**UVPHA1V8**	PWR		**USXGMII 1.8 V Domain Supply**

2.2.4.11 Power Supply for Twisted Pair Interface (TPI) Analog Front End (AFE)

This section specifies the power supply pins for TPI (AFE).

Table 14 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
A6, A16, B1, B6, C2, C6, C14, D3, E5, E9, E13, G5, G7, G11, G15, J5, J9, J13, U5, U9, U13, W5, W7, W11, AA5, AA9, AA13, AB3, AC2, AC6, AC14, AD1, AD6, AE1, AE6, AE16	**TPVSSA**	GND		**Twisted Pair Ground**

2.2.4.12 Ground

This section specifies the ground pins.

Table 15 Power Supply Pins

Pin No.	Name	Pin Type	Buffer Type	Function
A21, A24, A25, C1, C20, C23, D2, E17, E21, E3, F2, J17, K1, K2, L5, L7, L11, L15, M3, N5, N9, N13, N17, P2, P3, R5, R7, R11, R15, R17, V2, W15, Y1, AA3, AA17, AB2, AC16, AC18, AC22, AD16, AD23, AE23	**VSS**	GND		**General Device Ground** Ground
B25, D23, E24, E25, G19, H23, J21, L19	**UVSS**	GND		**USXGMII Ground**
F25, K23, M25, N19, N21, P23, R19, U17, U21, V23, V25, W19, AA23, AA21, AB25, AC23, AE24, AE25	**SVSS**	GND		**SGMII Ground**
B18, B20	**VSS_XO**	GND		**General Device Ground** XO ground

3 Functional Description

This chapter describes the functional description of the package.

3.1 Power Supply, Clock and Reset

This section provides the information required to power up the GPY241.

3.1.1 Power Supply

The number of power supply levels depends on the SerDes used to communicate with the MAC:

- When SGMII is used to connect to the MAC, two external power supplies of 3.3 V and 0.95 V are required.
- When USXGMII is used to connect to the MAC, in addition to the two external power supplies of 3.3 V and 0.95 V, an additional 1.8 V supply must also be supplied to the USXGMII interface and Low Jitter PLL.

Section 7.9 documents the detailed power supply connection requirements.

3.1.2 Clock

An external 25 MHz crystal must be connected to the GPY241. **Section 7.7.9** documents the required crystal specification. An internal PLL circuit generates all the required internal clocks.

3.1.3 Reset Generation

The external hardware reset input (HRSTN pin) resets all the hardware modules including the pin strapping information during boot:

- Driving the HRSTN pin low causes an asynchronous reset of the GPY241 system.
- Releasing the HRSTN pin high triggers the power-on sequence and boot-up procedure.

The HRSTN pin is internally connected to a weak internal pull-up resistor.

3.1.4 Power-On Sequence

The GPY241 powers on when the power is applied as shown in **Figure 17** and **Figure 18**.

The steps executed at power on are:

- Locking of internal PLL.
- Calibration of internal voltage using a high precision external reference resistor connected to the RCAL pin.
- Reading of pin strap information, as described in **Section 3.1.5**.
- Booting of the microprocessor from internal ROM.
- Auto-negotiation on the Ethernet twisted pair interface and USXGMII/SGMII interface using the speed capability of 2.5 Gbps, full duplex.
- Training and link up in accordance with the IEEE 802.3 **[5]** and SGMII **[8]** standards.

3.1.5 Configuration by Pin Strapping

The GPY241 device is configurable by means of pin strapping on a number of the GPIO pins.The pin strapping configurations are captured during the chip power-on sequence, up until the reset initialization is complete.

The pin strap values are set to logical high or low by connecting the corresponding pin via an external 1 kΩ resistor to either ground or 3.3 V.

Table 16 and **Table 17** describe the pin strap mapping.

Table 16 Pin Names Used for Pin Strapping

Ball Name	Pin Number	Configuration Item Description
GPC1	A23	PS_PHY_MADDR(4)
GPC2	A22	PS_PHY_MADDR(3)
GPC3	B22	PS_PHY_MADDR(2)
PHY_GPIO0	AA1	PS_DATA_IF_MODE
MDINT	AD22	PS_MINT_POL

Table 17 Pin Strapping Configuration Description

Pin Strapping Signals	Description
PS_PHY_MADDR(4:2)	**MDIO PHY Address** This is to specify the most significant 3 bits of the MDIO address. The lowest 2 bits are hard-coded to 0,1,2,3 for each BASE-T port of the GPY241.
PS_MINT_POL	**MDIO Interrupt Polarity** This is to specify the polarity of the MDIO interrupt. For automatic configuration of the MDIO Interrupt polarity, this configuration bit may be connected to the input of the MDIO interrupt pad. 0_B **HIGH** MDIO Interrupt is active high 1_B **LOW** MDIO Interrupt is active low
PS_DATA_IF_MODE	**Data Interface Mode** This is to specify which type of data interface is used. 0_B **USXGMII** USXGMII mode 1_B **SGMII** SGMII mode

An alternative way to configure the GPY241 after the boot process is to use the MDIO interface and write into various control registers, as detailed in **Section 3.2**.

3.2 Configuration via MDIO Management Interface

It is possible to connect the external controller's station manager (STA) to the chip's slave MDIO interface. This allows access to the MDIO and MMD registers standardized in IEEE 802.3, enabling the STA to control the chip configuration and retrieve status information. The MDIO transactions are any of the 3 types described in IEEE 802.3 Clause 22, Clause 22 Extended, and Clause 45 **[5]**. **Chapter 4** lists the MDIO registers.

Figure 4 shows the minimum time required for the MDIO to be available for access.

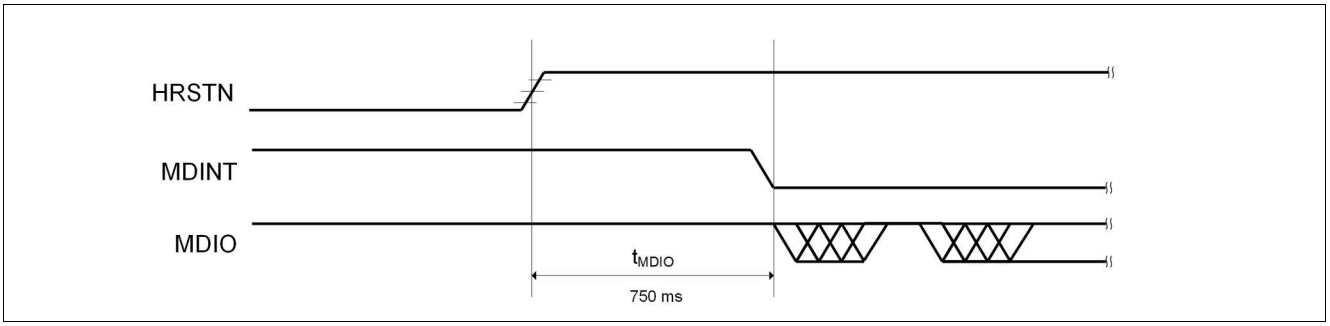


Figure 4 MDIO Access Timing

3.3 Ethernet PHY Interface

The Ethernet PHY implements the physical layer of the Ethernet standard. It supports Digital Signal Processing (DSP) and Analog Signal Processing (ASP) functions in transmitting data over the twisted pair cable.

3.3.1 Twisted Pair Interface

The TPI of the GPY241 is fully compliant with IEEE 802.3. The GPY241 integrates series resistors required to terminate the TPI links with a 100 Ω nominal impedance to facilitate a low-power implementation and to reduce PCB costs. As a consequence, it is possible to connect the TPI pins directly via a transformer to the RJ45 connector. Additional external circuitry is required for common-mode termination and rejection. **Figure 5** shows a schematic of the TPI circuitry that takes these components into account.

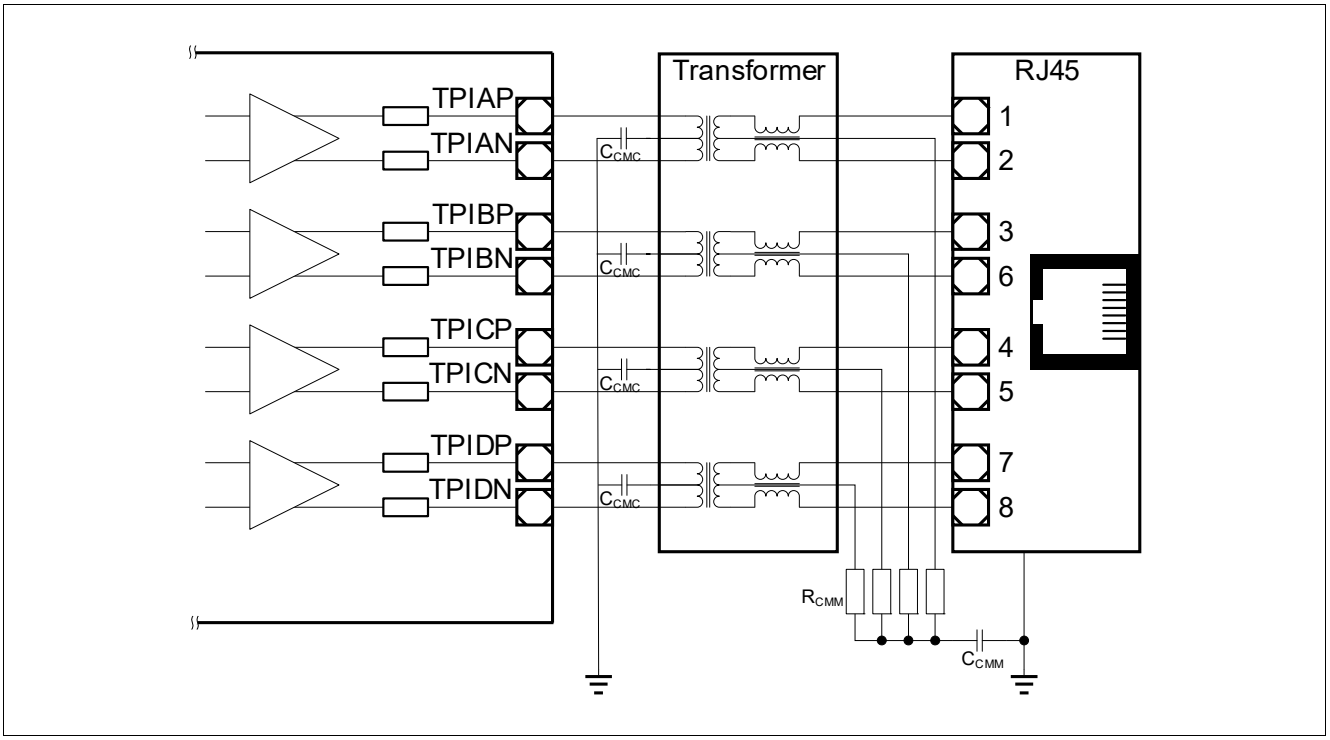


Figure 5 Twisted-Pair Interface of GPY241 Including Transformer and RJ45 Plug

3.3.2 Transformerless Ethernet (TLE)

Transformerless Ethernet (TLE) is required for backplane applications where the use of a transformer is not necessarily required to fulfill the galvanic decoupling requirements of the isolation specifications. In such applications, removing the transformer reduces both the external bill of material and the space requirements on the PCB.

As the GPY241 incorporates a voltage-mode line driver, the only stringent requirement is to use AC coupling. AC coupling is achievable using simple SMD type series capacitors. The value of the capacitors is selected such that the high-pass characteristics correspond to an equivalent standard transformer based application. The recommended value is $C_{coupling}$ = 100 nF. **Figure 6** shows the external circuitry for TLE.

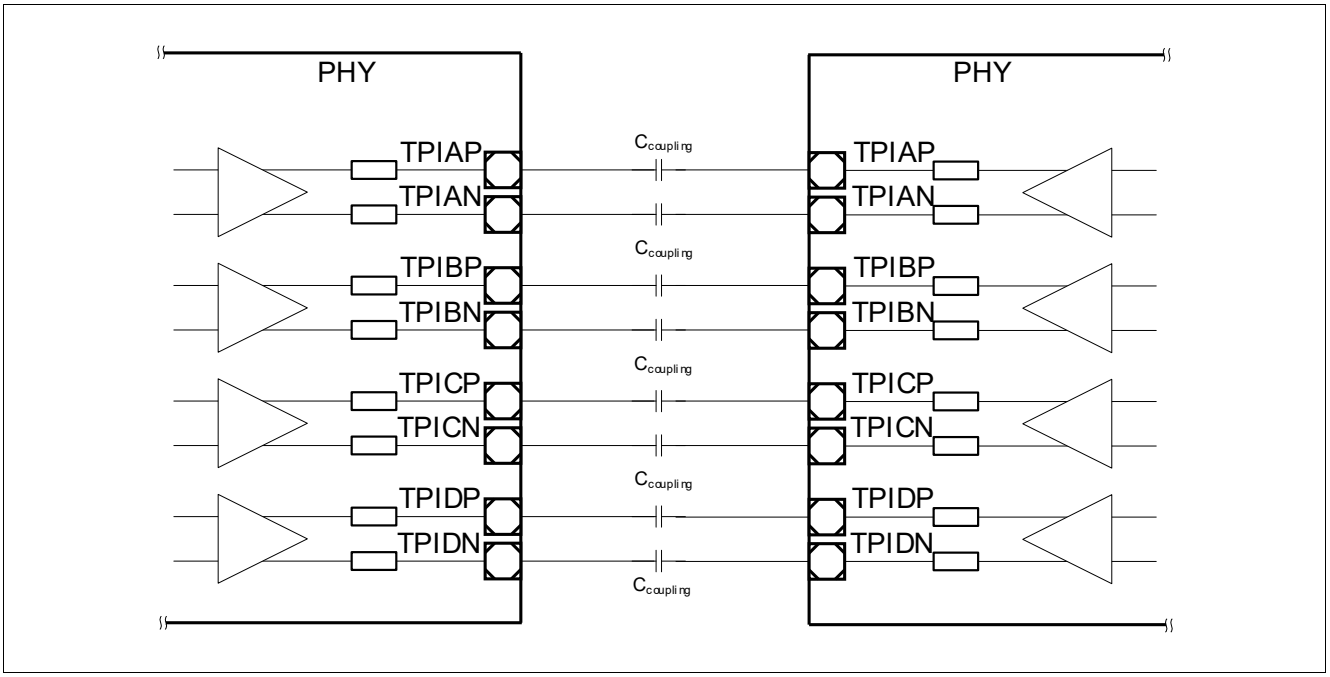


Figure 6 External Circuitry for the Transformerless Ethernet Application

3.3.3 Auto-Negotiation (ANEG)

The GPY241 supports ANEG as part of the startup procedure to exchange capability information with the link partner. ANEG is enabled at GPY241 initialization and its 2.5 Gbps speed capability is advertised.

The ANEG procedure is executed according to IEEE 802.3 Clause 28, Clause 40 **[5]**, and IEEE 802.3bz Clause 126 **[6]**.

When the link partner does not support ANEG, the GPY241 extracts the link speed configuration using parallel detection as described in Clause 28**.**

When required, a STA connected to the MDIO interface is able to reprogram the GPY241 advertised capability. The STA is also able to disable ANEG. In this situation the system configuration must ensure compatibility between link partners to allow link up in a compatible mode.

Attention: STD_CTRL.DPLX only takes effect when the ANEG process is disabled and the GPY TPI is not operating in loopback mode, that is, bits STD_CTRL.ANEN and STD_CTRL.LB are set to zero. Forced half duplex mode (STD_CTRL.DPLX = 0b0) is only supported in 10BASE-T/100BASE-TX speed modes. This field is ignored for higher speeds.

3.3.4 Auto-Downspeed (ADS)

The ADS feature implements a process to decrease the operating speed of the link when the link quality is insufficient. The feature ensures maximum interoperability even in harsh, or inadequate, cable infrastructure environments. In particular, ADS is applied during the 2.5GBASE-T/1000BASE-T training phase. ADS is also necessary when the quality or characteristics of the cable in use cannot support the advertised speed.

For example, it is possible to advertise 2.5GBASE-T/1000BASE-T during ANEG when both link partners are connected via a cable that does not support the 4-pair Gigabit Ethernet mode. The GPY241 detects such configurations to avoid repeating link up failures and clears Gigabit capability in the ANEG advertisement registers. After the resulting link down, the next ANEG procedure no longer advertises 1000BASE-T/2.5GBASE-T. The next link up is done at the next advertised speed below 1000 Mbps.

The GPY241 also executes an ADS procedure when the signal quality is not suited to a 1000BASE-T/2.5GBASE-T link up due to increased alien noise or over long cables.

When the GPY241 is configured to advertise no speed capability below 1000 Mbps, the ADS feature is disabled automatically.

3.3.5 Polarity Reversal Correction

For each of the 4 pairs, the GPY241 automatically detects and corrects any inversion of the signal polarity on the P and N signals. The detection is done during the auto-negotiation phase. The detected polarity is frozen when the link has been established, and remains unchanged until the link is dropped.

The polarity corrections applied are indicated in the register: PMA_MGBT_POLARITY (register 1.130); and are valid when auto-negotiation is complete.

3.3.6 Auto-Crossover Correction

To maximize interoperability, even in inadequate wiring environments, the GPY241 automatically performs cable crossover (MDI-X) correction. **Table 18** lists the supported pair-mappings detectable and correctable by the device.

The purpose is to compensate for any non-standard (ANSI TIA/EIA-568-A:1995) cabling, both straight-through, and crossover cable connections. The GPY241 automatically detects and corrects any crossed cable configuration, where the transmit-receive pairing between partners does not match. The auto-crossover function is fully compliant with IEEE 802.3, Clause 40.4.4 **[5]**, in 1000BASE-T and 2.5GBASE-T mode.

The corrections applied are indicated in the register: PMA_MGBT_POLARITY (register 1.130); and are valid when auto-negotiation is complete.

Table 18 Supported Twisted Pair Mappings on a CAT5 or Better Cable

Crossover Modes on RJ45[1)]		**RJ45 Pinning**							
Mode	**Description**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
11	Straight cable, standard compliant	TPIAP **(A+)**	TPIAN **(A-)**	TPIBP **(B+)**	TPICP **(C+)**	TPICN **(C-)**	TPIBN **(B-)**	TPIDP **(D+)**	TPIDN **(D-)**
00	Full Gigabit Ethernet MDI-X This is the standard compliant MDI-X with pair A/B swapped and pair C/D swapped.	TPIBP **(B+)**	TPIBN **(B-)**	TPIAP **(A+)**	TPIDP **(D+)**	TPIDN **(D-)**	TPIAN **(A-)**	TPICP **(C+)**	TPICN **(C-)**

1) This pin assignment is according to TIA/EIA-568-A/B.

3.3.7 Wake-on-LAN (WoL)

The GPY241 supports wake-on-LAN. The GPY241 generates an interrupt to an external controller when it detects special WoL Ethernet packets. This allows the controller to enter sleep mode when there is no Ethernet traffic to process, and be woken up when traffic starts. WoL packets are detected for all link speeds. **Figure 7** shows this scenario.

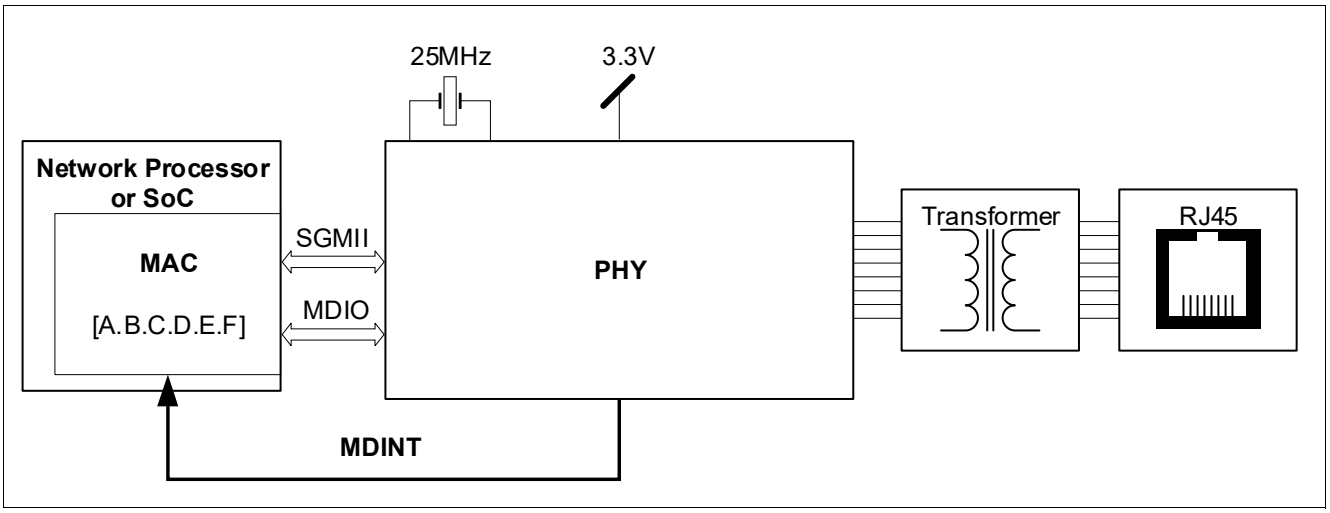


Figure 7 Block Diagram of WoL Application

The most commonly used WoL packet is called a magic packet. A magic packet contains the MAC address of the device to be woken up, and an optional password called SecureON. The MAC address and the optional SecureON password relevant for the WoL logic inside the GPY241 are configurable in the WOL MDIO registers in the Vendor Specific 2, VSPEC2 MMD, device described in **Chapter 4**. When such a configured magic packet is received by the GPY241, an MDINT interrupt is issued.

Table 19 gives an example programming sequence for these configuration registers.

Table 19 Programming Sequence for the Wake-on-LAN Functionality

Step	Register Access	Remark
1	`MDIO.MMD.WOLAD01` = $EEFF_H$	Program the fifth and sixth MAC address bytes
2	`MDIO.MMD.WOLAD23` = $CCDD_H$	Program the third and fourth MAC address bytes
3	`MDIO.MMD.WOLAD45` = $AABB_H$	Program the first and second MAC address bytes
4	`MDIO.MMD.WOLPW01` = 4455_H	Program the fifth and sixth SecureON password bytes
5	`MDIO.MMD.WOLPW23` = 2233_H	Program the third and fourth SecureON password bytes
6	`MDIO.MMD.WOLPW45` = 0011_H	Program the first and second SecureON password bytes
7	`MDIO.PHY.IMASK.WOL` = 1_B	Enable the wake-on-LAN interrupt mask
8	`MDIO.MMD.WOLCTRL.WOL.EN` = 1_B	Enable wake-on-LAN functionality

3.4 SGMII Interface

The GPY241 implements a serial data interface, called SGMII or SerDes, to connect to another chip implementing the MAC layer (MAC SoC). The data rates supported by the SGMII interface are the same as for the TPI (10 Mbps, 100 Mbps, 1 Gbps, or 2.5 Gbps). These rates correspond to baud rates of 1.25 Gbaud (for 10/100/1000 Mbps using data repetition), and 3.125 Gbaud (for 2.5 Gbps).

3.4.1 Selection of Gigabit PHY

There are 4 Gigabit PHYs in the GPY241. For any given transaction, the MDIO interface is only able to access the standard registers of one Gigabit PHY. A dedicated PHY Selector API selects the Gigabit PHY that is accessed via the MDIO interface.

3.4.2 SGMII Control and Status Registers

The GPY241 API **[1]** describing the driver software executed on the MAC SoC must be followed to configure the SGMII interface.

The MAC SoC uses MDIO registers to retrieve the TPI and SGMII status of the selected Gigabit PHY of the GPY241. This is explained in **Section 3.4.1**.

The API controls the SGMII interface using 2 MDIO registers described in **Figure 8**:

- VSPEC1_SGMII_CTRL is used to enable and configure the SGMI auto-negotiation or force a link configuration. Programming this register is optional as the SGMII interface comes up in a default configuration after reset that does not need any additional control from the STA. The STA is also able to control the SGMII reset, SGMII power down or SGMII loopback using this register. Until SGMII is in the power down (VSPEC1_SGMII_CTRL.PD = 1) state, the programming of other bits in the VSPEC1_SGMII_CTRL register is ignored.
- VSPEC1_SGMII_STAT is a read-only register that is used by the STA to retrieve the SGMII link status, data rate and auto-negotiation completion status.

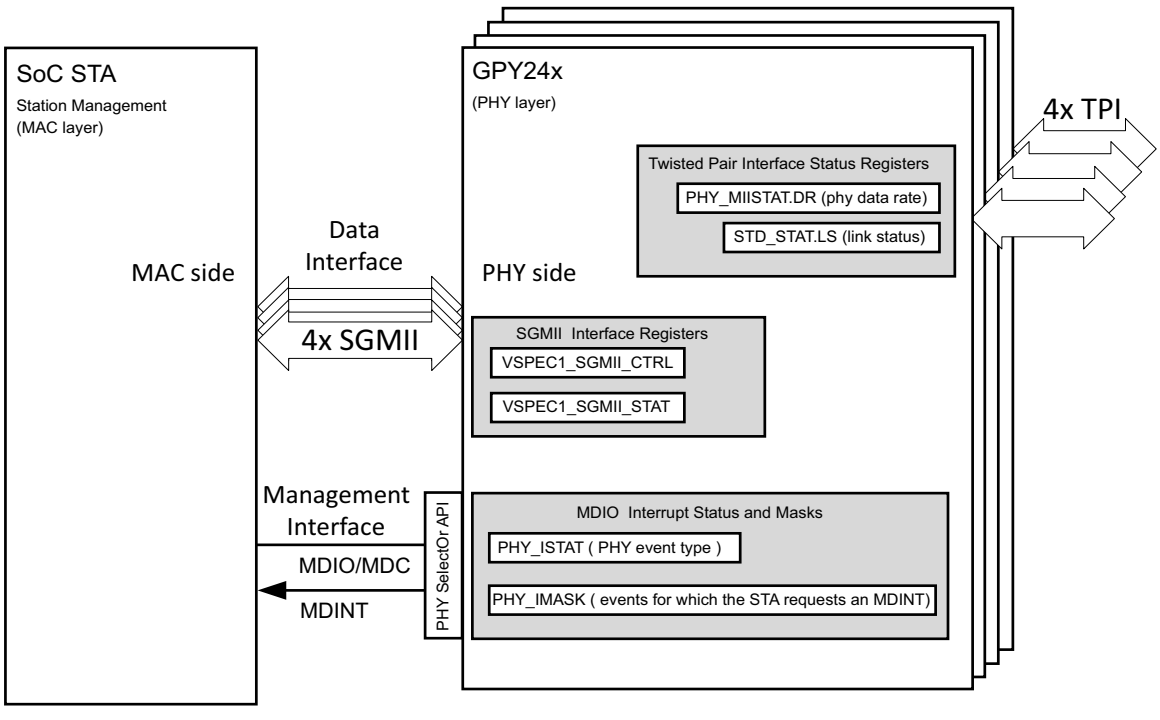


Figure 8 GPY241 SGMII Configuration and Status Registers

3.4.3 Operation Procedure

The SoC is responsible for monitoring the PHY_ISTAT events, TPI data rate, and link status.

- LSTC: PHY link status change with new status indicated in STD_STATS.LS
- LSPC: PHY link speed change with new TPI speed indicated in PHY_MIISTAT.DR

The GPY24x PHY side SGMII is set up by the GPY24x at the same speed as the TPI link. The MAC SoC is responsible for programming the MAC side SGMII at the matching speed.

The PHY_ISTAT event fields in the PHY ISTAT MDIO register:

- LSTC: Link State Change
- LSPC: Link Speed Change
- DXMC: Duplex Mode Change
- MDIXC: MDIX Change, Polarity Change
- ADSC: Auto-Downspeed Event
- TEMP: PVT Sensor Event
- LP: Low Power Event
- LOR: SyncE Loss of Reference
- ANCE: ANEG Complete or ANEG Error
- NPRX: ANEG Next Page RX
- NPTX: ANEG Next Page TX
- MSRE: Master Slave Resolution Error
- WOL: Wake-on-LAN Event

3.4.4 SGMII Configuration at Power Up

The GPY241 SGMII interface is configured to operate automatically after reset. The STA does not have to change the register VSPEC1_SGMII_CTRL to operate in this default mode:

- SGMII auto-negotiation is enabled.
- The TPI configuration after link up defines the SGMII PHY-side configuration. The MAC-side SoC must configure its SGMII MAC-side interface to match the GPY241 PHY-side configuration, as explained in **Section 3.4.5**, **Section 3.4.6**, and **Section 3.4.7**.

3.4.5 SGMII PHY-Side Setup According to TPI Setup

The GPY241 PHY-side SGMII is set up by the GPY241 at the same speed as the twisted pair interface (TPI) link. To operate the GPY241 in this mode, VSPEC1_SGMII_CTRL.FIXED2G5 must be programmed to 0. This is the default mode.

When a link status changes on the TPI (up/down and speed change), the GPY241 reconfigures its SGMII automatically. In particular, the SGMII clock is changed when the speed changes from 2.5 Gbps to lower speeds, or vice-versa.

3.4.6 SGMII PHY-Side Setup Fixed Irrespective of TPI Setup

The GPY241 PHY-side SGMII is fixed to 2.5G mode irrespective of the twisted pair interface (TPI) link. To operate the GPY241 in this mode, VSPEC1_SGMII_CTRL.FIXED2G5 must be programmed to 1 (default value is 0).

When GPY241 operation in this mode is intended, MaxLinear recommends that the GPY241 is switched to this mode by programming VSPEC1_SGMII_CTRL.FIXED2G5 to 1 when the MDIO interface is available after power up. When a link status changes on the TPI (up/down and speed change), the SGMII on the GPY241 operates at 2.5G speed. To alleviate the packet drops due to the rate mismatch on the SGMII and TPI link, the host MAC must enable flow control to detect and react to the PAUSE frames generated by the PHY. An internal buffer path is enabled in this mode, thus introducing latency.

3.4.7 SGMII MAC-Side Setup by MAC SoC

The MAC SoC (STA) is responsible for monitoring the PHY_STAT events, which indicate TPI data rate and link status. The methods available for the MAC SoC to monitor link status or link speed changes are:

- Using the MDIO interface MDINT interrupt and reading the associated event.
- Using the MDIO interface polling (reading) of the link status register STD_STAT.LS.
- Restarting the SGMII ANEG, which conveys the new link parameters. In this case, the SGMII Cisco ANEG must be enabled after power up.

In all three cases:

- The GPY241 reconfigures the PHY-side SGMII to match the TPI setup.
- The MAC SoC must set up the MAC-side SGMII to match the PHY-side SGMII.

3.4.8 SGMII Link Monitoring by MAC SoC

The GPY241 indicates its interface status using using these registers, listed in **Section 3.4.3**:

- MDIO register PHY_MIISTAT indicates the TPI status.
- MDIO register SGMII_STAT indicates the SGMII status.

A change of status on the TPI is indicated by the MDIO interrupt MDINT, which is generated when the STA has programmed the event mask in the PHY_IMASK register. These interrupts correspond to any of these events occurring on the TPI:

- LSTC: Link State Change
- LSPC: Link Speed Change
- DXMC: Duplex Mode Change

- MDIXC: MDIX Change, Polarity Change
- ADSC: Auto-Downspeed Event
- TEMP: PVT Sensor Event
- LP: Low Power Event
- LOR: SyncE Loss of Reference
- ANCE: ANEG Complete or ANEG Error
- NPRX: ANEG Next Page RX
- NPTX: ANEG Next Page TX
- MSRE: Master Slave Resolution Error
- WOL: Wake-on-LAN Event

The MDINT signal is deasserted by the GPY241 when the MAC SoC STA performs a read access to the MDIO register PHY_ISTAT.

The events relevant to the TPI status that are useful for monitoring SGMII are LSTC and LSPC.

3.4.8.1 Actions on TPI Link Down / Link Up Status Change

The GPY241 does not systematically bring the SGMII link down when the TPI link is down. The STA is able to read the status on each side (SGMII and TPI) and make the appropriate decision about whether to bring the SGMII link down. For example, when the TPI status is in link down for too long, the STA may also decide to power down the SGMII.

3.4.8.2 New TPI Link Up at Same Speed

This section contains a scenario which describes a transition on the TPI that does not require any restart or change of mode on the SGMII interface:

- The SGMII interface is set to a specific speed and the SGMII link is up.
- The TPI goes to link down – and link up.
- When the TPI is down, the SGMII side is transmitting Idle packets.
- The TPI links up at the same speed as before.

In these cases, the GPY241 does not reprogram the PHY-side SGMII.

3.4.8.3 Change of Speed After a New Link Up on TPI

This section contains a scenario which describes a transition on the TPI that requires a change of mode on SGMII:

As a PHY-side SGMII controller, the GPY241 enforces the speed on the MAC-side SGMII.

For a change in TPI speed within the [10/100/1000 Mbps] rate subset, there is no change in baud speed on SGMII:

- The new TPI configuration is reflected in the MDIO status registers; the MDINT interrupt is triggered to indicate the change as explained in **Section 3.4.8**.
- The GPY241 programs its SGMII to the new speed. In particular, for speeds of 10 Mbps and 100 Mbps, the GPY241 SGMII PCS performs data repetition by 100x and 10x, respectively.
- The SGMII lane clock remains unchanged at 1.25 Gbaud clock speed.
- When the Cisco ANEG protocol is enabled, the GPY241 conveys the changed speed parameters by restarting the SGMII ANEG.
- When the Cisco ANEG protocol is disabled, the GPY241 changes the SGMII configuration immediately and expects the MAC SoC to monitor the link change and match the same configuration.

For a change in data speed from the SGMII subset [10/100/100 Mbps] to the SGMII* subset [2.5 Gbps], the SGMII lane baud speed must be changed to the over clocked 3.125 Gbaud:

- The new TPI configuration is reflected in the MDIO status registers; the MDINT interrupt is triggered to indicate the change as explained in **Section 3.4.8**.
- The GPY241 reprograms its SGMII to the 3.125 Gbaud clock speed.

- When the Cisco ANEG protocol is enabled, the GPY241 conveys the changed speed parameters by restarting the SGMII ANEG.
- When the Cisco ANEG protocol is disabled, the GPY241 changes the SGMII configuration immediately and expects the MAC SoC to monitor the link change and match the same configuration.
- The MAC SoC reconfigures its MAC-side SGMII to the new baud rate.

3.4.9 Auto-Negotiation Modes Supported by SGMII

Two modes are supported for the SGMII auto-negotiation protocol:

- Cisco Serial-GMII Specification 1.8 **[8]**
- 1000BX IEEE 802.3 following IEEE Clause 37 **[5]**

The information exchange mechanism of ANEG is the same in both modes, but the parameters communicated are slightly different. The 1000BX scheme allows for some parameters to be aligned with the highest common capability between the two sides of the SerDes. The Cisco SGMII scheme uses the protocol to communicate the configuration requested by the PHY-side SGMII to the MAC-side SGMII, such as a speed request, it is a one-way request.

The parameters communicated by the Cisco ANEG protocol **[8]** from SGMII-PHY to SGMII-MAC are:

- Link up or link down indication (reflects the TPI status)
- Half duplex or full duplex mode
- Data rate (standard only supports 10 Mbps to 1000 Mbps)
- EEE capability support
- EEE clock stop capability support

The parameters exchanged by the 1000BX ANEG protocol **[5]** are:

- Remote fault
- Pause support and mode (symmetrical or asymmetrical)
- Half duplex or full duplex

MaxLinear recommends implementing the Cisco ANEG protocol for standard applications.

3.4.9.1 Enabling SGMII Auto-Negotiation Mode

SGMII auto-negotiation is ON at power up. Disable or enable ANEG by setting the register field:

VSPEC1_SGMII_CTRL.ANEN.

In the default case:

- The GPY241 PHY-side SGMII is configured by the GPY241 to match the TPI link configuration.
- The GPY241 uses ANEG to convey the new link parameters to the MAC SoC.
- The SoC MAC-side SGMII must be configured by the MAC SoC to match the GPY241 PHY-side SGMII configuration.

3.5 USXGMII Interface

The GPY241 implements an alternate serial data interface, called USXGMII, to connect to another chip implementing the MAC layer (MAC SoC). The SerDes is connected externally to a MAC SoC via a single SerDes lane in USXGMII. The interface supports the PCH preamble usage to transport control or timestamp indications between the MAC SoC and the PHY. **Table 20** lists the data rates supported by the USXGMII interface.

Upon change of speed request from one of the Gigabit PHYs, the GPY241 initiates USXGMII auto-negotiation and new link up.

Speed Features

USXGMII with clause 37 auto-negotiation is supported for these modes:

- Speed and duplex modes are auto-determined without software involvement
- 2.5 Gbps, 10.3125 GT/s, XGMII mode
- 1 Gbps, 10.3125 GT/s, GMII mode
- 100 Mbps, 10.3125 GT/s, GMII/MII mode (GMII mode or MII mode are statically configurable)
- 10 Mbps, 10.3125 GT/s, GMII/MII mode (GMII mode or MII mode are statically configurable)

Table 20 XPCS Feature List

Modes	Baudrate	Coding	Link speed	XPCS Clause	Auto-Negotiation Clause
10G-USXGMII-4P	10.3125 GT/s	64b/66b	2.5 Gbps, 1 Gbps, 100 Mbps, and 10 Mbps	49.0	37.0

3.5.1 USXGMII Configuration at Power Up

The GPY241 USXGMII interface is configured to operate automatically after reset. The STA does not have to change the register VSPEC1_SGMII_CTRL.USXGMII_REACH to operate in this default mode:

- USXGMII auto-negotiation is enabled by default.
- The TPI configuration after link up defines the corresponding USXGMII PHY-side port configuration. The MAC-side SoC must configure its USXGMII MAC-side interface to match the GPY241 PHY-side configuration.
- The GPY241 API **[1]** describes the procedure to update the Rx / Tx equalization parameters. The GPY automatically updates the Rx / Tx equalization parameters for standard trace lengths based on the trace length programmed in VSPEC1_SGMII_CTRL.USXGMII_REACH. For custom trace lengths, the Rx / Tx equalization parameters are configured using the API.

3.6 LED Interface

This section describes the LED interface.

3.6.1 LED

The GPY241 allows 12 LEDs to be used for visual status indication. Each LED pin drives either a single color LED or dual color LED.

3.6.2 LED Configuration

The GPY241 API **[1]** describing the driver software executed on the MAC SoC must be followed to configure this interface.

Figure 9 shows the external LED connected to either ground or the power rail in single color mode.

The Power Mode is only supported for single color LEDs.

Figure 10 and **Figure 11** illustrate the connection of single and dual color LEDs when the pin is also used for pin strapping.

*Note: These figures do not show the full recommended circuits with all the necessary components. Refer to the relevant HDK/EVK PCB design documentation for more details **[3]**.*

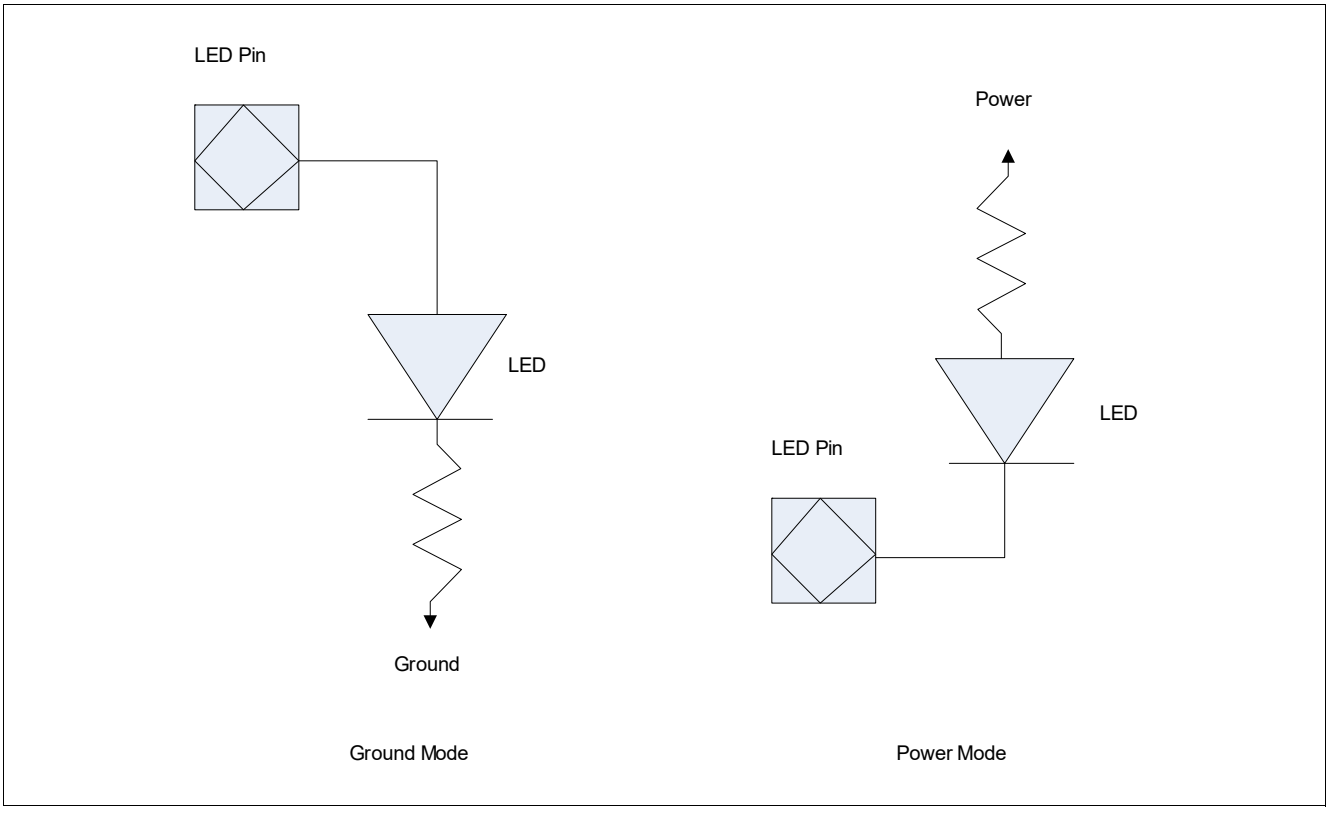


Figure 9 LED Connection Options to Ground or Power Supply

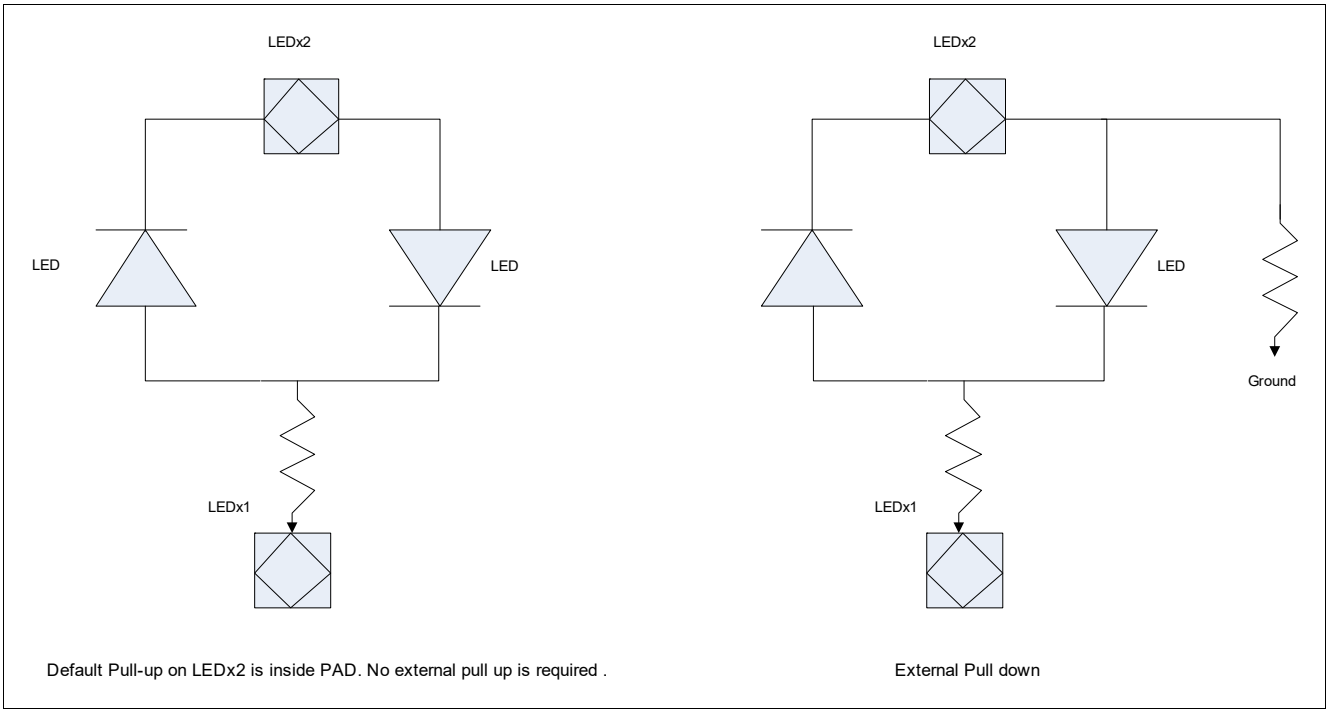


Figure 10 Connection of a Dual Color LED and Configuring Pin Strap Value

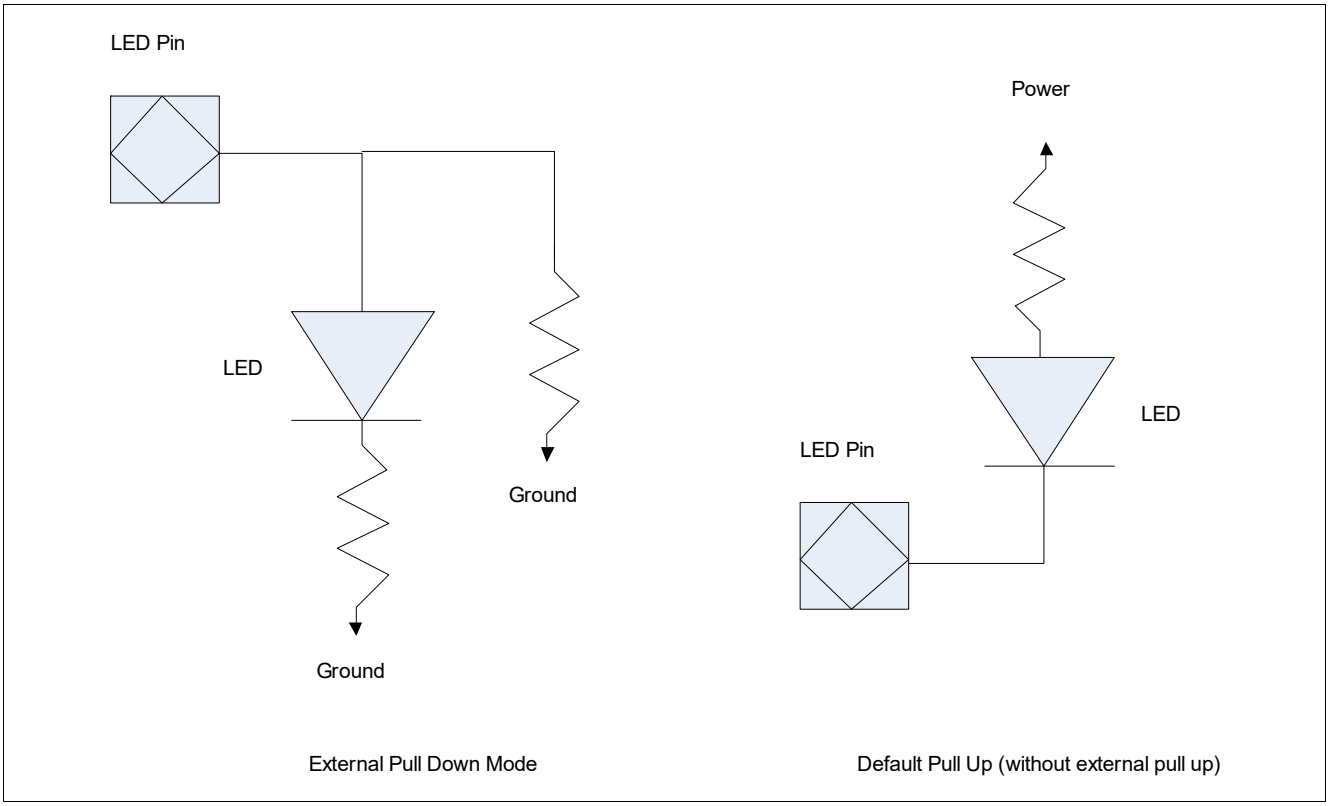


Figure 11 Connection of a Single Color LED and Configuring Pin Strap Value

3.6.3 LED Brightness Control

There are two LED brightness modes configurable by the GPY API, based on the system requirement.

- LED Brightness Level Maximum Mode
  Fixed level signal (no pulses) for maximum brightness, which is also available as a control signal for other purposes.
- LED Brightness Level Control Mode (Constant Mode)
  Allows the configuration of 16 levels of LED brightness as described in **Brightness Control**.

Brightness Control

This block controls the brightness of the LED by controlling the time duration for which the LED is on/off. The persistence characteristic of the eye causes it to perceive this as LED brightness. When LED is off, the output is disabled. When the LED is on, the output is enabled. The brightness control affects the LED output enable directly.

Figure 12 shows the brightness control frequency is 81.25 Hz, where each period is divided into 64 slots.

When the LED brightness control is disabled, the LED is enabled in all 64 slots.

When the LED brightness control is enabled, the LED is enabled for n consecutive slots, where n is determined by the configured brightness level. The LED output is disabled in the 64th slot.

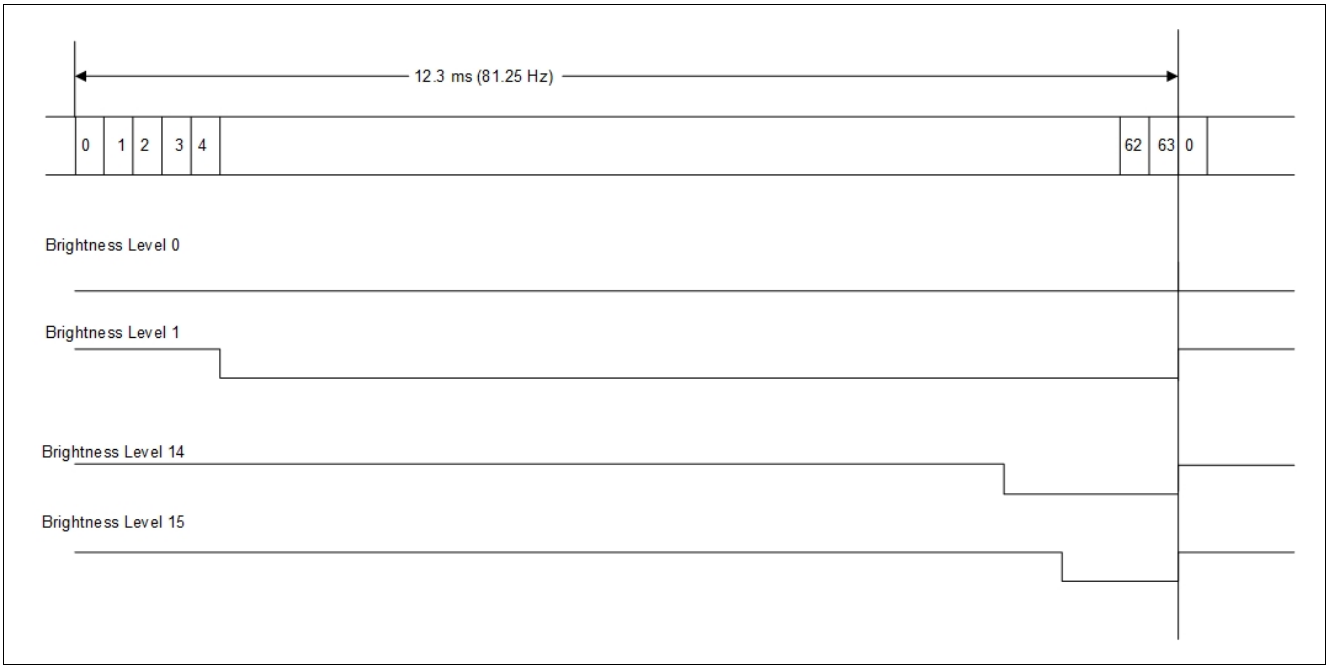


Figure 12 LED Brightness Control by Controlling LED Output Enable/Disable

3.7 Precision Time Protocol Feature

This section introduces the Precision Time Protocol (PTP) feature.

3.7.1 PTP Feature Purpose

The GPY241 provides support for the Precision Time Protocol, defined by the PTP Protocol IEEE 1588 Version 2, IEEE 802.1as, and IEEE P802.3bf, which is used to precisely synchronize clocks at the system level. The station manager (STA) selects GPC1, GPC2, or GPC3 alternate functions to input a time stamp synchronization request signal (TsSync). For each edge transition of the TsSync signal, the GPY241 captures a time stamp. Alternatively, for more precision, the GPY241 supports hardware assisted physical layer time stamping. In this case, the TsSync is triggered by the physical layer.

The time stamp is inserted in a PTP event message. The PTP protocol is executed by the STA at the OSI layer above the UDP/ IP or MAC layer. The PTP protocol chooses 1-step or 2-step time stamping; both are supported by the GPY241:

- **2-step time stamping**
  This scheme uses a Follow_Up message to carry the time stamp of the corresponding sync message. The time stamp is not inserted in the sync message on the fly while the packet is being transmitted, but later in the next PTP message. This scheme allows the GPY241 to perform hardware-assisted precise time stamping capture, using the PHY layer to precisely indicate when the packet Start-of-Frame Delimiter (SFD) symbol is sent out or received on the physical layer. The time stamp, together with the corresponding packet CRC, is stored in a memory area on the GPY241. The STA reads this time stamp using the MDIO interface.
- **1-step time stamping**
  This scheme is used to reduce the number of PTP messages. In this scheme, the GPY241 MAC inserts the time stamp in the sync message on the fly when it passes through the GPY MAC layer. The GPY241 inserts the time stamp in the PTP sync message on the fly.

3.7.2 PTP Feature Configuration

The GPY241 API **[1]** describing the driver software executed on the MAC SoC must be followed to configure this feature.

The steps used by the API to configure and enable the 1588 feature are:

1. (Optional) The STA uses the GPIO configuration API to select GPC1, GPC2, or GPC3 to be used to input the TsSync. This is not required when 2-step PTP mode is chosen, because the TsSync is generated internally by the GPY241 physical layer in that case.
2. The STA selects 1-step or 2-step PTP mode in the MDIO VSPEC1_PM_CTRL register.
3. The STA enables the 1588 feature in the MDIO VSPEC1_PM_CTRL register. This triggers the GPY241 firmware to configure the internal GMAC and Packet Manager to capture the time stamps of the PTP packets.

In the case of 2-step PTP mode, the STA MAC SoC retrieves the time stamp and CRC to associate it to the PTP follow-up message.

3.8 Pulse Per Second Feature

This section introduces the Pulse Per Second (PPS) feature.

3.8.1 PPS Feature Purpose

The GPY241 provides support for PPS signal generation, which is used at the system level to synchronize various chips. The general purpose clock pins GPC1, GPC2, or GPC3 are configured for this purpose.

3.8.2 PPS Feature Configuration

The GPY241 API **[1]** describing the driver software executed on the MAC SoC must be followed to configure this feature.

The steps used by the API to configure and enable the PPS feature are:

1. (Optional) The STA uses the configuration API to configure the desired PPS frequency; the default is 1 second.
2. The STA enables the PPS feature. This triggers the GPY241 firmware to configure the GPY241 MAC and Packet Manager to output a PPS signal on the selected GPC1, GPC2, or GPC3.

3.9 Smart-AZ Feature

The Smart-AZ feature is relevant when the GPY241 is connected to a MAC SoC that does not implement the EEE feature in its MAC layer. In this case, the MAC SoC is not able to initiate a transition to the low-power idle state.

To alleviate the limitation of such a MAC SoC, the GPY241 detects the conditions that may lead to low-power idle and generates the control messages to enter EEE mode in accordance with the IEEE 802.3az standard.

The Smart-AZ feature is always enabled.

3.10 Power Management

This section describes the power management functions of the GPY241.

3.10.1 Power States

Figure 13 illustrates the power states and transitions of the GPY241. In this state diagram, the (0.11) syntax corresponds to the value of bit 11 from register 0 in device 0, which is STD_CTRL.PD. This is the Power Down (PD) bit in MDIO STD_CTRL described in **Chapter 4**. The STA is able to use this STD_CTRL.PD field to bring the physical interface into the POWER DOWN state.

The other states are automatically entered by the GPY241 depending on the context, and following the Energy Efficient Ethernet protocol. This is done without need for any intervention from the STA.

The Normal Link Pulse (NLP) and Fast Link Pulse (FLP) are received on the twisted pair interface from a link partner and used to wake up the GPY241 and enter auto-negotiation.

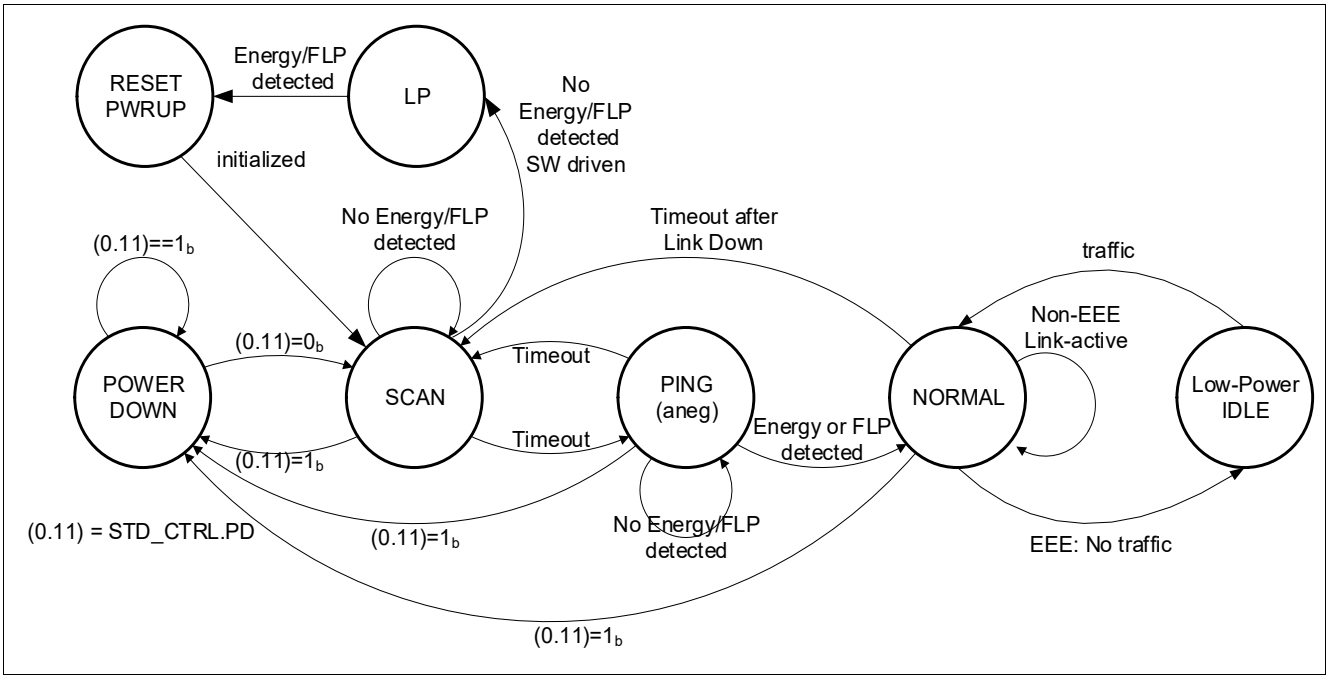


Figure 13 State Diagram for Power Down State Management

3.10.2 RESET Power Up

The GPY241 starts up in the RESET Power Up (PWRUP) state after either a hardware reset or power up.

After initialization, the GPY241 always transitions to the SCAN state.

3.10.3 POWER DOWN State

The POWER DOWN state is entered by setting the PD bit (0.11) of the MDIO standard register STD_CTRL to 1, regardless of the current state of the device. The POWER DOWN state corresponds to power down as specified in IEEE 802.3, Clause 22.2.4.1.5. Some signal processing blocks are stopped to save energy, but the GPY241 still responds to MDIO messages. The SGMII interface to the MAC SoC is also switched off.

Exiting the POWER DOWN state is triggered by setting the PD bit (0.11) of STD_CTRL to '0', which initiates a transition to the SCAN state.

3.10.4 SCAN State

The SCAN state differs from the POWER DOWN state in that the receiver periodically scans for signal energy or FLP bursts on the twisted pair interface. There is no transmission in this state. When an FLP burst is received, the GPY241 enters the auto-negotiation protocol to exchange capabilities with the link partner and establish a data link in the NORMAL state.

3.10.5 PING State

The PING state is similar to the SCAN state except that the transceiver transmits an FLP burst onto the TPI for a programmable amount of time. This is used to wake potential link partners from the power down state. This state corresponds to the state of ANEG described in Clause 28 of the IEEE standard **[5]**.

3.10.6 LP State

The GPY241's low power (LP) state is enabled by configuring the MDIO register PHY_CTL2.LP. This LP state is not applicable to the master port (default port 0), regardless of the setting of this bit. The LP state is entered automatically when there is no Ethernet cable connected to the GPY241. The GPY241 firmware detects this condition when no energy or LP is present on the twisted pair interface and enters the LP state. It is intended to set the GPY241 into its maximum power saving state. In this state, most digital domains are in reset. Only a minimal amount of circuitry (analog/digital) operates in order to detect signal energy on the receiver of one twisted pair interface and trigger a wake-up.

When the port is in the LP state, the STAs do not have access to the corresponding MDIO/MMD registers.

The LP state is exited upon detection of signal energy on the twisted pair (either NLP or FLP). The port transitions to the RESET Power Up state automatically. The STA host is also able to trigger an LP state exit by applying an API to wake up the specific port that has entered the low power state.

The STA host may be informed of the LP entry condition. By setting the PHY_IMASK.LP bit to ACTIVE, the STA requests the MDINT interrupt from the port when the entry conditions are met. All the LP related control bits and communication mechanism between the STA and the GPY are shown in the flowchart in **Figure 14**.

The STA host may be informed of the LP exit condition. By setting the VSPEC1_IMASK.CDET bit to ACTIVE, the STA requests the MDINT interrupt from the port (including master port) when energy on the link is detected during auto-negotiation. Although the LP state is not applicable to the master port, this bit is applicable to the master port. So even if no port is in the LP state, it can trigger this interrupt whenever energy is first detected on the link. If the STA triggers the LP state exit via a wake-up request, and there is no energy on the link after the LP state exit, no interrupt will be asserted.

Attention: An active-high MDINT in push-pull mode (default is tristate mode) is not supported in Low Power mode.

Attention: VSPEC1_IMASK.CDET is not supported in forced speed 10BASE-T/100BASE-TX mode. Auto-negotiation is needed to support this feature.

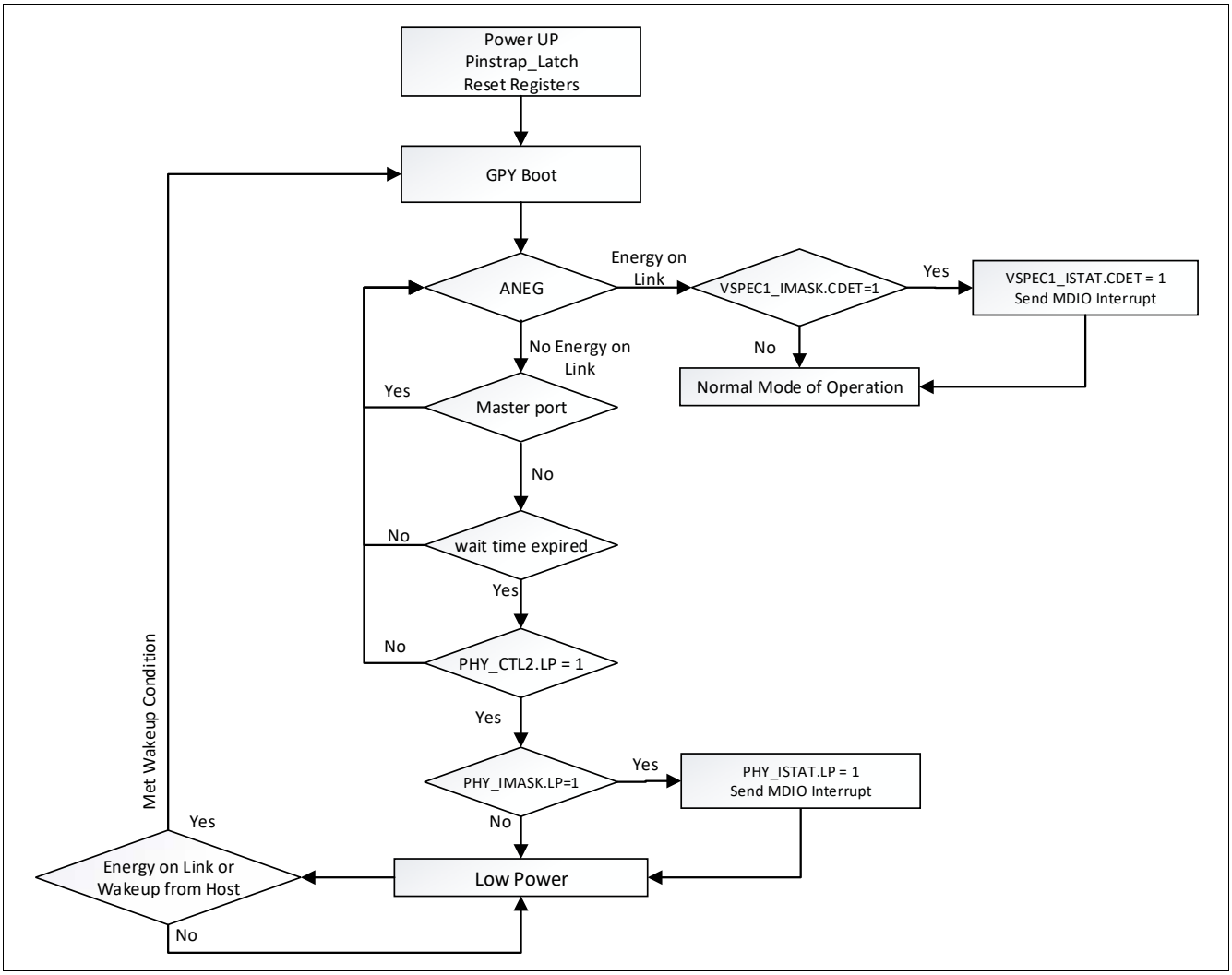


Figure 14 LP Sequence

Table 21 LP State Entry and Exit Sequence

Step	State	Remark
1	ACTIVE The LP feature is enabled by setting PHY_CTL2.LP = 1	Use MDIO register PHY_CTL2.LP to enable or disable the LP feature.
2	ANEG, Ability Detect	The firmware detects that no energy is seen on the cable when no FLP is received for a long period of time. If the Low Power feature is not enabled, this time is fixed to between 6.4 seconds and 9.6 seconds. If the Low Power feature is enabled, this time is configured using the register: VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM. Time in seconds = 4 x value programmed. Default time is 4 seconds (VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM = 1). There is an initial time of between 2.4 seconds and 5.6 seconds, which adds on to the programmed time.
3	LP Entry Timer	This time is configured with register: VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM. The value is set in steps of 4 seconds. Default time is 4 seconds.
4	LP Entry	The GPY241 saves MDIO LP persistent registers. An interrupt is sent to indicate entry into the LP state.
5	LP State	Power consumption is saved in this state. The GPY241 listen to energy pulses from the link partner ANEG as a condition to trigger an exit from the LP state. Only a minimal amount of circuitry operates in order to detect signal energy on TPI and trigger a wake-up. The port LEDs and MDIO interface are disabled.
6	LP Exit (Option 1) Based on energy detected on the cable.	The GPY241 restores the MDIO LP persistent registers. The STA is responsible for restoring any custom MDIO information that was not saved in the group of LP persistent registers. An interrupt is sent to indicate an exit from the LP state.
7	LP Exit (Option 2) Based on a wake-up request from the STA.	The STA is able to request an LP exit by using an API which will be provided. GPY241 restores the MDIO LP persistent registers.The STA is responsible to restore any custom MDIO information that were not saved in the group of LP persistent registers. No interrupt is sent to notify LP exit.
8	ANEG, LINK-UP and ACTIVE	The GPY241 operates in normal power modes.

These are persistent MDIO registers saved and restored during LP entry-exit.

1. STD_CTRL.SSM
2. STD_CTRL.DPLX
3. STD_CTRL.ANEN
4. STD_CTRL.SSL
5. STD_AN_ADV.TAF
6. STD_AN_ADV.XNP
7. STD_GCTRL.MBTHD
8. STD_GCTRL.MBTFD
9. STD_GCTRL.MS
10. STD_GCTRL.MSEN
11. PHY_IMASK
12. PHY_CTL1.AMDIX
13. PHY_CTL1.MDIAB
14. PHY_CTL1.MDICD
15. PHY_CTL1.POLA
16. PHY_CTL1.POLB
17. PHY_CTL1.POLC
18. PHY_CTL1.POLD
19. ANEG_CTRL.ANEG_ENAB
20. ANEG_MGBT_AN_CTRL.LDL
21. ANEG_MGBT_AN_CTRL.FR
22. ANEG_MGBT_AN_CTRL.FR2G5BT
23. ANEG_MGBT_AN_CTRL.AB2G5BT
24. ANEG_MGBT_AN_CTRL.PT
25. ANEG_MGBT_AN_CTRL.MS_MAN_EN
26. ANEG_MGBT_AN_CTRL.MSCV
27. ANEG_EEE_AN_ADV1.EEE_100BTX
28. ANEG_EEE_AN_ADV1.EEE_1000BT
29. ANEG_EEE_AN_ADV2.EEE2G5
30. VSPEC1_SGMII_CTRL.ANMODE
31. VSPEC1_SGMII_CTRL.SSM
32. VSPEC1_SGMII_CTRL.EEE_CAP
33. VSPEC1_SGMII_CTRL.DPLX
34. VSPEC1_SGMII_CTRL.RXINV
35. VSPEC1_SGMII_CTRL.ANEN
36. VSPEC1_SGMII_CTRL.SSL
37. VSPEC1_NBT_DS_CTRL.NO_NRG_RST
38. VSPEC1_NBT_DS_CTRL.DOWNSHIFTEN
39. VSPEC1_NBT_DS_CTRL.DOWNSHIFT_THR
40. VSPEC1_NBT_DS_CTRL.NRG_RST_CNT
41. VSPEC1_NBT_DS_CTRL.FORCE_RST
42. VSPEC1_LED0
43. VSPEC1_LED1
44. VSPEC1_LED2
45. VSPEC1_PM_CTRL.PM_EN
46. VSPEC1_PM_CTRL.PTP_1588_EN
47. VSPEC1_PM_CTRL.PTP_1588_STEP
48. VSPEC1_PM_CTRL.SYNCE_EN
49. VSPEC1_PM_CTRL.SYNCE_CLK
50. VSPEC1_SGMII_CTRL.USXGMII_REACH

51. VSPEC1_SGMII_CTRL.SGMII_FIXED2G5
52. VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM
53. VSPEC1_PM_CTRL.MDIO_MODE
54. VSPEC1_IMASK.CDET

3.10.7 NORMAL State

The NORMAL state is used to establish and maintain a link connection. When a connection is dropped, the GPY241 moves back into the SCAN state.

3.10.8 Low Power IDLE State: Energy-Efficient Ethernet

The IEEE 802.3 standard **[5]** describes the Energy-Efficient Ethernet (EEE) operation that is supported by the GPY241. EEE is supported in the various speeds of 100BASE-TX, 1000BASE-T, and 2.5GBASE-T. The general idea of EEE is to save power during periods of low link utilization. Instead of sending active idle data, the transmitters are switched off for a short period of time. This is called the quiet period in the standard. The link is kept active by means of a frequent refresh cycle initiated by the PHY itself while in the low power state. This sequence is repeated until a wake request is generated by one of the link partner MACs. The GPY241 follows the IEEE 802.3 standard regarding EEE. **Figure 15** illustrates the principle. This state is entered automatically when the low power idle conditions are met.

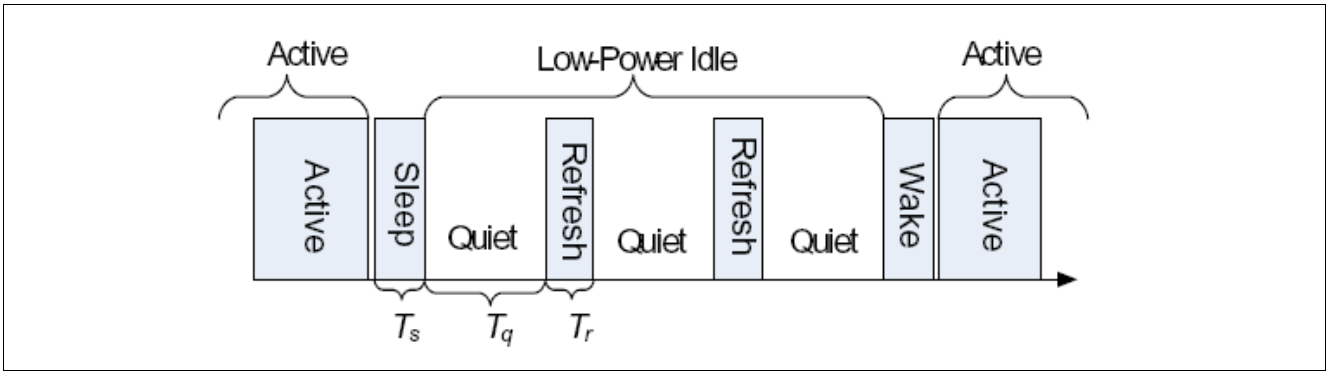


Figure 15 EEE Low Power Idle Sequence

3.11 Firmware Upgrade

The GPY241 provides a firmware upgrade feature that allows feature and functional enhancements of the GPY241 in the field.

The GPY241 is initially provided with a permanent on-chip firmware image in a one-time programmable memory (OTP). It is possible to download a new firmware image via the GPY241 to a low-cost serial flash memory device connected to the GPY241's SPI interface; the GPY241 is then able to fetch the upgraded firmware from the flash memory after a reboot.

For security reasons, the GPY241 only accepts firmware images that are electronically signed by MaxLinear. When authentication of the flash image by the GPY241 fails, or the download of the image is aborted or fails, the GPY241 defaults to running from the internal firmware image in OTP.

The GPY API **[1]** describing the driver software executed on the MAC SoC must be followed to execute this feature. It provides information on the update process and which actions are required in the MAC SoC application.

Security features to prevent rollback of the image to a previous version (flash anti-rollback) and to prevent flash memory wear-out due to frequent updates (flash anti-wear out) are not supported within the GPY241. When the system (SoC) to which the GPY241 is attached mandates such features, they must be supported by the system itself.

- The host software is expected to verify that the new firmware is a higher version than the previously installed firmware before downloading it to the flash memory.
- The system is also expected to ensure that firmware is only installed when there is new firmware available and not attempt to install new firmware after every reboot.
- Flash memory components typically support a minimum of 100,000 erase/program cycles, so flash wear-out is unlikely. However, ensuring a minimum interval between flash updates decreases the likelihood of wear-out. An interval of 1 hour sets the minimum time before wear-out to longer than 11 years.

4 MDIO and MMD Register Interface Description

This chapter describes the MDIO and MMD registers, which are standardized by IEEE 802.3 [5] and [6], and available to support the GPY241 feature set. These registers are accessible by an external management entity (also called STA in IEEE) to control, configure or read the status of the GPY241. After power-on, the GPY241 resets the MDIO and MMD registers to default values that are sufficient to operate without specific programing.

All the register definitions, behaviors and fields are strictly compliant with the IEEE 802.3 [5] and [6]. Refer to IEEE 802.3 for more detailed explanations of the registers. The only registers that are not referenced in IEEE 802.3 are two register groups that are vendor specific, VSPEC1 and VSPEC2. These allow custom functions related to the GPY241. In the register descriptions, the section or table references refer to the IEEE 802.3 [5] and [6] documents.

4.1 MDIO-Specific Terminology

This list describes how these common IEEE802.3 terms relate to MDIO and MMD register concepts discussed in this chapter.

- **STA**: Station Management. A host connected to the MDIO interface. STAs are generally Media Access Controllers (MACs). The STA drives the MDIO bus as a clock master and the GPY241 is MDIO slave.
- **PHY**: Physical Layer. In the GPY241 this encompasses Analog Signal Processing, Digital Signal Processing, PCS. The PHY contains several sub-layers that are individually manageable entities known as MDIO manageable devices (MMDs).
- **MMD**: MDIO Manageable Device. Section 4.3 lists the MMDs available in the GPY241.
- **Device**: In the context of MDIO/MMD registers, a device is a register bank grouped by logical sub-layers of the PHY layer.
- **Clause**: Refers to a particular section of the IEEE 802.3 standard [5] and [6]. In particular Clause 22 describes MDIO device 0, and Clause 45 describes the other MMDs.
- **MII**: Media Independent Interface. This encompasses the MDIO and the GMII as described in Clause 22. STD registers in device 0 are also called MII registers.

4.2 Register Naming and Numbering

The register numbering convention in this document is similar to that of IEEE 802.3:

The numbering syntax uses 3 numbers, a.b.c, as specified in IEEE 802.3 paragraph 45.1 **[5]**, and the notation is generalized to Clause 22 registers in device 0 “STD”. The alphanumeric syntax also uses the same structure and uses the names of the MMD devices, registers and register fields separated by underscore and dot as described below.

4.2.1 Register Numbering

The syntax is as follows, with a, b, c written as decimal numbers:

a.b.c = <DEVICE_NUMBER>.<REGISTER_NUMBER>.<FIELD_NUMBER>

When the last indicator (c) is omitted, the register numbering refers to the full register.

When a field is more than a single bit, the bit range is indicated using a semicolon (e.g. 1:3 is the field of bits 1 to 3). In an MDIO register, the least significant bit is bit 0 and most significant bit is bit 15. All MDIO registers are 16 bit wide.

4.2.2 Register Naming

The syntax is as follows, with AA, BB, CC written as alphanumeric strings:

AA.BB.CC = <DEVICE_NAME>_<REGISTER_NAME>.<FIELD_NAME>

When the last indicator (CC) is omitted, the register naming refers to the full register.

The fields named Res, RES1, RES2 refer to reserved fields as per IEEE 802.3 documents.

4.2.3 Examples

STD_STAT.ANOK is the name of the field 0.1.5, which indicates that auto-negotiation is complete.

ANEG_CTRL.ANEG_RESTART is the name of the field 7.0.9, which allows the STA to restart the Ethernet ANEG procedure.

ANEG_PHYID1 is the complete 16-bit register number 7.2, for the PHY identifier 1 number.

VSPEC1_LED1.BLINKS is the 4-bit wide field number 30.2.15:12, which contains LED1 slow blinking configuration.

4.3 MMD Devices Present in GPY241

The MMD devices implement groups of standardized registers under the management of the STA. They are defined in IEEE 802.3.

Table 22 MDIO / MMD Devices Present in GPY241

MDIO / MMD Name	Device Number (decimal)	Description
STD	0	MDIO Standard Device as described in Clause 22. This also contains a number of PHY registers that are GPY241 specific.
PMAPMD	1	Control and status registers related to the PMA/PMD signal processing modules.
PCS	3	Control and status registers related to the PCS encoding/decoding device.
ANEG	7	Control and status registers related to the auto-negotiation device.
VSPEC1	30	GPY241-specific LED control and GPY241 SGMII control.
VSPEC2	31	GPY241-specific wake-on-LAN control.

4.4 Responsibilities of the STA

The GPY241 responds to all published register addresses for the device and returns a value of zero for undefined and unsupported registers.

In accordance with IEEE 802.3 guidelines, it is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs of the GPY241.

The GPY241 ignores writes to the PMA/PMD speed selection bits that select speeds which are not advertised in the PMA/PMD speed ability register. The PMA/PMD speed selection defaults to a supported ability.

4.5 MDIO Access Protocols to Read / Write Registers

All the MDIO/MMD registers are accessible from an external chip connected to the MDIO bus on the MDIO and MDC pins. The GPY241 supports several MDIO frame protocols:

- Clause 22: To access Device 0
- Clause 22 Extended: To access other devices (Dev 1: PMAPMD, Dev 3: PCS, Dev7: ANEG, Dev 30: VSPEC1, DEV 31: VSPEC2) using the indirection scheme specified by IEEE 802.3.
- Clause 45: to access all devices

Both Clause 22 Extended and Clause 45 are used to access MMD devices. However, the mechanism implemented in the GPY241 provides faster speeds using Clause 45, so there are some differences in latencies in the MDIO reply:

- The Clause 22 Extended protocol involves the GPY241 an indirection mechanism.
- The Clause 45 protocol provides faster replies.

The Clause 22 registers are accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. Refer to IEEE 802.3 section 45 **[5]**.

5 MDIO Registers Detailed Description

Table 23 Register Access Type

Mode	Symbol
Status Register (Status or Ability Register)	RO
Read-Write Register (MDIO Register)	RW
Read-Write Self-Clearing Register (bit is cleared after read from MDIO)	RWSC
Read-Only Self-Clearing Register (bit is cleared after read from MDIO)	ROSC

5.1 Standard Management Registers

This section describes the IEEE 802.3 standard management registers corresponding to Clause 22.

Table 24 Registers Overview

Register Short Name	Register Long Name	Reset Value
STD_CTRL	STD Control (Register 0.0)	3040_H
STD_STAT	Status Register (Register 0.1)	7949_H
STD_PHYID1	PHY Identifier 1 (Register 0.2)	$67C9_H$
STD_PHYID2	PHY Identifier 2 (Register 0.3)	$DC00_H$ 1)
STD_AN_ADV	Auto-Negotiation Advertisement (Register 0.4)	$91E1_H$
STD_AN_LPA	Auto-Negotiation Link Partner Ability (Register 0.5)	$11E0_H$
STD_AN_EXP	Auto-Negotiation Expansion (Register 0.6)	0064_H
STD_AN_NPTX	Auto-Negotiation Next Page Transmit Register (Register 0.7)	2001_H
STD_AN_NPRX	Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)	0000_H
STD_GCTRL	Gigabit Control Register (Register 0.9)	0200_H
STD_GSTAT	Gigabit Status Register (Register 0.10)	0000_H
STD_MMDCTRL	MMD Access Control Register (Register 0.13)	0000_H
STD_MMDDATA	MMD Access Data Register (Register 0.14)	0000_H
STD_XSTAT	Extended Status Register (Register 0.15)	2000_H

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

5.1.1 Standard Management Registers

This section describes all the STD registers in detail.

STD Control (Register 0.0)

This register controls the main functions of the PHY.

IEEE Standard Register=0.0

STD_CTRL **Reset Value**

STD Control (Register 0.0) **3040_H**

15	14	13	12	11	10	9	8	7	6	5 … 0
RST	LB	SSL	ANEN	PD	ISOL	ANRS	DPLX	COL	SSM	RES
rwsc	rw	rw	rw	rw	rw	rwsc	rw	rw	rw	ro

Field	Bits	Type	Description
RST	15	RWSC	**Reset** Resets the PHY to its default state. Active links are terminated. This is a self-clearing bit, which is set to zero by the hardware after a reset is performed. Refer to IEEE 802.3-2008 22.2.4.1.1. 0_B **NORMAL** Normal operational mode 1_B **RESET** Resets the device.
LB	14	RW	**Loopback on GMII** This mode enables looping back of MII data (SGMII) from the transmit to the receive direction. No data is transmitted to the Ethernet PHY. The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test. 0_B **NORMAL** Normal operational mode 1_B **ENABLE** Closes the loopback from Tx to Rx at xMII.
SSL	13	RW	**Forced Speed Selection LSB** This bit only takes effect when the auto-negotiation process is disabled, that is, bit ANEN is set to zero. This is the lower bit (LSB) of the forced speed selection. In conjunction with the highest bit (MSB), the following encoding is valid: MSB LSB bit values: 0 0 = 10 Mbps 0 1 = 100 Mbps 1 0 = 1000 Mbps 1 1 = Reserved, defaults to 2500 Mbps when the PMA_CTRL register 1.0.5:2 is equal to [0 1 1 0]. The standard procedure to force 2500 Mbps (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0]. The GPY PHY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13.
ANEN	12	RW	**Auto-Negotiation Enable** Allows enabling and disabling of the auto-negotiation process capability of the PHY. When enabled, the force bits for duplex mode (CTRL.DPLX) and the speed selection (CTRL.SSM, CTRL.SSL) become inactive; otherwise, the force bits define the PHY operation. Refer to IEEE 802.3-2008 22.2.4.1.4. 0_B **DISABLE** Disable the auto-negotiation protocol. 1_B **ENABLE** Enable the auto-negotiation protocol.
PD	11	RW	**Power Down** Forces the device into a power down state (SLEEP) in which power consumption is the bare minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode. Refer to IEEE 802.3-2008 22.2.4.1.5. 0_B **NORMAL** Normal operational mode 1_B **POWERDOWN** Forces the device into power down mode.

Field	Bits	Type	Description (cont'd)
ISOL	10	RW	**Isolate** The isolation mode isolates the PHY from the MAC. The MAC interface inputs are ignored, whereas the MAC interface outputs are set to tristate (high-impedance). Refer to IEEE 802.3-2008 22.2.4.1.6. 0_B **NORMAL** Normal operational mode 1_B **ISOLATE** Isolates the PHY from the MAC
ANRS	9	RWSC	**Restart Auto-Negotiation** Restarts the auto-negotiation process on the MDI. This bit does not have any effect when auto-negotiation is disabled using (CTRL.ANEN). This bit is self-clearing after the auto-negotiation process is initiated. Refer to IEEE 802.3-2008 22.2.4.1.7. 0_B **NORMAL** Stay in current mode. 1_B **RESTART** Restart auto-negotiation.
DPLX	8	RW	**Forced Duplex Mode** This bit only takes effect when the auto-negotiation process is disabled, that is, bit CTRL.ANEN is set to zero. This bit controls the forced duplex mode. It allows forcing of the PHY into full or half duplex mode. This bit does not take effect in loopback mode, that is, when bit CTRL.LB is set to 1. Refer to IEEE 802.3-2008 22.2.4.1.8. The duplex mode may only be forced to half duplex in 10BASE-T and 100BASE-TX speed modes. This field is ignored for higher speeds. 0_B **HD** Half duplex 1_B **FD** Full duplex
COL	7	RW	**Collision Test** Allows testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency. Refer to IEEE 802.3-2008 22.2.4.1.9. 0_B **DISABLE** Normal operational mode 1_B **ENABLE** Activates the collision test.
SSM	6	RW	**Forced Speed Selection MSB** This bit only takes effect when the auto-negotiation process is disabled, that is, bit ANEN is set to zero. This is the most significant bit (MSB) of the forced speed selection. In conjunction with the lower bit, (LSB), the following encoding is valid: MSB LSB: 0 0 = 10 Mbps 0 1 = 100 Mbps 1 0 = 1000 Mbps 1 1 = Reserved, defaults to 2500 Mbps when the PMA_CTRL (1.0.5:2 = [0 1 1 0]). The preferred way to force 2500 Mbps (when ANEG is disabled) is to program PMA_CTRL with 1.0.6 = 1.0.13 = 1 and 1.0.5:2 = [0 1 1 0]. The GPY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13
RES	5:0	RO	**Reserved** Write as zero, ignore on read.

Status Register (Register 0.1)

This register contains status and capability information about the device. All the bits are read-only. A write access by the MAC does not have any effect. Refer to IEEE 802.3-2008 22.2.4.2.

IEEE Standard Register=0.1

STD_STAT **Reset Value**

Status Register (Register 0.1) **7949_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CBT4	**CBTXF**	**CBTXH**	**XBTF**	**XBTH**	**CBT2F**	**CBT2H**	**EXT**	**RES**	**MFPS**	**ANOK**	**RF**	**ANAB**	**LS**	**JD**	**XCAP**
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rolh	ro	roll	rolh	ro

Field	Bits	Type	Description
CBT4	15	RO	**IEEE 100BASE-T4** Specifies the 100BASE-T4 ability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
CBTXF	14	RO	**IEEE 100BASE-TX Full Duplex** Specifies the 100BASE-TX full duplex capability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
CBTXH	13	RO	**IEEE 100BASE-TX Half Duplex** Specifies the 100BASE-TX half duplex capability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
XBTF	12	RO	**IEEE 10BASE-T Full Duplex** Specifies the 10 BASE-T full duplex capability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
XBTH	11	RO	**IEEE 10BASE-T Half Duplex** Specifies the 10BASE-T half duplex capability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
CBT2F	10	RO	**IEEE 100BASE-T2 Full Duplex** Specifies the 100BASE-T2 full duplex capability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
CBT2H	9	RO	**IEEE 100BASE-T2 Half Duplex** Specifies the 100BASE-T2 half duplex capability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.

Field	Bits	Type	Description (cont'd)
EXT	8	RO	**Extended Status** The extended status registers are used to specify 1000 Mbps speed capabilities in the register XSTAT. Refer to IEEE 802.3-2008 Clause 22.2.4.2.16. 0_B **DISABLED** No extended status information available in register 15. 1_B **ENABLED** Extended status information available in register 15.
RES	7	RO	**Reserved** Ignore when read.
MFPS	6	RO	**Management Preamble Suppression** Specifies the MF preamble suppression ability. Refer to IEEE 802.3-2008 22.2.4.2.9. 0_B **DISABLED** PHY requires management frames with preamble. 1_B **ENABLED** PHY accepts management frames without preamble.
ANOK	5	RO	**Auto-Negotiation Completed** Indicates whether the auto-negotiation process is completed or in progress. Refer to IEEE 802.3-2008 22.2.4.2.10. 0_B **RUNNING** Auto-negotiation process is in progress. 1_B **COMPLETED** Auto-negotiation process is completed.
RF	4	ROLH	**Remote Fault** Indicates the detection of a remote fault event. Refer to IEEE 802.3-2008 22.2.4.2.11. GPY doesn't indicate RF. 0_B **INACTIVE** No remote fault condition detected. 1_B **ACTIVE** Remote fault condition detected.
ANAB	3	RO	**Auto-Negotiation Ability** Specifies the auto-negotiation ability. Refer to IEEE 802.3-2008 22.2.4.2.12. 0_B **DISABLED** PHY is not able to perform auto-negotiation. 1_B **ENABLED** PHY is able to perform auto-negotiation.
LS	2	ROLL	**Link Status** Indicates the link status of the PHY to the link partner. Refer to IEEE 802.3-2008 22.2.4.2.13. 0_B **INACTIVE** The link is down. No communication with link partner possible. 1_B **ACTIVE** The link is up. Data communication with link partner is possible.
JD	1	ROLH	**Jabber Detect** Indicates that a jabber event has been detected. Refer to IEEE 802.3-2008 22.2.4.2.14. 0_B **NONE** No jabber condition detected. 1_B **DETECTED** Jabber condition detected.
XCAP	0	RO	**Extended Capability** Indicates the availability and support of extended capability registers. Refer to IEEE 802.3-2008 22.2.4.2.15. 0_B **DISABLED** Only base registers are supported. 1_B **ENABLED** Extended capability registers are supported.

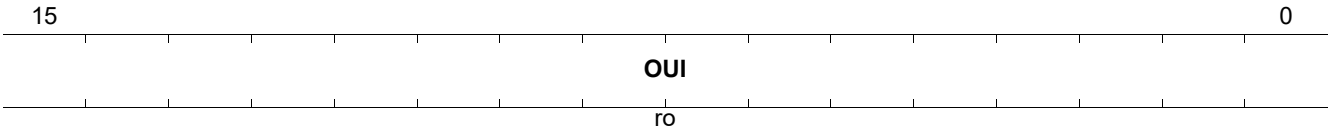
PHY Identifier 1 (Register 0.2)

This code specifies the Organizationally Unique Identifier (OUI), and the vendor's model and revision number.

IEEE Standard Register=0.2

STD_PHYID1 **Reset Value**

PHY Identifier 1 (Register 0.2) **$67C9_H$**



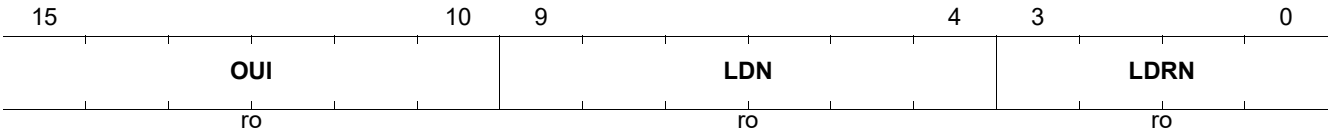
Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18**

PHY Identifier 2 (Register 0.3)

IEEE Standard Register=0.3

STD_PHYID2 **Reset Value**

PHY Identifier 2 (Register 0.3) **$DC00_H$**



Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several different products.
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number[1)] to distinguish between several versions of this device.

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

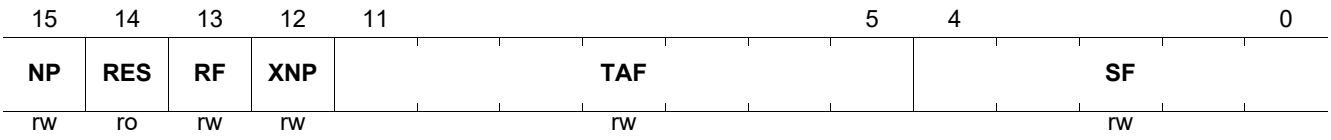
Auto-Negotiation Advertisement (Register 0.4)

This register contains the advertised abilities of the PHY during auto-negotiation.

IEEE Standard Register=0.4

STD_AN_ADV **Reset Value**

Auto-Negotiation Advertisement (Register 0.4) **$91E1_H$**



Field	Bits	Type	Description
NP	15	RW	**Next Page** The next page indication is encoded in bit AN_ADV.NP regardless of the selector field value or link code word encoding. The PHY always advertises NP when a 1000BASE-T mode is advertised during auto-negotiation. Refer to IEEE 802.3-2008 28.2.1.2.6. 0_B **INACTIVE** No next page to follow. 1_B **ACTIVE** Additional next page(s) to follow.
RES	14	RO	**Reserved** Write as zero, ignore on read.
RF	13	RW	**Remote Fault** The remote fault bit allows indication of a fault to the link partner. Refer to IEEE 802.3-2008 28.2.1.2.4. 0_B **NONE** No remote fault is indicated. 1_B **FAULT** A remote fault is indicated.
XNP	12	RW	**Extended Next Page** Indicates that the GPY supports transmission of extended next pages (XNP). 0_B **UNABLE** GPY is XNP unable. 1_B **ABLE** GPY is XNP able.
TAF	11:5	RW	**Technology Ability Field** The technology ability field is an 7-bit wide field containing information indicating supported technologies. The GPY supports 10BASE-T (half and full duplex), 100BASE-TX (half and full duplex) and both symmetric and asymmetric PAUSE. 40_H **PS_ASYM** Advertise asymmetric pause 20_H **PS_SYM** Advertise symmetric pause 10_H **DBT4** Advertise 100BASE-T4 08_H **DBT_FDX** Advertise 100BASE-TX full duplex 04_H **DBT_HDX** Advertise 100BASE-TX half duplex 02_H **XBT_FDX** Advertise 10BASE-T full duplex 01_H **XBT_HDX** Advertise 10BASE-T half duplex
SF	4:0	RW	**Selector Field** The selector field is a 5-bit wide field for encoding 32 possible messages. Selector field encodings are defined in IEEE 802.3-2008 Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the selector field are not to be transmitted. Refer to IEEE 802.3-2008 28.2.1.2.1. 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

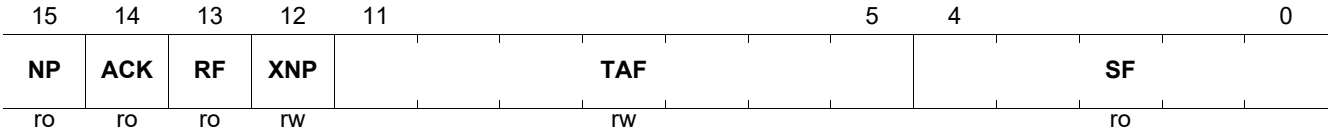
Auto-Negotiation Link Partner Ability (Register 0.5)

IEEE Standard Register=0.5

When the auto-negotiation is complete, this register contains the advertised ability of the link partner. The bit definitions are a direct representation of the received link code word.

STD_AN_LPA **Reset Value**

Auto-Negotiation Link Partner Ability (Register 0.5) **$11E0_H$**



Field	Bits	Type	Description
NP	15	RO	**Next Page** Next page request indication from the link partner. Refer to IEEE 802.3-2008 28.2.1.2.6. 0_B **INACTIVE** No next page to follow. 1_B **ACTIVE** Additional next pages to follow.
ACK	14	RO	**Acknowledge** Acknowledgment indication from the link partner's link code word. Refer to IEEE 802.3-2008 28.2.1.2.5. 0_B **INACTIVE** The device did not successfully receive its link partner's link code word. 1_B **ACTIVE** The device successfully received its link partner's link code word.
RF	13	RO	**Remote Fault** Remote fault indication from the link partner. Refer to IEEE 802.3-2008 28.2.1.2.4. 0_B **NONE** Remote fault is not indicated by the link partner. 1_B **FAULT** Remote fault is indicated by the link partner.
XNP	12	RW	**Extended Next Page** Indicates that the GPY supports the transmission of extended next pages (XNP). 0_B **UNABLE** Link partner is XNP unable. 1_B **ABLE** Link partner is XNP able.
TAF	11:5	RW	**Technology Ability Field** 40_H **PS_ASYM** Advertise asymmetric pause 20_H **PS_SYM** Advertise symmetric pause 10_H **DBT4** Advertise 100BASE-T4 08_H **DBT_FDX** Advertise 100BASE-TX full duplex 04_H **DBT_HDX** Advertise 100BASE-TX half duplex 02_H **XBT_FDX** Advertise 10BASE-T full duplex 01_H **XBT_HDX** Advertise 10BASE-T half duplex
SF	4:0	RO	**Selector Field** 00001_B**IEEE802DOT3** Select the IEEE 802.3 technology

Auto-Negotiation Expansion (Register 0.6)

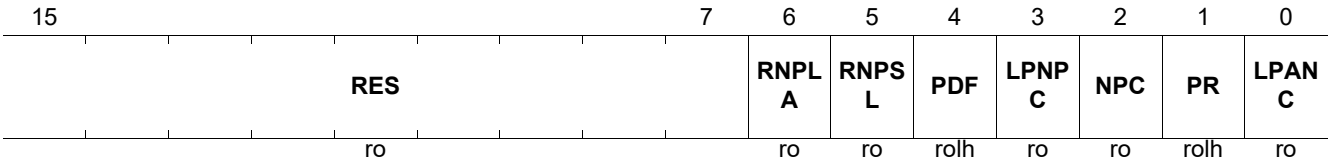
This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. This register is valid only after the auto-negotiation is completed.

Refer to IEEE 802.3 28.2.4.1.5.

IEEE Standard Register=0.6

STD_AN_EXP **Reset Value**

Auto-Negotiation Expansion (Register 0.6) **0064_H**



Field	Bits	Type	Description
RES	15:7	RO	**Reserved** Write as zero, ignore on read.
RNPLA	6	RO	**Receive Next Page Location Able** According to 802.3 - 2015, indicate that the Rx NP location is indicated by field RNPSL. 0_B **UNABLE** Received Next Page Storage Location is not specified by bit (6.5). 1_B **ABLE** Received Next Page Storage Location is specified by bit (6.5).
RNPSL	5	RO	**Receive Next Page Storage Location** According to 802.3 - 2015, indicate that the Rx NP is in register 0.8 for the GPY. 0_B **FIVE** Link partner next pages are stored in register 5. 1_B **EIGHT** Link partner next pages are stored in register 8.
PDF	4	ROLH	**Parallel Detection Fault** 0_B **NONE** A fault has not been detected via the parallel detection function. 1_B **FAULT** A fault has been detected via the parallel detection function.
LPNPC	3	RO	**Link Partner Next Page Capable** 0_B **UNABLE** Link partner is unable to exchange next pages. 1_B **CAPABLE** Link partner is capable of exchanging next pages.
NPC	2	RO	**Next Page Capable** 0_B **UNABLE** GPY is unable to exchange next pages. 1_B **CAPABLE** GPY is capable of exchanging next pages.
PR	1	ROLH	**Page Received** 0_B **NONE** A new page has not been received. 1_B **RECEIVED** A new page has been received.
LPANC	0	RO	**Link Partner Auto-Negotiation Capable** 0_B **UNABLE** Link partner is unable to auto-negotiate. 1_B **CAPABLE** Link partner is auto-negotiation capable.

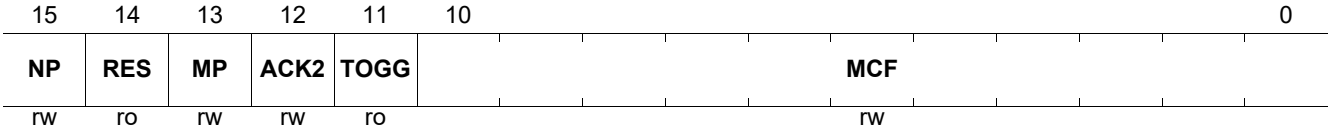
Auto-Negotiation Next Page Transmit Register (Register 0.7)

The auto-negotiation next page transmit register contains the next page link code word to be transmitted when next page ability is supported. Refer to IEEE 802.3 28.2.4.1.6.

IEEE Standard Register=0.7

STD_AN_NPTX **Reset Value**

Auto-Negotiation Next Page Transmit Register (Register 0.7) **2001_H**



Field	Bits	Type	Description
NP	15	RW	**Next Page** 0_B **INACTIVE** Last page 1_B **ACTIVE** Additional next page(s) to follow.
RES	14	RO	**Reserved** Write as zeros, ignore on read.
MP	13	RW	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RW	**Acknowledge 2. GPY Does Not Comply** 0_B **INACTIVE** Device is not able to comply with message. 1_B **ACTIVE** Device complies with message.
TOGG	11	RO	**Toggle** This bit always takes the opposite value of the Toggle bit in the previously exchanged link code word. Refer to IEEE 802.3-2008 28.2.3.4. 0_B **ZERO** Previous value of the transmitted link code word was ONE. 1_B **ONE** Previous value of the transmitted link code word was ZERO.

Field	Bits	Type	Description (cont'd)
MCF	10:0	RW	**Message or Unformatted Code Field** When the Message Page bit is set to 1 (0.7.13), this field is the Message Code Field of a message page used in next page exchange. The message codes are described in IEEE802.3 Appendix 28C. It is used to indicate the type of message in UCF1 and UCF2. 0x0 = Reserved 0x1 = Null message 0x2 = One Unformatted Page (UP) with TAF follows 0x3 = Two UPs with TAF follows 0x4 = Remote fault details message 0x5 = OUI message 0x6 = PHY ID message 0x7 = 100BASE-T2 message 0x8 = 1000BASE-T message 0x9 = MULTIGBASE-T message 0xA = EEE technology capability follows in next UP 0xB = OUI XNP

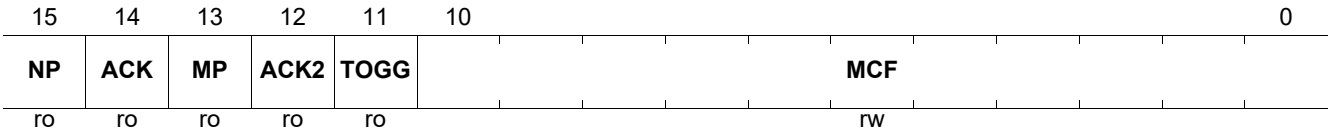
Auto-Negotiation Link Partner Received Next Page Register (Register 0.8)

This register contains the next page link code word received from the link partner. Refer to IEEE 802.3-2008 28.2.4.1.7.

IEEE Standard Register=0.8

STD_AN_NPRX **Reset Value**

Auto-Negotiation Link Partner Received Next Page Register (Register 0.8) **0000_H**



Field	Bits	Type	Description
NP	15	RO	**Next Page** Refer to IEEE 802.3-2008 28.2.3.4. 0_B **INACTIVE** No next pages to follow. 1_B **ACTIVE** Additional next page(s) to follow.
ACK	14	RO	**Acknowledge** Refer to IEEE 802.3-2008 28.2.3.4. 0_B **INACTIVE** The device did not successfully receive its link partner's link code word. 1_B **ACTIVE** The device successfully received its link partner's link code word.

Field	Bits	Type	Description (cont'd)
MP	13	RO	**Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. Refer to IEEE 802.3-2008 28.2.3.4. 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page
ACK2	12	RO	**Acknowledge 2** Refer to IEEE 802.3-2008 28.2.3.4. 0_B **INACTIVE** Device is not able to comply with the message. 1_B **ACTIVE** Device complies with the message.
TOGG	11	RO	**Toggle** This bit always takes the opposite value of the Toggle bit in the previously exchanged link code word. Refer to IEEE 802.3-2008 28.2.3.4. 0_B **ZERO** Previous value of the transmitted link code word was ONE. 1_B **ONE** Previous value of the transmitted link code word was ZERO.
MCF	10:0	RW	**Message or Unformatted Code Field** This field is the Message Code Field of a message page used in next page exchange. The message codes are described in IEEE802.3 Appendix 28C. It is used to indicate the type of message in UCF1 and UCF2. 0x0 = Reserved 0x1 = Null message 0x2 = One Unformated Page (UP) with TAF follows 0x3 = Two UPs with TAF follows 0x4 = Remote fault details message 0x5 = OUI message 0x6 = PHY ID message 0x7 = 100BASE-T2 message 0x8 = 1000BASE-T message 0x9 = MULTIGBASE-T message 0xA = EEE technology capability follows in next UP 0xB = OUI XNP

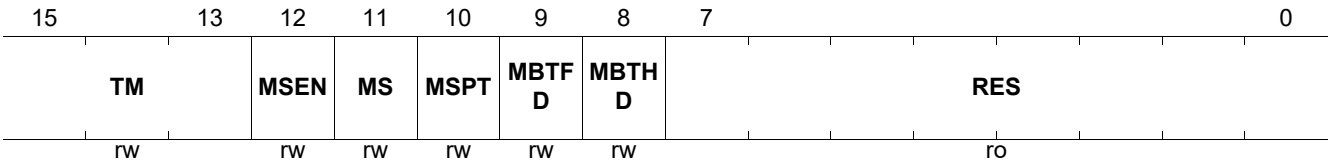
Gigabit Control Register (Register 0.9)

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. Refer to IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.9

STD_GCTRL **Reset Value**

Gigabit Control Register (Register 0.9) **0200_H**



Field	Bits	Type	Description
TM	15:13	RW	**Transmitter Test Mode** This register field allows enabling of the standard transmitter test modes. Refer to IEEE 802.3-2008 Table 40-7. 000_B **NOP** Normal operation 001_B **WAV** Test mode 1 transmit waveform test 010_B **JITM** Test mode 2 transmit jitter test in MASTER mode 011_B **JITS** Test mode 3 transmit jitter test in SLAVE mode 100_B **DIST** Test mode 4 transmitter distortion test
MSEN	12	RW	**Master/Slave Manual Configuration Enable** Refer to IEEE 802.3-2008 40.5.1.1. 0_B **DISABLED** Disable master/slave manual configuration value. 1_B **ENABLED** Enable master/slave manual configuration value.
MS	11	RW	**Master/Slave Config Value** Allows forcing of master or slave mode manually when AN_GCTRL.MSEN is set to logical 1. Refer to IEEE 802.3-2008 40.5.1.1. 0_B **SLAVE** Configure PHY as SLAVE during master/slave negotiation. 1_B **MASTER** Configure PHY as MASTER during master/slave negotiation.
MSPT	10	RW	**Master/Slave Port Type** Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function. Refer to IEEE 802.3-2008 40.5.1.1. 0_B **SPD** Single-port device 1_B **MPD** Multi-port device
MBTFD	9	RW	**1000BASE-T Full Duplex** Advertises the 1000BASE-T full duplex capability; always forced to 1 in converter mode. Refer to IEEE 802.3-2008 40.5.1.1. 0_B **DISABLED** Advertise PHY as not 1000BASE-T full duplex capable. 1_B **ENABLED** Advertise PHY as 1000BASE-T full duplex capable.
MBTHD	8	RW	**1000BASE-T Half Duplex** Always advertises the 1000BASE-T half duplex capability as disabled; the GPY does not support 1000BASE-T half duplex capability. 0_B **DISABLED** Advertise PHY as not 1000BASE-T half duplex capable. 1_B **ENABLED** Advertise PHY as 1000BASE-T half duplex capable.
RES	7:0	RO	**Reserved** Write as zero, ignore on read.

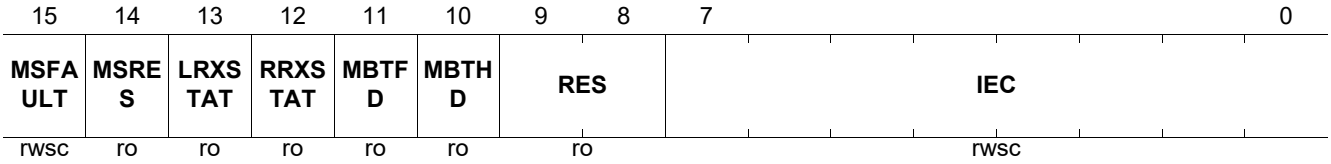
Gigabit Status Register (Register 0.10)

This is the status register used to reflect the Gigabit Ethernet status of the PHY. Refer to IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.10

STD_GSTAT **Reset Value**

Gigabit Status Register (Register 0.10) **0000_H**



Field	Bits	Type	Description
MSFAULT	15	RWSC	**Master/Slave Manual Configuration Fault** This bit is set when the number of failed MASTER-SLAVE resolutions reaches 7. It is cleared upon each read of GSTAT. This bit self clears on auto-negotiation enable or auto-negotiation complete. 0_B **OK** Master/slave manual configuration resolved successfully. 1_B **NOK** Master/slave manual configuration resolved with a fault.
MSRES	14	RO	**Master/Slave Configuration Resolution** 0_B **SLAVE** Local PHY configuration resolved to SLAVE. 1_B **MASTER** Local PHY configuration resolved to MASTER.
LRXSTAT	13	RO	**Local Receiver Status** Indicates the status of the local receiver. Refer to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. 0_B **NOK** Local receiver not OK. 1_B **OK** Local receiver OK.
RRXSTAT	12	RO	**Remote Receiver Status** Indicates the status of the remote receiver. Refer to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. 0_B **NOK** Remote receiver not OK. 1_B **OK** Remote receiver OK.
MBTFD	11	RO	**Link Partner Capable of Operating 1000BASE-T Full Duplex** Refer to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T full duplex. 1_B **ENABLED** Link partner is capable of operating 1000BASE-T full duplex.

Field	Bits	Type	Description (cont'd)
MBTHD	10	RO	**Link Partner Capable of Operating 1000BASE-T Half Duplex** Refer to IEEE 802.3-2008 40.5.1.1 register 10 in Table 40-3. 0_B **DISABLED** Link partner is not capable of operating 1000BASE-T half duplex. 1_B **ENABLED** Link partner is capable of operating 1000BASE-T half duplex.
RES	9:8	RO	**Reserved** Write as zero, ignore on read.
IEC	7:0	RWSC	**Idle Error Count** Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver receives idles.

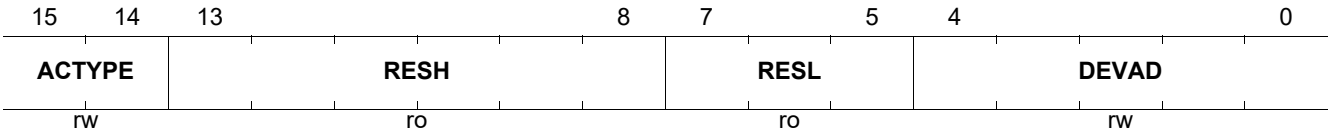
MMD Access Control Register (Register 0.13)

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. This uses address directing as specified in IEEE802.3 Clause 22 Extended.

IEEE Standard Register=0.13

STD_MMDCTRL **Reset Value**

MMD Access Control Register (Register 0.13) **0000_H**



Field	Bits	Type	Description
ACTYPE	15:14	RW	**Access Type Function** When the MMDDATA register is accessed via an address access (ACTYPE=0), the access is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD's address register direct the MMDDATA register data accesses to the appropriate registers within that MMD. 00_B **ADDRESS** Accesses to the MMDDATA register access the MMD individual address register. 01_B **DATA** Accesses to the MMDDATA register access the register within the MMD selected. 10_B **DATA_PI** Accesses to the MMDDATA register access the register within the MMD selected. 11_B **DATA_PIWR** Accesses to the MMDDATA register access the register within the MMD selected.
RESH	13:8	RO	**Reserved** Write as zero, ignored on read.
RESL	7:5	RO	**Reserved** Write as zero, ignored on read.

Field	Bits	Type	Description (cont'd)
DEVAD	4:0	RW	**Device Address** The DEVAD field directs any accesses of register MMDDATA to the appropriate MMD as described in IEEE 802.3-2008 Clause 45.2.

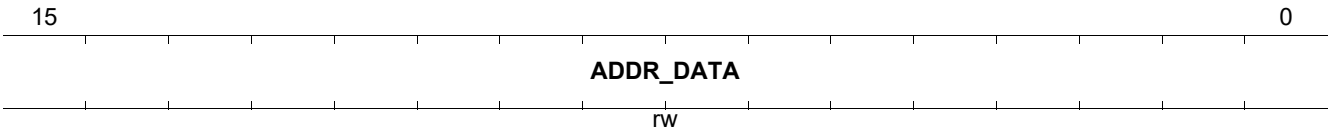
MMD Access Data Register (Register 0.14)

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space. For more information on MMD access, refer to IEEE 802.3-2008 Clause 22.2.4.3.12, Clause 45.2 and Annex 22D.

IEEE Standard Register=0.14

STD_MMDDATA **Reset Value**

MMD Access Data Register (Register 0.14) **0000_H**



Field	Bits	Type	Description
ADDR_DATA	15:0	RW	**Address or Data Register** This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. The MMDCTRL register defines which function is currently valid.

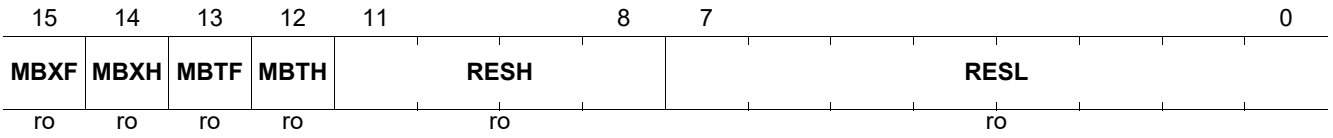
Extended Status Register (Register 0.15)

This register contains extended status and capability information about the PHY. All the bits are read-only. A write access does not have any effect.

IEEE Standard Register=0.15

STD_XSTAT **Reset Value**

Extended Status Register (Register 0.15) **2000_H**



Field	Bits	Type	Description
MBXF	15	RO	**1000BASE-X Full Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X full duplex. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.

Field	Bits	Type	Description (cont'd)
MBXH	14	RO	**1000BASE-X Half Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-X half duplex. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
MBTF	13	RO	**1000BASE-T Full Duplex Capability** Specifies whether the PHY is capable of operating 1000BASE-T full duplex. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
MBTH	12	RO	**1000BASE-T Half Duplex Capability** GPY do not support 1000BASE-T half duplex capability. 0_B **DISABLED** PHY does not support this mode. 1_B **ENABLED** PHY supports this mode.
RESH	11:8	RO	**Reserved** Ignore when read.
RESL	7:0	RO	**Reserved** Ignore when read.

5.2 GPY-specific Management Registers

This section describes the GPY-specific management registers in device 0.

Table 25 Registers Overview

Register Short Name	Register Long Name	Reset Value
PHY_STAT1	Physical Layer Status 1 (Register 0.17)	0000_H
PHY_CTL1	Physical Layer Control 1 (Register 0.19)	0001_H
PHY_CTL2	Physical Layer Control 2 (Register 0.20)	0006_H
PHY_ERRCNT	Error Counter (Register 0.21)	0000_H
PHY_MIISTAT	Media-Independent Interface Status (Register 0.24)	0000_H
PHY_IMASK	Interrupt Mask Register (Register 0.25)	0000_H
PHY_ISTAT	Interrupt Status Register (Register 0.26)	0000_H
PHY_LED	LED Control Register (Register 0.27)	$FF00_H$
PHY_FWV	Firmware Version Register (Register 0.30)	0000_H

5.2.1 GPY-specific Management Registers

This section describes all the PHY registers in detail.

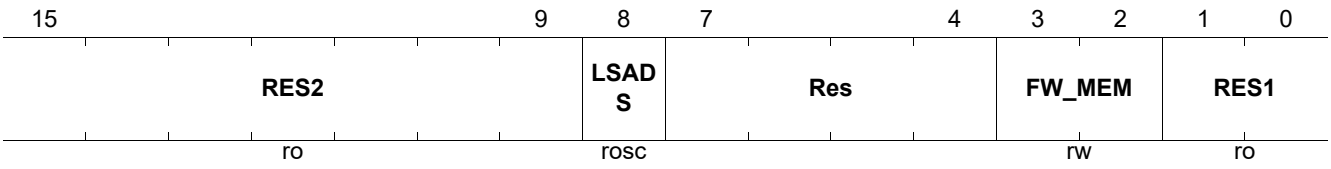
Physical Layer Status 1 (Register 0.17)

This register reports PHY link information, for example link-up, polarity reversals, and port mapping. The content of this register is only valid when the link is up.

IEEE Standard Register=0.17

PHY_STAT1 **Reset Value**

Physical Layer Status 1 (Register 0.17) **0000_H**



Field	Bits	Type	Description
RES2	15:9	RO	**Reserved** Write as zero, ignored on read.
LSADS	8	ROSC	**Link Speed Auto-Downspeed Status** Monitors the status of the auto-downspeed. 0_B **NORMAL** Did not perform any link speed auto-downspeed. 1_B **DETECTED** Detected an auto-downspeed.

Field	Bits	Type	Description (cont'd)
FW_MEM	3:2	RW	**Firmware Memory Location** Indicates memory target used for firmware execution. 00_B **ROM** Firmware is executed from ROM. 01_B **OTP** Firmware is executed from OTP. 10_B **FLASH** Firmware is executed from FLASH. 11_B **RAM** Firmware is executed from SRAM.
RES1	1:0	RO	**Reserved** Write as zero, ignored on read.

Physical Layer Control 1 (Register 0.19)

This register controls the PHY functions.

IEEE Standard Register=0.19

PHY_CTL1 **Reset Value**

Physical Layer Control 1 (Register 0.19) **0001_H**

15	12	11	8	7	6	5	4	3	2	1	0
TLOOP	**RES**	**TXADJ**		**POLD**	**POLC**	**POLB**	**POLA**	**MDICD**	**MDIAB**	**RES**	**AMDIX**
		rw		rw	rw	rw	rw	rw	rw	ro	rw

Field	Bits	Type	Description
TLOOP	15:13	RW	**Test Loop** Configures predefined test loops. 000_B **OFF** Test loops are switched off - normal operation. 001_B **NETL** Near-end test loop 010_B **FETL** Far-end test loop. Others: Reserved.
TXADJ	11:8	RW	**Transmit Level Adjustment** Transmit level adjustment is used to fine tune the transmit amplitude of the PHY. The amplitude adjustment is valid for all supported speed modes. The adjustment is performed in digits. One digit represents 3.125 percent of the nominal amplitude. The scaling factor is gain = 1 + signed(TXADJ)*2^-7.
POLD	7	RW	**Polarity Inversion Control on Port D** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLC	6	RW	**Polarity Inversion Control on Port C** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
POLB	5	RW	**Polarity Inversion Control on Port B** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion

Field	Bits	Type	Description (cont'd)
POLA	4	RW	**Polarity Inversion Control on Port A** 0_B **NORMAL** Polarity normal 1_B **INVERTED** Polarity inversion
MDICD	3	RW	**Mapping of MDI Ports C and D** Used when Auto-MDIX is OFF to force the MDIX cable crossover configuration. 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
MDIAB	2	RW	**Mapping of MDI Ports A and B** Used when Auto-MDIX is OFF to force the MDIX cable crossover configuration. 0_B **MDI** Normal MDI mode 1_B **MDIX** Crossover MDI-X mode
RES	1	RO	**Reserved**
AMDIX	0	RW	**PHY Performs Auto-MDI/MDI-X or Uses Manual MDI/MDI-X** 0_B **MANUAL** PHY uses manual MDI/MDI-X. 1_B **AUTO** PHY performs Auto-MDI/MDI-X.

Physical Layer Control 2 (Register 0.20)

This register controls the PHY functions.

IEEE Standard Register=0.20

PHY_CTL2 **Reset Value**

Physical Layer Control 2 (Register 0.20) **0006_H**

15	10	9	8	7	5	4	3	2	1	0
Res		SDETP	STICKY	RES1		RES2	LP	PSCL	ANPD	LPI
		rw	rw	ro		rw	rw	rw	rw	rw

Field	Bits	Type	Description
SDETP	9	RW	**Signal Detection Polarity for the 1000BASE-X PHY** Allows specification of the signal detection polarity of the SIGDET input. Although this bit is reset to 0, its actual value depends on the pin-strapping configuration when no EEPROM is detected. 0_B **LOWACTIVE** SIGDET input is low active. 1_B **HIGHACTIVE** SIGDET input is high active.
STICKY	8	RW	**Sticky-Bit Handling** Setting this bit to 1 ensures that all the vendor specific registers (of type RW) in the PHY (device 0), VSPEC1 (device 30), and VSPEC2 (device 31) are not changed during a MDIO reset or software reset of the GPY. This allows the STA to keep the configurations chosen before reset. 0_B **OFF** Sticky-bit handling is disabled. 1_B **ON** Sticky-bit handling is enabled.

Field	Bits	Type	Description (cont'd)
RES1	7:5	RO	**Reserved** Write as zero, ignored on read.
RES2	4	RW	**Reserved**
LP	3	RW	**Low Power Mode** Low Power Mode (LP) allows the GPY to save energy by disabling most of the digital logic to reduce power consumption to its lowest level. The entry to LP is triggered when the PHY does not sense any energy on the cable and no link pulses (NLP, FLP, Beacons) are received. After spending VSPEC1_NBT_DS_CTRL.NRG_RST_CNT without energy in the ABILITY_DETECT state defined by IEEE802.3 Clause 28, and after the timer defined VSPEC1_LOW_POWER_ENTRY_TIME.LPE_TIM expired, the PHY enters LP. 0_B **OFF** LP is disabled. The GPY does not enter LP. 1_B **ON** LP is enabled. The GPY enters LP when no energy is sensed.
PSCL	2	RW	**Power Consumption Scaling Depending on Link Quality** Allows enabling/disabling of the power consumption scaling depending on the link quality. 0_B **OFF** PSCL is disabled. 1_B **ON** PSCL is enabled.
ANPD	1	RW	**Auto-Negotiation Power Down** Allows enabling/disabling of the power down modes during auto-negotiation looking for a link partner. 0_B **OFF** ANPD is disabled. 1_B **ON** ANPD is enabled.
LPI	0	RW	**Assert LPI via MDIO** Controls asserts/de-asserts of the LPI by the MDIO instead of following the (X)GMII LPI. Used to force the EEE on the TPI (ignoring the LPI indication from MAC). 0_B **DE-ASSERT** LPI is de-asserted on TPI. 1_B **ASSERT** LPI is asserted on TPI.

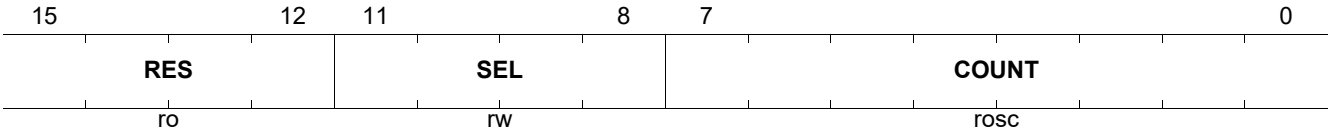
Error Counter (Register 0.21)

This register controls the error counter. It allows the number of errors detected in the PHY to be counted for monitoring purposes.

IEEE Standard Register=0.21

PHY_ERRCNT **Reset Value**

Error Counter (Register 0.21) **0000_H**



Field	Bits	Type	Description
RES	15:12	RO	**Reserved** Write as zero, ignored on read.
SEL	11:8	RW	**Select Error Event** Configures which error type the error counter counts: 0000_B**RXERR** Receive errors are counted. 0001_B**RXACT** Receive frames are counted. 0010_B**ESDERR** ESD errors are counted. 0011_B**SSDERR** SSD errors are counted. 0100_B**TXERR** Transmit errors are counted. 0101_B**TXACT** Transmit frames events are counted. 0110_B**COL** Collision events are counted. 1000_B**NLD** Number of Link Down events are counted. 1001_B**NDS** Number of auto-downspeed events are counted. 1010_B**CRC** CRC counter 1011_B**TTL** Time to Link
COUNT	7:0	ROSC	**Counter Value** This counter value is updated each time the selected error event is detected. The counter value is reset every time a read operation on this register is performed or the error event is changed. The counter saturates at value 0xFF.

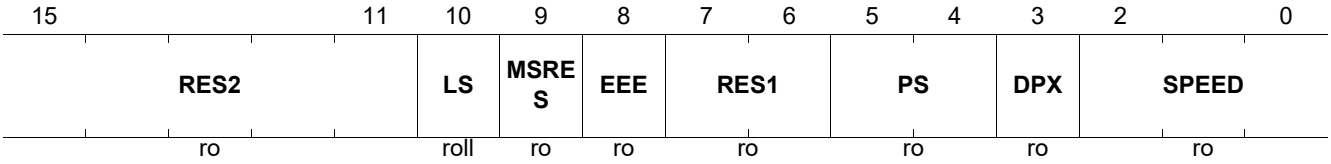
Media-Independent Interface Status (Register 0.24)

This register contains status information on the Ethernet link, concatenated in a single register to allow concise status read by the STA in a single register.

IEEE Standard Register=0.24

PHY_MIISTAT **Reset Value**

Media-Independent Interface Status (Register 0.24) **0000_H**



Field	Bits	Type	Description
RES2	15:11	RO	**Reserved** Write as zero, ignored on read.
LS	10	ROLL	**Link Status of GPY Ethernet PHY Operation** Indicates the link status of the PHY. 0_B **INACTIVE** The link is down. No communication with link partner possible. 1_B **ACTIVE** The link is up. Data communication with link partner is possible.
MSRES	9	RO	**Master/Slave Configuration** Indicates the Master/Slave Configuration 0_B **SLAVE** Local PHY configuration is SLAVE after ANEG. 1_B **MASTER** Local PHY configuration is MASTER after ANEG.
EEE	8	RO	**Energy-Efficient Ethernet Mode** 0_B **OFF** EEE is disabled after auto-negotiation resolution. 1_B **ON** EEE is enabled after auto-negotiation resolution.
RES1	7:6	RO	**Reserved**
PS	5:4	RO	**Pause Status for Flow Control** 00_B **NONE** No PAUSE 01_B **TX** Transmit PAUSE 10_B **RX** Receive PAUSE 11_B **TXRX** Both transmit and receive PAUSE
DPX	3	RO	**GPY Ethernet PHY Duplex Mode** 0_B **HDX** Half duplex 1_B **FDX** Full duplex
SPEED	2:0	RO	**GPY Ethernet PHY Speed** 000_B **TEN** 10 Mbps 001_B **FAST** 100 Mbps 010_B **GIGA** 1000 Mbps 011_B **ANEG** Auto-negotiation mode 100_B **BZ2G5** 2.5 Gbps

Interrupt Mask Register (Register 0.25)

This register defines the mask for the Interrupt Status Register (ISTAT), which contains the event source for the MDINT interrupt sent from the GPY to an external chip.

The information about the interrupt source is indicated in the ISTAT register.

IEEE Standard Register=0.25

PHY_IMASK **Reset Value**

Interrupt Mask Register (Register 0.25) **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WOL	**MSRE**	**NPRX**	**NPTX**	**ANE**	**ANC**	**Res**	**LOR**	**LP**	**TEMP**	**ADSC**	**MDIPC**	**MDIXC**	**DXMC**	**LSPC**	**LSTC**
rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WOL	15	RW	**Wake-on-LAN Event Mask** When active and masked in IMASK, the MDINT is activated upon detection of a valid wake-on-LAN event. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
MSRE	14	RW	**Master/Slave Resolution Error Mask** When active, MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
NPRX	13	RW	**Next Page Received Mask** When active, MDINT is activated upon reception of a next page in STD.AN_NPRX. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
NPTX	12	RW	**Next Page Transmitted Mask** When active, MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
ANE	11	RW	**Auto-Negotiation Error Mask** When active, MDINT is activated upon detection of an auto-negotiation error. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
ANC	10	RW	**Auto-Negotiation Complete Mask** When active, MDINT is activated upon completion of the auto-negotiation process. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.

Field	Bits	Type	Description (cont'd)
LOR	8	RW	**SyncE Loss Of Reference** When active, MDINT is activated upon loss of SyncE reference clock. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
LP	7	RW	**LP Entry Indication Mask** 0_B **INACTIVE** Interrupt is masked out. The STA does not need to be informed of the event. 1_B **ACTIVE** Interrupt is activated. The STA receives MDINT when the PHY is about to enter LP.
TEMP	6	RW	**TEMP** 0_B **INACTIVE** Interrupt is masked out. The STA does not need to be informed of the event. 1_B **ACTIVE** Interrupt is activated. The interrupt is triggered when the temperature goes beyond the normal operating range.
ADSC	5	RW	**Link Speed Auto-Downspeed Detect Mask** When active, MDINT is activated upon detection of a link speed auto-downspeed event. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
MDIPC	4	RW	**MDI Polarity Change Detect Mask** When active, MDINT is activated upon detection of an MDI polarity change event. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
MDIXC	3	RW	**MDIX Change Detect Mask** When active, MDINT is activated upon detection of an MDI/MDIX cross-over change event. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
DXMC	2	RW	**Duplex Mode Change Mask** When active, MDINT is activated upon detection of full or half duplex change. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
LSPC	1	RW	**Link Speed Change Mask** When active, MDINT is activated upon detection of link speed change. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.
LSTC	0	RW	**Link State Change Mask** When active, MDINT is activated upon detection of link status change. 0_B **INACTIVE** Interrupt is masked out. 1_B **ACTIVE** Interrupt is activated.

Interrupt Status Register (Register 0.26)

This register defines the event source for the MDINT interrupt sent from the GPY to an external chip.

PHY_ISTAT is a cleared on read by the STA.

IEEE Standard Register=0.26

PHY_ISTAT **Reset Value**

Interrupt Status Register (Register 0.26) **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WOL	**MSRE**	**NPRX**	**NPTX**	**ANE**	**ANC**	**Res**	**LOR**	**LP**	**TEMP**	**ADSC**	**MDIPC**	**MDIXC**	**DXMC**	**LSPC**	**LSTC**
rosc	rosc	rosc	rosc	rosc	rosc		rosc	rosc	rosc	rosc	rosc	rosc	rosc	rosc	rosc

Field	Bits	Type	Description
WOL	15	ROSC	**Wake-on-LAN Interrupt Status** When bit is set, the MDINT is activated upon detection of a valid wake-on-LAN event. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** WoL event is the source of the interrupt.
MSRE	14	ROSC	**Master/Slave Resolution Error Interrupt Status** When bit is set, the MDINT is activated upon detection of a master/slave resolution error during a 1000BASE-T auto-negotiation. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** MSRE event is the source of the interrupt.
NPRX	13	ROSC	**Next Page Received Interrupt Status** When bit is set, the MDINT is activated upon reception of a next page in STD.AN_NPRX. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** NPRX event is the source of the interrupt.
NPTX	12	ROSC	**Next Page Transmitted Interrupt Status** When bit is set, the MDINT is activated upon transmission of the currently stored next page in STD.AN_NPTX. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** NPTX event is the source of the interrupt.
ANE	11	ROSC	**Auto-Negotiation Error Interrupt Status** When bit is set, the MDINT is activated upon detection of an auto-negotiation error. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** ANEG error event is the source of the interrupt.
ANC	10	ROSC	**Auto-Negotiation Complete Interrupt Status** When bit is set, the MDINT is activated upon completion of the auto-negotiation process. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** ANEG complete event is the source of the interrupt.

Field	Bits	Type	Description (cont'd)
LOR	8	ROSC	**SyncE Loss Of Reference** When bit is set, MDINT is activated upon loss of SyncE reference clock. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** LOR Change event is the source of the interrupt.
LP	7	ROSC	**LP Entry Indication** 0_B **INACTIVE** No indication of LP entry. 1_B **ACTIVE** Indication of LP entry.
TEMP	6	ROSC	**TEMP** Indicates that thermal mitigation action must be taken when the temperature goes beyond the normal operating range. It is recommended that the SoC initiates a link down and changes the speed capability to cool the device back to the normal temperature range. When the temperature reaches the maximum absolute rating, the GPY resets for safety purposes. Thermal mitigation must ensure that the maximum absolute temperature limits are never reached. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** TEMP Change event is the source of the interrupt.
ADSC	5	ROSC	**Link Speed Auto-Downspeed Detect Interrupt Status** When bit is set, the MDINT is activated upon detection of a link speed auto-downspeed event. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** ADSC Change event is the source of the interrupt.
MDIPC	4	ROSC	**MDI Polarity Change Detect Interrupt Status** When bit is set, the MDINT is activated upon detection of an MDI polarity change event. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** MDIPC Change event is the source of the interrupt.
MDIXC	3	ROSC	**MDIX Change Detect Interrupt Status** When bit is set, the MDINT is activated upon detection of an MDI/MDIX cross-over change event. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** MDIX Change event is the source of the interrupt.
DXMC	2	ROSC	**Duplex Mode Change Interrupt Status** When bit is set, the MDINT is activated upon detection of a full or half duplex change. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** Duplex Mode Change event is the source of the interrupt.
LSPC	1	ROSC	**Link Speed Change Interrupt Status** When bit is set, the MDINT is activated upon detection of link speed change. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** Link Speed Change event is the source of the interrupt.
LSTC	0	ROSC	**Link State Change Interrupt Status** When bit is set, the MDINT is activated upon detection of link status change. 0_B **INACTIVE** This event is not the interrupt source. 1_B **ACTIVE** Link State Change event is the source of the interrupt.

LED Control Register (Register 0.27)

This register contains the control bits for direct access to the LEDs by setting the on/off LEDxA bits (where x is from 0 to 4).

To directly control the LED, the integrated LED functions must be disabled by the LEDxEN bit in this register.

The integrated LED functions are specified in the more sophisticated LED control registers in the MMD device VSPEC1.

IEEE Standard Register=0.27

PHY_LED **Reset Value**

LED Control Register (Register 0.27) **$FF00_H$**

15	12	11	10	9	8	7	4	3	2	1	0
INV		LED3EN	LED2EN	LED1EN	LED0EN	RES1		LED3DA	LED2DA	LED1DA	LED0DA
rw		rw	rw	rw	rw	ro		rw	rw	rw	rw

Field	Bits	Type	Description
INV	15:12	RW	**Invert LED Output** This provides a per LED control to invert the output of the LEDs. Set to 1 to support LEDs that are driven by VDDs. Set to 0 to support LEDs that are driven by the output pins of this product.
LED3EN	11	RW	**Enable Integrated Function of LED3** Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED3DA. 0_B **DISABLE** Disables the integrated LED function. 1_B **ENABLE** Enables the integrated LED function.
LED2EN	10	RW	**Enable Integrated Function of LED2** Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED2DA. 0_B **DISABLE** Disables the integrated LED function. 1_B **ENABLE** Enables the integrated LED function.
LED1EN	9	RW	**Enable Integrated Function of LED1** Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED1DA. 0_B **DISABLE** Disables the integrated LED function. 1_B **ENABLE** Enables the integrated LED function.
LED0EN	8	RW	**Enable Integrated Function of LED0** Write a 0 to this bit to disable the pre-configured integrated function for this LED. The LED remains off unless directly accessed via LED0DA. 0_B **DISABLE** Disables the integrated LED function. 1_B **ENABLE** Enables the integrated LED function.
RES1	7:4	RO	**Reserved** Write as zero, ignored on read.

Field	Bits	Type	Description (cont'd)
LED3DA	3	RW	**Direct Access to LED3** Write a 1 to this bit to illuminate the LED. LED3EN must be set to zero. 0_B **OFF** Switch off the LED. 1_B **ON** Switch on the LED.
LED2DA	2	RW	**Direct Access to LED2** Write a 1 to this bit to illuminate the LED. LED2EN must be set to zero. 0_B **OFF** Switch off the LED. 1_B **ON** Switch on the LED.
LED1DA	1	RW	**Direct Access to LED1** Write a 1 to this bit to illuminate the LED. LED1EN must be set to zero. 0_B **OFF** Switch off the LED. 1_B **ON** Switch on the LED.
LED0DA	0	RW	**Direct Access to LED0** Write a 1 to this bit to illuminate the LED. LED0EN must be set to zero. 0_B **OFF** Switch off the LED. 1_B **ON** Switch on the LED.

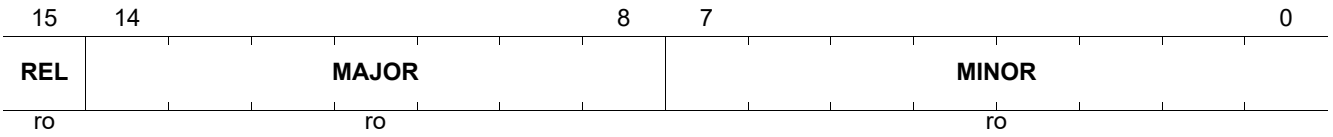
Firmware Version Register (Register 0.30)

This register contains the version of the PHY firmware. The firmware initializes the version number at boot time with its current software version. This register is read-only by the external STA.

IEEE Standard Register=0.30

PHY_FWV **Reset Value**

Firmware Version Register (Register 0.30) **0000_H**



Field	Bits	Type	Description
REL	15	RO	**Release Indication** This parameter indicates either a test or a release version. 0_B **TEST** Indicates a test version. 1_B **RELEASE** Indicates a released version.
MAJOR	14:8	RO	**Major Version Number** Specifies the main version release number of the firmware.
MINOR	7:0	RO	**Minor Version Number** Specifies the sub-version release number of the firmware.

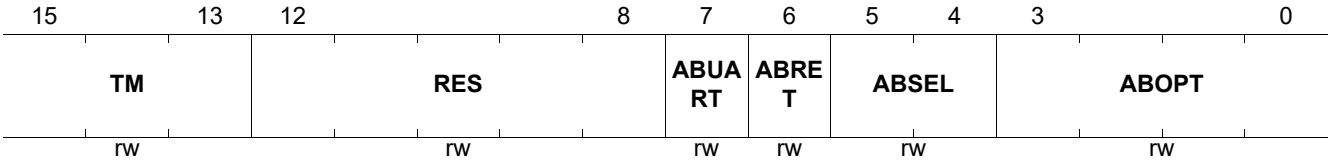
Internal Test Modes CDIAG and ABIST (Register 0.31)

This is the control register used to configure the Gigabit Ethernet behavior of the PHY. Refer to IEEE 802.3-2008 40.5.1.1.

IEEE Standard Register=0.31

PHY_TEST **Reset Value**

Internal Test Modes CDIAG and ABIST (Register 0.31) **0000_H**



Field	Bits	Type	Description
TM	15:13	RW	**Proprietary Test Modes ABIST and CDIAG** Enter the test mode. Any value different from 6 or 7 has no effect. 110_B **CDIAG** GPY-specific cable diagnostic 111_B **ABIST** GPY-specific analog built-in self-test
RES	12:8	RW	**Reserved**
ABUART	7	RW	**ABIST UART output for debug** When this bit is set to 1, it enables a detail report on the debug UART output. This is used to debug the feature and not in production mode, because in that case the two LED signals are not used to indicate completion or pass fail. An alternative to the UART output is to read the STB via MDIO commands. 0_B **NORMAL** ABIST normal output 1_B **UART** ABIST output to UART
ABRET	6	RW	**ABIST ReTrig** When this bis is set to 1, it enables a restart of the selected ABIST test. This is used to debug the feature and not in production mode. 0_B **NORMAL** Normal Mode 1_B **RETRIG** Restart the current ABIST Test.
ABSEL	5:4	RW	**ABIST Sub-mode Selection** 00_B **ANALOG** ABIST Analog Tests 01_B **DC** ABIST DC Tests 01_B **RES** Reserved 11_B **RES** Reserved

Field	Bits	Type	**Description** (cont'd)
ABOPT	3:0	RW	**ABIST Option for DC test** In ABIST DC test 0000, ABIST DC test for 10BASE-T mode LD, maximum positive differential level 0001, ABIST DC test for 1000BASE-T mode LD, maximum positive differential level 0010, ABIST DC test for 10BASE-T mode LD, 0 differential level 0011, ABIST DC test for 1000BASE-T mode LD, 0 differential level 0100, ABIST DC test for 10BASE-T mode LD, maximum negative differential level 0101, ABIST DC test for 1000BASE-T mode LD, maximum negative differential level 0110, ABIST DC test for 2.5GBASE-T mode LD, maximum positive differential level 0111, ABIST DC test for 2.5GBASE-T mode LD, 0 differential level 1000, ABIST DC test for 2.5GBASE-T mode LD, maximum negative differential level

6 MMD Registers Detailed Description

Table 26 Register Access Type

Mode	Symbol
Status Register (Status or Ability Register)	RO
Read-Write Register (MDIO Register)	RW
Read-Write Self-Clearing Register (bit is cleared after read from MDIO)	RWSC
Read-Only Self-Clearing Register (bit is cleared after read from MDIO)	ROSC

6.1 Standard PMAPMD Registers for MMD=0x01

Table 27 Registers Overview

Register Short Name	Register Long Name	Reset Value
PMA_CTRL1	PMA/PMD Control 1 (Register 1.0)	2058_H
PMA_STAT1	PMA/PMD Status 1 (Register 1.1)	0000_H
PMA_DEVID1	PHY Identifier 1 (Register 1.2)	$67C9_H$
PMA_DEVID2	PHY Identifier 2 (Register 1.3)	$DC00_H$ [1)]
PMA_SPEED_ABILITY	PMA/PMD Speed Ability (Register 1.4)	2070_H
PMA_DIP1	Devices in Package 1 (Register 1.5)	$008B_H$
PMA_DIP2	Devices in Package 2 (Register 1.6)	$C000_H$
PMA_CTL2	PMA/PMD Control 2 (Register 1.7)	0030_H
PMA_STAT2	PMA/PMD Status 2 (Register 1.8)	8200_H
PMA_EXT_ABILITY	PMA/PMD Extended Ability (Register 1.11)	$41A0_H$
PMA_PACKID1	AN Package Identifier (Register 1.14)	$67C9_H$
PMA_PACKID2	AN Package Identifier (Register 1.15)	$DC00_H$
PMA_MGBT_EXTAB	PMAPMD Extended Ability (Register 1.21)	0001_H
PMA_MGBT_STAT	MULTIGBASE-T Status (Register 1.129)	0000_H
PMA_MGBT_POLARITY	MULTIGBASE-T Pair Swap and Polarity (Register 1.130)	0003_H
PMA_MGBT_TX_PBO	MULTIGBASE-T Tx Power Backoff and PHY Short Reach Setting (Register 1.131)	0000_H
PMA_MGBT_TEST_MODE	MULTIGBASE-T Test Mode (Register 1.132)	0000_H
PMA_MGBT_SNR_OPMARGIN_A	MULTIGBASE-T SNR Margin Channel A (Register 1.133)	0000_H
PMA_MGBT_SNR_OPMARGIN_B	MULTIGBASE-T SNR Margin Channel B (Register 1.134)	0000_H
PMA_MGBT_SNR_OPMARGIN_C	MULTIGBASE-T SNR Margin Channel C (Register 1.135)	0000_H
PMA_MGBT_SNR_OPMARGIN_D	MULTIGBASE-T SNR Margin Channel D (Register 1.136)	0000_H
PMA_MGBT_MINMARGIN_A	MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137)	0000_H
PMA_MGBT_MINMARGIN_B	MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138)	0000_H
PMA_MGBT_MINMARGIN_C	MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139)	0000_H
PMA_MGBT_MINMARGIN_D	MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140)	0000_H
PMA_MGBT_POWER_A	MULTIGBASE-T Rx Power Channel A (Register 1.141)	0000_H
PMA_MGBT_POWER_B	MULTIGBASE-T Rx Power Channel B (Register 1.142)	0000_H
PMA_MGBT_POWER_C	MULTIGBASE-T Rx Power Chan C (Register 1.143)	0000_H
PMA_MGBT_POWER_D	MULTIGBASE-T Rx Power Chan D (Register 1.144)	0000_H
PMA_MGBT_SKEW_DELAY_0	MULTIGBASE-T Skew Delay 0 (Register 1.145)	0000_H
PMA_MGBT_SKEW_DELAY_1	MULTIGBASE-T Skew Delay 1 (Register 1.146)	0000_H

Table 27 Registers Overview (cont'd)

Register Short Name	Register Long Name	Reset Value
PMA_MGBT_FAST_RETRAIN_STA_CTRL	MULTIGBASE-T Skew Delay 2 (Register 1.147)	0000_H
PMA_TIMESYNC_CAP	PMA TimeSync Capability Indication (Register 1.1800)	0000_H

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

6.1.1 Standard PMAPMD Registers for MMD=0x01

This section describes all the PMAPMD registers in detail.

PMA/PMD Control 1 (Register 1.0)

IEEE Standard Register=1.0

PMA_CTRL1 **Reset Value**

PMA/PMD Control 1 (Register 1.0) **2058_H**

15	14	13	12	11	10 … 7	6	5 … 2	1	0
RST	Res	SSL	Res	LOW_POW*	Res	SSM	SPEED_SEL	NS1	NS2
rw		rw		rw		rw	rw	ro	ro

Field	Bits	Type	Description
RST	15	RW	**Reset** 1 = PMA/PMD reset 0 = Normal operation
SSL	13	RW	**Speed Selection (LSB)** Used in conjunction with field SPEED_SEL_MSB. MSB LSB: 1 1 = Bits 5:2 are used to select speed (SPEED_SEL field) 1 0 = 1000 Mbps 0 1 = 100 Mbps 0 0 = 10 Mbps
LOW_POWER	11	RW	**Low Power** 1 = Enter Low power mode 0 = Normal operation
SSM	6	RW	**Speed Selection (MSB)** Used in conjunction with field SPEED_SEL_LSB. MSB LSB: 1 1 = bits 5:2 select speed (SPEED_SEL field) 1 0 = 1000 Mbps 0 1 = 100 Mbps 0 0 = 10 Mbps

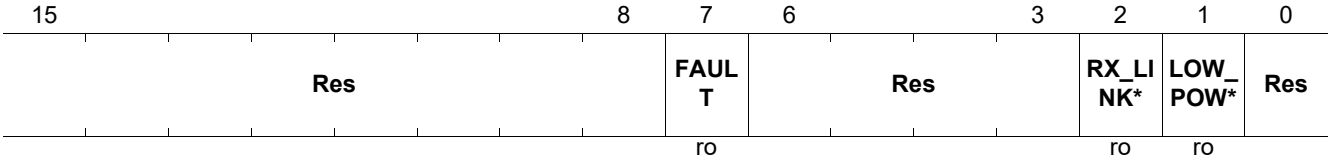
Field	Bits	Type	Description (cont'd)
SPEED_SEL	5:2	RW	**Speed Selection** Bit usage (from bit 5 to bit 2): 1 x x x = Reserved 0 1 1 1 = Not supported 0 1 1 0 = 2.5 Gbps 0 1 0 0 = Not supported, defaults to 2.5 Gbps 0 0 1 1 = Not supported, defaults to 2.5 Gbps 0 0 1 0 = Not supported, defaults to 2.5 Gbps 0 0 0 1 = Not supported, defaults to 2.5 Gbps 0 0 0 0 = Not supported, defaults to 2.5 Gbps
NS1	1	RO	**Not Supported** PMA remote loopback mode is not supported by the GPY.
NS2	0	RO	**Not Supported** PMA local loopback mode is not supported by the GPY.

PMA/PMD Status 1 (Register 1.1)

IEEE Standard Register=1.1

PMA_STAT1 **Reset Value**

PMA/PMD Status 1 (Register 1.1) **0000_H**



Field	Bits	Type	Description
FAULT	7	RO	**Fault** 1 = Fault condition detected 0 = Fault condition not detected
RX_LINK_STATUS	2	RO	**Receive Link Status** 1 = PMA/PMD receive link up 0 = PMA/PMD receive link down
LOW_POWER_ABILITY	1	RO	**Low Power Ability** 1 = PMA/PMD supports low power mode. 0 = PMA/PMD does not support low power mode.

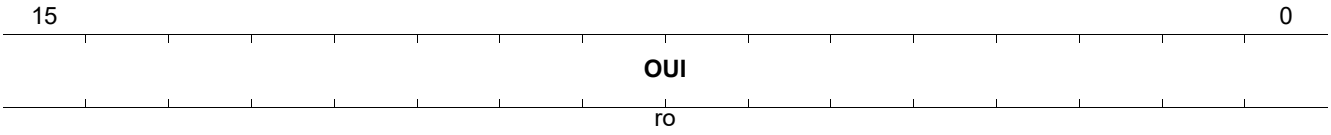
PHY Identifier 1 (Register 1.2)

IEEE Standard Register=1.2

Bits 31 - 16 of Device ID

PMA_DEVID1 **Reset Value**

PHY Identifier 1 (Register 1.2) **$67C9_H$**



Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier** Organizationally Unique Identifier Bits 3:18

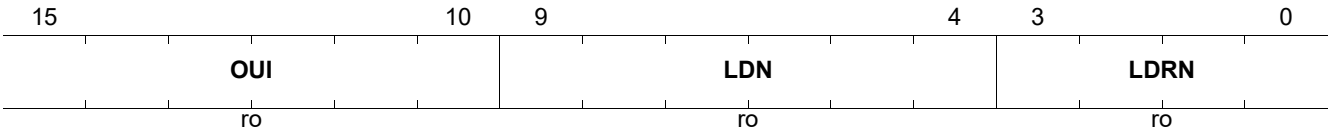
PHY Identifier 2 (Register 1.3)

IEEE Standard Register=1.3

Bits 15 - 0 of Device ID

PMA_DEVID2 **Reset Value**

PHY Identifier 2 (Register 1.3) **$DC00_H$**



Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several different products.
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number[1)] to distinguish between several versions of this device.

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

PMA/PMD Speed Ability (Register 1.4)

IEEE Standard Register=1.4

PMA_SPEED_ABILITY **Reset Value**

PMA/PMD Speed Ability (Register 1.4) **2070_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**CAP_5G**	**CAP_2G5**	**RES2**	**Res**		**CAP_100G**	**CAP_40G**	**CAP_10_***	**CAP_10M**	**CAP_100M**	**CAP_100***	**Res**	**R10PASS***	**CAP_2BA***	**CAP_10G***
	ro	ro	ro			ro	ro	ro	ro	ro	ro		ro	ro	ro

Field	Bits	Type	Description
CAP_5G	14	RO	**Not Supported** 1 = PMA/PMD is capable of operating at 5 Gbps. 0 = PMA/PMD is not capable of operating as 5 Gbps.
CAP_2G5	13	RO	**2.5 G capable** 1 = PMA/PMD is capable of operating at 2.5 Gbps. 0 = PMA/PMD is not capable of operating as 2.5 Gbps.
RES2	12	RO	**Reserved** Value always 0
CAP_100G	9	RO	**Not Supported** 1 = PMA/PMD is capable of operating at 100 Gbps. 0 = PMA/PMD is not capable of operating as 100 Gbps.
CAP_40G	8	RO	**Not Supported** 1 = PMA/PMD is capable of operating at 40 Gbps. 0 = PMA/PMD is not capable of operating as 40 Gbps.
CAP_10_1G	7	RO	**Not Supported** 1 = PMA/PMD is capable of operating at 10 Gbps downstream and 1 Gbps upstream. 0 = PMA/PMD is not capable of operating at 10 Gbps downstream and 1 Gbps upstream.
CAP_10M	6	RO	**10M capable** 1 = PMA/PMD is capable of operating at 10 Mbps. 0 = PMA/PMD is not capable of operating as 10 Mbps.
CAP_100M	5	RO	**100M capable** 1 = PMA/PMD is capable of operating at 100 Mbps. 0 = PMA/PMD is not capable of operating at 100 Mbps.
CAP_1000M	4	RO	**1000M capable** 1 = PMA/PMD is capable of operating at 1000 Mbps. 0 = PMA/PMD is not capable of operating at 1000 Mbps.
R10PASS_TS_CAPABLE	2	RO	**Not Supported** 1 = PMA/PMD is capable of operating as 10PASS-TS. 0 = PMA/PMD is not capable of operating as 10PASS-TS.

Field	Bits	Type	Description (cont'd)
CAP_2BASE_TL	1	RO	**Not Supported** 1 = PMA/PMD is capable of operating as 2BASE-TL. 0 = PMA/PMD is not capable of operating as 2BASE-TL.
CAP_10G_CAP	0	RO	**Not Supported** 1 = PMA/PMD is capable of operating at 10 Gbps. 0 = PMA/PMD is not capable of operating at 10 Gbps.

Devices in Package 1 (Register 1.5)

IEEE Standard Register=1.5

PMA_DIP1 **Reset Value**

Devices in Package 1 (Register 1.5) **$008B_H$**

15	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		SEP_PMA*	SEP_PMA*	SEP_PMA*	SEP_PMA*	ANEG	TC	DTE_XS	PHY_XS	PCS	WIS	PMD_PMA	CLAUSE_*
ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
RES	15:12	RO	**Reserved** Ignore on Read
SEP_PMA_4	11	RO	**Separate PMA (4)** 1 = Separate PMA (4) present in package. 0 = Separate PMA (4) not present in package.
SEP_PMA_3	10	RO	**Separate PMA (3)** 1 = SeparatedPMA (3) present in package. 0 = Separate PMA (3) not present in package.
SEP_PMA_2	9	RO	**Separate PMA (2)** 1 = Separate PMA (2) present in package. 0 = Separate PMA (2) not present in package.
SEP_PMA_1	8	RO	**Separate PMA (1)** 1 = Separate PMA (1) present in package. 0 = Separate PMA (1) not present in package.
ANEG	7	RO	**Auto-Negotiation Present** This bit is always set to 1 in the GPY. 1 = Auto-negotiation present in package. 0 = Auto-negotiation not present in package.
TC	6	RO	**TC Present** 1 = TC present in package. 0 = TC not present in package.
DTE_XS	5	RO	**DTE XS Present** 1 = DTE XS present in package. 0 = DTE XS not present in package.

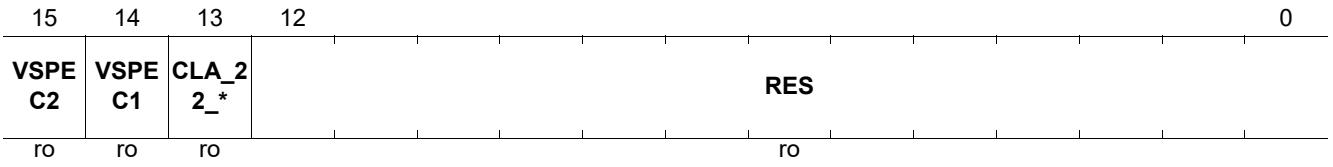
Field	Bits	Type	Description (cont'd)
PHY_XS	4	RO	**PHY XS Present** 1 = PHY XS present in package. 0 = PHY XS not present in package.
PCS	3	RO	**PCS Present** This bit is always set to 1 in the GPY. 1 = PCS present in package. 0 = PCS not present in package.
WIS	2	RO	**WIS Present** 1 = WIS present in package. 0 = WIS not present in package.
PMD_PMA	1	RO	**PMD/PMA Present** This bit is always set to 1 in the GPY. 1 = PMA/PMD present in package. 0 = PMA/PMD not present in package.
CLAUSE_22	0	RO	**Clause 22 Registers Present** This bit is always set to 1 in the GPY. 1 = Clause 22 registers present in package. 0 = Clause 22 registers not present in package.

Devices in Package 2 (Register 1.6)

IEEE Standard Register=1.6

PMA_DIP2 **Reset Value**

Devices in Package 2 (Register 1.6) **$C000_H$**



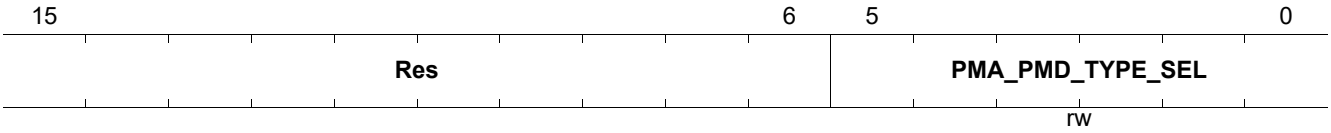
Field	Bits	Type	Description
VSPEC2	15	RO	**Vendor-specific Device 2** This bit is always set to 1 in the GPY. 1 = Vendor-specific device 2 present in package. 0 = Vendor-specific device 2 not present in package.
VSPEC1	14	RO	**Vendor-specific Device 1** This bit is always set to 1 in the GPY. 1 = Vendor-specific device 1 present in package. 0 = Vendor-specific device 1 not present in package.
CLA_22_EXT	13	RO	**Clause 22 Extension** 1 = Clause 22 extension present in package. 0 = Clause 22 extension not present in package.
RES	12:0	RO	**Reserved** Ignore on read.

PMA/PMD Control 2 (Register 1.7)

IEEE Standard Register=1.7

PMA_CTL2 **Reset Value**

PMA/PMD Control 2 (Register 1.7) **0030_H**



Field	Bits	Type	Description
PMA_PMD_TYPE_SEL	5:0	RW	**PMA/PMD Type Selection** 5 4 3 2 1 0 1 1 0 0 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 1 1 0 0 0 0 = 2.5GBASE-T PMA 1 0 1 1 x x = Unsupported, defaults to 2.5GBASE-T PMA 1 0 1 0 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 1 0 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 1 0 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 1 0 0 0 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 0 1 1 x = Unsupported, defaults to 2.5GBASE-T PMA 1 0 0 1 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 0 1 0 0 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 0 0 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 0 0 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 0 0 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 1 0 0 0 0 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 1 1 x x = Unsupported, defaults to 2.5GBASE-T PMA 0 1 1 0 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 1 0 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 1 0 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 1 0 0 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 1 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 1 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 1 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 1 0 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 0 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 0 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 0 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 1 0 0 0 0 = Unsupported, defaults to 2.5GBASE-T PMA

Field	Bits	Type	Description (cont'd)
PMA_PMD_TYPE_SEL	5:0	RW	**PMA/PMD Type Selection (cont'd)** 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 1 1 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 1 0 0 = 1000BASE-T PMA/PMD 0 0 1 0 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 0 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 0 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 1 0 0 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 1 0 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 1 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 1 0 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 0 1 = Unsupported, defaults to 2.5GBASE-T PMA 0 0 0 0 0 0 = Unsupported, defaults to 2.5GBASE-T PMA Others = Reserved

PMA/PMD Status 2 (Register 1.8)

IEEE Standard Register=1.8

PMA_STAT2 **Reset Value**

PMA/PMD Status 2 (Register 1.8) **8200_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_PRESENT		TX_FAUL*	RX_FAUL*	TX_FAULT	RX_FAULT	EXT_ABI*	PMD_TX_*	RMGBT_S*	RMGBT_L*	RMGBT_E*	RMGBT_L*	RMGBT_S*	RMGBT_L*	RMGBT_E*	PMA_LOC*
ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
DEVICE_PRESENT	15:14	RO	**Device Present** 1 0 = Device responding at this address. 1 1 = No device responding at this address. 0 1 = No device responding at this address. 0 0 = No device responding at this address.
TX_FAULT_ABILITY	13	RO	**Transmit Fault Ability** 1 = PMA/PMD has the ability to detect a fault condition on the transmit path. 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path.
RX_FAULT_ABILITY	12	RO	**Receive Fault Ability** 1 = PMA/PMD has the ability to detect a fault condition on the receive path. 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path.

Field	Bits	Type	Description (cont'd)
TX_FAULT	11	RO	**Transmit Fault** 1 = Fault condition on transmit path. 0 = No fault condition on transmit path.
RX_FAULT	10	RO	**Receive Fault** 1 = Fault condition on receive path. 0 = No fault condition on receive path.
EXT_ABILITIES	9	RO	**Extended Abilities** 1 = PMA/PMD has extended abilities listed in register 1.11. 0 = PMA/PMD does not have extended abilities.
PMD_TX_DISABLE	8	RO	**PMD Transmit Disable** 1 = PMD has the ability to disable the transmit path. 0 = PMD does not have the ability to disable the transmit path.
RMGBT_SR_ABILITY	7	RO	**MULTIGBASE-SR Ability** 1 = PMA/PMD is able to perform MULTIGBASE-SR. 0 = PMA/PMD is not able to perform MULTIGBASE-SR.
RMGBT_LR_ABILITY	6	RO	**MULTIGBASE-LR Ability** 1 = PMA/PMD is able to perform MULTIGBASE-LR. 0 = PMA/PMD is not able to perform MULTIGBASE-LR.
RMGBT_ER_ABILITY	5	RO	**MULTIGBASE-ER Ability** 1 = PMA/PMD is able to perform MULTIGBASE-ER. 0 = PMA/PMD is not able to perform MULTIGBASE-ER.
RMGBT_LX4_ABILITY	4	RO	**MULTIGBASE-LX4 Ability** 1 = PMA/PMD is able to perform MULTIGBASE-LX4. 0 = PMA/PMD is not able to perform MULTIGBASE-LX4.
RMGBT_SW_ABILITY	3	RO	**MULTIGBASE-SW Ability** 1 = PMA/PMD is able to perform MULTIGBASE-SW 0 = PMA/PMD is not able to perform MULTIGBASE-SW
RMGBT_LW_ABILITY	2	RO	**MULTIGBASE-LW Ability** 1 = PMA/PMD is able to perform MULTIGBASE-LW. 0 = PMA/PMD is not able to perform MULTIGBASE-LW.
RMGBT_EW_ABILITY	1	RO	**MULTIGBASE-EW Ability** 1 = PMA/PMD is able to perform MULTIGBASE-EW. 0 = PMA/PMD is not able to perform MULTIGBASE-EW.
PMA_LOCAL_LOOPBACK	0	RO	**PMA Local Loopback** 1 = PMA has the ability to perform a local loopback function. 0 = PMA does not have the ability to perform a local loopback function.

PMA/PMD Extended Ability (Register 1.11)

IEEE Standard Register=1.11

PMA_EXT_ABILITY **Reset Value**

PMA/PMD Extended Ability (Register 1.11) **$41A0_H$**

15	14	13	11	10	9	8	7	6	5	4	3	2	1	0
Res	**R2G5_EX***	**Res**		**R40G_10***	**P2MP_AB***	**R10BASE***	**R100BAS***	**R1000BA***	**R1000BA***	**RMGBT_K***	**RMGBT_K***	**RMGBT_A***	**RMGBT_L***	**RMGBT_C***
	ro			ro	ro	ro	ro	ro	ro	ro	ro	ro	ror	ror

Field	Bits	Type	Description
R2G5_EXT_ABILITIES	14	RO	**2.5G/5G Extended Abilities** 1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.21. 0 = PMA/PMD does not have 2.5G/5G extended abilities.
R40G_100G_EXT_ABILITIES	10	RO	**40G/100G Extended Abilities** 1 = PMA/PMD has 40G/100G extended abilities listed in register 1.13. 0 = PMA/PMD does not have 40G/100G extended abilities.
P2MP_ABILITY	9	RO	**P2MP Ability** 1 = PMA/PMD has P2MP abilities listed in register 1.12. 0 = PMA/PMD does not have P2MP abilities.
R10BASE_T_ABILITY	8	RO	**10BASE-T Ability** 1 = PMA/PMD is able to perform 10BASE-T. 0 = PMA/PMD is not able to perform 10BASE-T.
R100BASE_TX_ABILITY	7	RO	**100BASE-TX Ability** 1 = PMA/PMD is able to perform 100BASE-TX. 0 = PMA/PMD is not able to perform 100BASE-TX.
R1000BASE_KX_ABILITY	6	RO	**1000BASE-KX Ability** 1 = PMA/PMD is able to perform 1000BASE-KX. 0 = PMA/PMD is not able to perform 1000BASE-KX.
R1000BASE_T_ABILITY	5	RO	**1000BASE-T Ability** 1 = PMA/PMD is able to perform 1000BASE-T. 0 = PMA/PMD is not able to perform 1000BASE-T.
RMGBT_KR_ABILITY	4	RO	**MULTIGBASE-KR Ability** 1 = PMA/PMD is able to perform MULTIGBASE-KR. 0 = PMA/PMD is not able to perform MULTIGBASE-KR.
RMGBT_KX4_ABILITY	3	RO	**MULTIGBASE-KX4 Ability** 1 = PMA/PMD is able to perform MULTIGBASE-KX4. 0 = PMA/PMD is not able to perform MULTIGBASE-KX4.
RMGBT_ABILITY	2	RO	**10GBASE-T Ability** 1 = PMA/PMD is able to perform MULTIGBASE-T. 0 = PMA/PMD is not able to perform MULTIGBASE-T.
RMGBT_LRM_ABILITY	1	ROR	**MULTIGBASE-LRM Ability** 1 = PMA/PMD is able to perform MULTIGBASE-LRM. 0 = PMA/PMD is not able to perform MULTIGBASE-LRM.

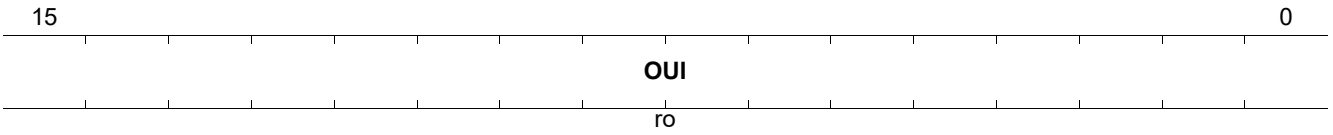
Field	Bits	Type	Description (cont'd)
RMGBT_CX4_ABILITY	0	ROR	**MULTIGBASE-CX4 Ability** 1 = PMA/PMD is able to perform MULTIGBASE-CX4. 0 = PMA/PMD is not able to perform MULTIGBASE-CX4.

AN Package Identifier (Register 1.14)

IEEE Standard Register=1.14

PMA_PACKID1 **Reset Value**

AN Package Identifier (Register 1.14) **$67C9_H$**



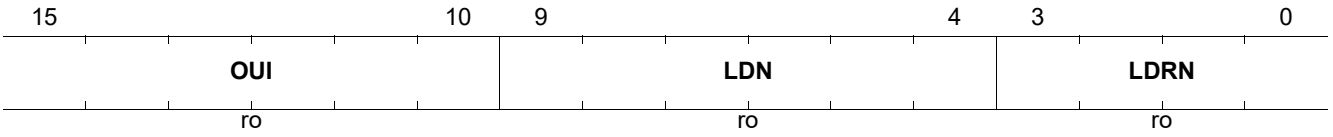
Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier** Organizationally Unique Identifier Bits 3:18

AN Package Identifier (Register 1.15)

IEEE Standard Register=1.15

PMA_PACKID2 **Reset Value**

AN Package Identifier (Register 1.15) **$DC00_H$**



Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several different products.
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number[1)] to distinguish between several versions of this device.

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

PMAPMD Extended Ability (Register 1.21)

Read only, write from STA has no effect

IEEE Standard Register=1.21

PMA_MGBT_EXTAB **Reset Value**

PMAPMD Extended Ability (Register 1.21) **0001_H**

Field	Bits	Type	Description
RES	15:2	RO	**Reserved** Value always 0
AB5G	1	RO	**PMA Ability to Perform 5GBASE-T** 0_B **UNABLE** PMA is not able to perform 5GBASE-T. 1_B **ABLE** PMA Able to perform 5GBASE-T.
AB2G5	0	RO	**PMA Ability to Perform 2.5GBASE-T** 0_B **UNABLE** PMA is not able to perform 2.5GBASE-T. 1_B **ABLE** PMA Able to perform 2.5GBASE-T.

MULTIGBASE-T Status (Register 1.129)

IEEE Standard Register=1.129

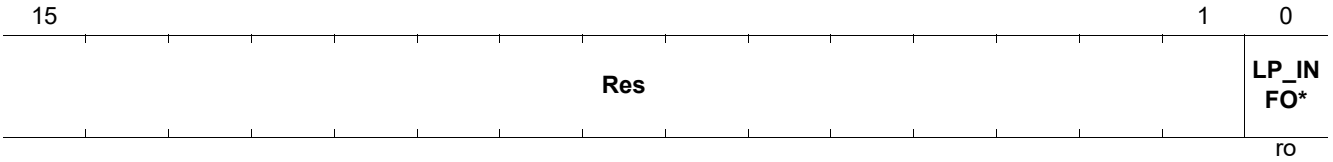
Indicates startup in 126.4.2.5 for 2.5G has been completed.

When read as a 1, indicates that the startup protocol defined in 126.4.2.5 (for 2.5G/5GBASE-T) has been completed (link_status=OK, pcs_status = OK), and that the contents of bits 1.130.11:0 (Polarity), 1.131.15:10 (PBO), 1.145.14:8 (Skew), 1.146.14:8, and 1.146.6:0 (Skew), which are established during the startup protocol, are valid.

When read as a zero, bit 1.129.0 indicates that the startup process has not been completed, and that the contents of these bits that are established during the startup protocol are invalid. A PMA must return a value of zero in bit 1.129.1 when the PMA link_status=FAIL.

PMA_MGBT_STAT **Reset Value**

MULTIGBASE-T Status (Register 1.129) **0000_H**



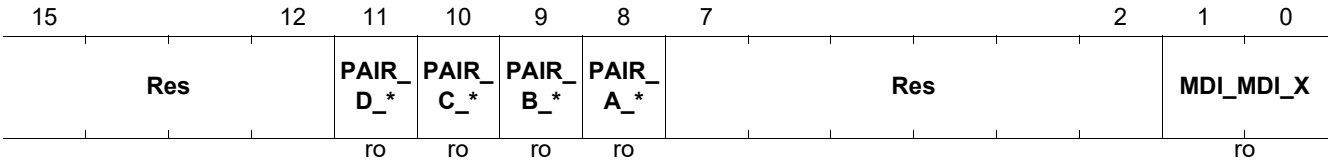
Field	Bits	Type	Description
LP_INFORMATION_VALID	0	RO	**LP Information Valid** When set this bit indicates the startup protocol (126.4.2.5) has completed. 1 = Link partner information is valid 0 = Link partner information is invalid

MULTIGBASE-T Pair Swap and Polarity (Register 1.130)

IEEE Standard Register=1.130

PMA_MGBT_POLARITY **Reset Value**

MULTIGBASE-T Pair Swap and Polarity (Register 1.130) **0003_H**



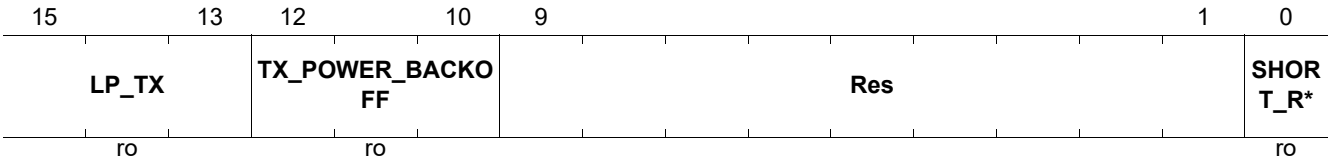
Field	Bits	Type	Description
PAIR_D_POLARITY	11	RO	**Pair D Polarity** 1 = Polarity of pair D is reversed. 0 = Polarity of pair D is not reversed.
PAIR_C_POLARITY	10	RO	**Pair C Polarity** 1 = Polarity of pair C is reversed. 0 = Polarity of pair C is not reversed.
PAIR_B_POLARITY	9	RO	**Pair B Polarity** 1 = Polarity of pair B is reversed. 0 = Polarity of pair B is not reversed.
PAIR_A_POLARITY	8	RO	**Pair A Polarity** 1 = Polarity of pair A is reversed. 0 = Polarity of pair A is not reversed.
MDI_MDI_X	1:0	RO	**MDI/MDI-X** Indicates the status of pair swaps at the MDI / MD-X. 00_B **ABCDCROSS** Pair AB and Pair CD crossover 01_B **CDCROSS** Pair CD crossover only 10_B **ABCROSS** Pair AB crossover only 11_B **NORMAL** No crossover

MULTIGBASE-T TX Power Backoff and PHY Short Reach Setting (Register 1.131)

IEEE Standard Register=1.131

PMA_MGBT_TX_PBO **Reset Value**

MULTIGBASE-T TX Power Backoff and PHY Short Reach Setting (Register 1.131) **0000_H**



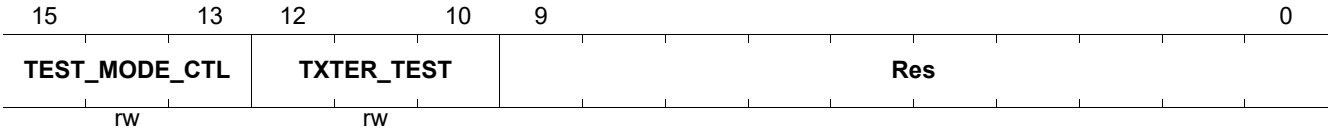
Field	Bits	Type	Description
LP_TX	15:13	RO	**Link Partner TX** The power backoff setting of the link partner. Bit number assignment: 15 14 13 ---------- 1 1 1 = 14 dB 1 1 0 = 12 dB 1 0 1 = 10 dB 1 0 0 = 8 dB 0 1 1 = 6 dB 0 1 0 = 4 dB 0 0 1 = 2 dB 0 0 0 = 0 dB
TX_POWER_BACKOFF	12:10	RO	**TX Power Backoff** The power backoff of PHY211 PMA. Bit number assignment: 12 11 10 ---------- 1 1 1 = 14 dB 1 1 0 = 12 dB 1 0 1 = 10 dB 1 0 0 = 8 dB 0 1 1 = 6 dB 0 1 0 = 4 dB 0 0 1 = 2 dB 0 0 0 = 0 dB
SHORT_REACH_MODE	0	RO	**Short Reach Mode** 1 = PHY is operating in short reach mode (not supported). 0 = PHY is not operating in short reach mode.

MULTIGBASE-T Test Mode (Register 1.132)

IEEE Standard Register=1.132

PMA_MGBT_TEST_MODE **Reset Value**

MULTIGBASE-T Test Mode (Register 1.132) **0000_H**



Field	Bits	Type	Description
TEST_MODE_CTL	15:13	RW	**Test Mode Control** 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal operation
TXTER_TEST	12:10	RW	**Transmitter Test** Frequencies for tones used in Test Mode 4. 1 1 1 = Reserved 1 1 0 = Dual tone 5 1 0 1 = Dual tone 4 1 0 0 = Dual tone 3 0 1 1 = Reserved 0 1 0 = Dual tone 2 0 0 1 = Dual tone 1 0 0 0 = Reserved

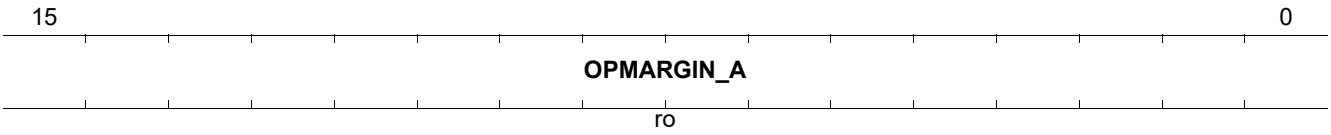
MULTIGBASE-T SNR Margin Channel A (Register 1.133)

Register 1.133 contains the current SNR operating margin measured at the slicer input for channel A for the MULTIGBASE-T PMA.

IEEE Standard Register=1.133

PMA_MGBT_SNR_OPMARGIN_A **Reset Value**

MULTIGBASE-T SNR Margin Channel A (Register 1.133) **0000_H**



Field	Bits	Type	Description
OPMARGIN_A	15:0	RO	**OPMARGIN_A** SNR operating margin measured at the slicer input for channel A.

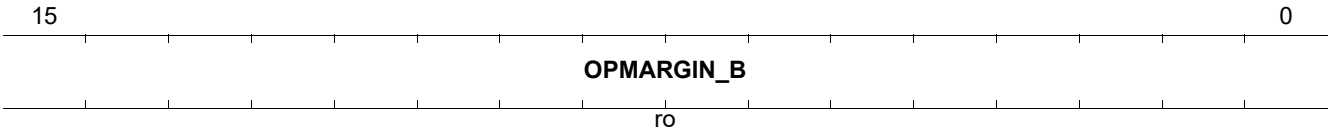
MULTIGBASE-T SNR Margin Channel B (Register 1.134)

Register 1.134 contains the current SNR operating margin measured at the slicer input for channel B for the MULTIGBASE-T PMA.

IEEE Standard Register=1.134

PMA_MGBT_SNR_OPMARGIN_B **Reset Value**

MULTIGBASE-T SNR Margin Channel B (Register 1.134) **0000_H**



Field	Bits	Type	Description
OPMARGIN_B	15:0	RO	**OPMARGIN_B** SNR operating margin measured at the slicer input for channel B.

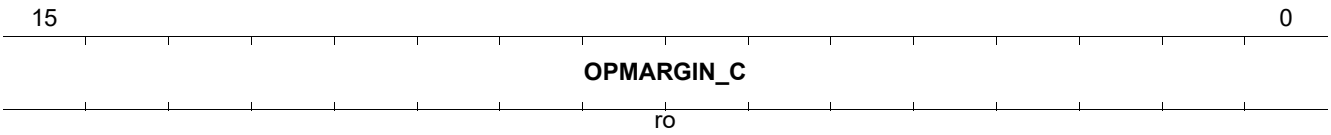
MULTIGBASE-T SNR Margin Channel C (Register 1.135)

Register 1.135 contains the current SNR operating margin measured at the slicer input for channel C for the MULTIGBASE-T PMA.

IEEE Standard Register=1.135

PMA_MGBT_SNR_OPMARGIN_C **Reset Value**

MULTIGBASE-T SNR Margin Channel C (Register 1.135) **0000_H**



Field	Bits	Type	Description
OPMARGIN_C	15:0	RO	**OPMARGIN_C** SNR operating margin measured at the slicer input for channel C.

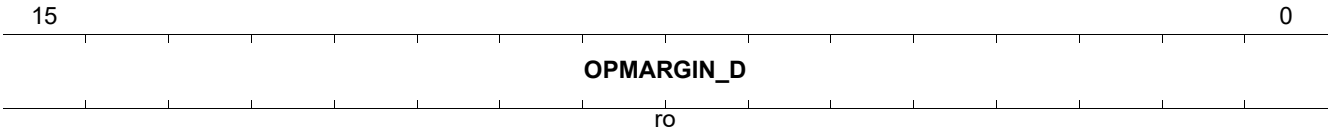
MULTIGBASE-T SNR Margin Channel D (Register 1.136)

Register 1.136 contains the current SNR operating margin measured at the slicer input for channel D for the MULTIGBASE-T PMA.

IEEE Standard Register=1.136

PMA_MGBT_SNR_OPMARGIN_D **Reset Value**

MULTIGBASE-T SNR Margin Channel D (Register 1.136) **0000_H**



Field	Bits	Type	Description
OPMARGIN_D	15:0	RO	**OPMARGIN_D** SNR operating margin measured at the slicer input for channel D.

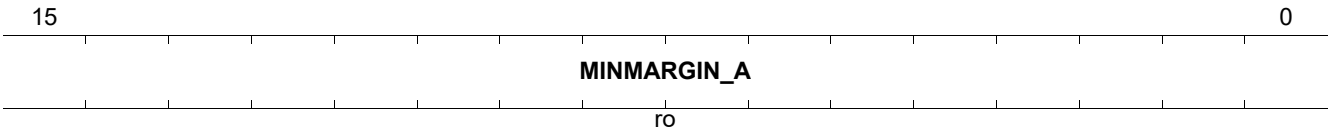
MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel A register (1.133) since the last read.

IEEE Standard Register=1.137

PMA_MGBT_MINMARGIN_A **Reset Value**

MULTIGBASE-T SNR Minimum Margin Channel A (Register 1.137) **0000_H**



Field	Bits	Type	Description
MINMARGIN_A	15:0	RO	**MINMARGIN_A** Lowest value observed in the SNR operating margin channel A register (1.133) since the last read.

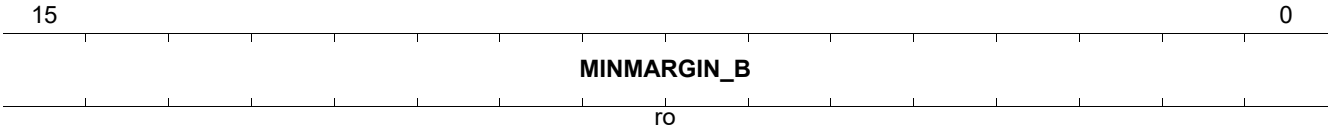
MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138)

The minimum margin channel A register contains a latched copy of the lowest value observed in the SNR operating margin channel B register (1.134) since the last read.

IEEE Standard Register=1.138

PMA_MGBT_MINMARGIN_B **Reset Value**

MULTIGBASE-T SNR Minimum Margin Channel B (Register 1.138) **0000_H**



Field	Bits	Type	Description
MINMARGIN_B	15:0	RO	**MINMARGIN_B** Lowest value observed in the SNR operating margin channel B register (1.134) since the last read.

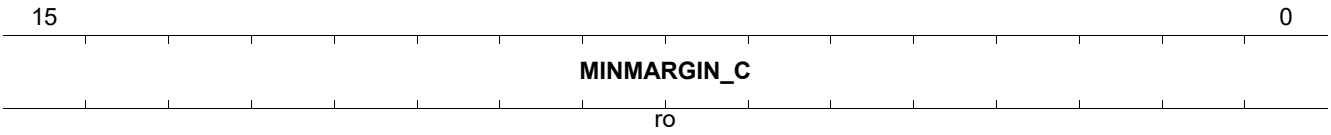
MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139)

The minimum margin channel C register contains a latched copy of the lowest value observed in the SNR operating margin channel C register (1.135) since the last read.

IEEE Standard Register=1.139

PMA_MGBT_MINMARGIN_C **Reset Value**

MULTIGBASE-T SNR Minimum Margin Chan C (Register 1.139) **0000_H**



Field	Bits	Type	Description
MINMARGIN_C	15:0	RO	**MINMARGIN_C** Lowest value observed in the SNR operating margin channel C register (1.135) since the last read.

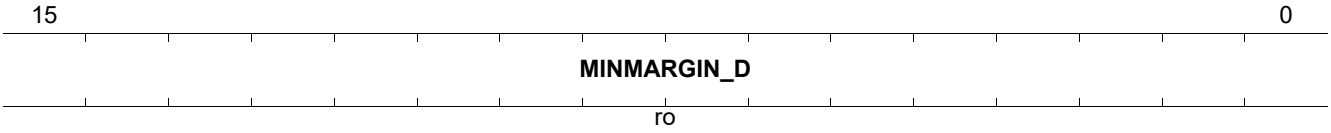
MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140)

The Minimum margin channel D register contains a latched copy of the lowest value observed in the SNR operating margin channel D register (1.136) since the last read.

IEEE Standard Register=1.140

PMA_MGBT_MINMARGIN_D **Reset Value**

MULTIGBASE-T SNR Minimum Margin Chan D (Register 1.140) **0000_H**



Field	Bits	Type	Description
MINMARGIN_D	15:0	RO	**MINMARGIN_D** Lowest value observed in the SNR operating margin channel D register (1.136) since the last read

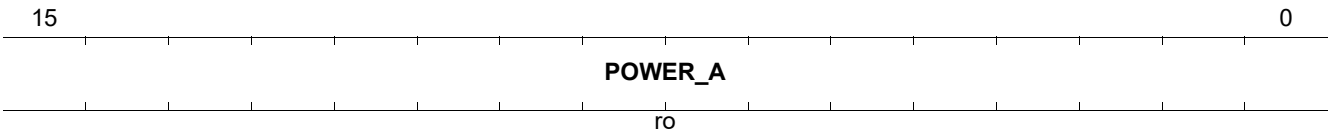
MULTIGBASE-T Rx Power Channel A (Register 1.141)

The Rx signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.141

PMA_MGBT_POWER_A **Reset Value**

MULTIGBASE-T Rx Power Channel A (Register 1.141) **0000_H**



Field	Bits	Type	Description
POWER_A	15:0	RO	**POWER_A** Receive signal power measured at the MDI during training.

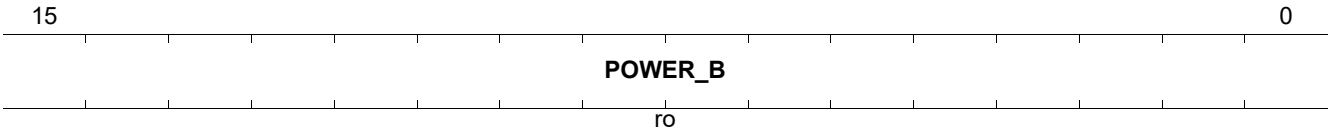
MULTIGBASE-T Rx Power Channel B (Register 1.142)

The Rx signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.142

PMA_MGBT_POWER_B **Reset Value**

MULTIGBASE-T Rx Power Channel B (Register 1.142) **0000_H**



Field	Bits	Type	Description
POWER_B	15:0	RO	**POWER_B** Receive signal power measured at the MDI during training.

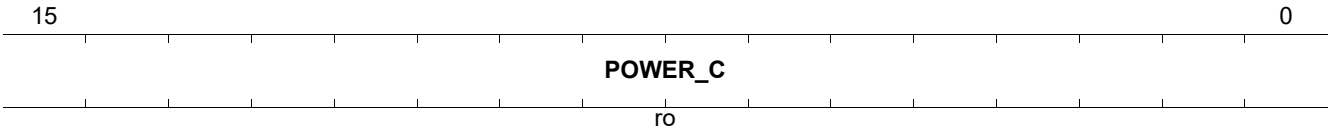
MULTIGBASE-T Rx Power Chan C (Register 1.143)

The Rx signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.143

PMA_MGBT_POWER_C **Reset Value**

MULTIGBASE-T Rx Power Chan C (Register 1.143) **0000_H**



Field	Bits	Type	Description
POWER_C	15:0	RO	**POWER_C** Receive signal power measured at the MDI during training.

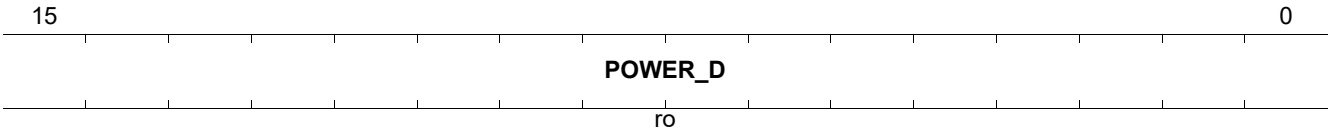
MULTIGBASE-T Rx Power Chan D (Register 1.144)

The Rx signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1.

IEEE Standard Register=1.144

PMA_MGBT_POWER_D **Reset Value**

MULTIGBASE-T Rx Power Chan D (Register 1.144) **0000_H**



Field	Bits	Type	Description
POWER_D	15:0	RO	**POWER_D** Receive signal power measured at the MDI during training.

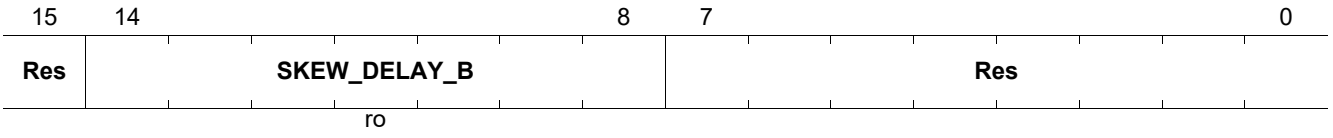
MULTIGBASE-T Skew Delay 0 (Register 1.145)

IEEE Standard Register=1.145

The skew delay reports the current skew delay on each of the pairs with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two’s complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. When the delay exceeds the maximum amount represented by the range -80 ns to +78.75 ns, the field displays the maximum value.

PMA_MGBT_SKEW_DELAY_0 **Reset Value**

MULTIGBASE-T Skew Delay 0 (Register 1.145) **0000_H**



Field	Bits	Type	Description
SKEW_DELAY_B	14:8	RO	**Skew Delay B** Skew delay for pair B.

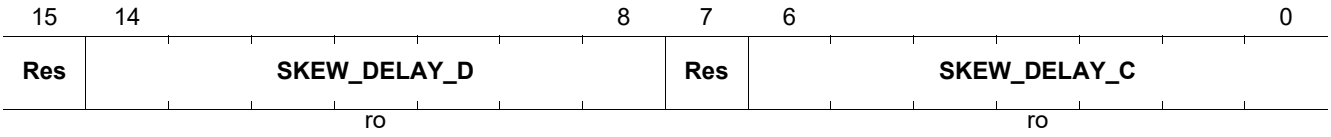
MULTIGBASE-T Skew Delay 1 (Register 1.146)

IEEE Standard Register=1.146

The skew delay reports the current skew delay on each of the pairs with respect to physical pair A. It is reported with 1.25 ns resolution to an accuracy of 2.5 ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. When the delay exceeds the maximum amount represented by the range -80 ns to +78.75 ns, the field displays the maximum value.

PMA_MGBT_SKEW_DELAY_1 **Reset Value**

MULTIGBASE-T Skew Delay 1 (Register 1.146) **0000_H**



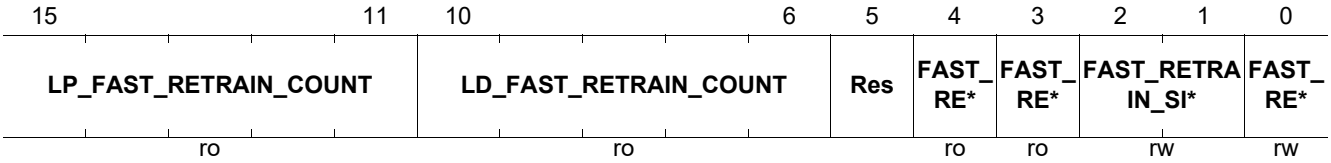
Field	Bits	Type	Description
SKEW_DELAY_D	14:8	RO	**Skew Delay D** Skew delay for pair D.
SKEW_DELAY_C	6:0	RO	**Skew Delay C** Skew delay for pair C.

MULTIGBASE-T Skew Delay 2 (Register 1.147)

IEEE Standard Register=1.147

PMA_MGBT_FAST_RETRAIN_STA_CTRL **Reset Value**

MULTIGBASE-T Skew Delay 2 (Register 1.147) **0000_H**



Field	Bits	Type	Description
LP_FAST_RETRAIN_COUNT	15:11	RO	**LP Fast Retrain Count** Counts the number of fast retrains requested by the link partner.
LD_FAST_RETRAIN_COUNT	10:6	RO	**LD Fast Retrain Count** Counts the number of fast retrains requested by the local device.
FAST_RETRAIN_ABILITY	4	RO	**Fast Retrain Ability** 1 = Fast retrain capability is supported. 0 = Fast retrain capability is not supported.

Field	Bits	Type	Description (cont'd)
FAST_RETRAIN_NEGOTIATED	3	RO	**Fast Retrain Negotiated** 1 = Fast retrain capability was negotiated. 0 = Fast retrain capability was not negotiated.
FAST_RETRAIN_SIG_TYPE	2:1	RW	**Fast Retrain Signal Type** 11 = Reserved 10 = PHY signals Link Interruption during fast retrain. 01 = PHY signals Local Fault during fast retrain. 00 = PHY signals IDLE during fast retrain.
FAST_RETRAIN_ENABLE	0	RW	**Fast Retrain Enable** 1 = Fast retrain capability is enabled. 0 = Fast retrain capability is disabled.

PMA TimeSync Capability Indication (Register 1.1800)

PMA TimeSync Capability indication register.

GPY does not support providing data path delay information.

IEEE Standard Register=1.1800

PMA_TIMESYNC_CAP **Reset Value**

PMA TimeSync Capability Indication (Register 1.1800) **0000_H**

Field	Bits	Type	Description
TXDEL	1	RO	**Transmit Data Path Delay Information** Not supported by the GPY. 0_B **NONE** PHYs do not have this capability. 1_B **CAPABLE** Minimum and maximum Tx data path delay available.
RXDEL	0	RO	**Receive Data Path Delay Information** Not supported by the GPY. 0_B **NONE** PHYs do not have this capability. 1_B **CAPABLE** Minimum and maximum Rx data path delay available.

6.2 Standard PCS Registers for MMD=0x03

This section describes the PCS registers for MMD device 0x03.

Table 28 Registers Overview

Register Short Name	Register Long Name	Reset Value
PCS_CTRL1	PCS Control 1 (Register 3.0)	$205C_H$
PCS_STAT1	PCS Status 1 (Register 3.1)	0000_H
PCS_DEVID1	PHY Identifier 1 (Register 3.2)	$67C9_H$
PCS_DEVID2	PHY Identifier 2 (Register 3.3)	$DC00_H$ 1)
PCS_SPEED_ABILITY	PCS Speed Ability (Register 3.4)	0040_H
PCS_DIP1	PCS Devices in Package 1 (Register 3.5)	$008B_H$
PCS_DIP2	PCS Devices in Package 2 (Register 3.6)	$C000_H$
PCS_CTRL2	PCS Control 2 (Register 3.7)	$000A_H$
PCS_STAT2	PCS Status 2 (Register 3.8)	9000_H
PCS_PACKID1	PCS Package Identifier 1 (Register 3.14)	$67C9_H$
PCS_PACKID2	PCS Package Identifier 2 (Register 3.15)	$DC00_H$
PCS_EEE_CAP	PCS EEE Capability (Register 3.20)	0006_H
PCS_EEE_CAP2	EEE Control and Capability 2 (Register 3.21)	0001_H
PCS_EEE_WAKERR	PCS EEE Status Register 1 (Register 3.22)	0000_H
PCS_2G5_STAT1	BASE-R and 10GBASE-T PCS Status 1 (Register 3.32)	0000_H
PCS_2G5_STAT2	MULTIGBASE-T PCS Status 2 (Register 3.33)	0000_H
PCS_TIMESYNC_CAP	PCS TimeSync Capability Register (Register 3.1800)	0000_H

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

6.2.1 Standard PCS Registers for MMD=0x03

This section describes all the PCS registers in detail.

PCS Control 1 (Register 3.0)

IEEE Standard Register=3.0

PCS_CTRL1 **Reset Value**

PCS Control 1 (Register 3.0) **$205C_H$**

15	14	13	12	11	10	9 … 7	6	5 … 2	1	0
RST	LOOP BACK	SSL	Res	LOW_ POW*	RXCK ST	Res	SSM	SPEED_SEL	Res	
rw	rw	rw		rw	rw		rw	rw		

Field	Bits	Type	Description
RST	15	RW	**Reset** 1 = PCS reset - Self Clearing 0 = Normal operation
LOOPBACK	14	RW	**Loopback** 1 = Enable loopback mode. 0 = Disable loopback mode.
SSL	13	RW	**Forced Speed Selection (LSB)** This bit is used in conjunction with SPEED_SEL_LSB MSB LSB 1 1 = Bits 5:2 select speed 1 0 = 1000 Mbps 0 1 = 100 Mbps 0 0 = 10 Mbps
LOW_POWER	11	RW	**Low Power** 1 = Low-power mode 0 = Normal operation
RXCKST	10	RW	**Clock Stop Enable** The MAC sets this bit to active to allow the GPY to stop the clocking during the LPI_MODE. 1 = The GPY stops the (X)GMII clock during LPI. 0 = Clock not stoppable.
SSM	6	RW	**Forced Speed Selection (MSB)** This bit is used in conjunction with SPEED_SEL_MSB. MSB LSB 1 1 = bits 5:2 select speed 1 0 = 1000 Mbps 0 1 = 100 Mbps 0 0 = 10 Mbps
SPEED_SEL	5:2	RW	**Forced Speed Selection Values** 1 1 x x = Reserved 0 1 1 1 = 2.5 Gbps 0 1 0 1 = Reserved 0 1 0 0 = Unsupported, defaults to 2.5 Gbps 0 0 1 1 = Unsupported, defaults to 2.5 Gbps 0 0 1 0 = Unsupported, defaults to 2.5 Gbps 0 0 0 1 = Unsupported, defaults to 2.5 Gbps 0 0 0 0 = Unsupported, defaults to 2.5 Gbps

PCS Status 1 (Register 3.1)

IEEE Standard Register=3.1

PCS_STAT1 **Reset Value**

PCS Status 1 (Register 3.1) **0000_H**

15	12	11	10	9	8	7	6	5	3	2	1	0
Res		TX_LPI_*	RX_LPI_*	TX_LPI_*	RX_LPI_*	FAULT	TXCKST	Res		PCS_RX_*	LOW_POW*	Res
		ro	ro	ro	ro	ro	ro			ro	ro	

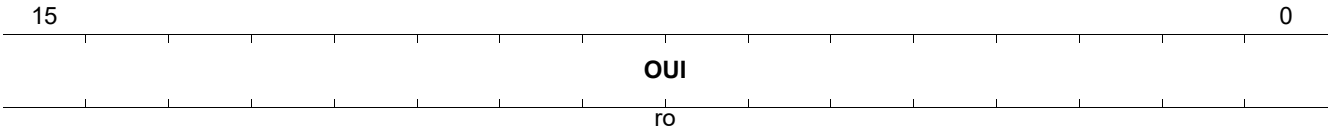
Field	Bits	Type	Description
TX_LPI_RXD	11	RO	**Tx LPI Received** 1 = Tx PCS received LPI. 0 = LPI not received.
RX_LPI_RXD	10	RO	**Rx LPI Received** 1 = Rx PCS received LPI. 0 = LPI not received.
TX_LPI_INDICATION	9	RO	**Tx LPI Indication** 1 = Tx PCS is currently receiving LPI. 0 = PCS is not currently receiving LPI.
RX_LPI_INDICATION	8	RO	**Rx LPI Indication** 1 = Rx PCS is currently receiving LPI. 0 = PCS is not currently receiving LPI.
FAULT	7	RO	**Fault** 1 = Fault condition detected. 0 = No fault condition detected.
TXCKST	6	RO	**Clock Stop Capable** 1 = The MAC is allowed to stop the clock during LPI. 0 = Clock not stoppable.
PCS_RX_LINK_STATUS	2	RO	**PCS Receive Link Status** 1 = PCS receive link up. 0 = PCS receive link down.
LOW_POWER_ABILITY	1	RO	**Low Power Ability** 1 = PCS supports low power mode. 0 = PCS does not support low power mode.

PHY Identifier 1 (Register 3.2)

IEEE Standard Register=3.2

PCS_DEVID1 **Reset Value**

PHY Identifier 1 (Register 3.2) **$67C9_H$**



Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18**

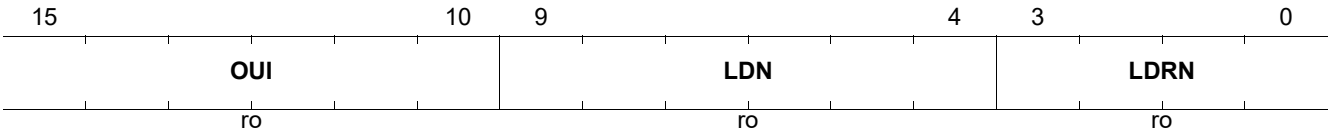
PHY Identifier 2 (Register 3.3)

Organizationally Unique Identifier Bits 19:24

IEEE Standard Register=3.3

PCS_DEVID2 **Reset Value**

PHY Identifier 2 (Register 3.3) **$DC00_H$**



Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several different products.
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number[1)] to distinguish between several versions of this device.

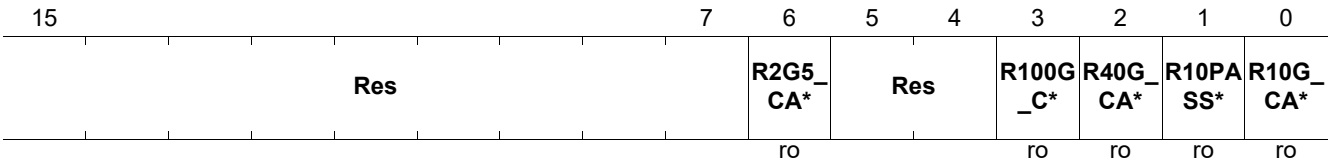
1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

PCS Speed Ability (Register 3.4)

IEEE Standard Register=3.4

PCS_SPEED_ABILITY **Reset Value**

PCS Speed Ability (Register 3.4) **0040_H**



Field	Bits	Type	Description
R2G5_CAPABLE	6	RO	**2G5 Capable** This bit is always set to 1 because the PCS is capable of operating at 2.5 Gbps.
R100G_CAPABLE	3	RO	**100G Capable** 1 = PCS is capable of operating at 100 Gbps. 0 = PCS is not capable of operating at 100 Gbps.
R40G_CAPABLE	2	RO	**40G Capable** 1 = PCS is capable of operating at 40 Gbps. 0 = PCS is not capable of operating at 40 Gbps.
R10PASS_TS_2BASE_TL	1	RO	**10PASS-TS/2BASE-TL Capable** 1 = PCS is capable of operating as the 10P/2B PCS. 0 = PCS is not capable of operating as the 10P/2B PCS.
R10G_CAPABLE	0	RO	**10G Capable** 1 = PCS is capable of operating at 10 Gbps. 0 = PCS is not capable of operating at 10 Gbps.

PCS Devices in Package 1 (Register 3.5)

IEEE Standard Register=3.5

PCS_DIP1 **Reset Value**

PCS Devices in Package 1 (Register 3.5) **$008B_H$**

15	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		SEPARAT*	SEP_PMA*	SEPARAT*	SEPARAT*	ANEG	TC	DTE_XS	PHY_XS	PCS	WIS_PRE*	PMD_PMA	CL22
ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
RES	15:12	RO	**Reserved** Ignore on read.
SEPARATED_PMA_4	11	RO	**Separate PMA (4)** 1 = Separate PMA (4) present in package.
SEP_PMA_3	10	RO	**Separate PMA (3)** 1 = Separate PMA (3) present in package. 0 = Separate PMA (3) not present in package.
SEPARATED_PMA_2	9	RO	**Separate PMA (2)** 1 = Separate PMA (2) present in package present. 0 = Separate PMA (2) not present in package.
SEPARATED_PMA_1	8	RO	**Separate PMA (1)** 1 = Separate PMA (1) present in package present. 0 = Separate PMA (1) not present in package.
ANEG	7	RO	**Auto-Negotiation Present** 1 = Auto-negotiation present in package. 0 = Auto-negotiation not present in package.
TC	6	RO	**TC Present** 1 = TC present in package. 0 = TC not present in package.
DTE_XS	5	RO	**DTE XS Present** 1 = DTE XS present in package. 0 = DTE XS not present in package.
PHY_XS	4	RO	**PHY XS Present** 1 = PHY XS present in package. 0 = PHY XS not present in package.
PCS	3	RO	**PCS Present** 1 = PCS present in package. 0 = PCS not present in package.
WIS_PRESENT	2	RO	**WIS Present** 1 = WIS present in package. 0 = WIS not present in package.

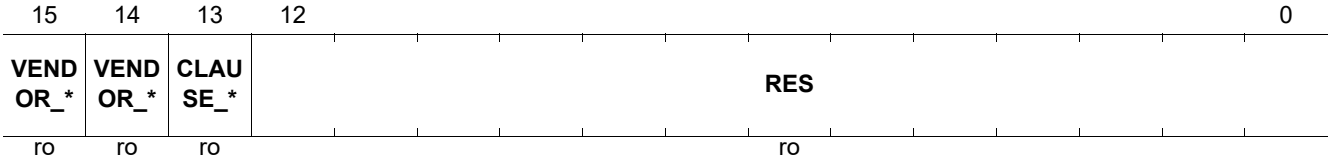
Field	Bits	Type	Description (cont'd)
PMD_PMA	1	RO	**PMD/PMA Present** 1 = PMA/PMD present in package. 0 = PMA/PMD not present in package.
CL22	0	RO	**Clause 22 Registers Present** 1 = Clause 22 registers present in package. 0 = Clause 22 registers not present in package.

PCS Devices in Package 2 (Register 3.6)

IEEE Standard Register=3.6

PCS_DIP2 **Reset Value**

PCS Devices in Package 2 (Register 3.6) **$C000_H$**



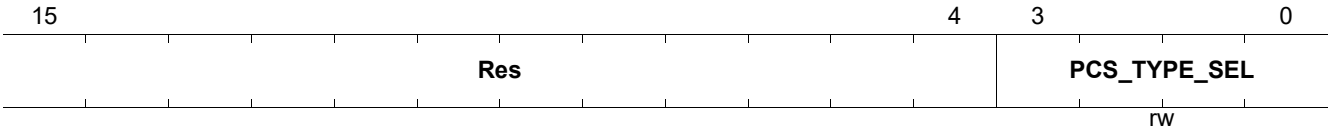
Field	Bits	Type	Description
VENDOR_SPECIFIC_DEVICE_2	15	RO	**Vendor-specific Device 2** 1 = Vendor-specific device 2 present in package. 0 = Vendor-specific device 2 not present in package.
VENDOR_SPECIFIC_DEVICE_1	14	RO	**Vendor-specific Device 1** 1 = Vendor-specific device 1 present in package. 0 = Vendor-specific device 1 not present in package.
CLAUSE_22_EXTENSION	13	RO	**Clause 22 Extension** 1 = Clause 22 extension present in package. 0 = Clause 22 extension not present in package.
RES	12:0	RO	**Reserved** Ignore on read.

PCS Control 2 (Register 3.7)

IEEE Standard Register=3.7

PCS_CTRL2 **Reset Value**

PCS Control 2 (Register 3.7) **$000A_H$**



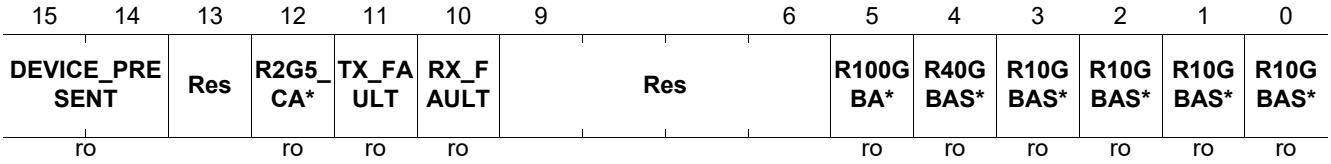
Field	Bits	Type	Description
PCS_TYPE_SEL	3:0	RW	**PCS Type Selection** 1 0 1 1 = Not supported, defaults to 2.5 Gbps 1 0 1 1 = Select 2.5 Gbps PCS type (Default) 0 1 0 1 Not supported, defaults to 2.5 Gbps 0 1 0 0 Not supported, defaults to 2.5 Gbps 0 0 1 1 Not supported, defaults to 2.5 Gbps 0 0 1 0 Not supported, defaults to 2.5 Gbps 0 0 0 1 Not supported, defaults to 2.5 Gbps 0 0 0 0 Not supported, defaults to 2.5 Gbps

PCS Status 2 (Register 3.8)

IEEE Standard Register=3.8

PCS_STAT2 **Reset Value**

PCS Status 2 (Register 3.8) **9000_H**



Field	Bits	Type	Description
DEVICE_PRESENT	15:14	RO	**Device Present** 1 0 = Device responding at this address. 1 1 = No device responding at this address. 0 1 = No device responding at this address. 0 0 = No device responding at this address.
R2G5_CAPABLE	12	RO	**2G5BASE-T Capable** 1 = PCS is able to support 2.5GBASE-T PCS type. 0 = PCS is not able to support 2.5GBASE-T.
TX_FAULT	11	RO	**Transmit Fault** 1 = Fault condition on transmit path. 0 = No fault condition on transmit path.

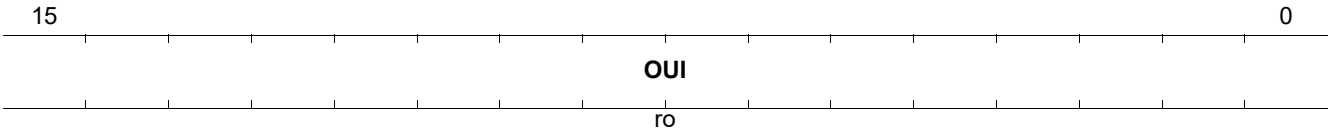
Field	Bits	Type	Description (cont'd)
RX_FAULT	10	RO	**Receive Fault** 1 = Fault condition on the receive path. 0 = No fault condition on the receive path.
R100GBASE_R_CAPABLE	5	RO	**100GBASE-R Capable** 1 = PCS is able to support 100GBASE-R PCS type. 0 = PCS is not able to support 100GBASE-R PCS type.
R40GBASE_R_CAPABLE	4	RO	**40GBASE-R Capable** 1 = PCS is able to support 40GBASE-R PCS type. 0 = PCS is not able to support 40GBASE-R PCS type.
R10GBASE_T_CAPABLE	3	RO	**10GBASE-T Capable** 1 = PCS is able to support 10GBASE-T PCS type. 0 = PCS is not able to support 10GBASE-T PCS type.
R10GBASE_W_CAPABLE	2	RO	**10GBASE-W Capable** 1 = PCS is able to support 10GBASE-W PCS type. 0 = PCS is not able to support 10GBASE-W PCS type.
R10GBASE_X_CAPABLE	1	RO	**10GBASE-X Capable** 1 = PCS is able to support 10GBASE-X PCS type. 0 = PCS is not able to support 10GBASE-X PCS type.
R10GBASE_R_CAPABLE	0	RO	**10GBASE-R Capable** 1 = PCS is able to support 10GBASE-R PCS types. 0 = PCS is not able to support 10GBASE-R PCS types.

PCS Package Identifier 1 (Register 3.14)

IEEE Standard Register=3.14

PCS_PACKID1 **Reset Value**

PCS Package Identifier 1 (Register 3.14) **$67C9_H$**



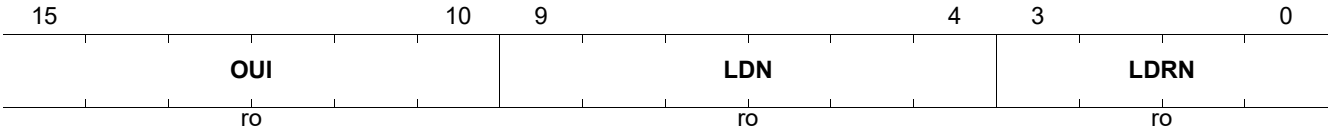
Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18**

PCS Package Identifier 2 (Register 3.15)

IEEE Standard Register=3.15

PCS_PACKID2 **Reset Value**

PCS Package Identifier 2 (Register 3.15) **$DC00_H$**



Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several different products.
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number to distinguish between several versions of this device.

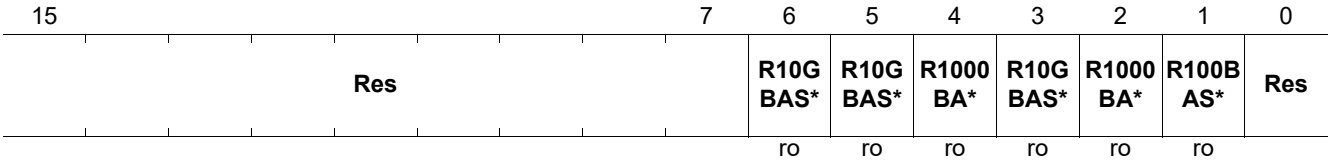
1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

PCS EEE Capability (Register 3.20)

IEEE Standard Register=3.20

PCS_EEE_CAP **Reset Value**

PCS EEE Capability (Register 3.20) **0006_H**



Field	Bits	Type	Description
R10GBASE_KR_EEE	6	RO	**10GBASE-KR EEE** 1 = EEE is supported for 10GBASE-KR. 0 = EEE is not supported for 10GBASE-KR.
R10GBASE_KX4_EEE	5	RO	**10GBASE-KX4 EEE** 1 = EEE is supported for 10GBASE-KX4. 0 = EEE is not supported for 10GBASE-KX4.
R1000BASE_KX_EEE	4	RO	**1000BASE-KX EEE** 1 = EEE is supported for 1000BASE-KX. 0 = EEE is not supported for 1000BASE-KX.

Field	Bits	Type	Description (cont'd)
R10GBASE_T_EEE	3	RO	**10GBASE-T EEE** 1 = EEE is supported for 10GBASE-T. 0 = EEE is not supported for 10GBASE-T.
R1000BASE_T_EEE	2	RO	**1000BASE-T EEE** 1 = EEE is supported for 1000BASE-T. 0 = EEE is not supported for 1000BASE-T.
R100BASE_TX_EEE	1	RO	**100BASE-TX EEE** 1 = EEE is supported for 100BASE-TX. 0 = EEE is not supported for 100BASE-TX.

EEE Control and Capability 2 (Register 3.21)

Read only, write from STA has no effect

IEEE Standard Register=3.21

PCS_EEE_CAP2 **Reset Value**

EEE Control and Capability 2 (Register 3.21) **0001_H**

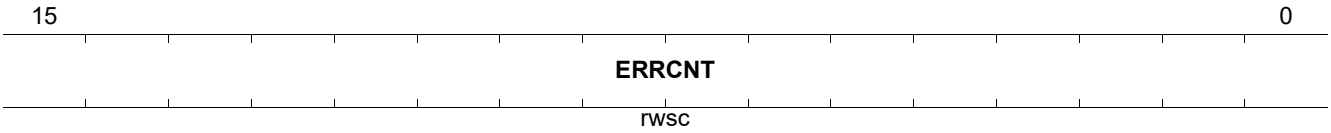
Field	Bits	Type	Description
RES	15:2	RO	**Reserved** Value always 0.
AB5GEEE	1	RO	**EEE Supported for 5GBASE-T** 0_B **UNABLE** EEE not supported for 5GBASE-T. 1_B **ABLE** EEE supported for 5GBASE-T.
AB2G5EEE	0	RO	**EEE Supported for 2.5GBASE-T** 0_B **UNABLE** EEE not supported for 2.5GBASE-T. 1_B **ABLE** EEE supported for 2.5GBASE-T.

PCS EEE Status Register 1 (Register 3.22)

IEEE Standard Register=3.22

PCS_EEE_WAKERR **Reset Value**

PCS EEE Status Register 1 (Register 3.22) **0000_H**



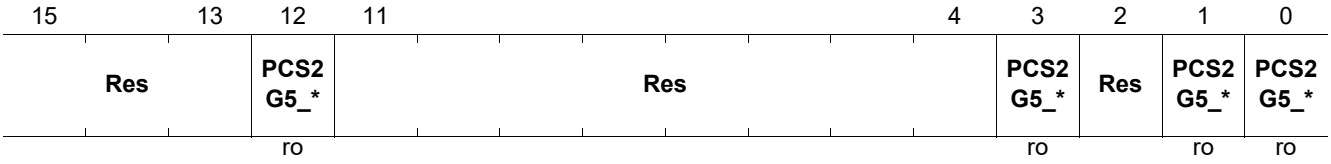
Field	Bits	Type	Description
ERRCNT	15:0	RWSC	**EEE Wake Error Counter** This is a 16-bit saturating counter indicating the number of times the GPY PHY fails to wake up within the EEE time. This counter is cleared upon read from the STA.

BASE-R and 10GBASE-T PCS Status 1 (Register 3.32)

IEEE Standard Register=3.32

PCS_2G5_STAT1 **Reset Value**

BASE-R and 10GBASE-T PCS Status 1 (Register 3.32) **0000_H**

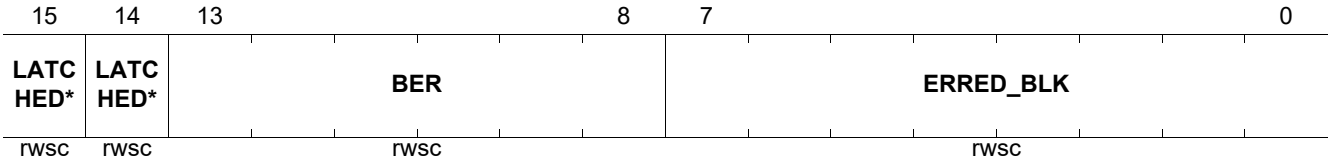


Field	Bits	Type	Description
PCS2G5_LINK_STATUS	12	RO	**BASE-R and 10GBase-T Rx Link Status** 1 = 2G5 PCS receive link up 0 = 2G5 PCS receive link down
PCS2G5_PAT_TEST_AB	3	RO	**10GBASE-R PRBS9 Pattern Testing Ability** 1 = PCS is able to support PRBS9 pattern testing. 0 = PCS is not able to support PRBS9 pattern testing.
PCS2G5_HI_BER	1	RO	**PCS 2G5 High BER** 1 = The 64B/65B receiver detects a BER above or equal to 10 ^ -4. 0 = The 64B/65B receiver detects a BER below 10 ^ -4. This bit is a direct reflection of the state of the hi_lfer variable in 126.3.6.2.2 for 2.5GBASE-T. A latch high view of this status is reflected in MDIO register 3.33.14.
PCS2G5_BLO_LOCK	0	RO	**PCS 2G5 Block Lock** 1 = 64B/65B receiver has block lock. 0 = 64B/65B receiver does not have block lock.

MULTIGBASE-T PCS Status 2 (Register 3.33)

PCS_2G5_STAT2 **Reset Value**

MULTIGBASE-T PCS Status 2 (Register 3.33) **0000_H**



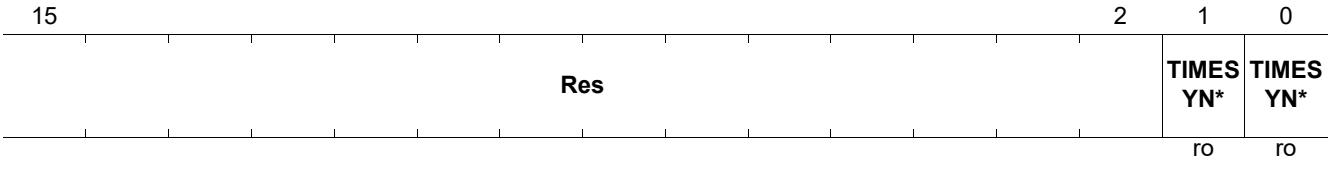
Field	Bits	Type	Description
LATCHED_BLOCK_LOCK	15	RWSC	**Latched Block Lock** 1 = PCS 2G5 has block lock. 0 = PCS 2G5 does not have block lock.
LATCHED_HIGH_BER	14	RWSC	**Latched High BER** 1 = PCS 2G5 has reported a high BER. 0 = PCS 2G5 did not report a high BER.
BER	13:8	RWSC	**BER** BER counter
ERRED_BLK	7:0	RWSC	**Errored Blocks** Errored blocks counter

PCS TimeSync Capability Register (Register 3.1800)

IEEE Standard Register=3.1800

PCS_TIMESYNC_CAP **Reset Value**

PCS TimeSync Capability Register (Register 3.1800) **0000_H**



Field	Bits	Type	Description
TIMESYNC_TX_PATH_DATA_DELAY	1	RO	**TimeSync Transmit Path Data Delay** 1 = PCS provides information on transmit path data delay in registers 3.1801 through 3.1804. 0 = PCS does not provide information on transmit path data delay. For the GPY, the value is always zero.

Field	Bits	Type	Description (cont'd)
TIMESYNC_RX_PATH_DATA_DELAY	0	RO	**TimeSync Receive Path Data Delay** 1 = PCS provides information on receive path data delay in registers 3.1805 through 3.1808. 0 = PCS does not provide information on receive path data delay. For the GPY, the value is always zero.

6.3 Standard Auto-Negotiation Registers for MMD=0x07

This register file contains the auto-negotiation registers for MMD device 0x07.

Table 29 Registers Overview

Register Short Name	Register Long Name	Reset Value
ANEG_CTRL	Auto-Negotiation Control (Register 7.0)	3000_H
ANEG_STAT	Auto-Negotiation Status (Register 7.1)	0008_H
ANEG_DEVID1	PHY Identifier 1 (Register 7.2)	$67C9_H$
ANEG_DEVID2	PHY Identifier 2 (Register 7.3)	$DC00_H$ 1)
ANEG_DIP1	Device in Package 1 (Register 7.5)	$008B_H$
ANEG_DIP2	Device in Package 2 (Register 7.6)	$C000_H$
ANEG_PACKID1	AN Package Identifier (Register 7.14)	$67C9_H$
ANEG_PACKID2	AN Package Identifier (Register 7.15)	$DC00_H$
ANEG_ADV	ANEG Advertisement for GPY (Register 7.16)	$91E1_H$
ANEG_LP_BP_AB	AN Link Partner Base Page Ability (Register 7.19)	$01E0_H$
ANEG_XNP_TX1	ANEG Local Dev XNP TX1 (Register 7.22)	0001_H
ANEG_XNP_TX2	ANEG Local Dev XNP TX2 (Register 7.23)	0000_H
ANEG_XNP_TX3	ANEG Local Dev XNP TX3 (Register 7.24)	0000_H
ANEG_LP_XNP_AB1	ANEG Link Partner XNP RX (Register 7.25)	0000_H
ANEG_LP_XNP_AB2	ANEG Link Partner XNP RX (Register 7.26)	0000_H
ANEG_LP_XNP_AB3	ANEG Link Partner XNP RX (Register 7.27)	0000_H
ANEG_MGBT_AN_CTRL	MULTI GBT AN Control (Register 7.32)	0082_H
ANEG_MGBT_AN_STA	MultiGBASE-T AN Status (Register 7.33)	0000_H
ANEG_EEE_AN_ADV1	EEE Advertisement 1 (Register 7.60)	0006_H
ANEG_EEE_AN_LPAB1	EEE Link Partner Ability 1 (Register 7.61)	0000_H
ANEG_EEE_AN_ADV2	EEE Advertisement 2 (Register 7.62)	0001_H
ANEG_EEE_LP_AB2	EEE Link Partner Ability 2 (Register 7.63)	0001_H
ANEG_MGBT_AN_CTRL2	MGBT ANEG Control 2 (Register 7.64)	0008_H

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

6.3.1 Standard Auto-Negotiation Registers for MMD=0x07

This section describes all the ANEG registers in detail.

Auto-Negotiation Control (Register 7.0)

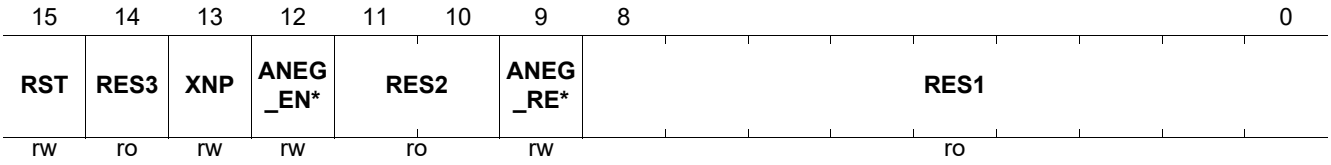
The register controls the main function of auto-negotiation as defined in Clause 45. Refer to IEEE 802.3 45.2.7.1.

This register mirrors register STD.CTRL from Clause 22.

IEEE Standard Register=7.0

ANEG_CTRL **Reset Value**

Auto-Negotiation Control (Register 7.0) **3000_H**



Field	Bits	Type	Description
RST	15	RW	**Reset** This bit resets the entire PHY to its default state. Active links are terminated. This is a self-clearing bit. The GPY firmware sets the bit to zero via the hardware when the reset has completed. 0_B **NORMAL** Normal GPY operation 1_B **RESET** GPY reset
RES3	14	RO	**Reserved** Value always zero, writes ignored.
XNP	13	RW	**Extended Next Page Control** 0_B **ZERO** Extended next page is disabled. 1_B **ONE** Extended next page is enabled.
ANEG_ENAB	12	RW	**Auto-Negotiation Enable** This bit enables the auto-negotiation process to determine the link configuration. Bit 7.0.12 is a copy of bit 0.12 in register 0 (STD_CTRL) (refer to 22.2.4.1.4). 0_B **ZERO** Auto-negotiation process is disabled. 1_B **ONE** Auto-negotiation process is enabled.
RES2	11:10	RO	**Reserved** Value always zero, writes ignored.
ANEG_RESTART	9	RW	**Restart Auto-Negotiation** The auto-negotiation process is restarted by setting bit 7.0.9 to 1. Bit 7.0.9 is a mirror of bit 0.9 in register 0 (STD_CTRL) (refer to IEEE 802.3 22.2.4.1.7). Completion of ANEG is indicated in bit 0.1.5 and 7.1.5. 0_B **ZERO** Normal operation 1_B **RESTART** Restart auto-negotiation process.

Field	Bits	Type	Description (cont'd)
RES1	8:0	RO	**Reserved** Value always zero, writes ignored.

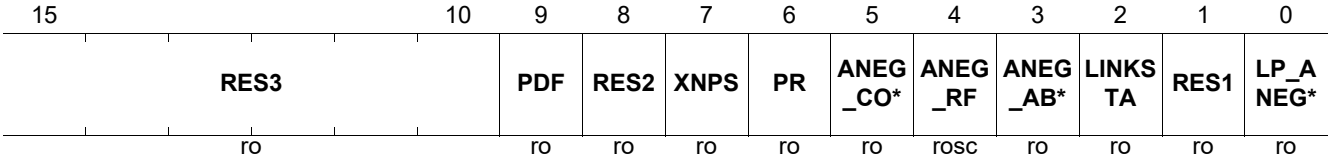
Auto-Negotiation Status (Register 7.1)

All the bits in the ANEG_STA status register are read only and correspond to the outcome or current status of the auto-negotiation process.

IEEE Standard Register=7.1

ANEG_STAT **Reset Value**

Auto-Negotiation Status (Register 7.1) **0008_H**



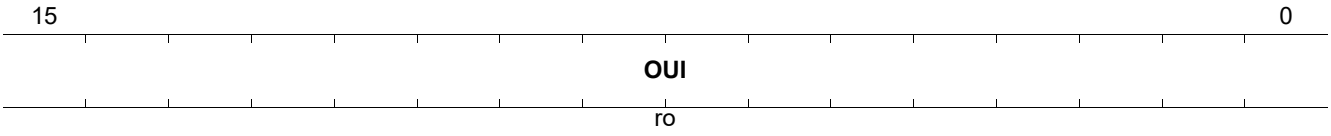
Field	Bits	Type	Description
RES3	15:10	RO	**Reserved** Value always zero, writes ignored.
PDF	9	RO	**Parallel Detection Fault** 0_B **NOFAULT** No fault detected. 1_B **FAULT** Fault detected via the parallel mechanism.
RES2	8	RO	**Reserved** Value always zero, writes ignored.
XNPS	7	RO	**Extended Next Page Status** When set to 1, bit 7.1.7 indicates that both the GPY and the link partner confirmed support for extended next page. When set to 0, bit 7.1.7 indicates that the extended next page feature is not used. 0_B **ZERO** Extended next page is not allowed. 1_B **ONE** Extended next page format is used.
PR	6	RO	**Page Received** The Page Received bit (7.1.6) is set to 1 to indicate that a new link codeword was received and stored in the AN LP Base Page ability registers 7.19, or AN LP XNP ability registers 7.25 to 7.27. 0_B **ZERO** No page received. 1_B **ONE** Page received.

Field	Bits	Type	Description (cont'd)
ANEG_COMPLETE	5	RO	**Auto-Negotiation Complete** When read as a 1, bit 7.1.5 indicates that the auto-negotiation process has completed, and that the contents of the auto-negotiation registers 7.16 and 7.19 are valid. When read as a 0, bit 7.1.5 indicates that the auto-negotiation process has not completed, and that the contents of the 7.19, 7.22 through 7.27, and 7.33 registers are as defined by the current state of the auto-negotiation protocol, or as written by manual configuration. 0_B **ZERO** Auto-negotiation process not completed. 1_B **ONE** Auto-negotiation process completed.
ANEG_RF	4	ROSC	**Remote Fault** When read as 1, bit 7.1.4 indicates that a remote fault condition was detected. Bit 7.1.4 is a copy of bit 1.4 in register 1, device 0 (refer to 22.2.4). 0_B **NORMAL** No remote fault condition detected. 1_B **FAULT** Remote fault condition detected.
ANEG_ABLE	3	RO	**Auto-Negotiation Ability** Bit 7.1.3 is a copy of bit 1.3 in register 1 (refer to 22.2.4). This is the ANEG ability of the GPY. 0_B **UNABLE** PHY is not able to perform auto-negotiation. 1_B **ABLE** PHY is able to perform auto-negotiation.
LINKSTA	2	RO	**Link Status** When read as 1, bit 7.1.2 indicates that the PMA/PMD has determined that a valid link has been established. This bit is a duplicate of the PMA/PMD link status bit in 1.1.2. This bit latches low so it does not represent the current status, but is used to indicate link drop since the last read from the management interface. Reading this bit from the MDIO resets the bit to the current value of the link. 0_B **DOWN** Link is down. 1_B **UP** Link is up.
RES1	1	RO	**Reserved** Value always zero, write ignored.
LP_ANEG_ABLE	0	RO	**Link Partner Auto-Negotiation Ability** 0_B **UNABLE** Link partner is not capable of auto-negotiation. 1_B **ABLE** Link partner is capable of auto-negotiation.

PHY Identifier 1 (Register 7.2)

ANEG_DEVID1 **Reset Value**

PHY Identifier 1 (Register 7.2) **$67C9_H$**



Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier**

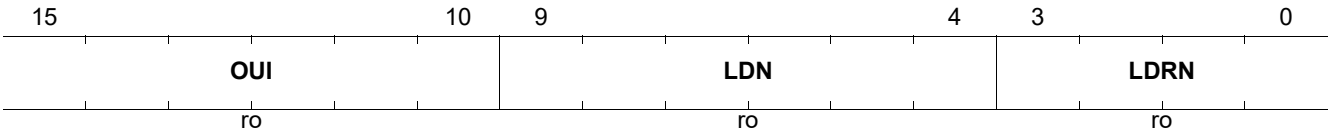
PHY Identifier 2 (Register 7.3)

Organizationally Unique Identifier

IEEE Standard Register=7.3

ANEG_DEVID2 **Reset Value**

PHY Identifier 2 (Register 7.3) **$DC00_H$**



Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several different products.
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number[1)] to distinguish between several versions of this device.

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

Device in Package 1 (Register 7.5)

IEEE Standard Register=7.5

ANEG_DIP1 **Reset Value**

Device in Package 1 (Register 7.5) **$008B_H$**

15	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		PMA4	PMA3	PMA2	PMA1	ANEG	TC	DTEXS	PHYXS	PCS	WIS	PMAPMD	CL22
ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
RES	15:12	RO	**Reserved** Ignore on read.
PMA4	11	RO	**Separate PMA4 Present in Package** 0_B **ABSENT** Separate PMA4 not present in package. 1_B **PRESENT** Separate PMA4 present in package.
PMA3	10	RO	**Separate PMA3 Present in Package** 0_B **ABSENT** Separate PMA3 not present in package. 1_B **PRESENT** Separate PMA3 present in package.
PMA2	9	RO	**Separate PMA2 Present in Package** 0_B **ABSENT** Separate PMA2 not present in package. 1_B **PRESENT** Separate PMA2 present in package.
PMA1	8	RO	**Separate PMA1 Present in Package** 0_B **ABSENT** Separate PMA1 not present inn package. 1_B **PRESENT** Separate PMA1 present in package.
ANEG	7	RO	**Auto-Negotiation Present in Package** 0_B **ABSENT** ANEG not present inn package. 1_B **PRESENT** ANEG present in package.
TC	6	RO	**TC Present in Package** 0_B **ABSENT** TC registers not present in package. 1_B **PRESENT** TC registers present in package.
DTEXS	5	RO	**DTE XS Present in Package** 0_B **ABSENT** DTE XS registers not present in package. 1_B **PRESENT** DTE XS registers present in package.
PHYXS	4	RO	**PHYXS Present in Package** 0_B **ABSENT** PHYXS registers not present in package. 1_B **PRESENT** PHYXS registers present in package.
PCS	3	RO	**PCS Present in Package** 0_B **ABSENT** PCS registers not present in package. 1_B **PRESENT** PCS registers present in package.
WIS	2	RO	**WIS Present in Package** 0_B **ABSENT** WIS registers present in package. 1_B **PRESENT** WIS registers present in package.

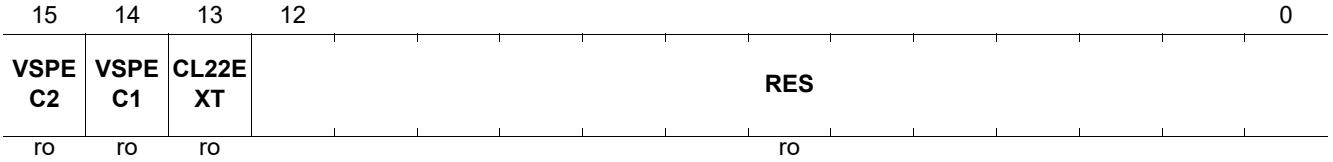
Field	Bits	Type	Description (cont'd)
PMAPMD	1	RO	**PMA PMD Present in Package** 0_B **ABSENT** PMA PMD registers not present in package. 1_B **PRESENT** PMA PMD registers present in package.
CL22	0	RO	**Clause 22 Register Present in Package** 0_B **ABSENT** Clause 22 registers no present in package. 1_B **PRESENT** Clause 22 registers present in package.

Device in Package 2 (Register 7.6)

IEEE Standard Register=7.6

ANEG_DIP2 **Reset Value**

Device in Package 2 (Register 7.6) **$C000_H$**



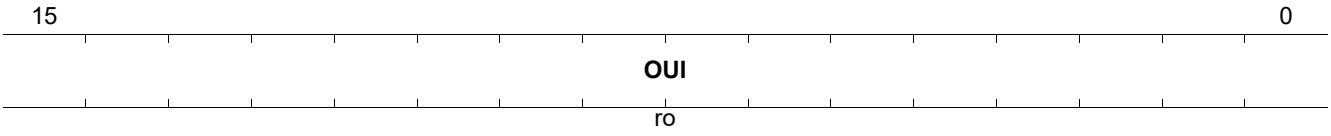
Field	Bits	Type	Description
VSPEC2	15	RO	**Vendor Specific Device 2 Present in Package** 0_B **ABSENT** Vendor Specific Device 2 not present in package. 1_B **PRESENT** Vendor Specific Device 2 present in package.
VSPEC1	14	RO	**Vendor Specific Device 1 Present in Package** 0_B **ABSENT** Vendor Specific Device 1 not present in package. 1_B **PRESENT** Vendor Specific Device 1 present in package.
CL22EXT	13	RO	**Clause 22 Extension Present in Package** 0_B **ABSENT** Clause 22 extension not present in package. 1_B **PRESENT** Clause 22 extension present in package.
RES	12:0	RO	**Reserved** Ignore on read.

AN Package Identifier (Register 7.14)

IEEE Standard Register=7.14

ANEG_PACKID1 **Reset Value**

AN Package Identifier (Register 7.14) **$67C9_H$**



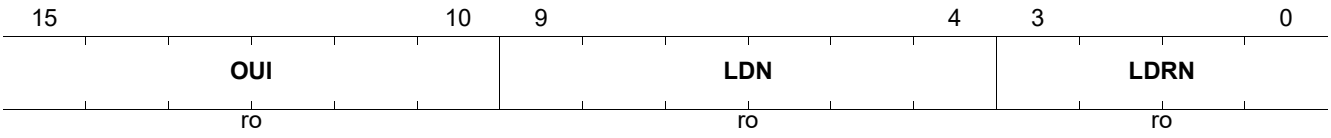
Field	Bits	Type	Description
OUI	15:0	RO	**Organizationally Unique Identifier Bits 3:18**

AN Package Identifier (Register 7.15)

IEEE Standard Register=7.15

ANEG_PACKID2 **Reset Value**

AN Package Identifier (Register 7.15) **$DC00_H$**



Field	Bits	Type	Description
OUI	15:10	RO	**Organizationally Unique Identifier Bits 19:24**
LDN	9:4	RO	**Device Number** Specifies the device number[1)] to distinguish between several different products.
LDRN	3:0	RO	**Device Revision Number** Specifies the device revision number[1)] to distinguish between several versions of this device.

1) For the device specific reset value, see the Product Naming table in the **Package Outline** chapter.

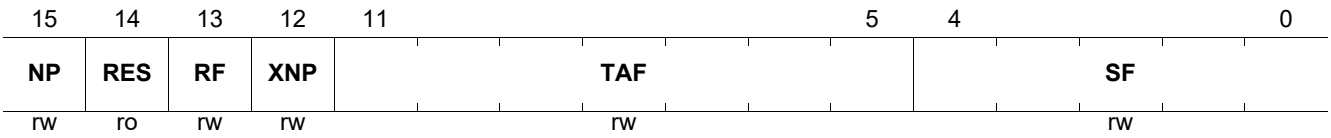
ANEG Advertisement for GPY (Register 7.16)

This register is a copy of the auto-negotiation advertisement register (Register 4). A read to the AN advertisement register (7.16) reports the value of the auto-negotiation advertisement register (Register 4); writes to the AN advertisement register (7.16) cause a write to occur to the auto-negotiation advertisement register (Register 4).

IEEE Standard Register=7.16

ANEG_ADV **Reset Value**

ANEG Advertisement for GPY (Register 7.16) **$91E1_H$**



Field	Bits	Type	Description
NP	15	RW	**Next Page Able** 0_B **INACTIVE** No next page allowed. 1_B **ACTIVE** Additional next page(s) to follow.
RES	14	RO	**Reserved** Write as zero, ignore on read.
RF	13	RW	**Remote Fault** The remote fault bit allows indication of a fault to the link partner. Refer to IEEE 802.3 28.2.1.2.4.
XNP	12	RW	**Transmission of Extended Next Pages** Indicates that the GPY is able to transmit extended next pages. 0_B **UNABLE** GPY is XNP unable. 1_B **ABLE** GPY is XNP able.
TAF	11:5	RW	**Technology Ability Field** The technology ability field is an 7-bit wide field containing information indicating supported technologies. The GPY supports 10BASE-T (half and full duplex), 100BASE-TX (half and full duplex), and both symmetric and asymmetric PAUSE. 40_H **PS_ASYM** Advertise asymmetric pause 20_H **PS_SYM** Advertise symmetric pause 10_H **DBT4** Advertise 100BASE-T4 08_H **DBT_FDX** Advertise 100BASE-TX full duplex 04_H **DBT_HDX** Advertise 100BASE-TX half duplex 02_H **XBT_FDX** Advertise 10BASE-T full duplex 01_H **XBT_HDX** Advertise 10BASE-T half duplex
SF	4:0	RW	**Selector Field** This field is always set to 1 because the GPY only supports the 802.3 Ethernet standard. 00001_B**IEEE8023** IEEE 802.3 technology.

AN Link Partner Base Page Ability (Register 7.19)

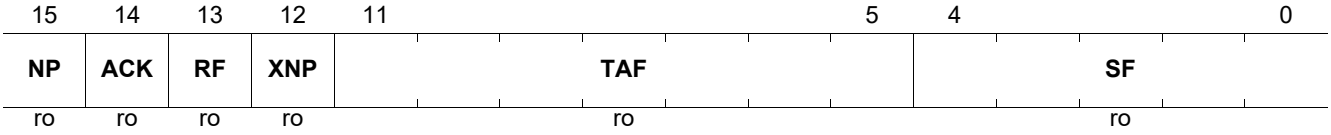
Register 7.19 is a copy of register 5 from Clause 28. It contains the Base Page received from the link partner.

All of the bits in the AN LP Base Page Ability register are read only.

IEEE Standard Register=7.19

ANEG_LP_BP_AB **Reset Value**

AN Link Partner Base Page Ability (Register 7.19) **$01E0_H$**



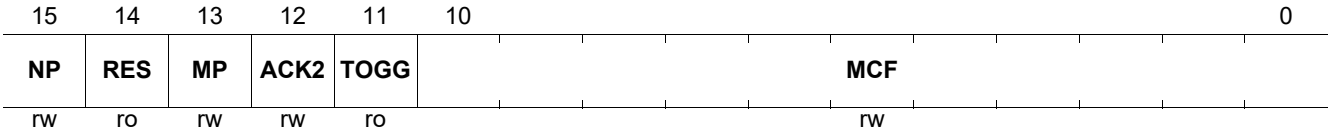
Field	Bits	Type	Description
NP	15	RO	**Link Partner Next Page** Next page request indication from the link partner. Refer to IEEE 802.3 28.2.1.2.6. 0_B **INACTIVE** No next page to follow. 1_B **ACTIVE** Additional next page to follow.
ACK	14	RO	**Link Partner Acknowledge** Acknowledgment indication from the link partner's link code word. Refer to IEEE 802.3 28.2.1.2.5. 0_B **INACTIVE** Device did not successfully receive its link partner's link code word. 1_B **ACTIVE** Device successfully received its link partner's link code word.
RF	13	RO	**Link Partner Remote Fault** Remote fault indication from the link partner. Refer to IEEE 802.3 28.2.1.2.4. 0_B **NONE** Remote fault is not indicated by the link partner. 1_B **FAULT** Remote fault is indicated by the link partner.
XNP	12	RO	**Link Partner XNP Ability** 0_B **UNABLE** Link partner is not XNP able. 1_B **ABLE** Link partner is XNP able.
TAF	11:5	RO	**Technology Ability Field** These bits indicate the link partner's supported technologies received in the Base Page. 40_H **PS_ASYM** Advertise asymmetric pause 20_H **PS_SYM** Advertise symmetric pause 10_H **DBT4** Advertise 100BASE-T4 08_H **DBT_FDX** Advertise 100BASE-TX full duplex 04_H **DBT_HDX** Advertise 100BASE-TX half duplex 02_H **XBT_FDX** Advertise 10BASE-T full duplex 01_H **XBT_HDX** Advertise 10BASE-T half duplex

Field	Bits	Type	Description (cont'd)
SF	4:0	RO	**Link Partner Selector Field** This selector field represents one of the 32 possible messages with encoding definitions defined in IEEE 802.3 Annex 28A. 0x00 = Reserved 0x01 = IEEE 802.3 0x02 = IEEE 802.9 ISLAN-16T 0x03 = IEEE 802.5 0x04 = IEEE 1394 0x05 -> 0x1F = Reserve

ANEG Local Dev XNP TX1 (Register 7.22)

ANEG_XNP_TX1 **Reset Value**

ANEG Local Dev XNP TX1 (Register 7.22) **0001_H**



Field	Bits	Type	Description
NP	15	RW	**Next Page** When the NP bit is set, the GPY requests to transmit one additional page. next page transmission ends when both ends of a link segment set their next page bits to logic 0, indicating that neither has anything additional to transmit. Refer to IEEE 802.3 28.2.3.4. 0_B **INACTIVE** No next page to follow. 1_B **ACTIVE** Additional next page(s) to follow.
RES	14	RO	**Reserved** Write as zero, ignore on read.
MP	13	RW	**Message Page** Message Page (MP) is used by the next page function to differentiate a Message Page from an Unformatted Page. Only message pages are used by the GPY. 0_B **UNFOR** Unformatted Page 1_B **MESSG** Message Page
ACK2	12	RW	**Acknowledge 2** Not used during GPY auto-negotiation. 0_B **INACTIVE** Device does not comply with message. 1_B **ACTIVE** Device complies with message.
TOGG	11	RO	**Toggle** The Toggle bit is used to ensure proper synchronization between the GPY and the link partner. Refer to IEEE 802.3 28.2.3.4. 0_B **ZERO** Previous value of the Tx LCW was ONE. 1_B **ONE** Previous value of the Tx LCW was ZERO.

Field	Bits	Type	Description (cont'd)
MCF	10:0	RW	**Message Code Field** When the Message Page bit is set to 1 (7.16.1), this field is the Message Code Field of a message page used in a next page exchange. The message codes are described in IEEE802.3 Appendix 28C. This is used to indicate the type of message in UCF1 and UCF2. 0x0 = Reserved 0x1 = Null message 0x2 = One Unformatted Page (UP) with TAF follows 0x3 = Two UPs with TAF follows 0x4 = Remote fault details message 0x5 = OUI message 0x6 = PHY ID message 0x7 = 100BASE-T2 message 0x8 = 1000BASE-T message 0x9 = MULTIGBASE-T message 0xA = EEE technology capability follows in next UP 0xB = OUI XNP

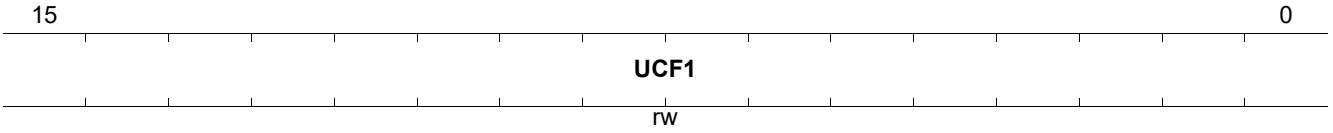
ANEG Local Dev XNP TX2 (Register 7.23)

Unformatted Code field 1 contains Seed information and advertises support of 1GBT full duplex and half duplex. Refer to 28.2.3.4.

IEEE Standard Register=7.23

ANEG_XNP_TX2 **Reset Value**

ANEG Local Dev XNP TX2 (Register 7.23) **0000_H**



Field	Bits	Type	Description
UCF1	15:0	RW	**Unformatted Code Field 1** Transmits Master-Slave Seed bit to facilitate auto-negotiation resolution, port type and duplex capability.

ANEG Local Dev XNP TX3 (Register 7.24)

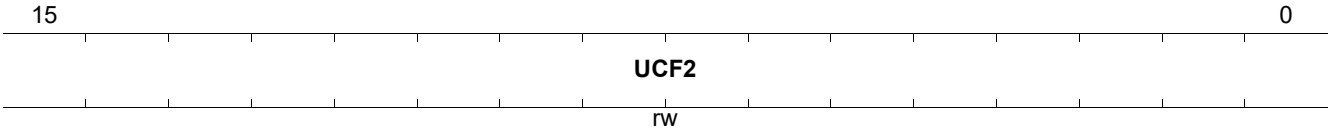
Unformatted Code field 2 - Register 7.24

Refer to 28.2.3.4.

IEEE Standard Register=7.24

ANEG_XNP_TX3 **Reset Value**

ANEG Local Dev XNP TX3 (Register 7.24) **0000_H**



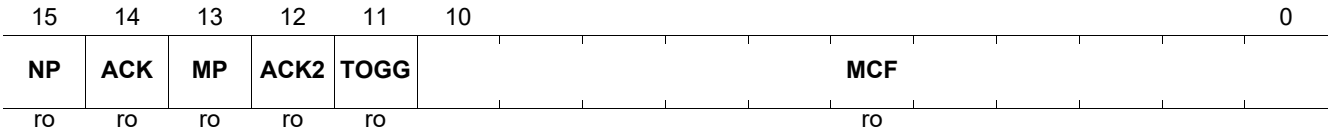
Field	Bits	Type	Description
UCF2	15:0	RW	**Unformatted Code Field 2** 2.5 GBASE-T ability is advertised by default

ANEG Link Partner XNP RX (Register 7.25)

IEEE Standard Register=7.25

ANEG_LP_XNP_AB1 **Reset Value**

ANEG Link Partner XNP RX (Register 7.25) **0000_H**



Field	Bits	Type	Description
NP	15	RO	**Link Partner Next Page** Refer to 28.2.3.4.3. The next page (NP) bit is used by the next page function to indicate whether or not this is the last next page to be transmitted. 0_B **INACTIVE** Last page 1_B **ACTIVE** Additional next page(s) to follow.
ACK	14	RO	**Link Partner Acknowledge** As defined in 28.2.1.2.5. The Acknowledge (Ack) bit is used by the auto-negotiation function to indicate that the GPY has successfully received its link partner's link codeword.
MP	13	RO	**Link Partner Message Page** Indicates that the content of MCF is either an unformatted page or a formatted message. Refer to IEEE 802.3 28.2.3.4. 0_B **UNFOR** Unformatted page 1_B **MESSG** Message page

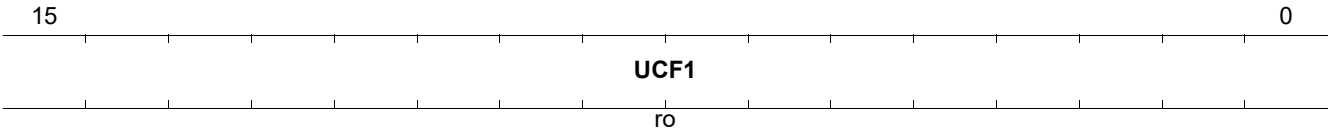
Field	Bits	Type	Description (cont'd)
ACK2	12	RO	**Link Partner Acknowledge 2** Refer to IEEE 802.3 28.2.3.4. 0_B **INACTIVE** Device not able to comply with message. 1_B **ACTIVE** Device complies with message.
TOGG	11	RO	**Link Partner Toggle** Refer to IEEE 802.3 28.2.3.4. This bit is set to the opposite of the TOGG bit in the previous page. 0_B **ZERO** Previous value of the TX LCW was ONE. 1_B **ONE** Previous value of the TX LCW was ZERO.
MCF	10:0	RO	**Link Partner Message Code Field** This field indicates the type of Message Code. Refer to IEEE802.3 28.2.3.4. 009_H **MC_2G5BT** Message Code for 2.5GBASE-T

ANEG Link Partner XNP RX (Register 7.26)

IEEE Standard Register=7.26

ANEG_LP_XNP_AB2 **Reset Value**

ANEG Link Partner XNP RX (Register 7.26) **0000_H**



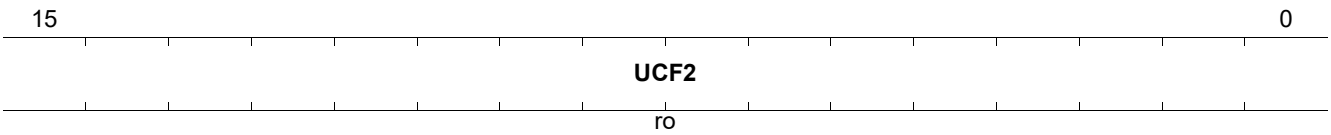
Field	Bits	Type	Description
UCF1	15:0	RO	**Unformatted Code Field 1** Refer to 28.2.3.4.

ANEG Link Partner XNP RX (Register 7.27)

IEEE Standard Register=7.27

ANEG_LP_XNP_AB3 **Reset Value**

ANEG Link Partner XNP RX (Register 7.27) **0000_H**



Field	Bits	Type	Description
UCF2	15:0	RO	**Unformatted Code Field 2** Refer to 28.2.3.4.

MULTI GBT AN Control Register (Register 7.32)

This register advertises the GPY capabilities.

IEEE Standard Register=7.32

ANEG_MGBT_AN_CTRL **Reset Value**

MULTI GBT AN Control Register (Register 7.32) **0082_H**

15	14	13	12	11 9	8	7	6	5	4 3	2	1	0
MS_MAN_*	**MSCV**	**PT**	**AB_10GBT**	**RES2**	**AB_5GBT**	**AB_2G5BT**	**FR_5GBT**	**FR_2G5BT**	**RES1**	**LDPMA**	**FR**	**LDL**
rw	rw	rw	ro	ro	ro	rw	ro	rw	ro	rw	rw	rw

Field	Bits	Type	Description
MS_MAN_EN	15	RW	**Master Slave Manual Config Enable** 0_B **ANEG** ANEG is used to determine the Master-Slave selection. 1_B **MAN** Manual configuration. The MSCV bit determines the Master-Slave selection.
MSCV	14	RW	**Master Slave Config Value** 0_B **SLAVE** Manual set to SLAVE. 1_B **MASTER** Manual set to MASTER.
PT	13	RW	**Port Type** 0_B **MASTER** Preference as Master - single port device. 1_B **SLAVE** Preference as Slave - multiport device.
AB_10GBT	12	RO	**10GBASE-T Ability** Not supported. Value always zero.
RES2	11:9	RO	**Reserved** Value always zero, writes ignored.
AB_5GBT	8	RO	**5GBASE-T Ability** Not supported by the GPY. 0_B **UNABLE** Do not advertise PHY as 5GBASE-T capable. 1_B **ABLE** Advertise PHY as 5GBASE-T capable. Not supported.
AB_2G5BT	7	RW	**2.5GBASE-T Ability** 0_B **UNABLE** Do not advertise PHY as 2.5GBASE-T capable. 1_B **ABLE** Advertise PHY as 2.5GBASE-T capable.
FR_5GBT	6	RO	**5GBASE-T Fast Retrain Ability** Not supported by GPY. Refer to 45.2.7.10 bz. 0_B **UNABLE** Do not advertise PHY as 5GBASE-T fast retrain able. 1_B **ABLE** Advertise PHY as 5GBASE-T fast retrain capable. Not supported.
FR_2G5BT	5	RW	**2.5GBASE-T Fast Retrain Ability** 0_B **UNABLE** Do not advertise PHY as 2.5G fast retrain able. 1_B **ABLE** Advertise PHY as 2.5G fast retrain able.
RES1	4:3	RO	**Reserved** Value always zero, writes ignored.

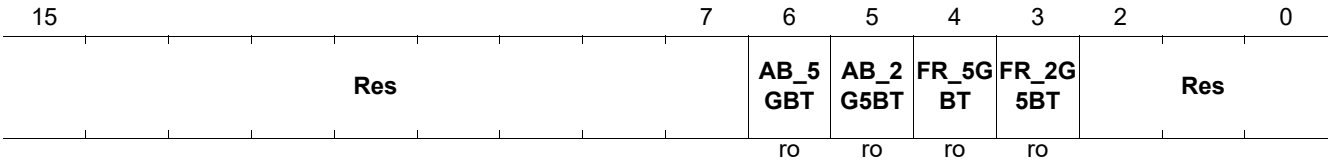
Field	Bits	Type	Description (cont'd)
LDPMA	2	RW	**GPY PMA Training Reset Request** When this bit is set to 1, the GPY expects the link partner to reset the PMA training PRBS for every PMA training frame. When this bit is set to 0, the GPY expects the link partner to run the PMA training PRBS continuously through every PMA training frame.
FR	1	RW	**Fast Retrain Ability**
LDL	0	RW	**GPY Loop Timing Ability**

MultiGBASE-T AN Status register (Register 7.33)

IEEE Standard Register=7.33

ANEG_MGBT_AN_STA **Reset Value**

MultiGBASE-T AN Status register (Register 7.33) **0000_H**



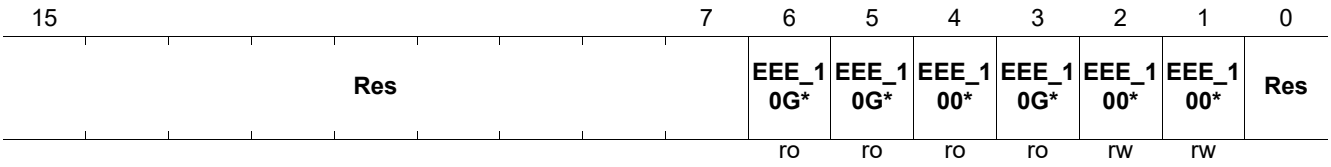
Field	Bits	Type	Description
AB_5GBT	6	RO	**5GBASE-T Ability of Link Partner** This bit is only valid when the link is established and ANEG completed. 0_B **UNABLE** Link partner is not capable of 5GBASE-T. 1_B **ABLE** Link partner is capable of 5GBASE-T.
AB_2G5BT	5	RO	**2.5GBASE-T Ability of Link Partner** This bit is only valid when the link is established and ANEG completed (bit 7.1.5 is set to 1). 0_B **UNABLE** Link partner is not capable of 2.5GBASE-T. 1_B **ABLE** Link partner is capable of 2.5GBASE-T.
FR_5GBT	4	RO	**5GBASE-T Fast Retrain Ability of Link Partner** This bit is only valid when the link is established and ANEG completed. 0_B **UNABLE** Link partner is not capable of 5GBASE-T fast retrain. 1_B **ABLE** Link partner is capable of 5GBASE-T fast retrain
FR_2G5BT	3	RO	**2.5GBASE-T Fast Retrain Ability of Link Partner** This bit is only valid when the link is established and ANEG completed (bit 7.1.5 is set to 1). 0_B **UNABLE** Link partner is not capable of 2.5GBASE-T fast retrain. 1_B **ABLE** Link partner is capable of 2.5GBASE-T fast retrain.

EEE Advertisement 1 (Register 7.60)

IEEE Standard Register=7.60

ANEG_EEE_AN_ADV1 **Reset Value**

EEE Advertisement 1 (Register 7.60) **0006_H**



Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_1000BT	2	RW	**Support of 1000BASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_100BTX	1	RW	**Support of 100BASE-TX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.

EEE Link Partner Ability 1 (Register 7.61)

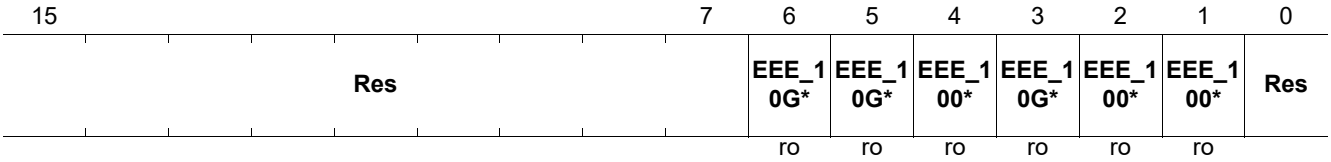
After the AN process is completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE AN advertisement 1 register.

IEEE Standard Register=7.61

All of the bits in the EEE LP ability 1 register are read only. A write operation to the EEE LP advertisement register has no effect.

ANEG_EEE_AN_LPAB1 **Reset Value**

EEE Link Partner Ability 1 (Register 7.61) **0000_H**



Field	Bits	Type	Description
EEE_10GBKR	6	RO	**Support of 10GBASE-KR EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_10GBKX4	5	RO	**Support of 10GBASE-KX4 EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_1000BKX	4	RO	**Support of 1000BASE-KX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_10GBT	3	RO	**Support of 10GBASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_1000BT	2	RO	**Support of 1000BASE-T EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.
EEE_100BTX	1	RO	**Support of 100BASE-TX EEE** 0_B **DISABLED** This PHY mode is not supported for EEE. 1_B **ENABLE** This PHY mode is supported for EEE.

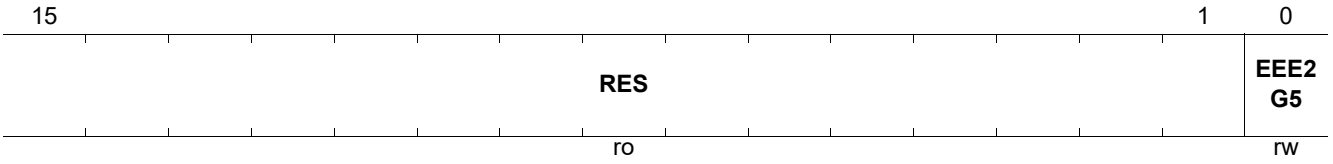
EEE Advertisement 2 (Register 7.62)

EEE advertisement 2 register is a continuation of EEE advertisement 1 register.

IEEE Standard Register=7.62

ANEG_EEE_AN_ADV2 **Reset Value**

EEE Advertisement 2 (Register 7.62) **0001_H**



Field	Bits	Type	Description
RES	15:1	RO	**Reserved**
EEE2G5	0	RW	**Advertise 2.5GBASE-T EEE Capability** 0_B **DISABLED** This PHY mode does not advertise 2.5GBASE-T EEE. 1_B **ENABLE** This PHY mode advertises 2.5GBASE-T EEE.

EEE Link Partner Ability 2 (Register 7.63)

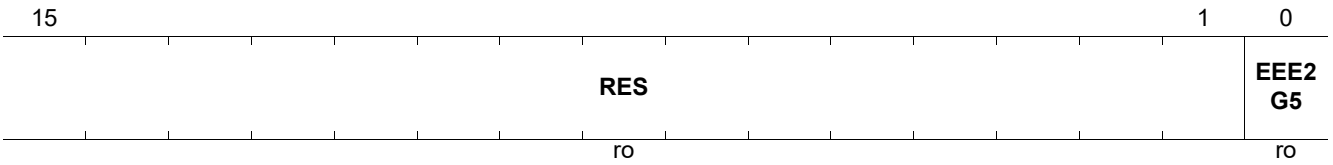
When the AN and training processes are complete, this register reflects the contents of the link partner's EEE advertisement 2 register.

IEEE Standard Register=7.63

All the bits in the EEE LP Ability 2 register are read-only. A write to the EEE LP Ability 2 register has no effect.

ANEG_EEE_LP_AB2 **Reset Value**

EEE Link Partner Ability 2 (Register 7.63) **0001_H**



Field	Bits	Type	Description
RES	15:1	RO	**Reserved**
EEE2G5	0	RO	**Link Partner Advertised 2.5GBASE-T EEE Capability** 0_B **DISABLED** LP not 2.5GBASE-T EEE capable. 1_B **ENABLE** LP 2.5GBASE-T EEE capable.

MGBT ANEG Control 2 (Register 7.64)

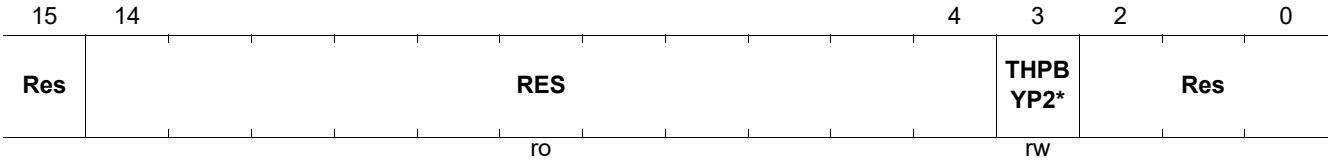
This register is an extension of the ANEG Control Register for Multi GBT. It is used for 2.5 G ANEG configuration.

IEEE Standard Register=7.64

Bit 7.64.3 is valid only when 7.32.5 is set to 1 advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, refer to 126.4.2.5.10. When bit 7.64.3 is set to 0, the GPY requests the link partner not to reset THP during fast retrain. When bit 7.64.3 is set to 1, the GPY requests the ink partner to initially reset THP during fast retrain.

ANEG_MGBT_AN_CTRL2 **Reset Value**

MGBT ANEG Control 2 (Register 7.64) **0008_H**



Field	Bits	Type	Description
RES	14:4	RO	**Reserved**
THPBYP2G5	3	RW	**THP Bypass During Fast Retrain** The GPY requests a THP bypass during fast retrain. 0_B **NORST** GPY requests partner NOT to initially reset THP during fast retrain. 1_B **RST** GPY requests partner to initially reset THP during fast retrain.

6.4 Vendor Specific 1 Device for MMD=0x1E

This register file contains GPY-specific registers for MMD=30 (decimal).

Table 30 Registers Overview

Register Short Name	Register Long Name	Reset Value
VSPEC1_LED0	Configuration for LED Pin 0 (Register 30.1)	0310_H
VSPEC1_LED1	Configuration for LED Pin 1 (Register 30.2)	0320_H
VSPEC1_LED2	Configuration for LED Pin 2 (Register 30.3)	0340_H
VSPEC1_SGMII_CTRL	Chip Level SGMII Control Register (Register 30.8)	$30DA_H$
VSPEC1_SGMII_STAT	Chip Level SGMII Status Register (Register 30.9)	0008_H
VSPEC1_NBT_DS_CTRL	NBASE-T Downshift Control Register (Register 30.10)	0400_H
VSPEC1_NBT_DS_STA	NBASE-T Downshift Status Register (Register 30.11)	0000_H
VSPEC1_PM_CTRL	Packet Manager Control (Register 30.12)	0083_H
VSPEC1_TEMP_STA	Temperature Code (Register 30.14)	0000_H
VSPEC1_LANE_ASP_MAP	ASP Mapping to Physical Lanes (Register 30.20)	$00E4_H$
VSPEC1_LOW_POWER_ENTRY_TIME	Time to Enter Low Power (Register 30.21)	0001_H

6.4.1 Vendor Specific 1 Device for MMD=0x1E

This section describes all the VSPEC1 registers in detail.

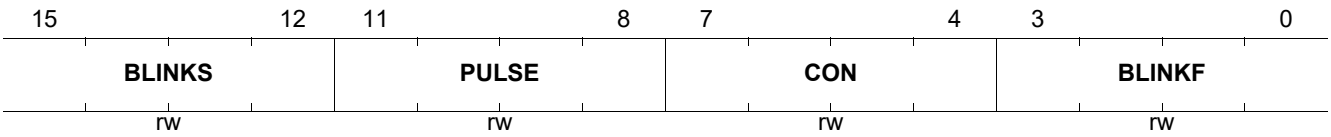
Configuration for LED Pin 0 (Register 30.1)

This register configures the behavior of the LED0 pin depending on predefined states or events the PHY has entered into or raised. Since more than one event/state may be active at the same time, more than one function may apply at the same time. The priority from highest to lowest is given by the order: PULSE, BLINKS, BLINKF, and CON. The LED PULSE for the selected activity is only displayed for the link speed selected in CON. When CON is selected as NONE, no PULSE is displayed on the LED for any activity. To avoid the LED being constantly on when it is configured for pulsing alone, set the NO_CON bit in the PULSE field (bit 11).

IEEE Standard Register=30.1

VSPEC1_LED0 **Reset Value**

Configuration for LED Pin 0 (Register 30.1) **0310_H**



Field	Bits	Type	Description
BLINKS	15:12	RW	**Slow Blinking Configuration** The BLINKS field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not active 0001_B**LINK10** Blink when link is 10 Mbps. 0010_B**LINK100** Blink when link is 100 Mbps. 0100_B**LINK1000** Blink when link is 1000 Mbps. 1000_B**LINK2500** Blink when link is 2500 Mbps.
PULSE	11:8	RW	**Pulsing Configuration** The PULSE field is a mask field that combines certain events, e.g., TXACT|RXACT, to generate a pulse on the LED when such an event is detected. 0000_B**NONE** No pulsing 0001_B**TXACT** Transmit activity 0010_B**RXACT** Receive activity 0100_B**COL** Collision 1000_B**NO_CON** Constant on behavior is switched off.
CON	7:4	RW	**Constant On Configuration** The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not active 0001_B**LINK10** On when link is 10 Mbps. 0010_B**LINK100** On when link is 100 Mbps. 0100_B**LINK1000** On when link is 1000 Mbps. 1000_B**LINK2500** On when link is 2500 Mbps.
BLINKF	3:0	RW	**Fast Blinking Configuration** The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** No active 0001_B**LINK10** Blink when Link is 10 Mbps. 0010_B**LINK100** Blink when Link is 100 Mbps. 0100_B**LINK1000** Blink when Link is 1000 Mbps. 1000_B**LINK2500** Blink when Link is 2500 Mbps.

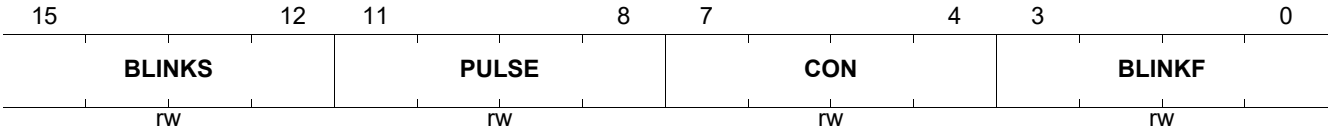
Configuration for LED Pin 1 (Register 30.2)

Configuration register for LED pin 1.

IEEE Standard Register=30.2

VSPEC1_LED1 **Reset Value**

Configuration for LED Pin 1 (Register 30.2) **0320_H**



Field	Bits	Type	Description
BLINKS	15:12	RW	**Slow Blinking Configuration** The BLINKS field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not active 0001_B**LINK10** Blink when link is 10 Mbps. 0010_B**LINK100** Blink when link is 100 Mbps. 0100_B**LINK1000** Blink when link is 1000 Mbps. 1000_B**LINK2500** Blink when link is 2500 Mbps.
PULSE	11:8	RW	**Pulsing Configuration** The PULSE field is a mask field that combines certain events, e.g., TXACT|RXACT, to generate a pulse on the LED when such an event is detected. 0000_B**NONE** No pulsing 0001_B**TXACT** Transmit activity 0010_B**RXACT** Receive activity 0100_B**COL** Collision 1000_B**NO_CON** Constant on behavior is switched off.
CON	7:4	RW	**Constant On Configuration** The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not active 0001_B**LINK10** On when link is 10 Mbps. 0010_B**LINK100** On when link is 100 Mbps. 0100_B**LINK1000** On when link is 1000 Mbps. 1000_B**LINK2500** On when link is 2500 Mbps.

Field	Bits	Type	Description (cont'd)
BLINKF	3:0	RW	**Fast Blinking Configuration** The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not active 0001_B**LINK10** Blink when link is 10 Mbps. 0010_B**LINK100** Blink when link is 100 Mbps. 0100_B**LINK1000** Blink when link is 1000 Mbps. 1000_B**LINK2500** Blink when link is 2500 Mbps.

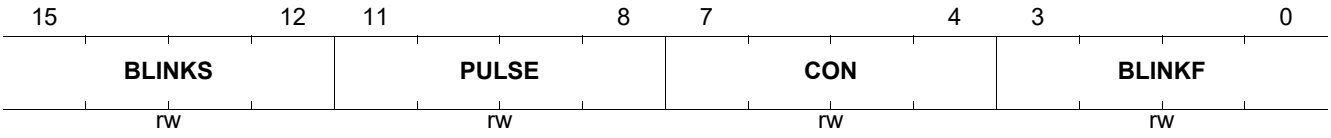
Configuration for LED Pin 2 (Register 30.3)

Configuration register for LED pin 2.

IEEE Standard Register=30.3

VSPEC1_LED2 **Reset Value**

Configuration for LED Pin 2 (Register 30.3) **0340_H**



Field	Bits	Type	Description
BLINKS	15:12	RW	**Slow Blinking Configuration** The Blink-S field selects the PHY states where the LED blinks with the predefined slow frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not active 0001_B**LINK10** Blink when link is 10 Mbps. 0010_B**LINK100** Blink when link is 100 Mbps. 0100_B**LINK1000** Blink when link is 1000 Mbps. 1000_B**LINK2500** Blink when link is 2500 Mbps.
PULSE	11:8	RW	**Pulsing Configuration** The PULSE field is a mask field that combines certain events, e.g., TXACT|RXACT, to generate a pulse on the LED when such an event is detected. 0000_B**NONE** No pulsing 0001_B**TXACT** Transmit activity 0010_B**RXACT** Receive activity 0100_B**COL** Collision 1000_B**NO_CON** Constant on behavior is switched off.

Field	Bits	Type	Description (cont'd)
CON	7:4	RW	**Constant On Configuration** The CON field selects the PHY states where the LED is constantly on. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not active 0001_B**LINK10** On when link is 10 Mbps. 0010_B**LINK100** On when link is 100 Mbps. 0100_B**LINK1000** On when link is 1000 Mbps. 1000_B**LINK2500** On when link is 2500 Mbps.
BLINKF	3:0	RW	**Fast Blinking Configuration** The BLINKF field selects the PHY states where the LED blinks with the predefined fast frequency. Each bit mask indicates a link speed. Combinations of these bit masks are used to provide a combination of link speed states to enable the behavior. 0000_B**NONE** Not Active 0001_B**LINK10** Blink when link is 10 Mbps. 0010_B**LINK100** Blink when link is 100 Mbps. 0100_B**LINK1000** Blink when link is 1000 Mbps. 1000_B**LINK2500** Blink when link is 2500 Mbps.

Chip Level SGMII Control Register (Register 30.8)

SGMII control register to set up SGMII modes.

IEEE Standard Register=30.8

VSPEC1_SGMII_CTRL **Reset Value**

Chip Level SGMII Control Register (Register 30.8) **$30DA_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	**LB**	**Res**	**ANEN**	**PD**	**RXINV**	**Res**		**EEE_CAP**	**Res**	**SGMII_F***	**Res**			**ANMODE**	
rw	rw		rw	rw	rw			rw		rw				rw	

Field	Bits	Type	Description
RST	15	RW	**Reset SGMII** This bit configures a self-clearing reset of the SGMII Interface. 0_B **NORM** Normal operation SGMII 1_B **RST** Reset SGMII
LB	14	RW	**Loopback** SGMII loopback 0_B **OFF** SGMII loopback is disabled. 1_B **ON** SGMII loopback is enabled.

Field	Bits	Type	Description (cont'd)
ANEN	12	RW	**ANEG Enable** When this bit is set to 1, the ANMODE field determines the auto-negotiation protocol. When this bit is set to 0, the speed is set to maximum in full duplex mode. Once the TPI link is up, the SGMII speed is automatically forced to match the TPI speed. This bit must be set to 0 when the SGMII_FIXED2G5 field is 1. The MAC SoC is able to access the actual TPI speed via the MDIO registers. 0_B **OFF** SGMII ANEG Disabled The speed is set to the maximum in full duplex mode for the initial link configuration (forced mode), until the TPI link is up. 1_B **ON** SGMII ANEG Enabled The negotiation style is configured by the ANMODE field.
PD	11	RW	**Power Down** SGMII power down 0_B **OFF** Normal operation SGMII 1_B **ON** SGMII power down
RXINV	10	RW	**Inversion of RX0_M and RX0_P** The purpose of inverting RxM and RxP is to simplify the PCB layout (not crossing lanes, allows 1 layer). 0_B **NORMAL** No inversion. Pin 28 is RX0_M, and pin 27 is RX0_P. 1_B **INVERT** Invert RX SGMII. Pin 28 is RX0_P, and pin 27 is RX0_M.
ANRS	9	RW	**Restart SGMII ANEG** This is a self-clearing bit once the ANEG process has been initiated. 0_B **NORMAL** Normal operation SGMII 1_B **RESTART** Restart SGMII ANEG
EEE_CAP	7	RW	**EEE SGMII ANEG** The EEE SGMII capability is advertised in ANEG. Used only when ANMODE = AN_CIS_PHY. 0_B **OFF** EEE is not advertised. 1_B **ON** EEE is advertised.
SGMII_FIXED 2G5	5	RW	**Force SGMII Interface to Remain in 2.5G Speed or TPI Link Speed** Irrespective of the TPI link speed, the SGMII operates at 2.5G speed when this bit is enabled. The GPY packet manager performs the rate adaptation, and Flow Control is used to backpressure the MAC SoC when required. 0_B **NO_FORCE** The SGMII speed is reconfigured by the GPY based on the TPI link speed. 1_B **FORCE** The SGMII speed is forced to the 2.5G speed.

Field	Bits	Type	Description (cont'd)
USXGMII_REACH	4:3	RW	**USXGMII Tx and Rx Configuration** This is based on the loop length between the GPY and the STA connected via the USXGMII interface. No action is taken when the USXGMII interface is not available in the GPY. 00_B **SHORT** Short Reach Configuration Short Reach Configuration of USXGMII Tx and Rx Equalization by firmware. 01_B **MEDIUM** Medium Reach Configuration Medium Reach Configuration of USXGMII Tx and Rx Equalization by firmware. 10_B **LONG** Long Reach Configuration Long Reach Configuration of USXGMII Tx and Rx Equalization by firmware. 11_B **CUSTOM** Custom Configuration At start-up, default settings are available after boot. When custom configuration of the USXGMII Tx and Rx Equalization is required, the parameters are configured by the GPY API using custom values.
ANMODE	1:0	rw	**SGMII ANEG Mode** This field defines the type of ANEG protocol when ANEG is enabled. 00_B **RES** Reserved. Do not use, defaults to AN_CIS_PHY. 01_B **AN_1000BX** IEEE 1000Bx SGMII ANEG Clause 37 SGMII 1000Bx ANEG is used. 10_B **AN_CIS_PHY** Cisco SGMII ANEG mode with the GPY acting as a PHY. ANEG is implemented as defined by the Cisco SGMII standard, as a PHY-side SGMII.This is the default configuration. 11_B **AN_CIS_MAC** Cisco SGMII ANEG mode with the GPY acting as a MAC. ANEG is implemented as defined by the Cisco SGMII standard, as a MAC-side SGMII.

Chip Level SGMII Status Register (Register 30.9)

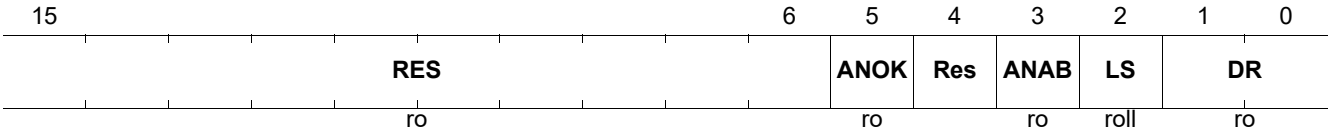
This is the SGMII status register.

All the bits in this status register are read only. A write has no effect.

IEEE Standard Register=30.9

VSPEC1_SGMII_STAT **Reset Value**

Chip Level SGMII Status Register (Register 30.9) **0008_H**



Field	Bits	Type	Description
RES	15:6	RO	**Reserved** Ignore when read.

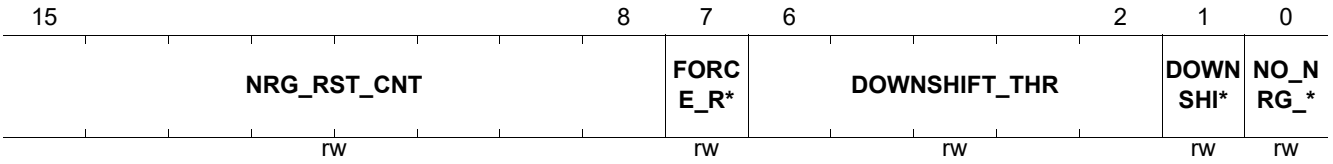
Field	Bits	Type	Description (cont'd)
ANOK	5	RO	**Auto-Negotiation Completed** Indicates whether the auto-negotiation process is completed or not. 0_B **RUNNING** Auto-negotiation process is in progress or not started. 1_B **COMPLETED** Auto-negotiation process is completed.
ANAB	3	RO	**Auto-Negotiation Ability** Specifies the auto-negotiation ability. 0_B **DISABLED** PHY is not able to perform auto-negotiation. 1_B **ENABLED** PHY is able to perform auto-negotiation.
LS	2	ROLL	**Link Status** Indicates the link status of the SGMII. 0_B **INACTIVE** The link is down. No communication with link partner possible. 1_B **ACTIVE** The link is up. Data communication with link partner is possible.
DR	1:0	RO	**SGMII Data Rate** This field indicates the operating data rate of SGMII when the link is up. 00_B **DR_10** SGMII link rate is 10 Mbps. 01_B **DR_100** SGMII link rate is 100 Mbps. 10_B **DR_1G** SGMII link rate is 1000 Mbps. 11_B **DR_2G5** SGMII link rate is 2500 Mbps.

NBASE-T Downshift Control Register (Register 30.10)

IEEE Standard Register=30.10

VSPEC1_NBT_DS_CTRL **Reset Value**

NBASE-T Downshift Control Register (Register 30.10) **0400_H**



Field	Bits	Type	Description
NRG_RST_CNT	15:8	RW	**Timer to Reset the Downshift Process** When the energy is zero for a duration equal to NRG_RST_CNT seconds, the ANEG advertised capabilities are reset to the maximum GPY capabilities. When NRG_RST_CNT is lower than 2, the ADS feature cannot be enabled. Default is 4 seconds. *Note: This timer only takes effect when **NO_NRG_RST** is set.*
FORCE_RST	7	RW	**Force Reset of Downwshift Process** Setting this bit to 1 immediately resets the ANEG advertised capabilities to the maximum GPY capabilities.

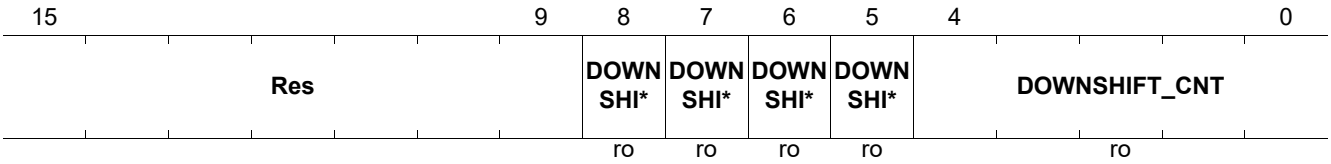
Field	Bits	Type	Description (cont'd)
DOWNSHIFT_THR	6:2	RW	**NBASE-T Downshift Training Counter Threshold** dsh_thr variable in NBASE-T specification This is a 4-bit counter from 0 to 15 used to control the number of training cycles allowed for linkup, otherwise downshift.
DOWNSHIFT_EN	1	RW	**NBASE-T Downshift Enable** dsh_en variable in NBASE-T specification 0_B **DISABLE** Disable NBT downshift. 1_B **ENABLE** Enable NBT downshift.
NO_NRG_RST	0	RW	**Advertise All Speeds if No Energy Detected** When no energy is detected, this resets to advertise all speeds. Energy variable in NBASE-T specification 0_B **DISABLE** Do not reset speeds advertised when no energy is detected. 1_B **ENABLE** Reset speeds advertised when no energy is detected.

NBASE-T Downshift Status Register (Register 30.11)

IEEE Standard Register=30.11

VSPEC1_NBT_DS_STA **Reset Value**

NBASE-T Downshift Status Register (Register 30.11) **0000_H**



Field	Bits	Type	Description
DOWNSHIFT_1G	8	RO	**Downshift from 1G to Lower Speed**
DOWNSHIFT_2G5	7	RO	**Downshift from 2.5 G to Lower Speed**
DOWNSHIFT_5G	6	RO	**Downshift 5G to Lower Speed** Not supported by the GPY.
DOWNSHIFT_10G	5	RO	**Downshift 10G to Lower Speed** Not supported by the GPY.
DOWNSHIFT_CNT	4:0	RO	**Training Attempt Counter** Counts training attempts to select the operating speed. dsh_cnt state variable in NBASE-T specification

Packet Manager Control (Register 30.12)

IEEE Standard Register=30.12

Control the Packet Manager Configuration

VSPEC1_PM_CTRL **Reset Value**

Packet Manager Control (Register 30.12) **0083_H**

15 12	11	10 9 8	7	6 5	4	3	2	1	0
Res	MDINT_M*	Res	MAC_FRE*	SYNCE_CLK	SYNCE_EN	PTP_1588*	PTP_1588*	RES	RES
	rw		rw	rw	rw	rw	rw	ro	rw

Field	Bits	Type	Description
MDINT_MODE	11	RW	**MDIO Interrupt Mode** Sets the mode of the MDIO interrupt signal. 0_B **TRI** Tristate modeMDIO interrupt signal is tristate when interrupt inactive. It will be driven only when interrupt is active. 1_B **PP** Push-pull modeMDIO interrupt signal is constantly driven.
MAC_FREQ_TUNE	7	RW	**Control Bit to Tune Frequency of MACs In USXGMII Mode** During the stress test of 100% bi-directional traffic for longer duration, the recommendation is to run the MACs at a slightly higher frequency to avoid packet drops in USXGMII mode. It is recommended to call the API for the correct programming sequence. In non-USXGMII mode, this bit has no effect. 0_B **PPM_0** MACs operate at frequency corresponding to line rate. 1_B **PPM_100** Long Duration Stress Test condition. MACs operate at frequency +100 ppm corresponding to line rate.
SYNCE_CLK	6:5	RW	**Configure the SyncE Clock Frequency Class** It is recommended to configure SyncE through the API. Write access to these bits are blocked in devices that do not support SyncE. 00_B **PSTN** SyncE clock frequency is PSTN class: 8 kHz. 01_B **EEC1** SyncE clock frequency is EEC-1 class: 2.048 MHz. 10_B **EEC2** SyncE clock frequency is EEC-2 class: 1.544 MHz. 11_B **RES** Reserved
SYNCE_EN	4	RW	**Enable SyncE Feature** Applicable to SyncE capable devices only. SyncE is disabled by default and it is recommended to enable SyncE through the API. Write access to this bit is blocked in devices that do not support SyncE. 0_B **DISABLE** Disable SyncE. 1_B **ENABLE** Enable SyncE.
PTP_1588_STEP	3	RW	**Configure 1588 Time Stamping Mode** 0_B **TWO_STEP** Two step time stamping 1_B **ONE_STEP** One step time stamping

Field	Bits	Type	Description (cont'd)
PTP_1588_EN	2	RW	**Enable Sync 1588 PTP Feature** 0_B **DISABLE** Disable 1_B **ENABLE** Enable
RES	1	RO	**Reserved** Ignore when read.
RES	0	RW	**Reserved**

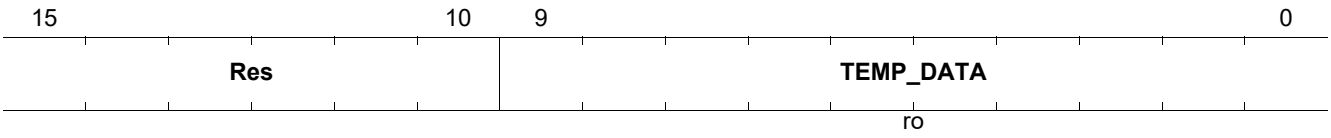
Temperature Code (Register 30.14)

The junction temperature code that is converted by the GPYAPI into a temperature in degrees Celsius.

IEEE Standard Register=30.14

VSPEC1_TEMP_STA **Reset Value**

Temperature Code (Register 30.14) **0000_H**



Field	Bits	Type	Description
TEMP_DATA	9:0	RO	**Code for Junction Temperature** This code is converted to the equivalent temperature in degrees Celsius by the GPY API driver. The STA must take thermal mitigation measures when the junction temperature exceeds the normal operating range. The code is invalid when the value is 0x0000. Conversion formula: T in Celsius = (-2.5761E-11)*N^4 + (9.7332E-8)*N^3+ (-1.9165E-04)*N^2+(3.0762E-1)*N +(-5.2156E+1) , with N = decimal value of the code TEMP_DATA For Tj = -40 degC, TEMP_DATA = 40.5 (decimal) For Tj= +125 degC, TEMP_DATA = 912 (decimal)

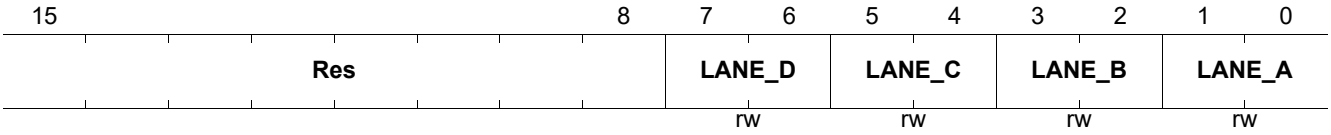
ASP Mapping to Physical Lanes (Register 30.20)

This register offers a programmable option to map physical lanes A, B, C, and D of the TPI to the ASPs. Each ASP must be mapped to each lane.

IEEE Standard Register=30.20

VSPEC1_LANE_ASP_MAP **Reset Value**

ASP Mapping to Physical Lanes (Register 30.20) **$00E4_H$**



Field	Bits	Type	Description
LANE_D	7:6	RW	**Map Physical Lane-D to the ASP** 00_B **ASPA** Map Physical Lane-D to the ASP-A. 01_B **ASPB** Map Physical Lane-D to the ASP-B. 10_B **ASPC** Map Physical Lane-D to the ASP-C. 11_B **ASPD** Map Physical Lane-D to the ASP-D.
LANE_C	5:4	RW	**Map Physical Lane-C to the ASP** 00_B **ASPA** Map Physical Lane-C to the ASP-A. 01_B **ASPB** Map Physical Lane-C to the ASP-B. 10_B **ASPC** Map Physical Lane-C to the ASP-C. 11_B **ASPD** Map Physical Lane-C to the ASP-D.
LANE_B	3:2	RW	**Map Physical Lane-B to the ASP** 00_B **ASPA** Map Physical Lane-B to the ASP-A. 01_B **ASPB** Map Physical Lane-B to the ASP-B. 10_B **ASPC** Map Physical Lane-B to the ASP-C. 11_B **ASPD** Map Physical Lane-B to the ASP-D.
LANE_A	1:0	RW	**Map Physical Lane-A to the ASP** 00_B **ASPA** Map Physical Lane-A to the ASP-A. 01_B **ASPB** Map Physical Lane-A to the ASP-B. 10_B **ASPC** Map Physical Lane-A to the ASP-C. 11_B **ASPD** Map Physical Lane-A to the ASP-D.

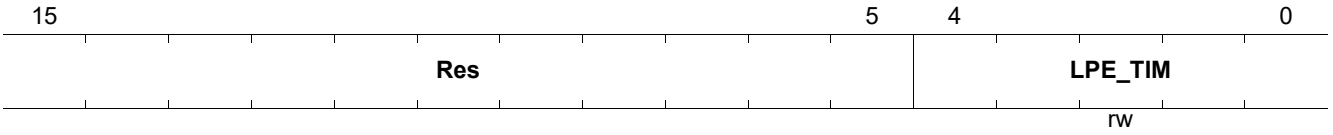
Time to Enter Low Power (Register 30.21)

Programmable option to delay the time taken to enter low power mode. This register has no effect on master port since it never enters low power mode.

IEEE Standard Register=30.21

VSPEC1_LOW_POWER_ENTRY_TIME **Reset Value**

Time to Enter Low Power (Register 30.21) **0001_H**



Field	Bits	Type	Description
LPE_TIM	4:0	RW	**Low Power Entry Time** This is the time taken from detection of no activity on the line to the low power completion. The granularity is 4 seconds and adds on to the initial time 2.4 seconds to 5.6 seconds.

6.5 Vendor Specific 2 Device for MMD=0x1F

This register file contains the GPY-specific registers for MMD=31 (decimal).

Table 31 Registers Overview

Register Short Name	Register Long Name	Reset Value
VPSPEC2_WOL_CTL	Wake-on-LAN Control Register (Register 31.3590)	0000_H
VPSPEC2_WOL_AD01	Wake-on-LAN Address Byte 0 and 1 (Register 31.3592)	0000_H
VPSPEC2_WOL_AD23	Wake-on-LAN Address Byte 2 and 3 (Register 31.3593)	0000_H
VPSPEC2_WOL_AD45	Wake-on-LAN Address Byte 4 and 5 (Register 31.3594)	0000_H
VPSPEC2_WOL_PW01	Wake-on-LAN SecureON Password Byte 0 (Register 31.3595)	0000_H
VPSPEC2_WOL_PW23	Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)	0000_H
VPSPEC2_WOL_PW45	Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)	0000_H

6.5.1 Vendor Specific 2 Device for MMD=0x1F

This section describes all the VSPEC2 registers in detail.

Wake-on-LAN Control Register (Register 31.3590)

This is the wake-on-LAN control register. Redirected to PCS_PDI_WOL_CTL.

IEEE Standard Register=31.3590

VPSPEC2_WOL_CTL **Reset Value**

Wake-on-LAN Control Register (Register 31.3590) **0000_H**

15 … 3	2	1	0
Res	SPWD_EN	RES	EN
	rw	ro	rw

Field	Bits	Type	Description
SPWD_EN	2	RW	**Secure-ON Password Enable** When this bit is set to enabled, the SecureON password is checked after 16 MAC address repetitions. 0_B **DISABLED** SecureON password check is disabled. 1_B **ENABLED** SecureON password check is enabled.
RES	1	RO	**Reserved** Must always be written to zero.
EN	0	RW	**Enables the Wake-on-LAN Functionality** When wake-on-LAN is enabled, the PHY scans for the configured magic packet and indicates its reception via the register bit ISTAT.WOL and optionally also via interrupt. 0_B **DISABLED** Wake-on-LAN functionality is disabled, 1_B **ENABLED** Wake-on-LAN functionality is enabled,

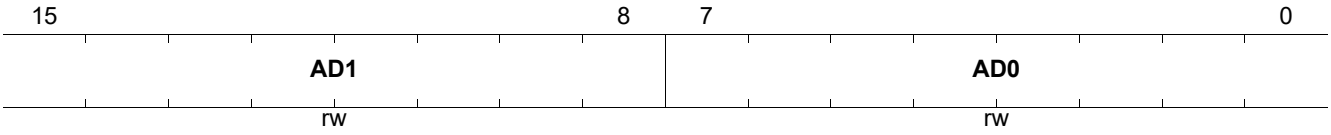
Wake-on-LAN Address Byte 0 and 1 (Register 31.3592)

Wake-on-LAN Address Byte 0 and 1. Redirected to PCS_PDI_WOL_AD01

IEEE Standard Register=31.3592

VPSPEC2_WOL_AD01 **Reset Value**

Wake-on-LAN Address Byte 0 and 1 (Register 31.3592) **0000_H**



Field	Bits	Type	Description
AD1	15:8	RW	**Address Byte 1** Defines byte 1 of the WoL-designated MAC address to which the PHY is sensitive.
AD0	7:0	RW	**Address Byte 0** Defines byte 0 of the WoL-designated MAC address to which the PHY is sensitive.

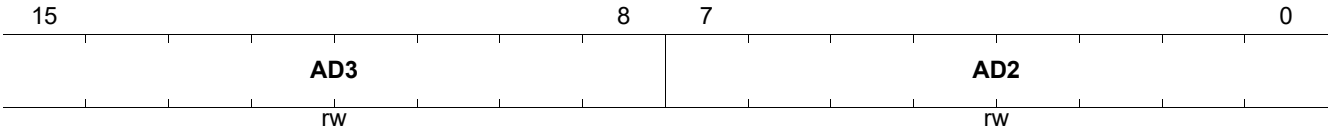
Wake-on-LAN Address Byte 2 and 3 (Register 31.3593)

Wake-on-LAN Address Byte 2 and 3. Redirected to PCS_PDI_WOL_AD23

IEEE Standard Register=31.3593

VPSPEC2_WOL_AD23 **Reset Value**

Wake-on-LAN Address Byte 2 and 3 (Register 31.3593) **0000_H**



Field	Bits	Type	Description
AD3	15:8	RW	**Address Byte 3** Defines byte 3 of the WoL-designated MAC address to which the PHY is sensitive.
AD2	7:0	RW	**Address Byte 2** Defines byte 2 of the WoL-designated MAC address to which the PHY is sensitive.

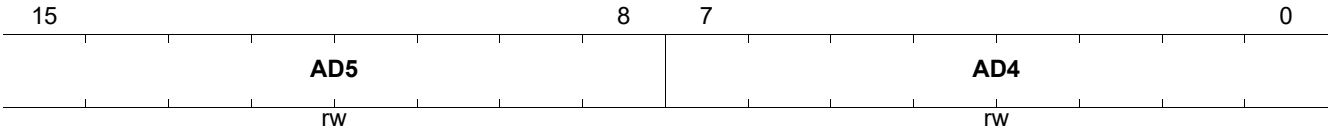
Wake-on-LAN Address Byte 4 and 5 (Register 31.3594)

Wake-on-LAN Address Byte 4 and 5. Redirected to PCS_PDI_WOL_AD45

IEEE Standard Register=31.3594

VPSPEC2_WOL_AD45 **Reset Value**

Wake-on-LAN Address Byte 4 and 5 (Register 31.3594) **0000_H**



Field	Bits	Type	Description
AD5	15:8	RW	**Address Byte 5** Defines byte 5 of the WoL-designated MAC address to which the PHY is sensitive.
AD4	7:0	RW	**Address Byte 4** Defines byte 4 of the WoL-designated MAC address to which the PHY is sensitive.

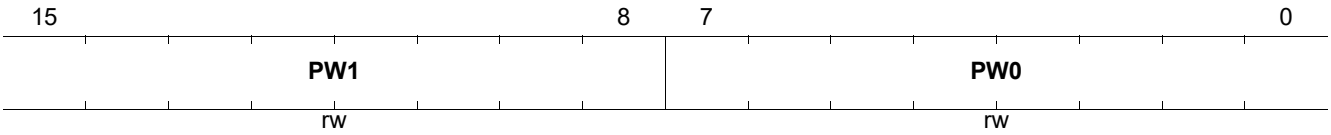
Wake-on-LAN SecureON Password Byte 0 (Register 31.3595)

Wake-on-LAN SecureON Password Byte 0. Redirected to PCS_PDI_WOL_PWD01

IEEE Standard Register=31.3595

VPSPEC2_WOL_PW01 **Reset Value**

Wake-on-LAN SecureON Password Byte 0 (Register 31.3595) **0000_H**



Field	Bits	Type	Description
PW1	15:8	RW	**SecureON Password Byte 1** Defines byte 1 of the WoL-designated SecureON password to which the PHY is sensitive.
PW0	7:0	RW	**SecureON Password Byte 0** Defines byte 0 of the WoL-designated SecureON password to which the PHY is sensitive.

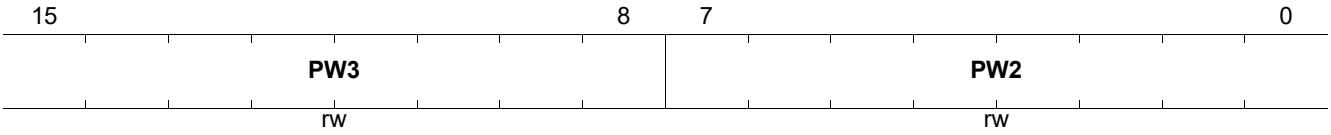
Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596)

Wake-on-LAN SecureON Password Byte 2 and 3. Redirected to PCS_PDI_WOL_PWD23

IEEE Standard Register=31.3596

VPSPEC2_WOL_PW23 **Reset Value**

Wake-on-LAN SecureON Password Byte 2 and 3 (Register 31.3596) **0000_H**



Field	Bits	Type	Description
PW3	15:8	RW	**SecureON Password Byte 3** Defines byte 3 of the WoL-designated SecureON password to which the PHY is sensitive.
PW2	7:0	RW	**SecureON Password Byte 2** Defines byte 2 of the WoL-designated SecureON password to which the PHY is sensitive.

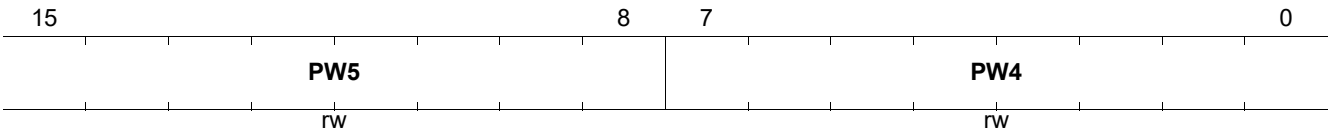
Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597)

Wake-on-LAN SecureON Password Byte 4 and 5. Redirected to PCS_PDI_WOL_PWD45

IEEE Standard Register=31.3597

VPSPEC2_WOL_PW45 **Reset Value**

Wake-on-LAN SecureON Password Byte 4 and 5 (Register 31.3597) **0000_H**



Field	Bits	Type	Description
PW5	15:8	RW	**SecureON Password Byte 5** Defines byte 5 of the WoL-designated SecureON password to which the PHY is sensitive.
PW4	7:0	RW	**SecureON Password Byte 4** Defines byte 4 of the WoL-designated SecureON password to which the PHY is sensitive.

7 Chip Electrical Characteristics

This chapter defines the electrical characteristics of the Gigabit Ethernet PHY.

7.1 Absolute Maximum Ratings

Table 32 shows the absolute maximum ratings for the Gigabit Ethernet PHY.

Table 32 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature Limits	T_{STG}	-55.0	–	125.0	°C	–
Soldering Temperature	T_{SOL}	–	–	260.0	°C	Compliance with Pb free re-flow soldering profile as J-STD-020D
Moisture Level 3 Temperature Limits	T_{ML3}	–	–	260.0	°C	According to IPS J-STD 020
Absolute Junction Temperature	T_{JABS}	-40.0		125	°C	Thermal solution must ensure that T_J never exceeds T_{JABS} max. The chip resets the device when T_J > T_{JABS} to prevent any damage occurring.
DC Voltage Limits on VDDP3V3_PAD Pins	V_{DDP3V3}	-0.5	–	+3.63	V	Generic PAD V_{HIGH} supply
DC Voltage Limits on VDDP_PAD Pins	V_{DDP}	-0.5	–	+3.63	V	Multi Voltage PAD V_{HIGH} supply
DC Voltage Limits on VDDA3V3_0, VDDA3V3_1, VDDA3V3_2, VDDA3V3_3 Pins	V_{DDA3V3}	-0.5	–	+3.63	V	Chip analog V_{HIGH} supply
DC Voltage Limits on VDDA3V3_XO, VDDA3V3_CDB, VDD3V3_LDO Pins	$V_{DDA3V3XO}$ $V_{DDA3V3CDB}$ $V_{DD3V3LDO}$	-0.5	–	+3.63	V	Chip clocking V_{HIGH} supply
DC Voltage Limits on SVPH3V3 Pins	V_{PH}	-0.5	–	+3.63	V	SGMII V_{HIGH} supply
DC Voltage Limits on UVPHA1V8, VDDA1V8_PLL Pins	V_{UPH} $V_{DDA1V8PLL}$	-0.5	–	+1.98	V	USXGMII, LJ PLL V_{HIGH} supply
DC Voltage Limits on VDDA0V9_0, VDDA0V9_1, VDDA0V9_2, VDDA0V9_3, VDDA0V9_CDB, VDDD0V9_PLL Pins	V_{DDA0V9} $V_{DDA0V9CDB}$ $V_{DDD0V9PLL}$	-0.5	–	+1.05	V	Chip V_{LOW} supply, LJ PLL V_{LOW} supply
DC Voltage Limits on VDD0V9_COR Pins	V_{DD}	-0.5	–	+1.05	V	Chip core V_{LOW} supply
DC Voltage Limits on SVP0V9, UVP0V9 Pins	V_P V_{UP}	-0.5	–	+1.05	V	SGMII, USXGMII V_{LOW} supply

Table 32 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC Voltage Limits on Any Other Pins[1] with Respect to Ground	V_{DC}	-0.5	–	V_{DDP3V3}+ 0.5	V	Unless specified otherwise
XTAL1 Input Voltage	V_{XTAL1}	-0.30	1.8	2.0	V	–
ESD HBM Robustness	$V_{ESD,HBM}$	–	–	1000.0	V	According to ANSI/ESDA/JEDEC JS-001-2014
ESD CDM Robustness	$V_{ESD,CDM}$	–	–	250.0	V	According to ANSI/ESDA/JEDEC JS-002-2014

1) This means any pin which is not a supply pin out of one of the domains: V_{DDP}, V_{PH}, V_P, V_{DDA3V3}, $V_{DDA3V3XO}$, $V_{DDA3V3CDB}$,$V_{DDA3V3AON}$, V_{DDA0V9}, V_{DD}, $V_{DD3V3LDO}$.

Attention: Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

7.2 Operating Range

Table 33 defines the limit values of voltages and temperature which may be applied to guarantee proper operation of the Gigabit Ethernet PHY.

Table 33 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature under Bias	T_A	0	–	70	°C	The thermal design must ensure that the maximum junction temperature is not exceeded. The use of a heat sink may be suitable.
Junction Temperature	T_j	–	–	110.0	°C	Thermal solution must ensure that T_j remains within operating range and never exceeds maximum absolute ratings.
Generic Pad Supply Voltage	V_{DDP3V3}	3.135	3.30	3.46	V	Generic PAD V_{HIGH} supply
Multi Voltage Pad Supply Voltage	V_{DDP}	3.135	3.30	3.46	V	Multi Voltage PAD V_{HIGH} supply
Analog High Supply Voltage	V_{DDA3V3}	3.135	3.30	3.46	V	Chip analog V_{HIGH} supply
XO High Supply Voltage	$V_{DDA3V3XO}$	3.135	3.30	3.46	V	Chip clocking V_{HIGH} supply
CDB High Supply Voltage	$V_{DDA3V3CDB}$	3.135	3.30	3.46	V	Chip clocking V_{HIGH} supply
LDO High Supply Voltage	$V_{DDA3V3LDO}$	3.135	3.30	3.46	V	Chip clocking V_{HIGH} supply
SGMII High Supply Voltage	V_{PH}	3.135	3.30	3.46	V	SGMII V_{HIGH} supply
USXGMII High Supply Voltage	V_{UPH}	1.71	1.80	1.89	V	USXGMII V_{HIGH} supply
LJ PLL High Supply Voltage	$V_{DDA1V8PLL}$	1.71	1.80	1.89	V	LJ PLL V_{HIGH} supply
Analog Low Supply Voltage	V_{DDA0V9}	0.903	0.95	0.998	V	Chip analog V_{LOW} supply
CDB Low Supply Voltage	$V_{DDA0V9CDB}$	0.903	0.95	0.998	V	Chip clocking V_{LOW} supply
LJ PLL Low Supply Voltage	$V_{DDD0V9PLL}$	0.903	0.95	0.998	V	LJ PLL V_{LOW} supply
Chip Core Supply Voltage	V_{DD}	0.903	0.95	0.998	V	Chip core V_{LOW} supply
SGMII Low Supply Voltage	V_P	0.903	0.95	0.998	V	SGMII V_{LOW} supply
USXGMII Low Supply Voltage	V_{UP}	0.903	0.95	0.998	V	USXGMII V_{LOW} supply
Ground	V_{SS}	0.00	0.00	0.00	V	–

Attention: Operations above the maximum values listed here for extended periods may adversely affect long-term reliability of the device.

7.3 Typical Power Consumption

Table 34 and Table 35 list the typical power consumption for different modes. Typical power is the power consumed by a nominal process device, nominal supply voltages, at 25°C ambient temperature and a CAT5e link segment.

The conditions for Link-up are full speed and bidirectional, full duplex traffic on all 4 ports.

Power numbers are given for the two SerDes configurations:

- SGMII - Table 34
- USXGMII - Table 35

Table 34 Typical Power Consumption in SGMII Configuration

	3.3 V V_{HIGH} Domain Current	0.95 V V_{LOW} Domain Current	Chip Power
Unit	**mA**	**mA**	**W**
2.5GBASE-T Link-Up, 100 m Cable	369	2189	3.30
2.5GBASE-T Link-Up, 30 m Cable	347	1796	2.85
2.5GBASE-T EEE	338	1437	2.48
1000BASE-T Link-Up, 100 m Cable	279	1067	1.93
1000BASE-T EEE	109	593	0.92
100BASE-TX Link-Up, 100 m Cable	145	516	0.97
100BASE-TX EEE	78	475	0.71
10BASE-Te Link-Up, 100 m Cable	103	449	0.77
Cable Unplugged - ANEG	110	473	0.81
Cable Unplugged - LP	42	206	0.33
Reset	6	26	0.04

Table 35 Typical Power Consumption in USXGMII Configuration

	3.3 V V_{HIGH} Domain Current	1.8 V V_{LOW} Domain Current	0.95 V V_{LOW} Domain Current	Chip Power
Unit	**mA**	**mA**	**mA**	**W**
2.5GBASE-T Link-Up, 100 m Cable	337	84	2291	3.44
2.5GBASE-T Link-Up, 30 m Cable	304	78	2050	3.09
2.5GBASE-T EEE	281	82	1500	2.50
1000BASE-T Link-Up, 100 m Cable	228	81	1098	1.94
1000BASE-T EEE	48	80	629	0.90
100BASE-TX Link-Up, 100 m Cable	95	80	542	0.97
100BASE-TX EEE	27	80	501	0.71
10BASE-Te Link-Up, 100 m Cable	53	80	476	0.77
Cable Unplugged - ANEG	50	78	455	0.74
Cable Unplugged - Low Power	29	78	289	0.51
Reset	6	0	26	0.04

7.4 Maximum Thermal Design Power

Table 36 lists the maximum Thermal Design Power (TDP). The TDP is the power consumption for a full traffic load and worst-case process, supply voltage, cable, and temperature conditions. This value is relevant to design the thermal solution.

Table 36 Maximum Power Consumption

	SGMII Mode	USXGMII Mode
Unit	**W**	**W**
Maximum Chip Power at Maximum Operating Range	6.06	6.06

Note: With a properly designed thermal solution (heat sink), it is unlikely that Tj exceeds the maximum operating junction temperature. An excess is reported in the MDIO register VSPEC1_TMP_STA and the STA can initiate a renegotiation to a lower link rate to get Tj back into the operating temperature range.

7.5 Peak Current

Table 37 provides the peak current to dimension the power supply. It is the maximum short term current consumption per rail for a full traffic load and worst-case process, supply voltage and temperature conditions that may occur in any operating state of the device. The peak current can be higher than the steady state current, for instance in training phases of the internal filters.

Table 37 Peak Current Per Rail

3.3 V V_{HIGH} Domain Current	1.8 V V_{LOW} Domain Current (UXSGMII only)	0.95 V V_{LOW} Domain Current
mA	**mA**	**mA**
600	100	5000

7.6 DC Characteristics

These sections document the DC characteristics of the Gigabit Ethernet PHY external interfaces.

7.6.1 Digital Interfaces

This section defines the DC characteristics of the GPIO interface as follows:

- General Purpose IO
- MDIO
- SPI
- Interrupts
- Clock Input and Outputs
- LED
- JTAG

Any subsequent reset time to keep HRTSN signal low is 100 ns.

Table 38 summarizes the DC characteristics for V_{DDP}=3.3 V.

Table 38 DC Characteristics of the GPIO Interfaces (VDDP=3.3 V)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	0.7*V_{DDP}	–	V_{DDP}+0.3	V	–
Input Low Voltage	V_{IL}	–0.3	–	0.3*V_{DDP}	V	–
Output High Voltage	V_{OH}	V_{DDP}-0.4	–	–	V	I_{OH}= 2, 4, 8, 12 mA
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL}= 2, 4, 8, 12 mA

7.6.2 Twisted Pair Interface

The TPI conforms to the specifications of 10BASE-Te (Clause 14), 100BASE-TX (Clause 25), 1000BASE-T (Clause 40) and 2.5GBASE-T (Clause 126) given in **[4]**, **[6]**, and **[7]**.

7.6.3 Built-in Temperature Sensor

Table 39 lists the parameters of the integrated temperature sensor.

Table 39 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature Range	T_{range}	-40		125	°C	Thermal mitigation measures must ensure that T_j remains within the operating range. When T_j exceeds the maximum ratings, the GPY performs a self-reset to prevent damage, and the next ANEG is re-started advertising a lower speed.
Resolution		–	10	–	bits	–
Accuracy		-5	–	+5	°C	–

7.7 AC Characteristics

These sections investigate the AC characteristics of the external interfaces.

T_A = 0 to 70°C, V_{DDP} = 3.3 V ± 5%, V_{SS} = 0 V

Timing measurements are made at minimum V_{IH} for a logical 1 and at maximum V_{IL} for a logical 0.

Figure 16 shows the AC testing input/output waveforms. The load capacitors are according to the specific interface standard, all non-specified interfaces use 30 pF as assumed loading.

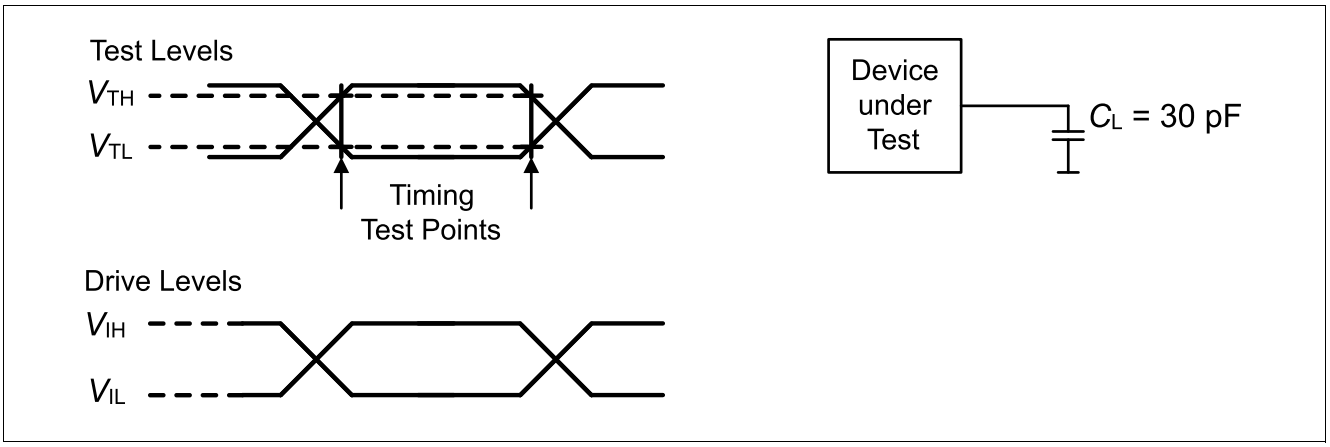


Figure 16 Input/Output Waveform for AC Tests

7.7.1 Power Up and Power Down Sequence

In this configuration, both V_{HIGH}, V_{UPH}, and V_{LOW} are supplied externally.

The High Voltage domain V_{HIGH} must always be at a higher voltage level than the Low Voltage Domain V_{LOW}. V_{HIGH} must always be at a higher voltage than V_{UPH}, and V_{UPH} must always be at a higher voltage than the Low Voltage Domain V_{LOW}.

V_{HIGH}, V_{UPH}, and V_{LOW} ramp-up times (t_{vh_rampup}, t_{vuph_rampup}, and t_{vl_rampup}) must be above the minimum requirement.

All the supply domains V_{HIGH}, V_{UPH}, and V_{LOW} must be stabilized before releasing the reset HRSTN.

During the power-down sequence, V_{HIGH} ramp down time must not be shorter than the minimum requirement.

The device reset HRSTN must be held for a t_{reset} time after the stabilization of the power supplies and pin strap values. When reset is released, the integrated PLL locks and the device boots up.

The GPY241 supports an asynchronous hardware reset HRSTN. **Table 40** lists the timing requirements of the power supply pins. The timings refer to the signal sequence waveforms depicted in **Figure 17** in SGMII mode of operation, and **Figure 18** in USXGMII mode of operation.

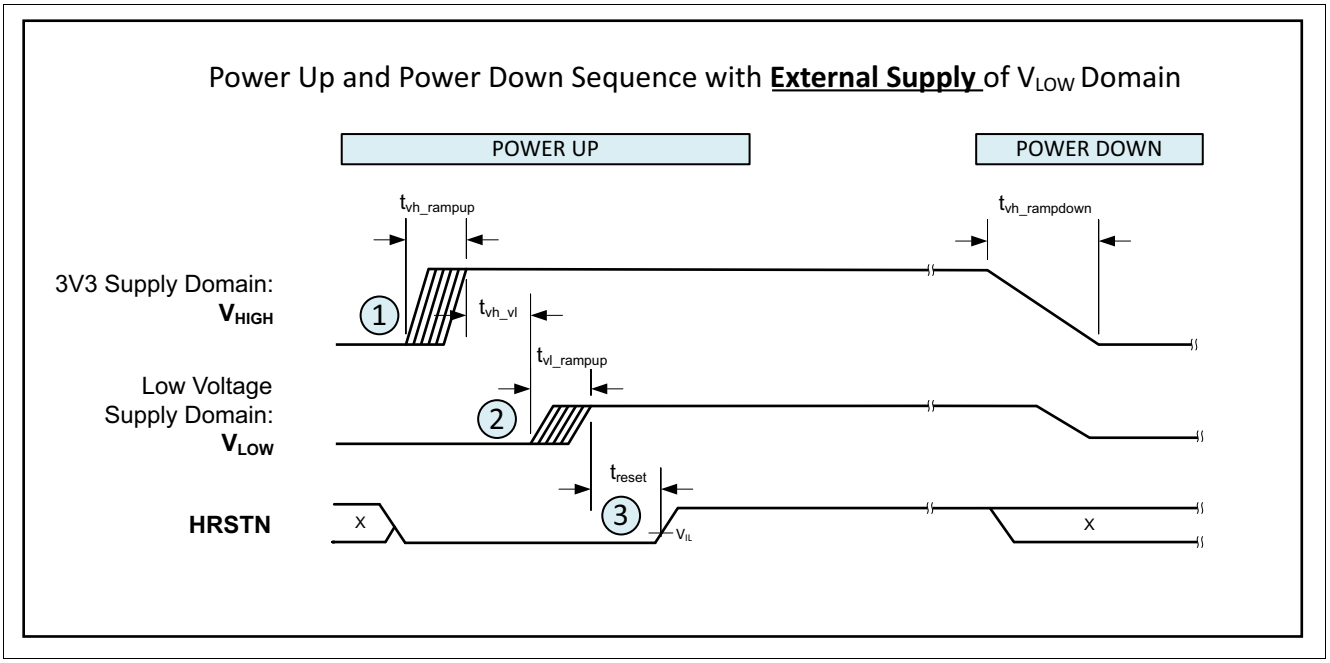


Figure 17 Timing Diagram for the Reset Sequence in SGMII Mode

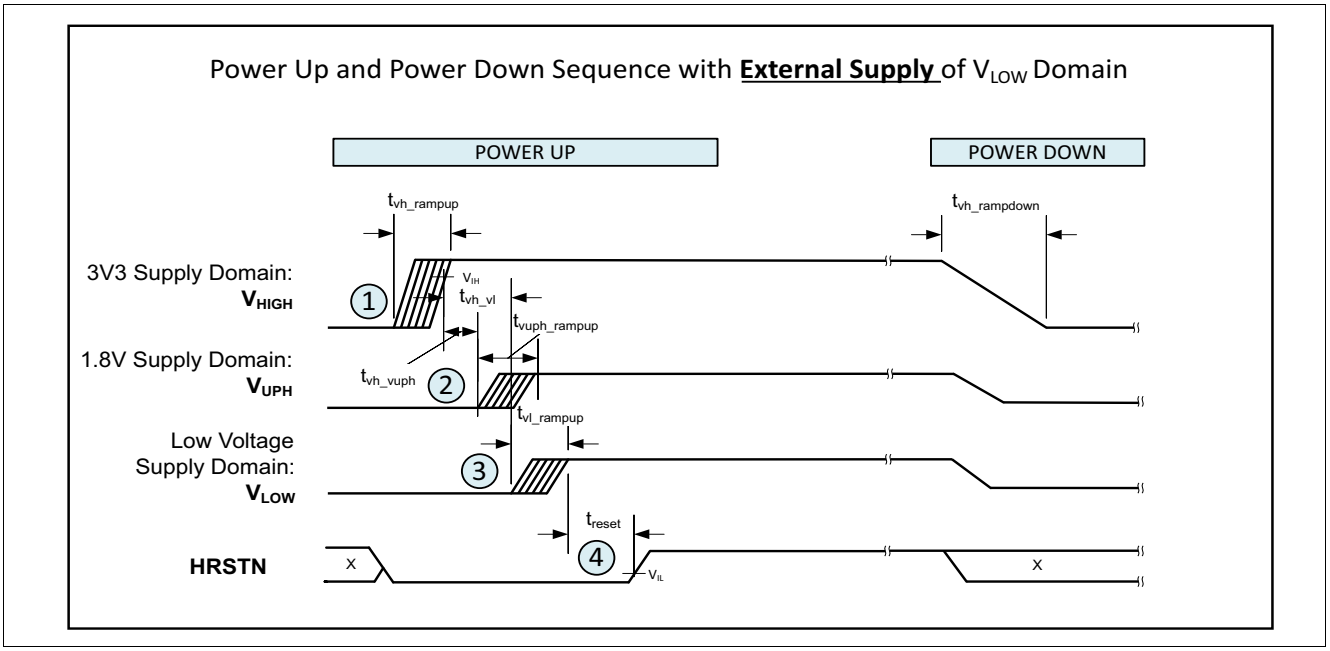


Figure 18 Timing Diagram for the Reset Sequence in USXGMII Mode

Table 40 Power Supply Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{HIGH} Domain Ramp Up	t_{vh_rampup}	50	–	–	µs	To avoid current surge.
V_{UPH} Domain Ramp Up	t_{vuph_rampup}	50	–	–	µs	To avoid current surge.
V_{LOW} Domain Ramp Up	t_{vl_rampup}	50	–	–	µs	To avoid current surge.
Delay between V_{HIGH} and V_{LOW} Domains Voltage Ramp Up	t_{vh_vl}	100	-	-	µs	The V_{LOW} voltage must never be higher than V_{HIGH} voltage
Delay between V_{HIGH} and V_{UPH} Domains Voltage Ramp Up	t_{vh_vuph}	50	-	-	µs	The V_{UPH} voltage must never be higher than V_{HIGH} voltage.
V_{HIGH} Domain Ramp Down	$t_{vh_rampdown}$	1.0	–	–	ms	The V_{LOW} voltage must never be higher than V_{HIGH} voltage.
Reset Time after V_{HIGH} and V_{LOW} Domains are Stabilized	t_{reset}	100	–	–	ns	HRSTN must be released after the power supplies have stabilized.

Rise and ramp down times are from 10% to 90% marks for V_{HIGH}, V_{LOW}, and HRSTN.

7.7.2 Input Clock

Table 41 lists the input clock requirements when not using a crystal, i.e., when an external reference clock is injected into the XTAL1 pin of the Gigabit Ethernet PHY. The requirements include the nominal frequency, frequency deviation, duty cycle, and signal characteristics. When a crystal is applied to generate the reference clock using the integrated XO, the clock requirements stated here are met explicitly as long as the specification for the crystal is satisfied.

Table 41 AC Characteristics of Input Clock on XTAL1 Pin

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz Input	f_{clk25}	–	25.0	–	MHz	–
Frequency Deviation[1)]		-50.0	–	+50.0	ppm	–
Duty Cycle		40.0	50.0	60.0	%	–
Rise/Fall Times		–	–	10.0	ns	–
Input Long Term Jitter (Jrms)		–	4.0	7.0	ps	1 kHz...10 MHz
Input High Voltage		0.6	–	2.0	V	–
Input Low Voltage		-0.3	–	0.2	V	–
Load Capacitance		–	15	–	pF	–

1) Including the frequency stability tolerance due to temperature, and aging effects over the product lifetime of 5 years

7.7.3 Power Supply Rail Requirements

Table 42 lists the required characteristics of the power supplies.

Table 42 AC Characteristics of the Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply Ripple on VDDA0V9, VDDA0V9PLL, VDDA0V9CDB	$R_{VDDA0V9}$ $R_{VDDA0V9}$ $R_{VDDA0V9}$	–	–	60.0	mV	Peak to Peak value
Power Supply Ripple on VP, VUP	R_{VP} R_{VUP}	–	–	60.0	mV	Peak to Peak value
Power Supply Ripple on VDD	R_{VDD}	–	–	60.0	mV	Peak to Peak value
Power Supply Ripple on VDDP	R_{VDDP}	–	–	100.0	mV	Peak to Peak value
Power Supply Ripple on VDDA3V3	$R_{VDDA3V3}$	–	–	100.0	mV	Peak to Peak value
Power Supply Ripple on VDDA3V3XO	$R_{VDDA3V3XO}$	–	–	100.0	mV	Peak to Peak value
Power Supply Ripple on VDDA3V3CDB	$R_{VDDA3V3CDB}$	–	–	100.0	mV	Peak to Peak value
Power Supply Ripple on VPH	R_{VPH}	–	–	100.0	mV	Peak to Peak value
Power Supply Ripple on VDD3V3LDO	$R_{VDD3V3LDO}$	–	–	100.0	mV	Peak to Peak value

7.7.4 MDIO Interface

Figure 19 shows a timing diagram of the MDIO interface for a clock cycle in the read-, write- and turnaround-modus, respectively. The timing measures are annotated. **Table 43** summarizes the defined absolute values.

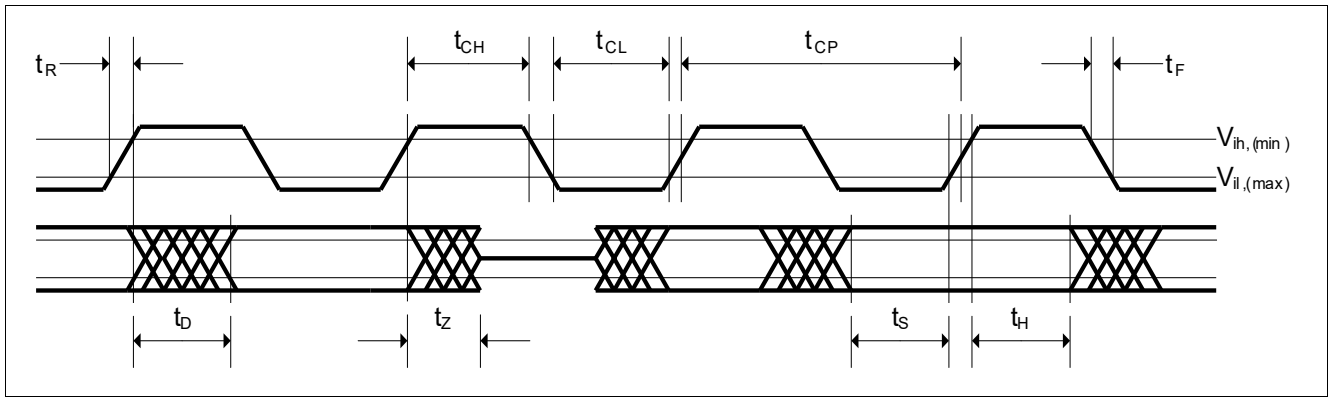


Figure 19 Timing Diagram for the MDIO Interface

Table 43 Timing Characteristics of the MDIO Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC High Time	t_{CH}	10.0	–	–	ns	Given timings are all subject to the MDC at the pin of the GPY241.
MDC Low Time	t_{CL}	10.0	–	–	ns	
MDC Clock Period	t_{CP}	40.0	400.0	–	ns	
MDC Clock Frequency[1)]	t_{CP}	–	2.5	25.0	MHz	
MDC Rise Time	t_R	–	–	5.0	ns	
MDC Fall Time	t_F	–	–	5.0	ns	
MDIO Input Setup Time subject to ↑ MDC	t_S	10.0	–	–	ns	GPY241 Receive
MDIO Input Hold Time subject to ↑ MDC	t_H	10.0	–	–	ns	GPY241 Receive
MDIO Output Delay Time subject to ↑ MDC	t_D	0.0	–	10	ns	GPY241 Transmit
Standard at 2.5 MHz						
MDIO Output Delay subject to ↑ MDC	t_D	0.0	–	300.0	ns	PHY Transmit

1) MDC clock supports range of frequencies, up to 25 MHz. Default/typical frequency is 2.5 MHz.

7.7.5 Serial Peripheral Interface (SPI)

Figure 20 shows the SPI master interface timing.

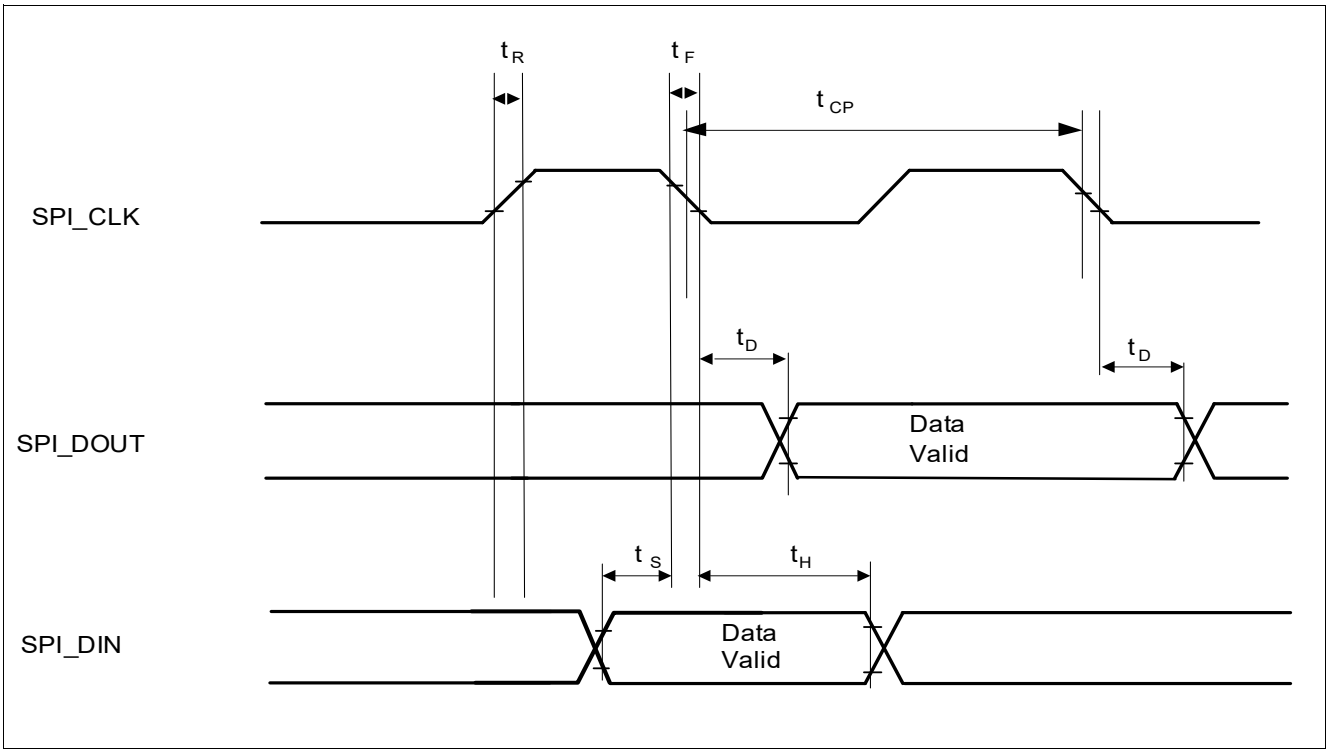


Figure 20 SPI Master Interface Timing

Table 44 SPI Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Master Mode						
Tx Data Output Delay	t_D	0	–	4	ns	–
Rx Data Input Setup Time	t_S	7	–	–	ns	–
Rx Data Hold Time	t_H	0	–	–	ns	–
SPI Clock Period (Master Mode)	t_{CP}	20	–	50	ns	-
SPI Clock Rise Time	t_R	–	–	5.0	ns	10% - 90%
SPI Clock Fall Time	t_F	–	–	5.0	ns	10% - 90%
SPI Clock Duty Cycle	D	45	–	55	%	–

7.7.6 JTAG Interface

The JTAG test interface is used for debugging the GPHYCPU and boundary scan.

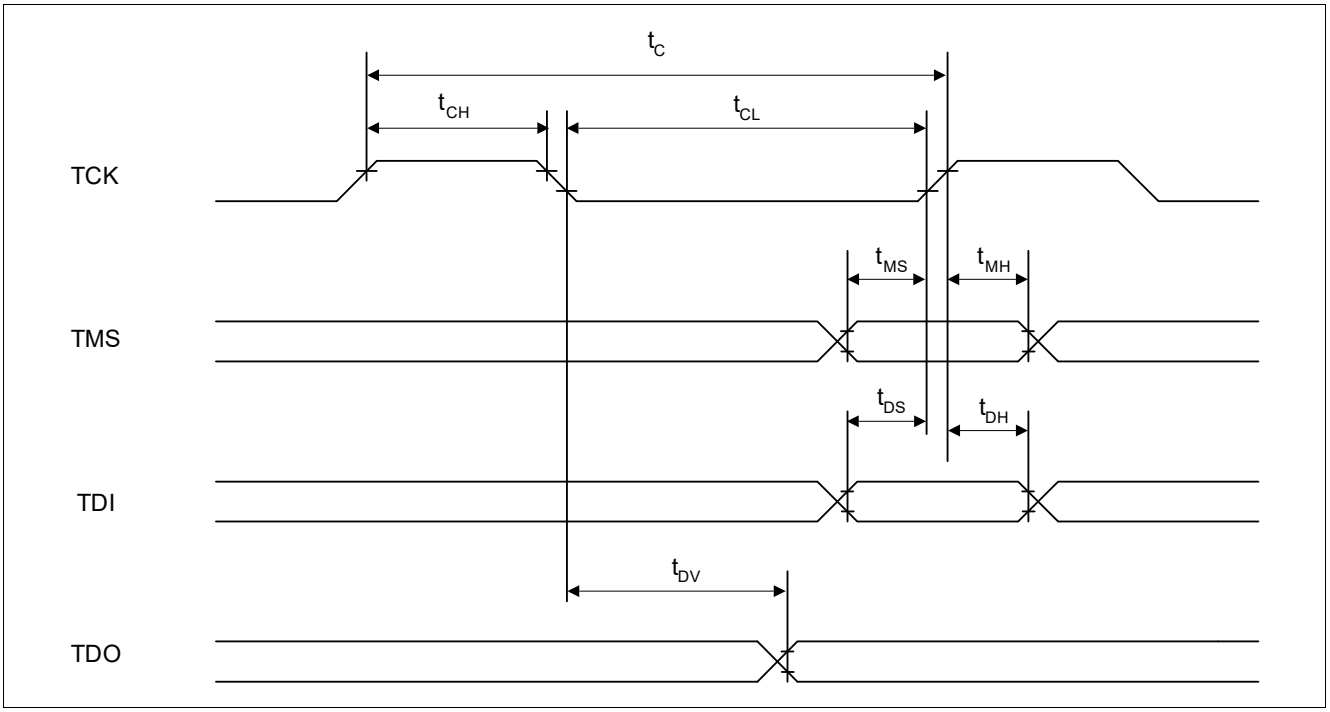


Figure 21 Test Interface Timing

Table 45 and Table 46 describe the timing values for the test interface.

Table 45 Test Interface Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK Clock Period	t_C	100	–	–	ns	–
TCK High Time	t_{CH}	40	–	–	ns	–
TCK Low Time	t_{CL}	40	–	–	ns	–

Table 46 JTAG Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TMS Setup Time	t_{MS}	40	–	–	ns	–
TMS Hold Time	t_{MH}	40	–	–	ns	–
TDI Setup Time	t_{DS}	40	–	–	ns	–
TDI Hold Time	t_{DH}	40	–	–	ns	–
Hold: $\overline{\text{TRST}}$ after TCK	t_{HD}	10	–	–	ns	–
TDO Valid Delay	t_{DV}	–	–	60	ns	–

7.7.7 SGMII Interface Timing

This section describes the AC characteristics of the SGMII Interface on the GPY241.

The SGMII Interface timing characteristics are described below:

- SGMII Transmit timing characteristics (**Section 7.7.7.1**)
- SGMII Receive timing characteristics (**Section 7.7.7.2**)

7.7.7.1 SGMII Transmit Timing Characteristics

Figure 22 shows the timing diagram of the transmit SGMII interface on the GPY241. **Table 47** specifies the timing requirements.

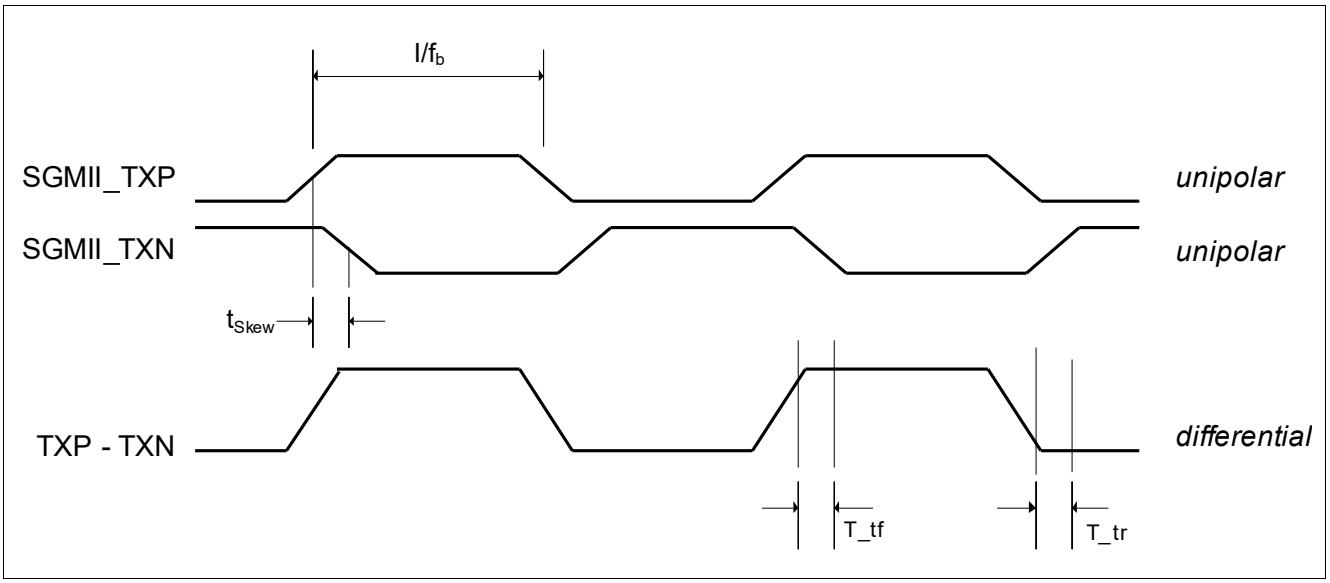


Figure 22 Transmit Timing Diagram of the SGMII (shows alternating data sequence)

Table 47 Transmit Timing Characteristics of the SGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transmit Baud Rate	f_b	-100 ppm	f_b	+100 ppm	Mbaud	f_b = 1.25/3.125 Gbaud
Differential Transmit Rise Time	T_t_r	30 ps	–	0.25 UI	–	20%→80%[1]
Differential Transmit Fall Time	T_t_f	30 ps	–	0.25 UI	–	80%→20%
Output Timing Jitter	T_T_J	–	–	0.30	UI_{pp}[2]	
Time Skew between Pairs	t_{Skew}	–	–	15	ps	–
Output Differential Voltage	V_{OD}	400	–	1600	mV	Peak-peak amplitude
Output Impedance (Differential)	R_O	80	100	120	Ω	–

1) UI = $1/f_b$, Unit Interval.

2) Refer to **[3]** for details. The p-p (peak to peak) measurement states the maximum to minimum amount of time deviation.

7.7.7.2 SGMII Receive Timing Characteristics

Figure 23 shows the timing diagram of the receive SGMII interface of the GPY241. **Table 48** specifies the timing requirements.

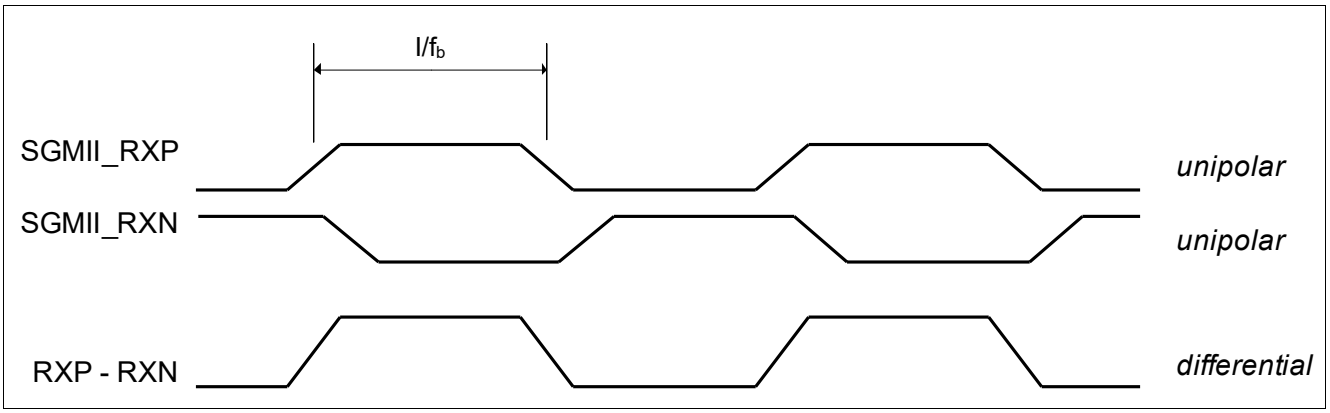


Figure 23 Receive Timing Diagram of the SGMII (alternating data input sequence)

Table 48 Receive Timing Characteristics of the SGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive Baud Rate	f_b	-100 ppm	f_b	+100 ppm	Mbaud	f_b = 1.25/3.125 Gbaud
Receive Data Jitter Tolerance	R_T_J	–	–	0.6	UI_{pp} [1)]	–
Input Differential Voltage	V_{ID}	200	–	1600	mV	Peak-peak amplitude
Input Impedance (Differential)	R_I	80	100	120	Ω	–

1) Refer to **[3]** for details.

7.7.8 UXSGMII Interface Timing

This section describes the AC characteristics of the UXSGMII Interface on the GPY241.

The UXSGMII Interface timing characteristics are described below:

- UXSGMII Transmit timing characteristics (**Section 7.7.8.1**)
- UXSGMII Receive timing characteristics (**Section 7.7.8.2**)

7.7.8.1 UXSGMII Transmit Timing Characteristics

Table 49 shows timing requirements of the UXSGMII interface on the GPY241.

Table 49 Transmit Timing Characteristics of the UXSGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference Differential Impedance	Z_d	–	100	–	Ω	–
Termination Mismatch	R_M	–	–	5	%	–
DC Common Mode Voltage	V_{cm}	0	–	3.6	V	–
Output Rise and Fall Time	t_{RH}, t_{FH}	24 ps	–	–	ps	20%→80%
Output AC Common Mode Voltage	–	–	–	15	mV	mV (RMS)
Differential Output Return Loss[1]	SDD22	20	–	–	dB	0.05-0.1 GHz
		10	–	–	dB	0.1-7.5 GHz
		–	–	–		7.5-15 GHz
Common Mode Output Return Loss[2]	SCC22	6	–	–	dB	0.1-15 GHz

1) Return loss given by equation SDD22(dB)=10 - 16.6 Log10(f/7.5), with f in GHz.
2) Common mode reference impedance is 25 Ω common mode return loss helps absorb reflections and noise for EMI.

7.7.8.2 UXSGMII Receive Timing Characteristics

Table 50 shows timing requirements of the UXSGMII interface on the GPY241.

Table 50 Receive Timing Characteristics of the UXSGMII

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference Differential Impedance	Z_d	–	100	–	Ω	–
Termination Mismatch	Z_M	–	–	5	%	–
AC Common Mode Voltage	–	–	–	25	mV	mV (RMS)
Differential Output Return Loss[1]	SDD11	20	–	–	dB	0.05-0.1 GHz
		10	–	–	dB	0.1-7.5 GHz
		–	–	–		7.5-15 GHz
Common Mode Input Return Loss[2]	SCC11	6	–	–	dB	0.1-15 GHz
Differential to Common Mode Input Conversion[2]	SCD11	12	–	–	dB	0.1-15 GHz

1) Return loss given by equation SDD11(dB)=10 - 16.6 Log10(f/7.5), with f in GHz.
2) Common mode reference impedance is 25 Ω. SCD11 relates to conversion of differential to common mode and the associated generation of EMI.

7.7.9 Crystal Specification

The 25 MHz crystal must follow the specification given in **Table 51**.

Table 51 Specification of the Crystal

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency with 25 MHz input	f_{clk25}	–	25.0	–	MHz	–
Total Frequency Stability	–	-50	–	+50	ppm	Refers to sum of all effects: e.g. general tolerance, aging, temperature dependency
Series Resonant Resistance	–	–	–	60	W	–
Drive Level	–	–	–	0.1	mW	–
Load Capacitance	C_L	–	18	–	pF	–
Shunt Capacitance	C_0	–	–	5	pF	–

7.8 External Circuitry

This section specifies the component characteristics of the external circuitry connected to the GPY241.

7.8.1 Twisted-Pair Common-Mode Rejection and Termination Circuitry

This section describes the external circuitry that is required to properly terminate the common mode of the Twisted Pair Interface (TPI). These external components are also required to perform proper rejection of alien disturbers injected into the common mode of the TPI. **Figure 24** shows a typical external circuit, and in particular the common-mode components. **Table 52** defines the component values and their supported tolerances.

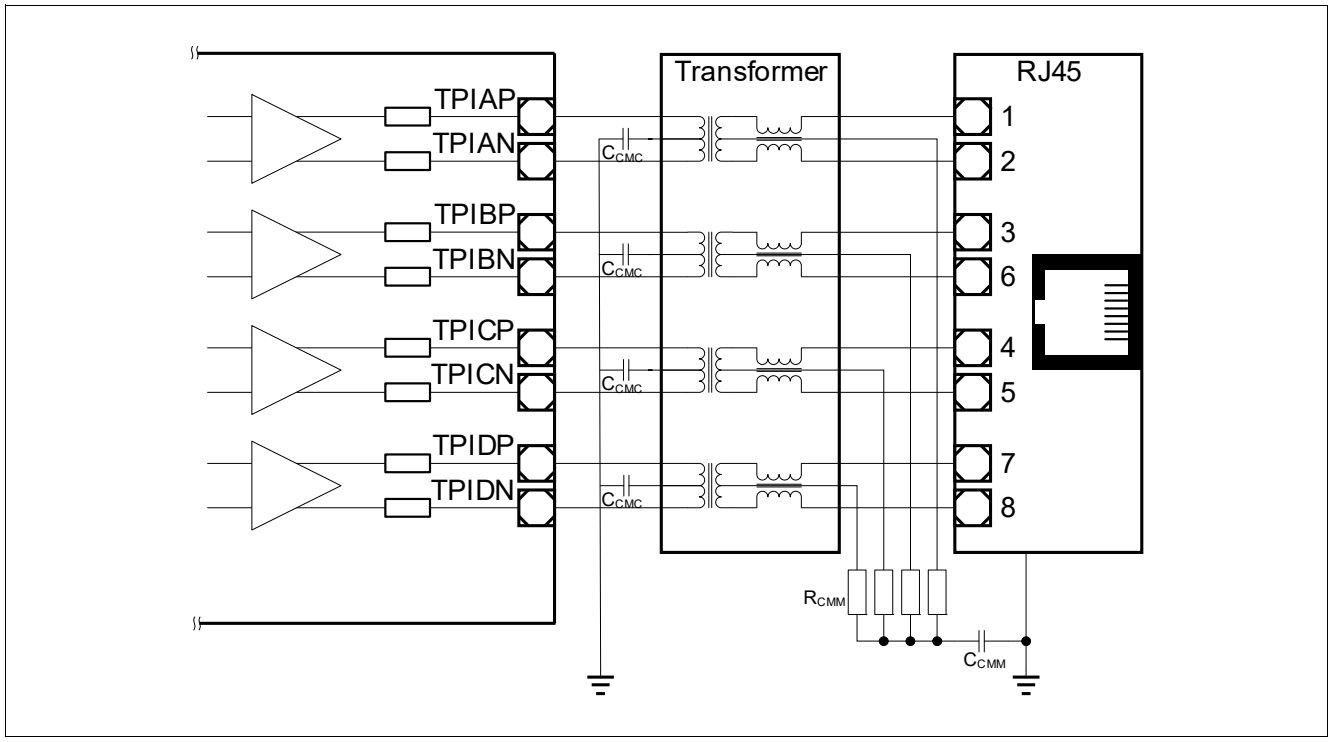


Figure 24 Twisted Pair Common-Mode Rejection and Termination Circuitry

Table 52 Electrical Characteristics for Common-Mode Rejection and Termination Circuitry

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Common-Mode Decoupling Capacitance (Media End)	C_{CMM}	800	1000	1200	pF	±20%, 2 kV
Common-Mode Decoupling Capacitance (Chip End)	C_{CMC}	80	100	120	nF	±20%, 2 kV
Common-Mode Termination Resistance (Media End)	R_{CMM}	67.5	75	82.5	Ω	±10%

7.8.2 Transformer (Magnetics)

This section specifies the required electrical characteristics of the transformer devices, also referred to as magnetics, that are supported. The specifications listed here guarantee proper operation according to IEEE 802.3 [4].

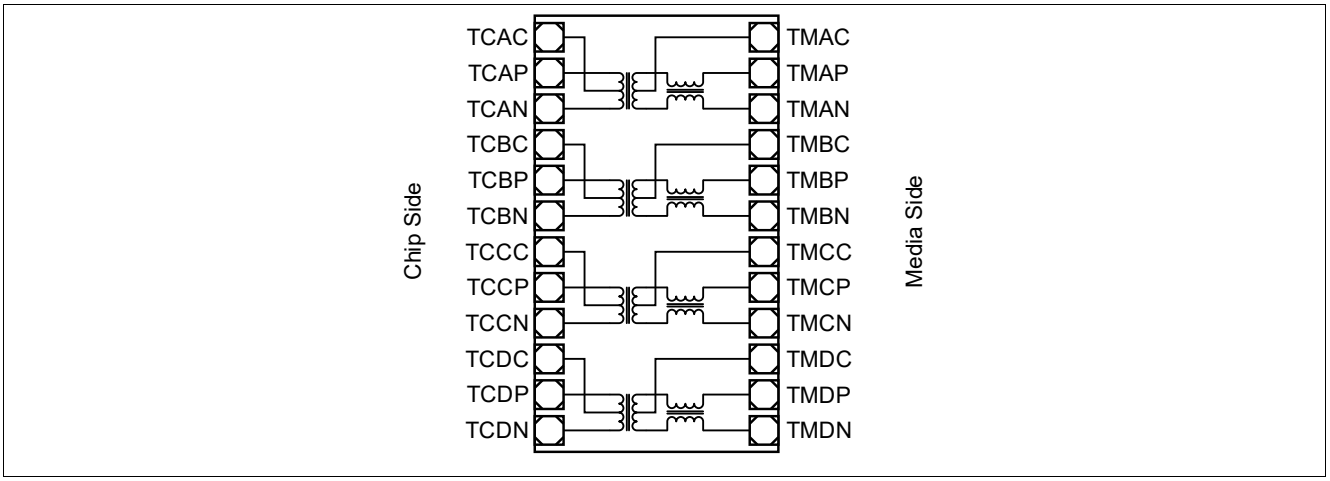


Figure 25 Schematic of an Ethernet Transformer Device

Figure 25 depicts a typical Gigabit Ethernet capable transformer device. Table 53 lists the characteristics of the supported transformer devices. These characteristics represent the minimum for achieving standard performance. Since the transformer significantly impacts the link performance, it is possible to increase the loop reach by selecting transformers with improved parameters.

Table 53 Electrical Characteristics for Supported Transformers (Magnetics)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Turns Ratio	1:tr	0.95	1.00	1.05		±5%
Differential-to-Common-mode Rejection	DCMR	40	–	–	dB	30 MHz
		35	–	–	dB	60 MHz
		30	–	–	dB	100 MHz
Crosstalk Attenuation	CTA	45	–	–	dB	30 MHz
		40	–	–	dB	60 MHz
		35	–	–	dB	100 MHz
Insertion Loss	IL	–	–	1	dB	1 MHz ≤ f ≤ 250 MHz
Return Loss	RL	16	–	–	dB	1 MHz ≤ f ≤ 40 MHz
Return Loss	RL	16-10*log10(f/40)	–	–	dB	40 MHz ≤ f ≤ 250 MHz

7.8.3 RJ45 Plug

Table 54 describes the electrical characteristics of the RJ45 plug to be used in conjunction with the GPY241.

Table 54 Electrical Characteristics for Supported RJ45 Plugs

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Crosstalk Attenuation	CTA	45	–	–	dB	30 MHz
		40	–	–	dB	60 MHz
		35	–	–	dB	100 MHz
Insertion Loss	IL	–	–	1	dB	1 MHz ≤ f ≤ 250 MHz
Return Loss	RL	16	–	–	dB	1 MHz ≤ f ≤ 40 MHz
Return Loss	RL	16-10*log10(f/40)	–	–	dB	40 MHz ≤ f ≤ 250 MHz

7.8.4 Calibration Resistors

An external resistor R_{CAL} of 22 kΩ 1% must be connected between the RCAL pin and ground to calibrate the GPY241 Ethernet analog modules.

Additionally, an external resistor R_{RESREF} of 200 Ω 1% must be connected between the RESREF pin and ground in order to calibrate the GPY241 SGMII and USXGMII analog modules.

Table 55 indicates the resistor values.

Table 55 Calibration Resistors Values

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPY241 Calibration Resistor	R_{CAL}	21780	22000	22220	Ω	±1%
SGMII/USXGMII PHY Calibration Resistor	R_{RESREF}	198	200	202	Ω	±1%

7.9 Power Supply

The power supply scheme for GPY241 depends on the SerDes interface used to communicate with the MAC SoC. 3.3 V and 0.95 V external power supply is to be connected to the respective power rails in SGMII/USXGMII mode. When GPY241 operates in USXGMII mode instead of SGMII mode, additionally an external supply of 1.8 V is required. For more details, refer to [2].

8 Package Outline

The product is assembled in a PG-VF2BGA-260 package, which complies with regulations requiring lead free material. The following parameters are generated in accordance with JEDEC JESD51 standards [11]. Four models are provided:

- In natural convection environment, still air at 85°C (Table 56)
- In natural convection environment, still air at 70°C (Table 57)
- With a thermal solution setting chip top temperature at 70°C (Table 58)
- According to compact 2-R model (Table 59)

Table 56 JEDEC Thermal Resistance Package Parameter - Still air conditions at 85°C

Item	Name/Value
Environmental Conditions	The chip is mounted on a 4-layer PCB (2S2P) according to JESD51-7 [11], PCB size 101.5mm x 114.5 mm Natural convection: still air, according to JESD51-2 [11] Ambient temperature: 85°C
Thermal Resistance - Junction to Ambient	$R_{th,\ JA}$ = 18.4 K/W
Thermal Delta - Junction to Case Top	Psi_{JCTop} = 0.02 K/W

Table 57 JEDEC Thermal Resistance Package Parameter - Still air conditions at 70°C

Item	Name/Value
Environmental Conditions	The chip is mounted on a 2-layer PCB (1S1P) according to JESD51-7 [11], PCB size 101.5mm x 114.5 mm Natural convection: still air, according to JESD51-2 [11] Ambient temperature: 70°C
Thermal Resistance - Junction to Ambient	$R_{th,\ JA}$ = 26.4 K/W
Thermal Delta - Junction to Case Top	Psi_{JCTop} = 0.02 K/W

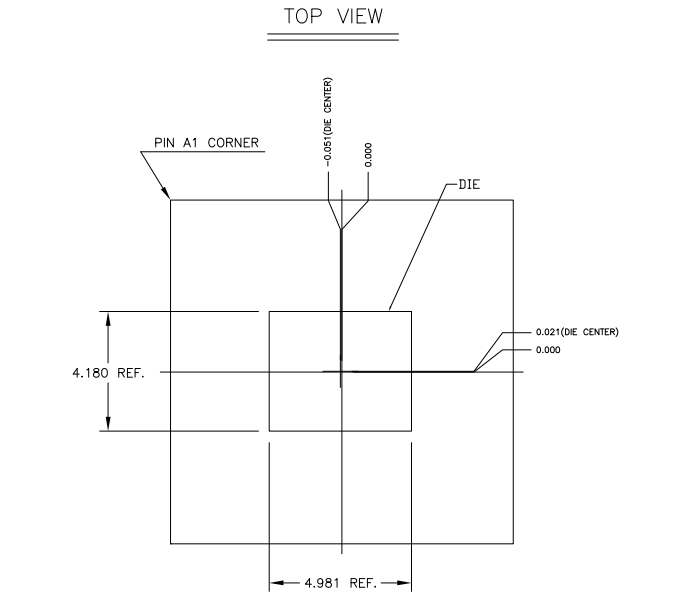
Table 58 JEDEC Thermal Resistance Package Parameter - With Thermal Solution Environment

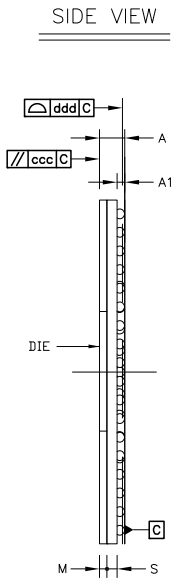
Item	Name/Value	Environment
Thermal Resistance - Junction to Case Top	$R_{th,\ JCtop}$ = 0.1 K/W	Cold plate on package top surface. Temp = 85°C. PCB with 16 thermal vias
Thermal Resistance - Junction to Board	$R_{th,\ JB}$ = 12.8 K/W	According to JESD51-8 [11] Ring style cold plate on PCB around 3 mm from package edge. Temp = 85°C. 4L PCB (2S2P) with 16 thermal vias.

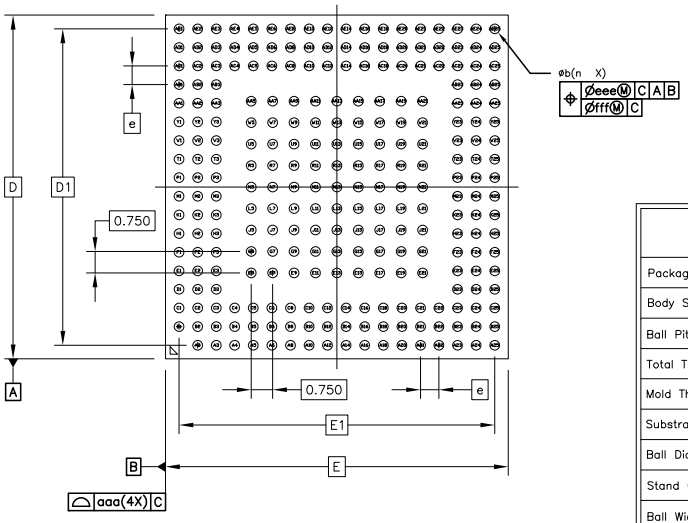
Table 59 JEDEC Thermal Resistance Package Parameter - Compact 2-R Model Network

Item	Name/Value
Thermal Resistance - Junction to Case Top	$R_{th,\ JCtop}$ = 0.1 K/W
Thermal Resistance - Junction to Case Bottom	$R_{th,\ JCbottom}$ = 7.76 K/W

Figure 26 shows the mechanical drawings for this package. The dimensions are in millimeters.







BOTTOM VIEW

		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			MFC VFBGA		
Body Size:	X	E	12.000		
	Y	D	12.000		
Ball Pitch :		e	0.650		
Total Thickness :		A	0.82	0.88	0.95
Mold Thickness :		M	0.260 Ref.		
Substrate Thickness :		S	0.351 Ref.		
Ball Diameter :			0.350		
Stand Off :		A1	0.220	0.270	0.320
Ball Width :		b	0.320	0.370	0.420
Package Edge Tolerance :		aaa	0.100		
Mold Parallelism :		ccc	0.100		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	260		
Edge Ball Center to Center :	X	E1	11.050		
	Y	D1	11.050		

PG-VF2BGA-260-C-1A

Figure 26 PG-VF2BGA-260 12 mm x 12 mm Package Outline

8.1 Ordering Information

Table 60 provides sales ordering information.

Table 60 Product Naming

Marketing Part Number	Ordering Part Number	S-Spec#	MMID	OTP Firmware Version	Device Number[1)]	Device Revision Number[2)]	PHY Identifier[3)]
GPY241	GPY241B0BC	SLNHK	999X65	0x8B83	0x24	0x1	0xDE41

1) LDN field in CL22 and CL45 registers.
2) LDRN field in CL22 and CL45 registers.
3) PHY Identifier 2 register 16-bit value.

Note: For more information about part numbers, as well as the most up-to-date information and additional information on environmental rating, go to https://www.maxlinear.com/support/product-change-notification.

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Attention: Refer to the latest revisions of the documents.

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Attention: Refer to the latest revisions of the documents.

Terminology

A

ADS	Auto-downspeed
AFE	Analog Front End
ANEG	Auto-negotiation
ANSI	American National Standards Institute
ASP	Analog Signal Processing

B

BER	Bit Error Rate
BW	Bandwidth

C

CAT5	Category 5 Cabling
CCR	Configuration Content Record
CDB	Clock Distribution Block
CDR	Clock and Data Recovery
CRC	Cyclic Redundancy Check
CRS	Carrier Sense

D

DEC	Digital Echo Canceler
DSP	Digital Signal Processing

E

EEE	Energy-Efficient Ethernet
EEPROM	Electrically Erasable Programmable ROM
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge

F

FLP	Fast Link Pulse

G

GbE	Gigabit Ethernet
GMII	Gigabit Media-Independent Interface
GPIO	General Purpose Input/Output

H

HBM	Human Body Model

I

IC	Integrated Circuit
ICV	Integrity Check Value
IEEE	Institute of Electrical and Electronics Engineers
IPG	Inter-Packet Gap

J

JTAG	Joined Test Action Group
L	
LAN	Local Area Network
LDO	Load Drop Out
LED	Light Emitting Diode
LJPLL	Low Jitter Phase-Locked Loop
LPI	Low Power Idle
LSB	Least Significant Bit
M	
MAC	Media Access Controller
MDI	Media-Dependent Interface
MDIO	Management Data Input/Output
MDIX	Media-Dependent Interface Crossover
MII	Media-Independent Interface
MMD	**MDIO** Manageable Device
MSB	Most Significant Bit
N	
NLP	Normal Link Pulse
NP	Next page
O	
OSI	Open Systems Interconnection
OUI	Organizationally Unique Identifier
P	
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PD	Powered Device
PHY	Physical Layer (device)
PLL	Phase-Locked Loop
PMA	Physical Media Attachment
PPS	Pulse Per Second
PTS	Precision Time Protocol
PSE	Power-Sourcing Equipment
R	
RX	Receive
S	
SA	Secure Association
SC	Secure Channel
SerDes	Serializer-Deserializer
SFD	Start-of-frame Delimiter
SGMII	Serial Gigabit Media-Independent Interface

SMD	Surface Mounted Device
SoC	System on Chip
STA	Station Management Entity (**MAC** SoC)
T	
TAP	Test Access Port
TLE	Transformerless Ethernet
TPI	Twisted Pair Interface
TsSync	Time Stamp Synchronization
TX	Transmit
U	
USXGMII	Universal Serial Multi(x) Gigabit Media Independent Interface
W	
WoL	Wake-on-**LAN**
X	
xMII	Symbolic shortening which denotes the set of supported **MII** Interfaces, e.g. **RGMII** and **SGMII**
XO	Crystal Oscillator

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