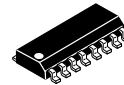
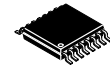


14-Stage Binary Ripple Counter With Oscillator

High-Performance Silicon-Gate CMOS



SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F

MC74HC4060A

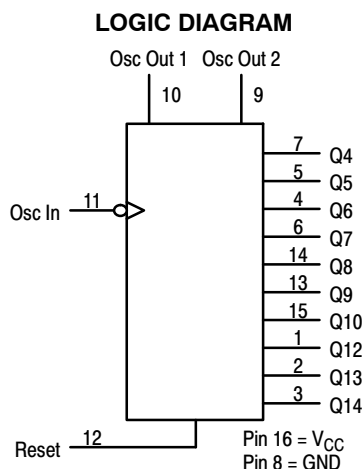
The MC74HC4060A is identical in pinout to the standard CMOS MC14060B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 14 master-slave flip-flops and an oscillator with a frequency that is controlled either by a crystal or by an RC circuit connected externally. The output of each flip-flop feeds the next and the frequency at each output is half of that of the preceding one. The state of the counter advances on the negative-going edge of the Osc In. The active-high Reset is asynchronous and disables the oscillator to allow very low power consumption during stand-by operation.

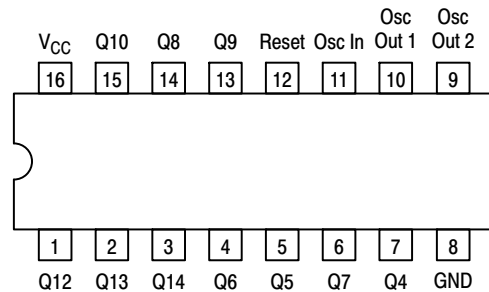
State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with Osc Out 2 of the HC4060A.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 390 FETs or 97.5 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

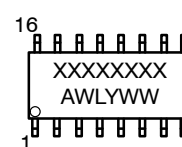


PIN ASSIGNMENT

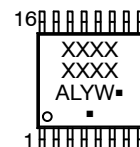


16-Lead Package (Top View)

MARKING DIAGRAMS



SOIC-16



TSSOP-16

- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or \blacksquare = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Clock	Reset	Output State
	L	No Change
	L	Advance to Next State
X	H	All Outputs Are Low

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 10

MC74HC4060A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V	
V _{IN}	DC Input Voltage	-0.5 to V _{CC} +0.5	V	
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} +0.5	V	
I _{IN}	DC Input Diode Current, per Pin	±20	mA	
I _{OUT}	DC Input Diode Current, Per Pin	±25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA	
I _{IK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})	±20	mA	
I _{OK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})	±20	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T _J	Junction Temperature Under Bias	+150	°C	
θ _{JA}	Thermal Resistance (Note 1)	SOIC-16 TSSOP-16	126 159	°C/W
P _D	Power Dissipation in Still Air at 25 °C	SOIC-16 TSSOP-16	995 787	mW
MSL	Moisture Sensitivity	Level 1	-	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	> 2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.5*	6.0	V
V _{IN} , V _{OUT}	DC Input, Output Voltage (Note 3)	0	V _{CC}	V
T _A	Operating Free-Air Temperature	-55	+125	°C
t _r , t _f	Input Rise or Fall Time	V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

* The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 11 with an external clock source.

MC74HC4060A

DC CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25 °C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1V or V _{CC} - 0.1V I _{out} ≤ 20μA	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V _{OH}	Minimum High-Level Output Voltage (Q4–Q10, Q12–Q14)	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	2.48	2.34	2.20	
		I _{out} ≤ 4.0 mA	4.5	3.98	3.84	3.70	
		I _{out} ≤ 5.2 mA	6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage (Q4–Q10, Q12–Q14)	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	0.26	0.33	0.40	
		I _{out} ≤ 4.0 mA	4.5	0.26	0.33	0.40	
		I _{out} ≤ 5.2 mA	6.0	0.26	0.33	0.40	
V _{OH}	Minimum High-Level Output Voltage (Osc Out 1, Osc Out 2)	V _{in} = V _{CC} or GND I _{out} ≤ 20μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{CC} or GND I _{out} ≤ 0.7 mA	3.0	2.48	2.34	2.20	
		I _{out} ≤ 1.0 mA	4.5	3.98	3.84	3.70	
		I _{out} ≤ 1.3 mA	6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage (Osc Out 1, Osc Out 2)	V _{in} = V _{CC} or GND I _{out} ≤ 20μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{CC} or GND I _{out} ≤ 0.7 mA	3.0	0.26	0.33	0.40	
		I _{out} ≤ 1.0 mA	4.5	0.26	0.33	0.40	
		I _{out} ≤ 1.3 mA	6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0μA	6.0	4	40	160	μA

AC CHARACTERISTICS (C_L = 50 pF)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25 °C	≤85 °C	≤125 °C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	9.0	8.0	MHz
		3.0	10	14	12	
		4.5	30	28	25	
		6.0	50	45	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Osc In to Q4* (Figures 1 and 4)	2.0	300	375	450	ns
		3.0	180	200	250	
		4.5	60	75	90	
		6.0	51	64	75	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Osc In to Q14* (Figures 1 and 4)	2.0	500	750	1000	ns
		3.0	350	450	600	
		4.5	250	275	300	
		6.0	200	220	250	
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figures 2 and 4)	2.0	195	245	300	ns
		3.0	75	100	125	
		4.5	39	49	61	
		6.0	33	42	53	

MC74HC4060A

AC CHARACTERISTICS (C_L = 50 pF) (continued)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25 °C	≤85 °C	≤125 °C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Q _n to Q _{n+1} (Figures 3 and 4)	2.0	75	95	125	ns
		3.0	60	75	95	
		4.5	15	19	24	
		6.0	13	16	20	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance		10	10	10	pF

* For T_A = 25 °C and C_L = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

$$V_{CC} = 2.0 \text{ V: } t_P = [93.7 + 59.3 (n-1)] \text{ ns}$$

$$V_{CC} = 4.5 \text{ V: } t_P = [30.25 + 14.6 (n-1)] \text{ ns}$$

$$V_{CC} = 3.0 \text{ V: } t_P = [61.5 + 34.4 (n-1)] \text{ ns}$$

$$V_{CC} = 6.0 \text{ V: } t_P = [24.4 + 12 (n-1)] \text{ ns}$$

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25 °C, V _{CC} = 5.0 V		pF
		35		

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

TIMING REQUIREMENTS

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25 °C	≤85 °C	≤125 °C	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	100	125	150	ns
		3.0	75	100	120	
		4.5	20	25	30	
		6.0	17	21	25	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	23	
		6.0	13	16	19	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	23	
		6.0	13	16	19	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

MC74HC4060A

PIN DESCRIPTIONS

INPUTS

Osc In (Pin 11)

Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter. Osc In may be driven by an external clock source.

Reset (Pin 12)

Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state (forcing all Q outputs low) and disables the oscillator.

OUTPUTS

Q4–Q10, Q12–Q14 (Pins 7, 5, 4, 6, 13, 15, 1, 2, 3)

Active-high outputs. Each Qn output divides the Clock input frequency by 2^N . The user should note the Q1, Q2, Q3 and Q11 are not available as outputs.

Osc Out 1, Osc Out 2 (Pins 9, 10)

Oscillator outputs. These pins are used in conjunction with Osc In and the external components to form an oscillator. When Osc In is being driven with an external clock source, Osc Out 1 and Osc Out 2 must be left open circuited. With the crystal oscillator configuration in Figure 6, Osc Out 2 must be left open circuited.

SWITCHING WAVEFORMS

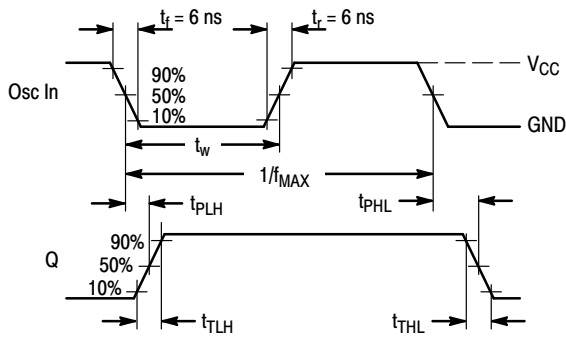


Figure 1.

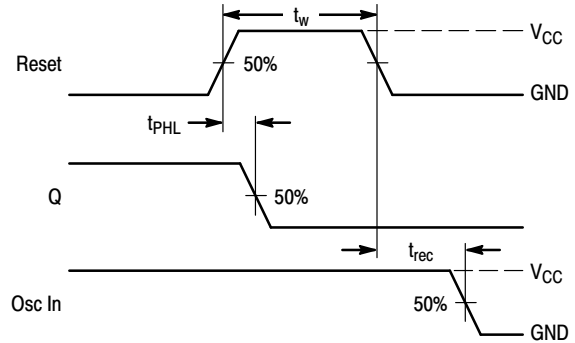


Figure 2.

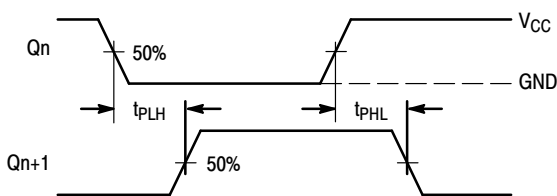
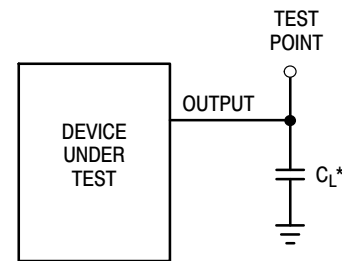


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

MC74HC4060A

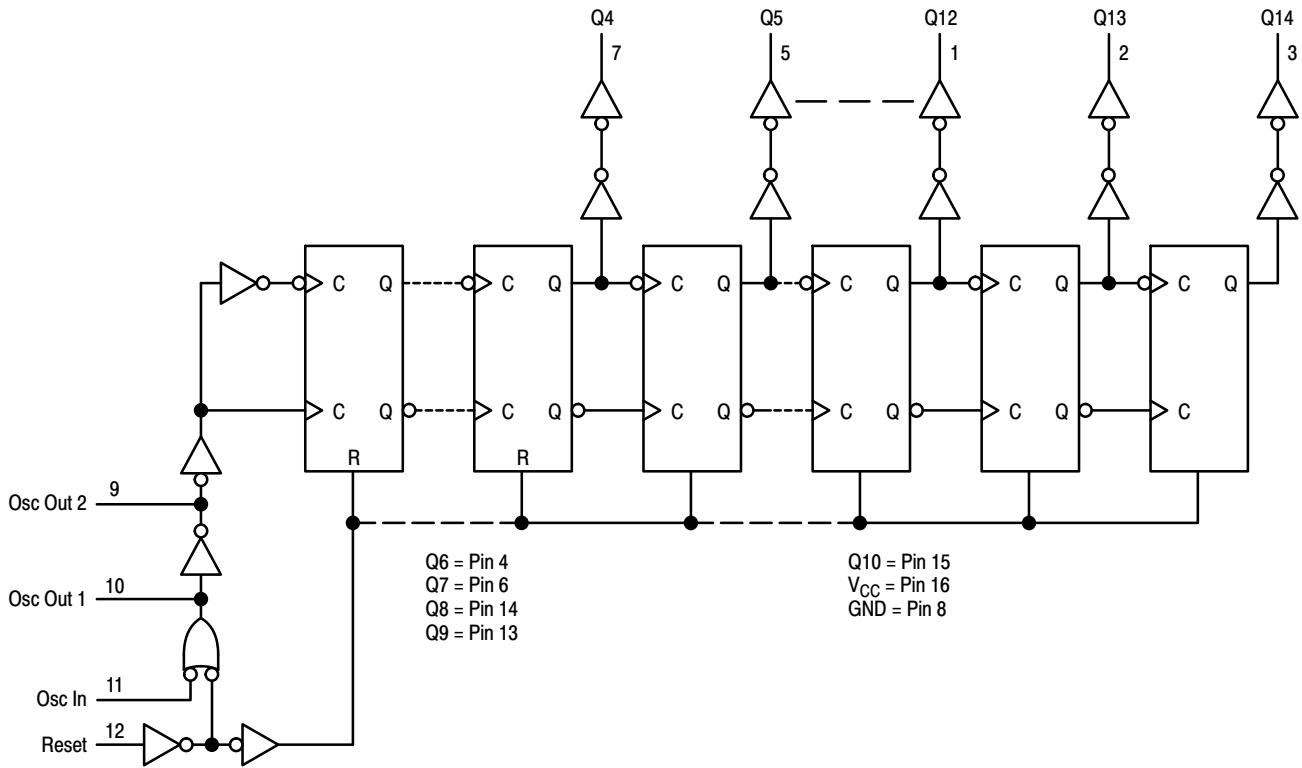


Figure 5. Expanded Logic Diagram

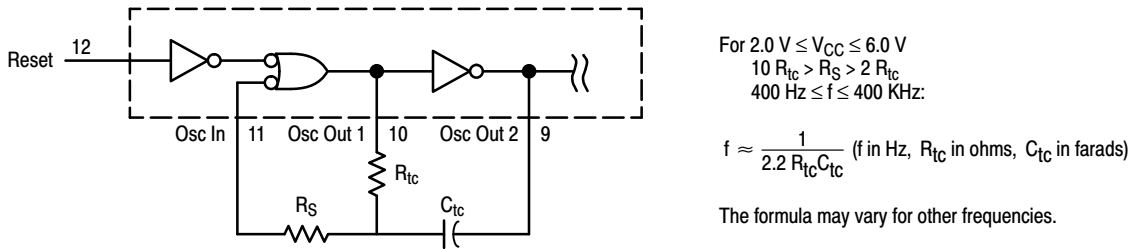


Figure 6. Oscillator Circuit Using RC Configuration

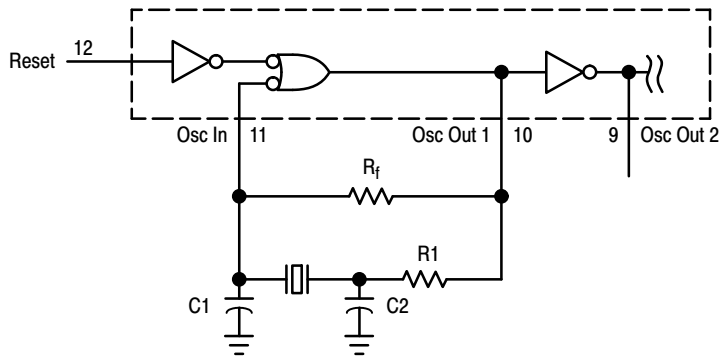


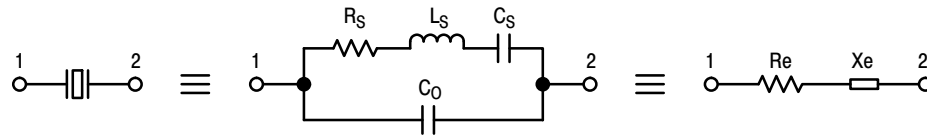
Figure 7. Pierce Crystal Oscillator Circuit

MC74HC4060A

TABLE 1. CRYSTAL OSCILLATOR AMPLIFIER SPECIFICATIONS ($T_A = 25\text{ }^\circ\text{C}$; Input = Pin 11, Output = Pin 10)

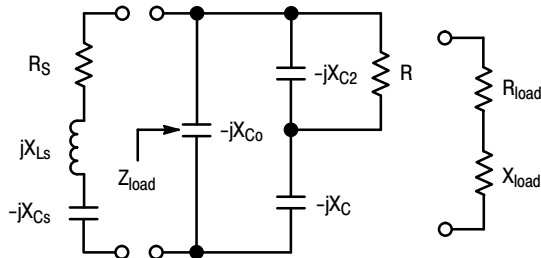
Type	Positive Reactance (Pierce)	
Input Resistance, R_{in}	60 M Ω Minimum	
Output Impedance, Z_{out} (4.5 V Supply)	200 Ω (See Text)	
Input Capacitance, C_{in}	5 pF Typical	
Output Capacitance, C_{out}	7 pF Typical	
Series Capacitance, C_a	5 pF Typical	
Open Loop Voltage Gain with Output at Full Swing, α	3 Vdc Supply	5.0 Expected Minimum
	4 Vdc Supply	4.0 Expected Minimum
	5 Vdc Supply	3.3 Expected Minimum
	6 Vdc Supply	3.1 Expected Minimum

PIERCE CRYSTAL OSCILLATOR DESIGN



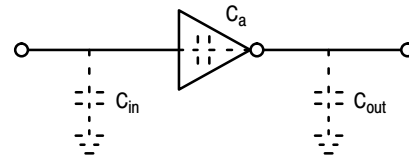
Value are supplied by crystal manufacturer (parallel resonant crystal).

Figure 8. Equivalent Crystal Networks



NOTE: $C = C_1 + C_{in}$ and $R = R_1 + R_{out}$. C_0 is considered as part of the load. C_a and R_i typically have minimal effect below 2 MHz.

Figure 9. Series Equivalent Crystal Load



Values are listed in Table 1.

Figure 10. Parasitic Capacitances of the Amplifier

DESIGN PROCEDURES

The following procedure applies for oscillators operating below 2 MHz where Z is a resistor R1. Above 2 MHz, additional impedance elements should be considered: C_{out} and C_a of the amp, feedback resistor R_f, and amplifier phase shift error from 180 °C.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{C_0}(R_s + jX_{L_s} - jX_{C_s})}{-jX_{C_0} + R_s + jX_{L_s} - jX_{C_s}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_s for the crystal should be used in the equation.

Step 2: Determine β, the attenuation, of the feedback network. For a closed-loop gain of 2, A_vβ = 2, β = 2/A_v where A_v is the gain of the HC4060A amplifier.

Step 3: Determine the manufacturer’s loading capacitance. For example: A manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load}. For example, a manufacturer specifies a crystal Q of 100,000. In-circuit Q is arbitrarily set at 20% below crystal Q or 80,000. Then R_{load} = (2πf_oL_s/Q) – R_s where L_s and R_s are crystal parameters.

Step 5: Simultaneously solve, using a computer,

$$\beta = \frac{X_C \cdot X_{C2}}{R \cdot R_e + X_{C2} (X_e - X_C)} \quad (\text{with feedback phase shift} = 180^\circ) \quad (\text{Eq 1})$$

$$X_e = X_{C2} + X_C + \frac{R_e X_{C2}}{R} = X_{C_{load}} \quad (\text{where the loading capacitor is an external load, not including } C_0) \quad (\text{Eq 2})$$

$$R_{load} = \frac{R X_{C_0} X_{C2} [(X_C + X_{C2})(X_C + X_{C_0}) - X_C(X_C + X_{C_0} + X_{C2})]}{X^2_{C2}(X_C + X_{C_0})^2 + R^2(X_C + X_{C_0} + X_{C2})^2} \quad (\text{Eq 3})$$

Here R = R_{out} + R1. R_{out} is amp output resistance, R1 is Z. The C corresponding to X_C is given by C = C1 + C_{in}.

Alternately, pick a value for R1 (i.e, let R1 = R_s). Solve Equations 1 and 2 for C1 and C2. Use Equation 3 and the fact that Q = 2πf_oL_s/(R_s + R_{load}) to find in-circuit Q. If Q is not satisfactory pick another value for R1 and repeat the procedure.

CHOOSING R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at Osc Out 2 (Pin 9). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

SELECTING R_f

The feedback resistor, R_f, typically ranges up to 20 MΩ. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth insures oscillation at the correct frequency plus roll-off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large

enough so as to not affect the phase of the feedback network in an appreciable manner.

ACKNOWLEDGEMENTS AND RECOMMENDED REFERENCES

The following publications were used in preparing this data sheet and are hereby acknowledged and recommended for reading:

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

D. Babin, “Designing Crystal Oscillators”, Machine Design, March 7, 1985.

D. Babin, “Guidelines for Crystal Oscillator Design”, Machine Design, April 25, 1985.

ALSO RECOMMENDED FOR READING:

E. Hafner, “The Piezoelectric Crystal Unit-Definitions and Method of Measurement”, Proc. IEEE, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, “Quartz Crystals for Frequency Control”, Electro-Technology, June, 1969.

P. J. Ottowitz, “A Guide to Crystal Selection”, Electronic Design, May, 1966.

MC74HC4060A

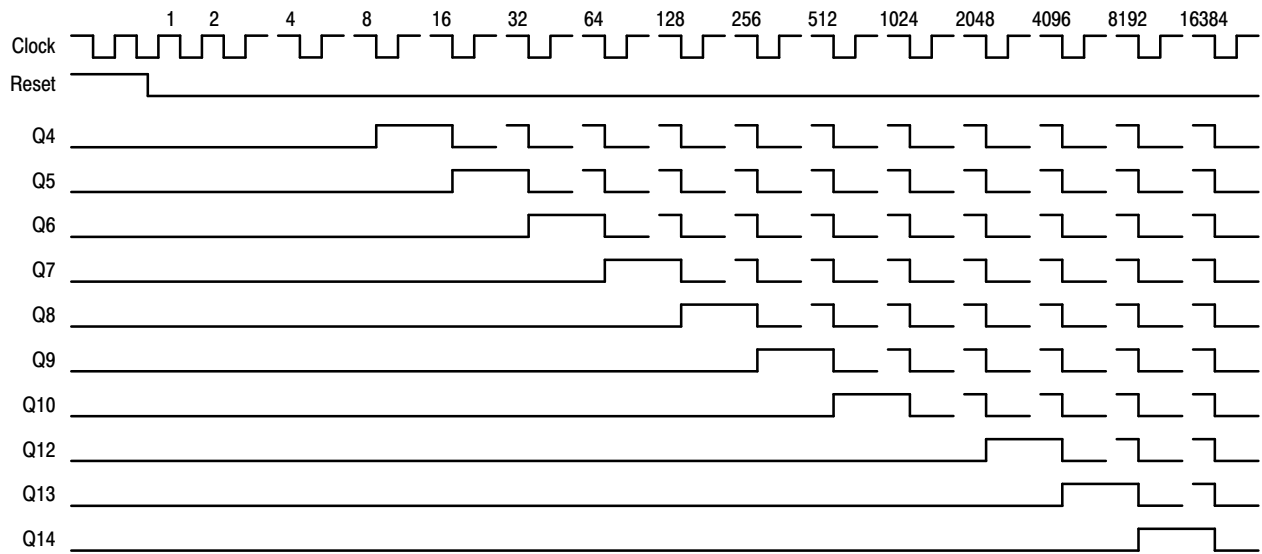


Figure 11. Timing Diagram

MC74HC4060A

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74HC4060ADR2G	HC4060AG	SOIC-16 (Pb-Free)	2500 Units / Reel
MC74HC4060ADR2G-Q*	HC4060AG	SOIC-16 (Pb-Free)	2500 Units / Reel
MC74HC4060ADTR2G	HC40 60A	TSSOP-16 (Pb-Free)	2500 Units / Reel
MC74HC4060ADTR2G-Q*	HC40 60A	TSSOP-16 (Pb-Free)	2500 Units / Reel

DISCONTINUED (Note 4)

Device	Package	Shipping [†]
MC74HC4060ADG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV74HC4060ADR2G*	SOIC-16 (Pb-Free)	2500 Units / Reel
MC74HC4060ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
NLVHC4060ADTR2G*	TSSOP-16 (Pb-Free)	2500 Units / Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

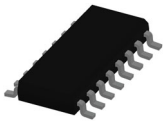
4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

* -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

REVISION HISTORY

Revision	Description of Changes	Date
12	Marking Diagrams update (p.1); "NLV Prefix" changed to "-Q Suffix" (p.1, p.5); Updates of Maximum Ratings table, Recommended Operating Conditions table, Ordering Information table and Figure 1.	10/20/2025
13	Added two "-Q" OPNs to Ordering Information table only	1/14/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

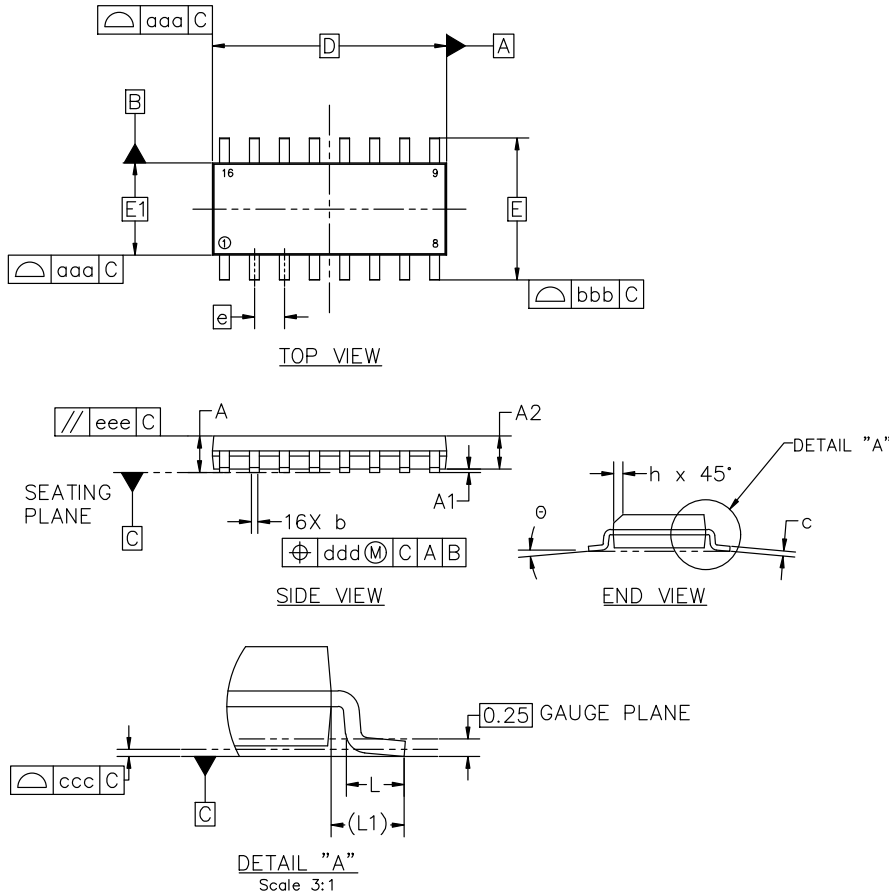


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

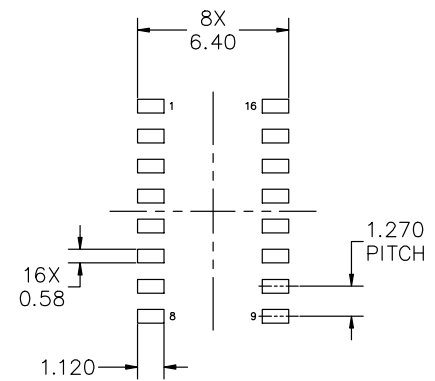
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

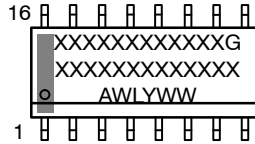
DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 1 OF 2

onsemi and onSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

**GENERIC
MARKING DIAGRAM***



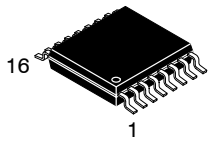
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH</p>	

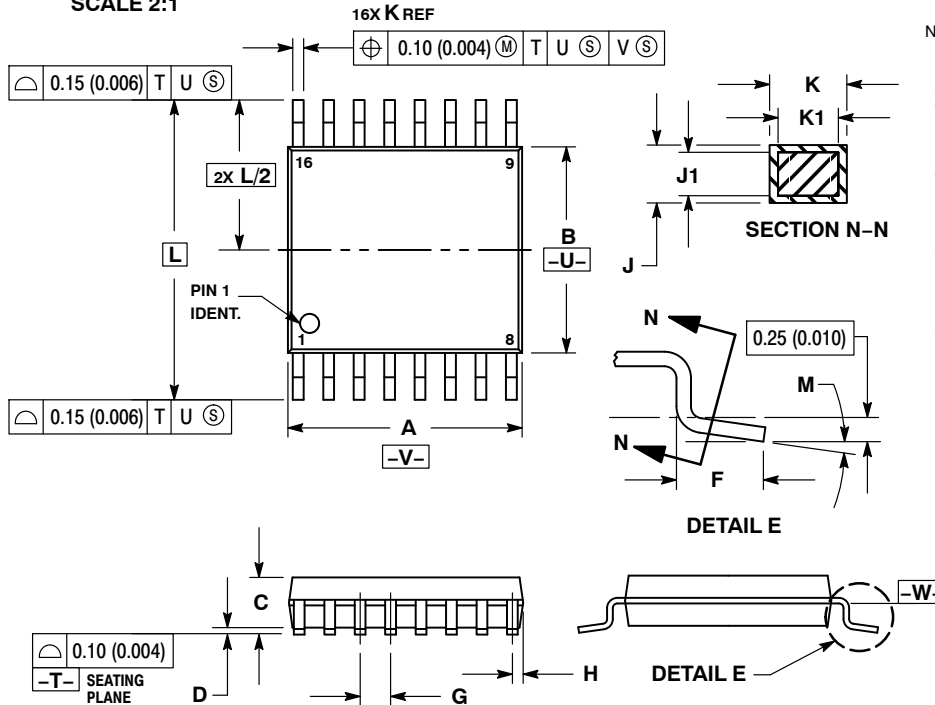
DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



TSSOP-16 WB
CASE 948F
ISSUE B

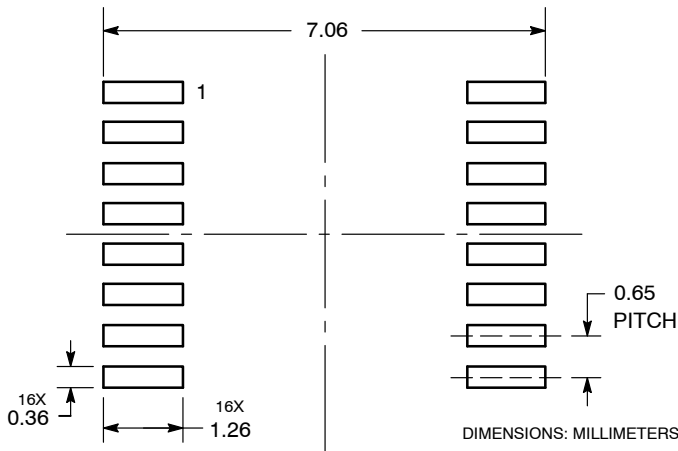
DATE 19 OCT 2006



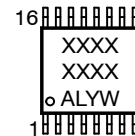
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED
SOLDERING FOOTPRINT*



GENERIC
MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales



Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View NLV74HC4060ADR2G on WIN SOURCE](#)

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management