THE DATASHEET OF

INA148UA

BURR - BROWN®

INA148

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±200V Common-Mode Voltage DIFFERENCE AMPLIFIER

FEATURES

- HIGH COMMON-MODE VOLTAGE:
  +75V at V_S = +5V
  ±200V at V_S = ±15V
- FIXED DIFFERENTIAL GAIN = 1V/V
- LOW QUIESCENT CURRENT: 260µA
- WIDE SUPPLY RANGE:
  Single Supply: 2.7V to 36V
  Dual Supplies: ±1.35V to ±18V
- LOW GAIN ERROR: 0.075% max
- LOW NONLINEARITY: 0.002% max
- HIGH CMR: 86dB
- SO-8 PACKAGE

APPLICATIONS

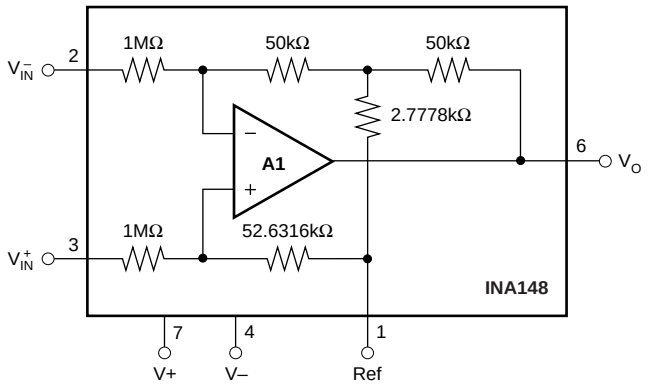
- CURRENT SHUNT MEASUREMENTS
- DIFFERENTIAL SENSOR AMPLIFIERS
- LINE RECEIVERS
- BATTERY POWERED SYSTEMS
- AUTOMOTIVE INSTRUMENTATION
- STACKED CELL MONITORS

DESCRIPTION

The INA148 is a precision, low-power, unity-gain difference amplifier with a high common-mode input voltage range. It consists of a monolithic precision bipolar op amp with a thin-film resistor network.

The on-chip resistors are laser trimmed for an accurate 1V/V differential gain and high common-mode rejection. Excellent temperature tracking of the resistor network maintains high gain accuracy and common-mode rejection over temperature. The INA148 will operate on single or dual supplies.

The INA148 is available in a small SO-8 surface-mount package and it is specified for the –40°C to +85°C extended industrial temperature range.



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SPECIFICATIONS: V_S = ±5V to ±15V Dual Supplies

At T_A = +25°C, R_L = 10kΩ connected to ground and Ref pin connected to ground, unless otherwise noted.

PARAMETER		CONDITIONS	INA148UA MIN	INA148UA TYP	INA148UA MAX	UNITS
OFFSET VOLTAGE (V_O)		**RTI[1][2]**				
Input Offset Voltage	V_{OS}	V_S = ±15V, V_{CM} = 0V		±1	±5	mV
		V_S = ±5V, V_{CM} = 0V		±1	±5	mV
Drift	$\Delta V_{OS}/\Delta T$	At T_A = –40°C to +85°C		±10		µV°C
vs Power Supply	PSRR	V_S = ±1.35V to ±18V, V_{CM} = 0V		±50	±400	µV/V
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	V_S = ±15V, $(V_{IN}^+) - (V_{IN}^-)$ = 0V	–200		+200	V
		V_S = ±5V, $(V_{IN}^+) - (V_{IN}^-)$ = 0V	–100		+80	V
Common-Mode Rejection	CMRR	V_S = ±15V, V_{CM} = –200V to +200V, R_S = 0Ω	70	86		dB
		V_S = ±5V, V_{CM} = –100V to +80V, R_S = 0Ω	70	86		dB
INPUT IMPEDANCE						
Differential				2		MΩ
Common Mode				1		MΩ
NOISE		**RTI[1][3]**				
Voltage Noise, f = 0.1Hz to 10Hz	e_n			17		µVp-p
Voltage Noise Density, f = 1kHz				880		nV/√Hz
GAIN						
Initial[1]				1		V/V
Gain Error		V_O = (V–) + 0.5 to (V+) – 1.5		±0.01	±0.075	%
vs Temperature				±3	±10	ppm/°C
Nonlinearity		V_S = ±15V, V_O = (V–) + 0.5 to (V+) – 1.5		±0.001	±0.002	% of FSR
		V_S = ±5V, V_O = (V–) + 0.5 to (V+) – 1.5		±0.001		% of FSR
FREQUENCY RESPONSE						
Small Signal Bandwidth				100		kHz
Slew Rate				1		V/µs
Settling Time: 0.1%		V_S = ±15V, 10V Step		21		µs
0.01%		V_S = ±15V, 10V Step		25		µs
0.1%		V_S = ±5V, 6V Step		21		µs
0.01%		V_S = ±5V, 6V Step		25		µs
Overload Recovery		50% Input Overload		24		µs
OUTPUT (V_O)						
Voltage Output		R_L = 100kΩ	(V–) + 0.25		(V+) – 1	V
		R_L = 10kΩ	(V–) + 0.5		(V+) – 1.5	V
Output Current	I_O					
Short-Circiuit Current		Continuous to Common		±13		mA
Capacitive Load		Stable Operation		10		nF
POWER SUPPLY						
Operating Range, Dual Supplies			±1.35		±18	V
Quiescent Current		V_{IN} = 0, I_O = 0		±260	±300	µA
TEMPERATURE RANGE						
Specified			–40		85	°C
Operating			–55		125	°C
Storage			–55		125	°C
Thermal Resistance	θ_{JA}	SO-8 Surface Mount		150		°C/W

NOTES: (1) Overall difference amplifier configuration. Referred to input pins (V_{IN}^+ and V_{IN}^-), gain = 1V/V (2) Input offset voltage specification includes effects of amplifier's input bias and offset currents. (3) Includes effects of input current noise and thermal noise contribution of resistor network.

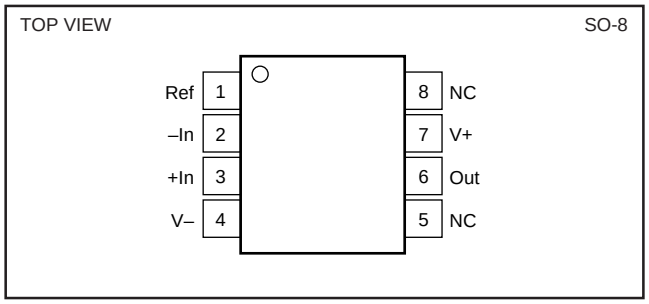
SPECIFICATIONS: V_S = +5V Single Supply

At T_A = +25°C, R_L = 10kΩ connected to V_S/2 and Ref pin connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITIONS	INA148UA MIN	INA148UA TYP	INA148UA MAX	UNITS
OFFSET VOLTAGE (V_O)		**RTI(1)(2)**				
Input Offset Voltage	V_{OS}	$V_{CM} = V_S/2$		±1	±5	mV
Drift	$\Delta V_{OS}/\Delta T$	At T_A = –40°C to +85°C		±10		µV°C
vs Power Supply	PSRR	V_S = +2.7V to +36V, $V_{CM} = V_S/2$		±50	±400	µV/V
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	$(V_{IN}^+) – (V_{IN}^-)$ = 0V, V_{REF} = 0.25V	–4		+75	V
		$(V_{IN}^+) – (V_{IN}^-)$ = 0V, $V_{REF} = V_S/2$	–47.5		+32.5	V
Common-Mode Rejection	CMRR	V_{CM} = –47.5V to +32.5V, R_S = 0Ω	70	86		dB
INPUT IMPEDANCE						
Differential				2		MΩ
Common Mode				1		MΩ
NOISE		**RTI(1)(3)**				
Voltage Noise, f = 0.1Hz to 10Hz	e_n			17		µVp-p
Voltage Noise Density, f = 1kHz				880		nV/√Hz
GAIN						
Initial(1)				1		V/V
Gain Error		V_O = +0.5V to +3.5V		±0.01	±0.075	%
vs Temperature				±3	±10	ppm/°C
Nonlinearity		V_O = +0.5V to +3.5V		±0.001		% of FSR
FREQUENCY RESPONSE						
Small Signal Bandwidth				100		kHz
Slew Rate				1		V/µs
Settling Time: 0.1%		V_S = +5V, 3V Step		21		µs
0.01%		V_S = +5V, 3V Step		25		µs
Overload Recovery		50% Input Overload		13		µs
OUTPUT (V_O)						
Voltage Output		R_L = 100kΩ	(V–) + 0.25		(V+) – 1	V
		R_L = 10kΩ	(V–) + 0.5		(V+) – 1.5	V
Output Current	I_O					
Short-Circiuit Current		Continuous to Common		±8		mA
Capacitive Load		Stable Operation		10		nF
POWER SUPPLY						
Operating Range, Single Supply			+2.7		+36	V
Quiescent Current		V_{IN} = 0, I_O = 0		260	300	µA
TEMPERATURE RANGE						
Specified			–40		85	°C
Operating			–55		125	°C
Storage			–55		125	°C
Thermal Resistance	θ_{JA}	SO-8 Surface Mount		150		°C/W

NOTES: (1) Overall difference amplifier configuration. Referred to input pins (V_{IN}^+ and V_{IN}^-), gain = 1V/V (2) Input offset voltage specification includes effects of amplifier's input bias and offset currents. (3) Includes effects of input current noise and thermal noise contribution of resistor network.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V–	36V
Signal Input Terminals, Continuous	±200V
Peak (0.1s)	±500V
Output Short Circuit to GND Duration	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

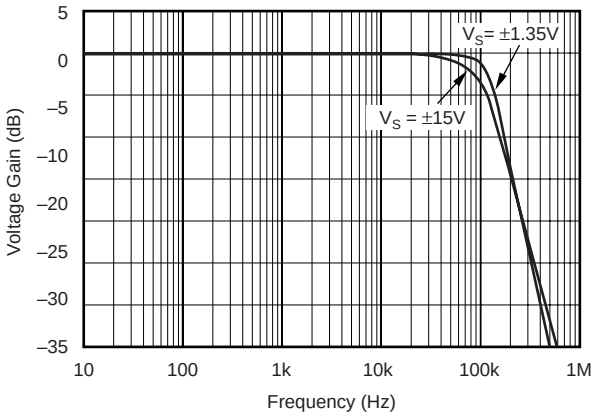
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
INA148UA	SO-8	182	–40°C to +85°C	INA148UA	INA148UA	Rails
"	"	"	"	"	INA148UA/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of “INA148UA/2K5” will get a single 2500-piece Tape and Reel.

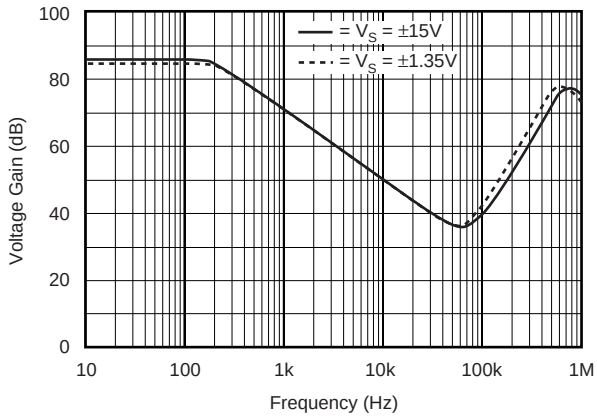
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, unless otherwise noted.

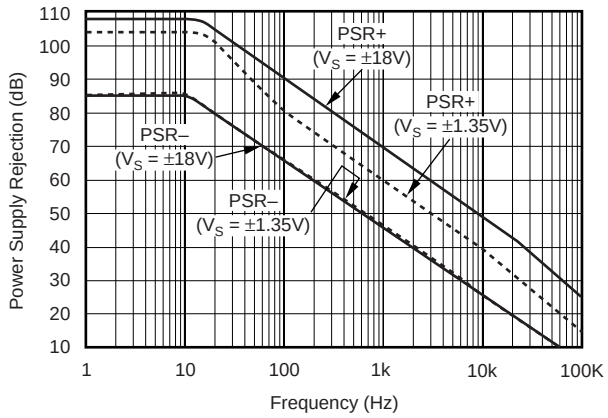
GAIN vs FREQUENCY



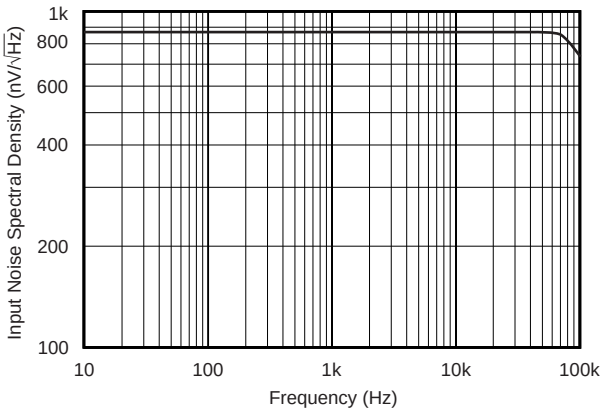
COMMON-MODE REJECTION vs FREQUENCY



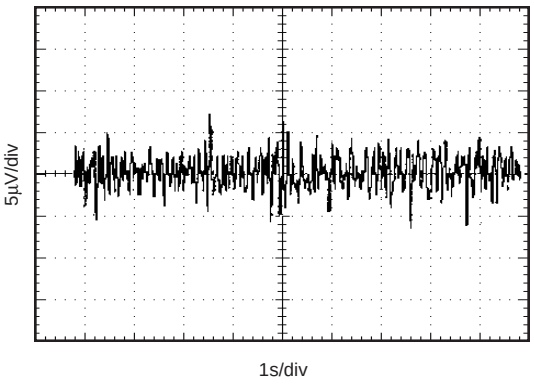
POWER SUPPLY REJECTION vs FREQUENCY



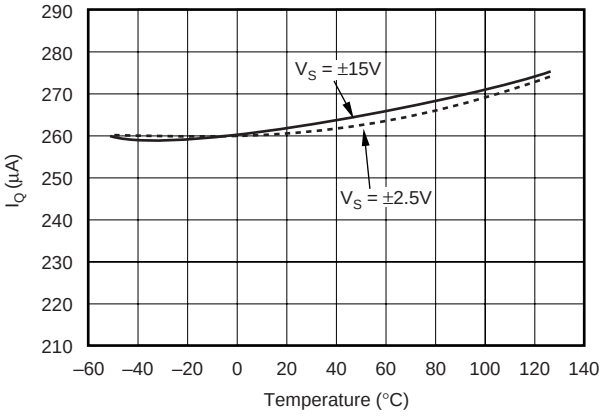
INPUT VOLTAGE NOISE SPECTRAL DENSITY



VOLTAGE NOISE (RTI)
0.1Hz to 10Hz



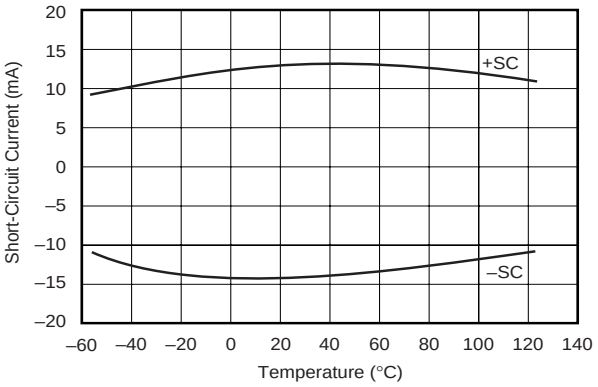
QUIESCENT CURRENT vs TEMPERATURE



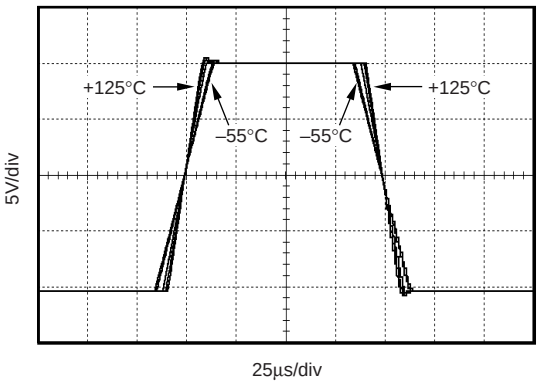
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, unless otherwise noted.

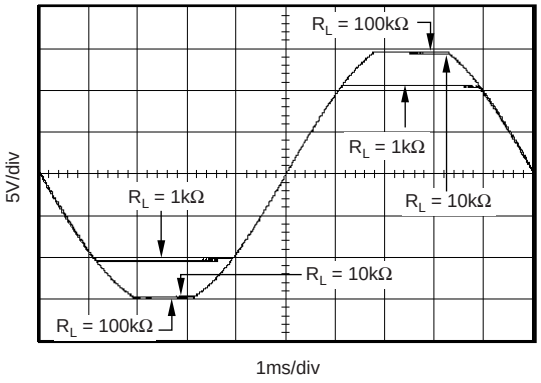
SHORT-CIRCUIT CURRENT vs TEMPERATURE



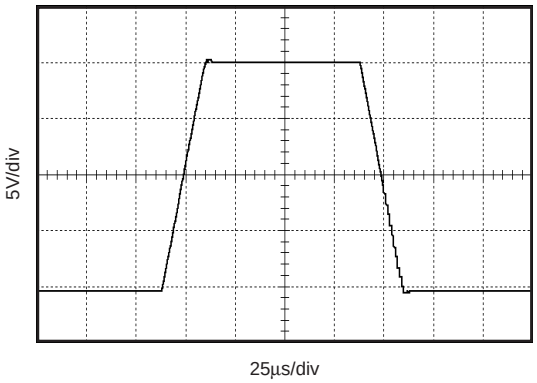
LARGE-SIGNAL STEP RESPONSE vs TEMPERATURE



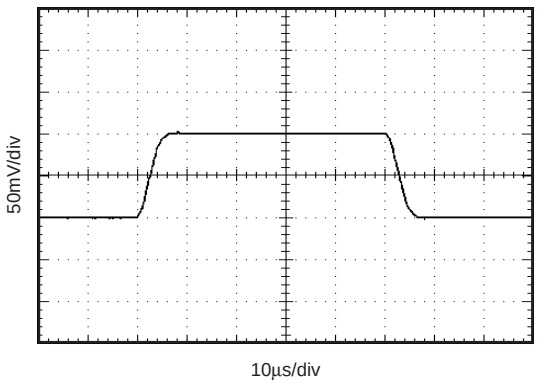
OUTPUT VOLTAGE SWING vs R_L



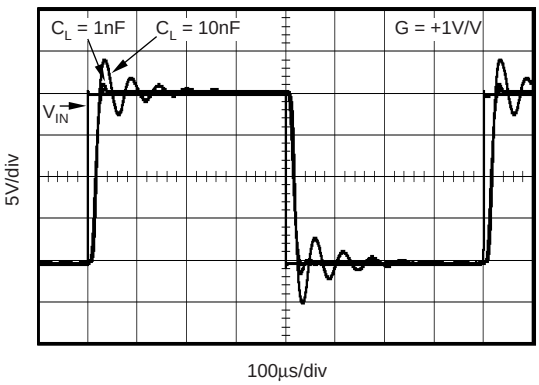
LARGE-SIGNAL STEP RESPONSE (R_L = 10kΩ, C_L = 10pF)



SMALL-SIGNAL STEP RESPONSE (R_L = 10kΩ, C_L = 10pF)



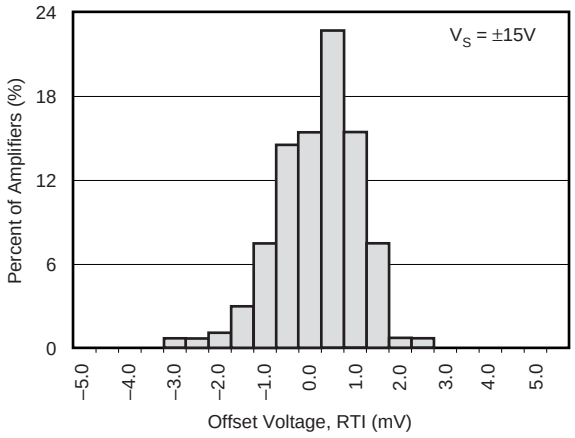
LARGE-SIGNAL CAPACITIVE LOAD RESPONSE (C_L = 1nF and 10nF)



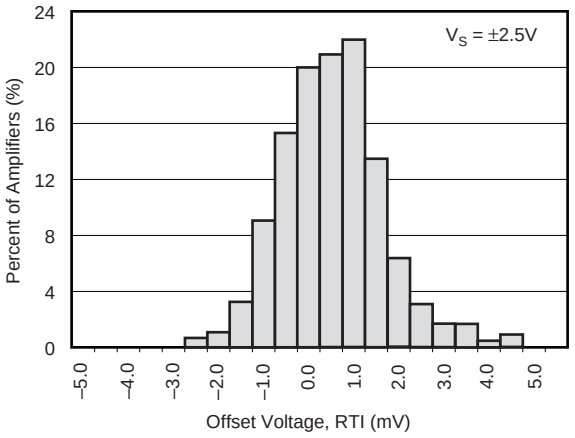
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, unless otherwise noted.

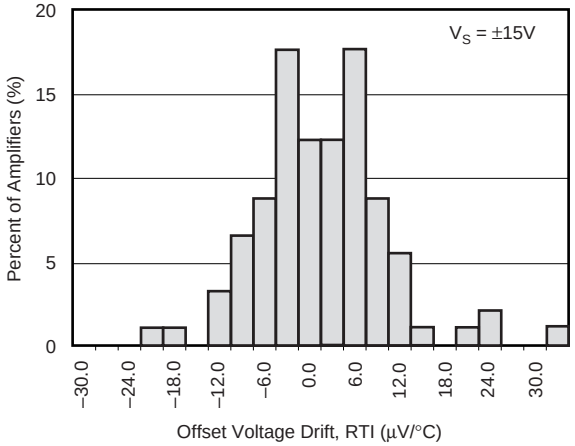
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



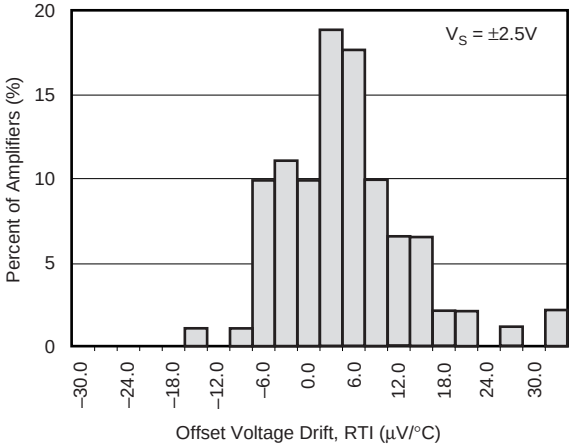
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



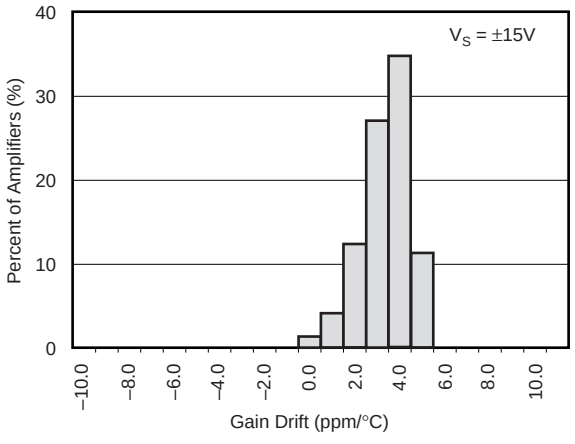
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



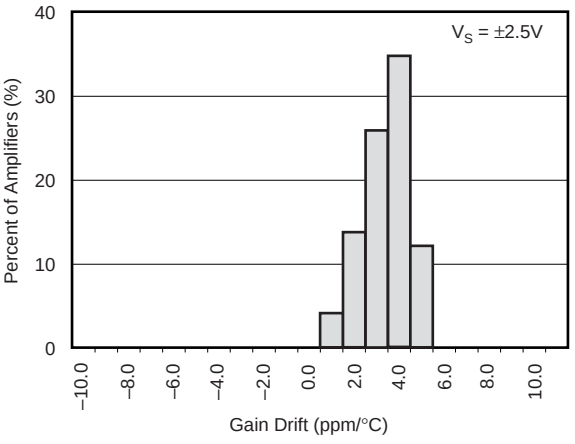
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



GAIN DRIFT PRODUCTION DISTRIBUTION



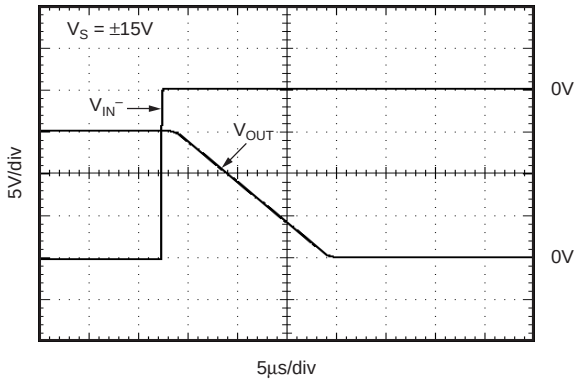
GAIN DRIFT PRODUCTION DISTRIBUTION



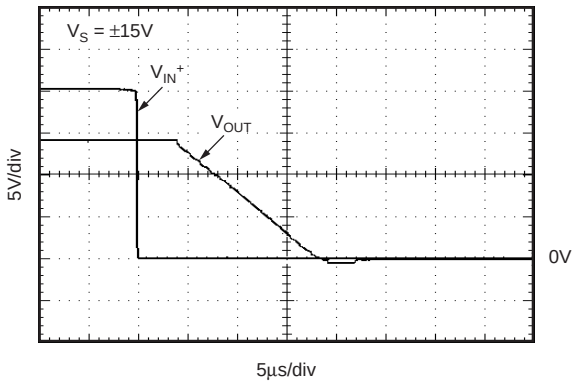
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ to common, and V_{REF} = 0V, unless otherwise noted.

INVERTING INPUT
50% OVERLOAD RECOVERY TIME



NON-INVERTING INPUT
50% OVERLOAD RECOVERY TIME



APPLICATION INFORMATION

The INA148 is a unity gain difference amplifier with a high common-mode input voltage range. A basic diagram of the circuit and pin connections is shown in Figure 1.

To achieve its high common-mode voltage range, the INA148 features a precision laser-trimmed thin-film resistor network with a 20:1 input voltage divider ratio. High input voltages are thereby reduced in amplitude, allowing the internal op amp to "see" input voltages that are within its linear operating range. A "Tee" network in the op amp feedback network places the amplifier in a gain of 20V/V, thus restoring the circuit's overall gain to unity (1V/V).

External voltages can be summed into the amplifier's output by using the Ref pin, making the differential amplifier a highly versatile design tool. Voltages on the Ref pin will also influence the INA148's common-mode voltage range.

In accordance with good engineering practice for linear integrated circuits, the INA148's power-supply bypass capacitors should be connected as close to pins 4 and 7 as practicable. Ceramic or tantalum types are recommended for use as bypass capacitors.

The input impedances are unusually high for a difference amplifier and this should be considered when routing input signal traces on a PC board. Avoid placing digital signal traces near the difference amplifier's input traces to minimize noise pickup.

OPERATING VOLTAGE

The INA148 is specified for ±15V and ±5V dual supplies and +5V single supplies. The INA148 can be operated with single or dual supplies with excellent performance.

The INA148 is fully characterized for supply voltages from ±1.35V to ±18V and over temperatures of –55ºC to +125 ºC. Parameters that vary significantly with operating voltage, load conditions, or temperature are shown in the Typical Performance Curves section.

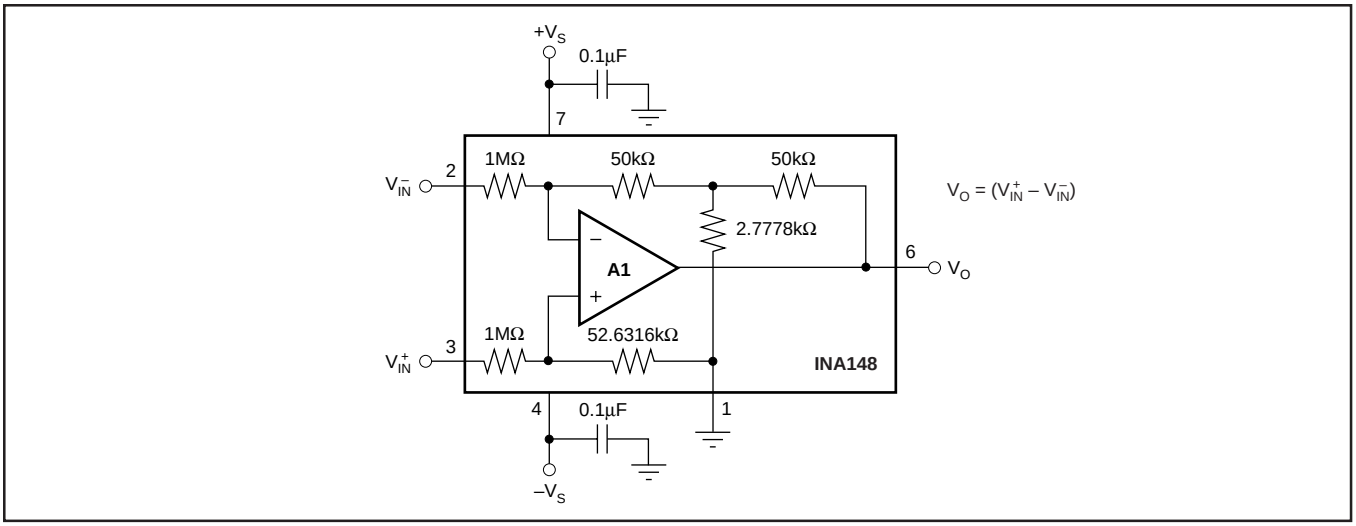


FIGURE 1. Basic Circuit Connections.

THE GAIN EQUATION

An internal on-chip resistor network sets the overall differential gain of the INA148 to precisely 1V/V. It's output is accordance with the equation:

$$V_{OUT} = (V_{IN}^{+} - V_{IN}^{-}) + V_{REF} \quad (1)$$

COMMON-MODE RANGE

The 20:1 input resistor ratio of the INA148 provides an input common-mode range that extends well beyond its power supply rails.

The exact input voltage range depends on the amplifier's power-supply voltage and the voltage applied to the Ref terminal (pin 1). Typical input voltage ranges at different power supply voltages can be found in the applications circuits section.

OFFSET TRIM

The INA148 is laser-trimmed for low offset voltage and drift. Most applications will require no external offset adjustment.

Since a voltage applied to the reference (Ref) pin (pin 1) will be summed directly into the amplifier's output signal, this technique can be used to null the amplifier's input offset voltage. Figure 2 shows an optional circuit for trimming the offset voltage.

To maintain high common-mode rejection (CMR), the source impedance of any signal applied to the Ref terminal should be very low (≤5Ω).

A source impedance of only 10Ω at the Ref pin will reduce the INA148's CMR to approximately 74dB. High CMR can be restored if a resistor is added in series with the amplifier's positive input terminal (pin 3). This resistor should be 19 times the source impedance that drives the Ref pin. For example, if the Ref pin sees a source impedance of 10Ω, a resistor of 190Ω should be added in series with pin 3.

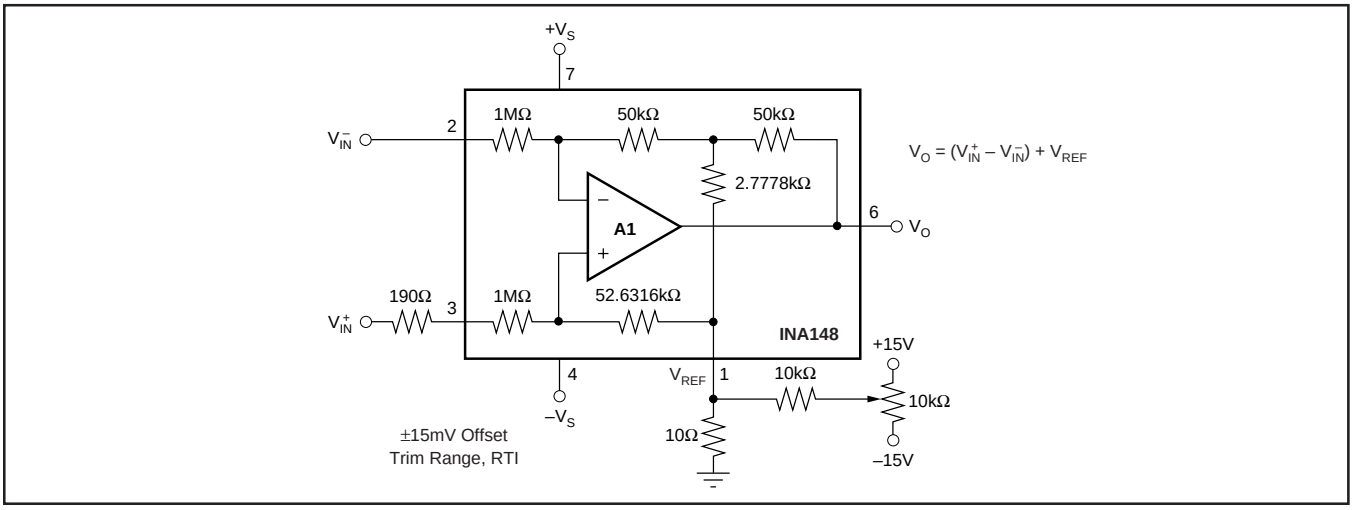


FIGURE 2. Optional Offset Trim Voltage.

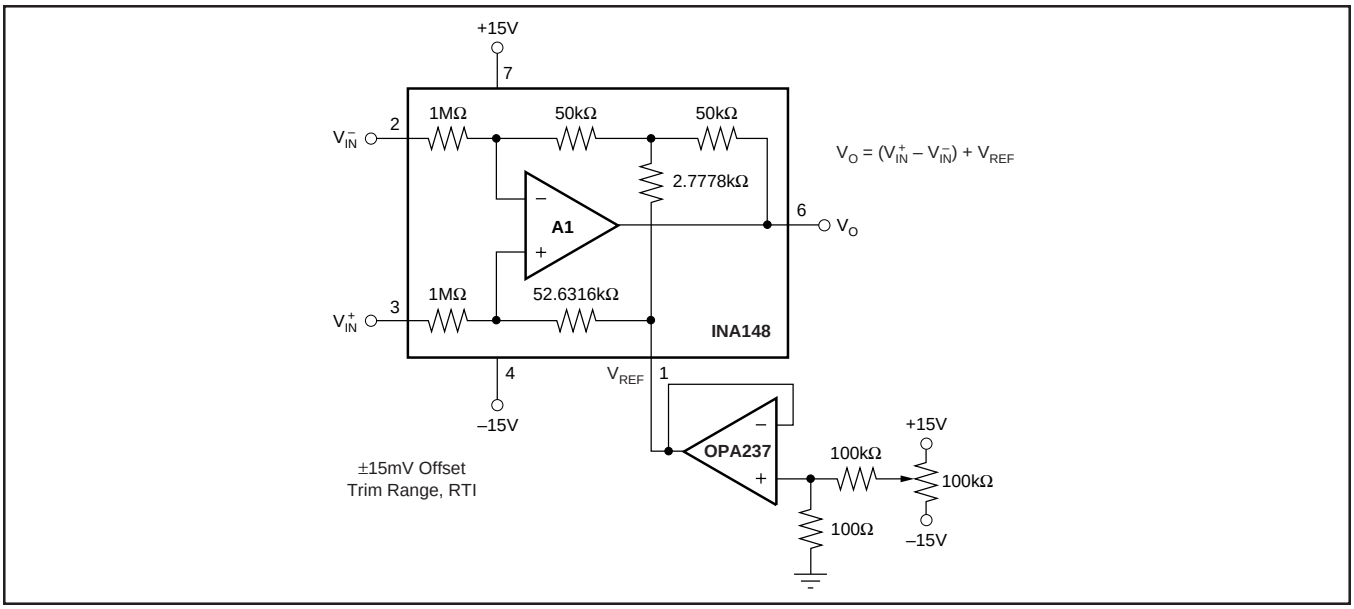


FIGURE 3. Preferred Offset Trim Circuit.

Preferably, the offset trim voltage applied to the Ref pin should be buffered with an amp such as an OPA237 (see Figure 3). In this case, the op amp output impedance is low enough that no external resistor is needed to maintain the INA148's excellent CMR.

INPUT IMPEDANCE

The input resistor network determines the impedance of each of the INA148's inputs. It is approximately 1MΩ. Unlike an instrumentation amplifier, signal source impedances at the two input terminals must be nearly equal to maintain good common-mode rejection.

A mismatch between the two inputs' source impedances will cause a differential amplifier's common-mode rejection to be degraded. With a source impedance imbalance of only 500Ω, CMR can fall to approximately 66dB.

Figure 4 shows a common application—measuring power supply current through a shunt resistor (R_S). A shunt resistor creates an unbalanced source resistance condition that can degrade a differential amplifier's common mode rejection.

Unless the shunt resistor is less than approximately 100Ω, an additional equal compensating resistor (R_C) is recommended to maintain input balance and high CMR.

Source impedances (or shunts) greater than 5kΩ are not recommended, even if they are "perfectly" compensated. This is because the internal resistor network is laser-trimmed for accurate voltage divider ratios, but not necessarily to absolute values. Input resistors are shown as 1MΩ, however, this is only their nominal value.

In practice, the input resistors' absolute values may vary by as much as 30 percent. The two input resistors match to about 5 percent, so adding compensating resistors greater than 5kΩ can cause a serious mismatch in the resulting resistor network voltage divider ratios, thus degrading CMR.

Attempts to extend the INA148 input voltage range by adding external resistors is not recommended for the reasons just described in the last paragraph. CMR will suffer a serious degradation unless the resistors are carefully trimmed for CMR and gain. This is an iterative adjustment and can be tedious and time consuming.

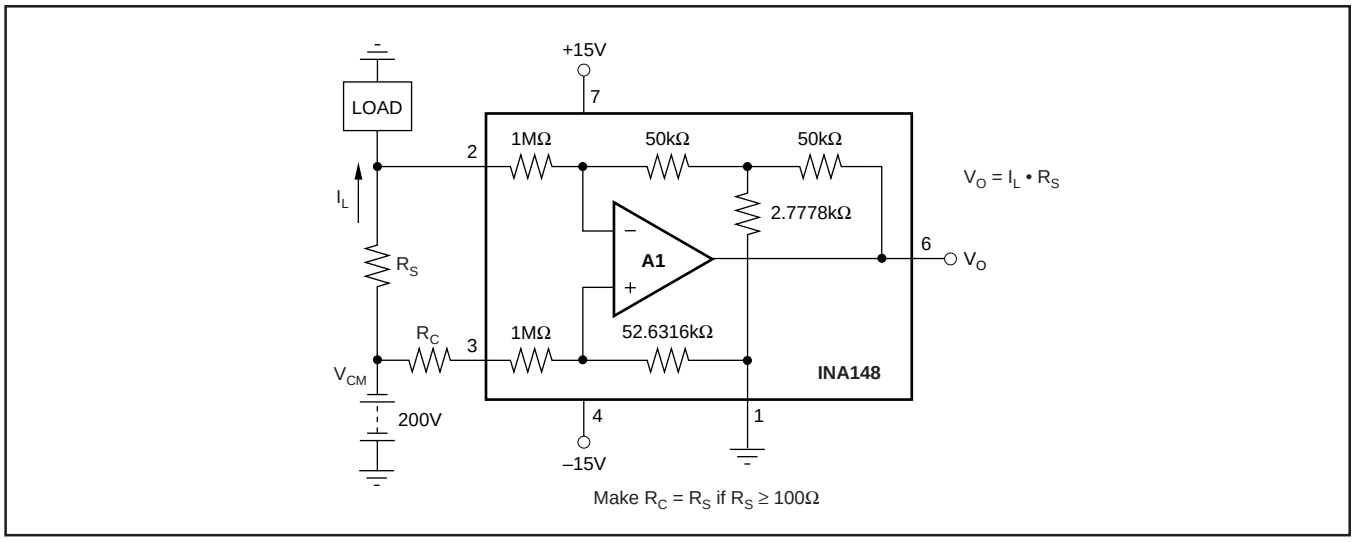


FIGURE 4. Shunt-Resistor Current Measurement Circuit.

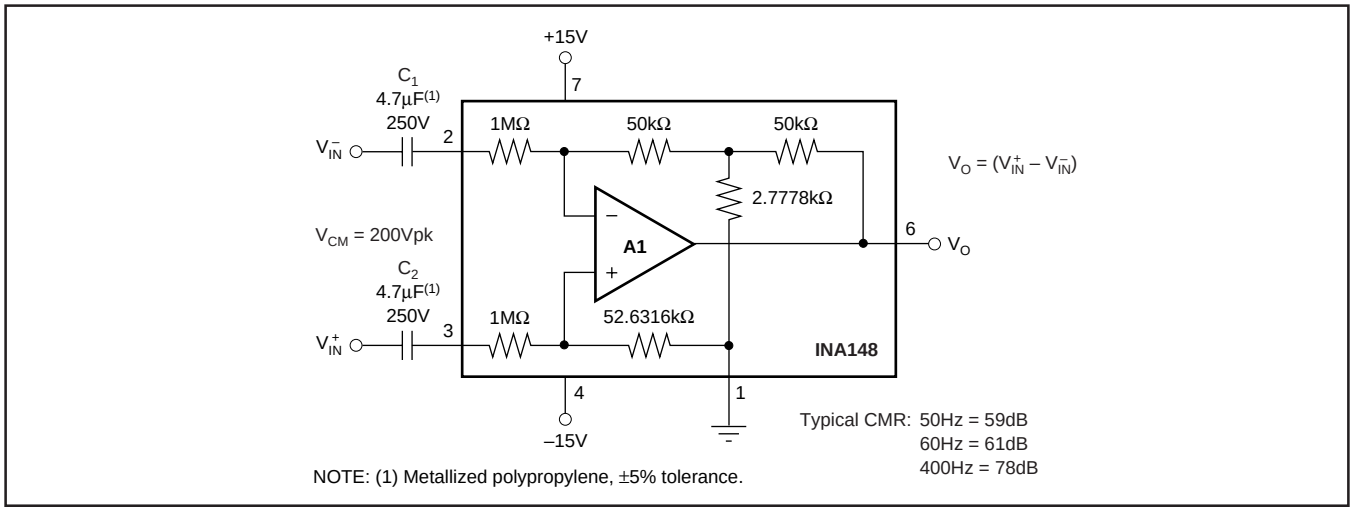


FIGURE 5. AC-Coupled Difference Amplifier.

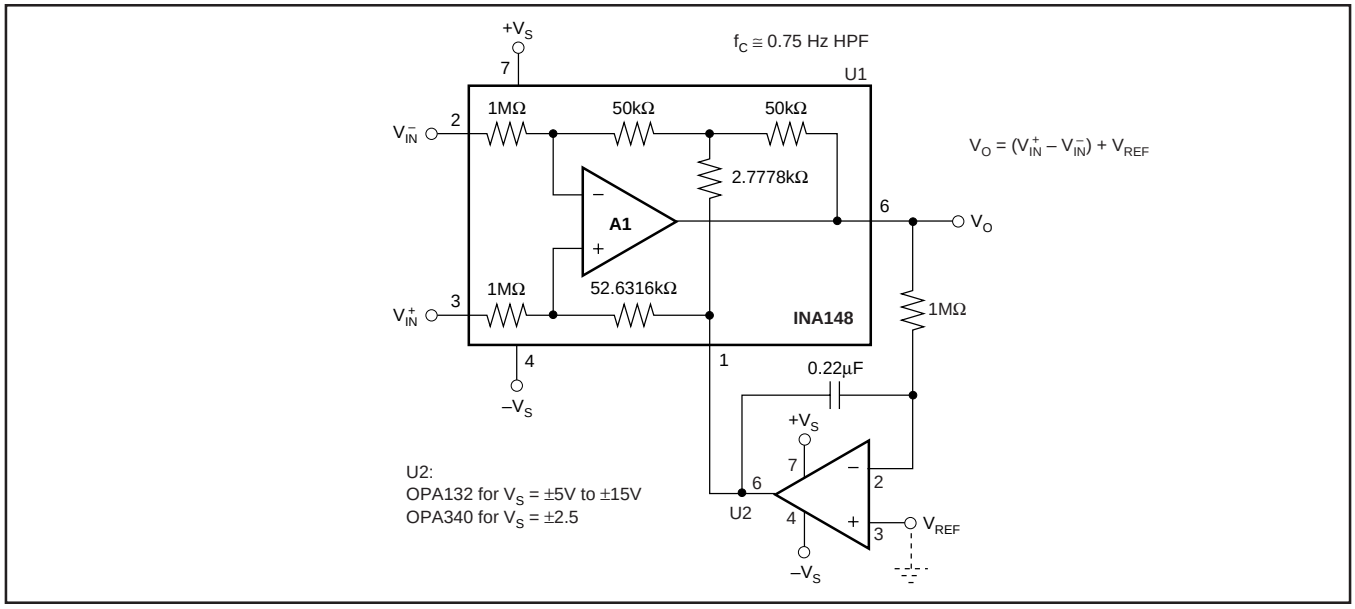


FIGURE 6. Quasi-AC-Coupled Differential Amplifier.

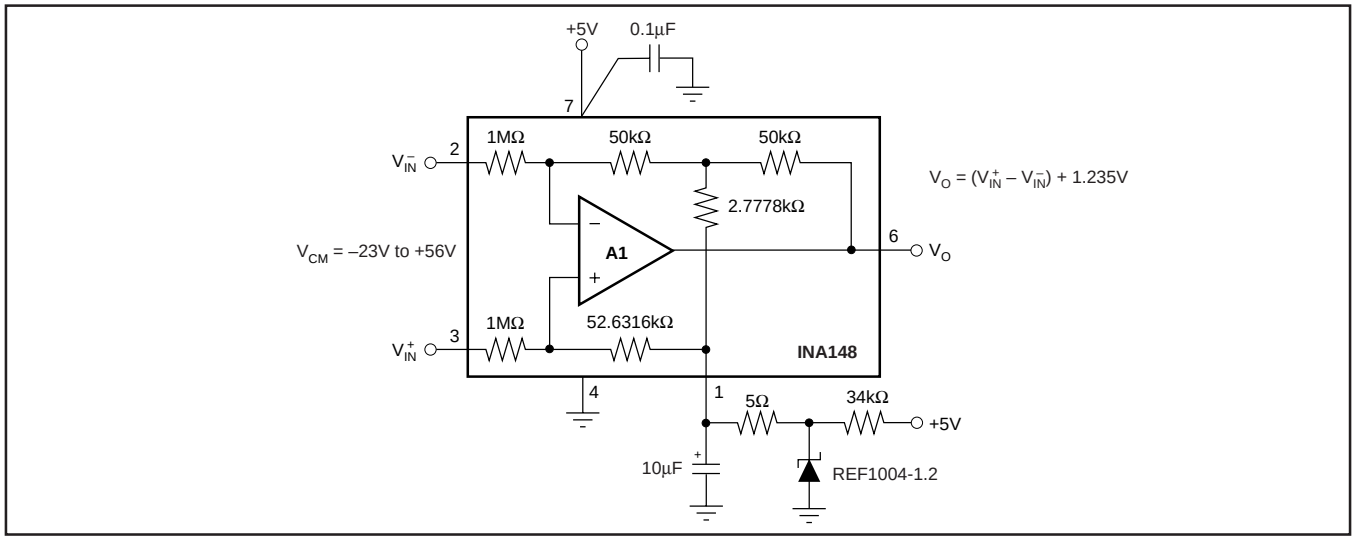


FIGURE 7. Single-Supply Differential Amplifier.

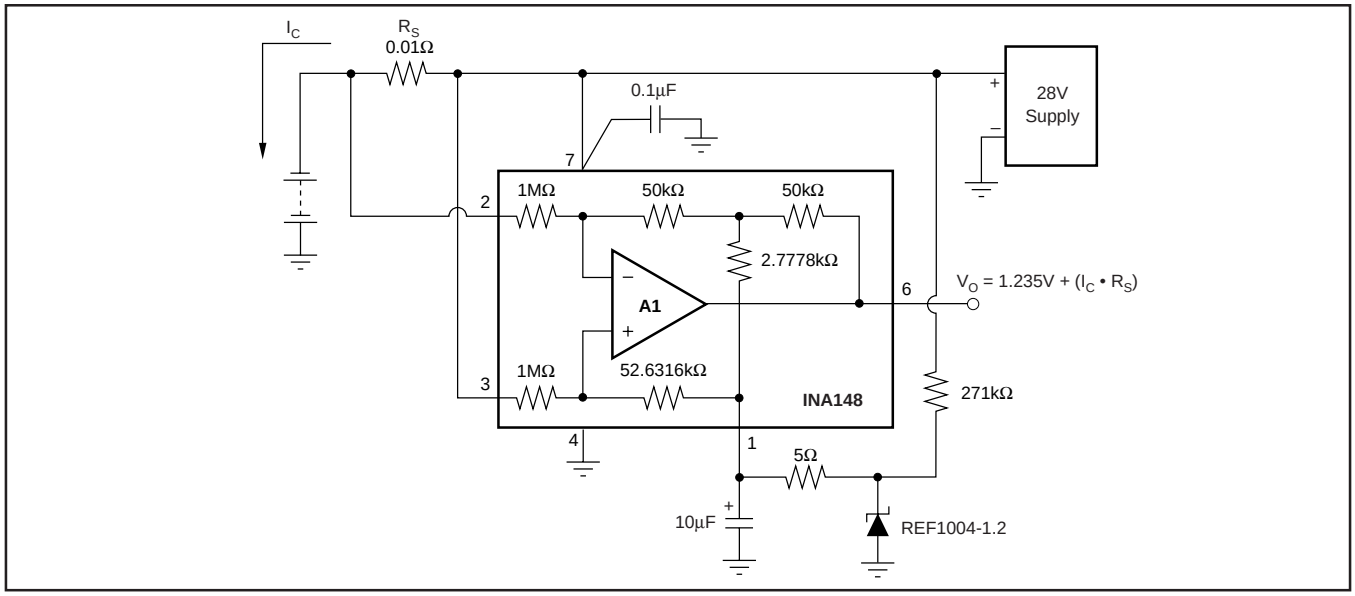


FIGURE 8. Battery Monitor Circuit.

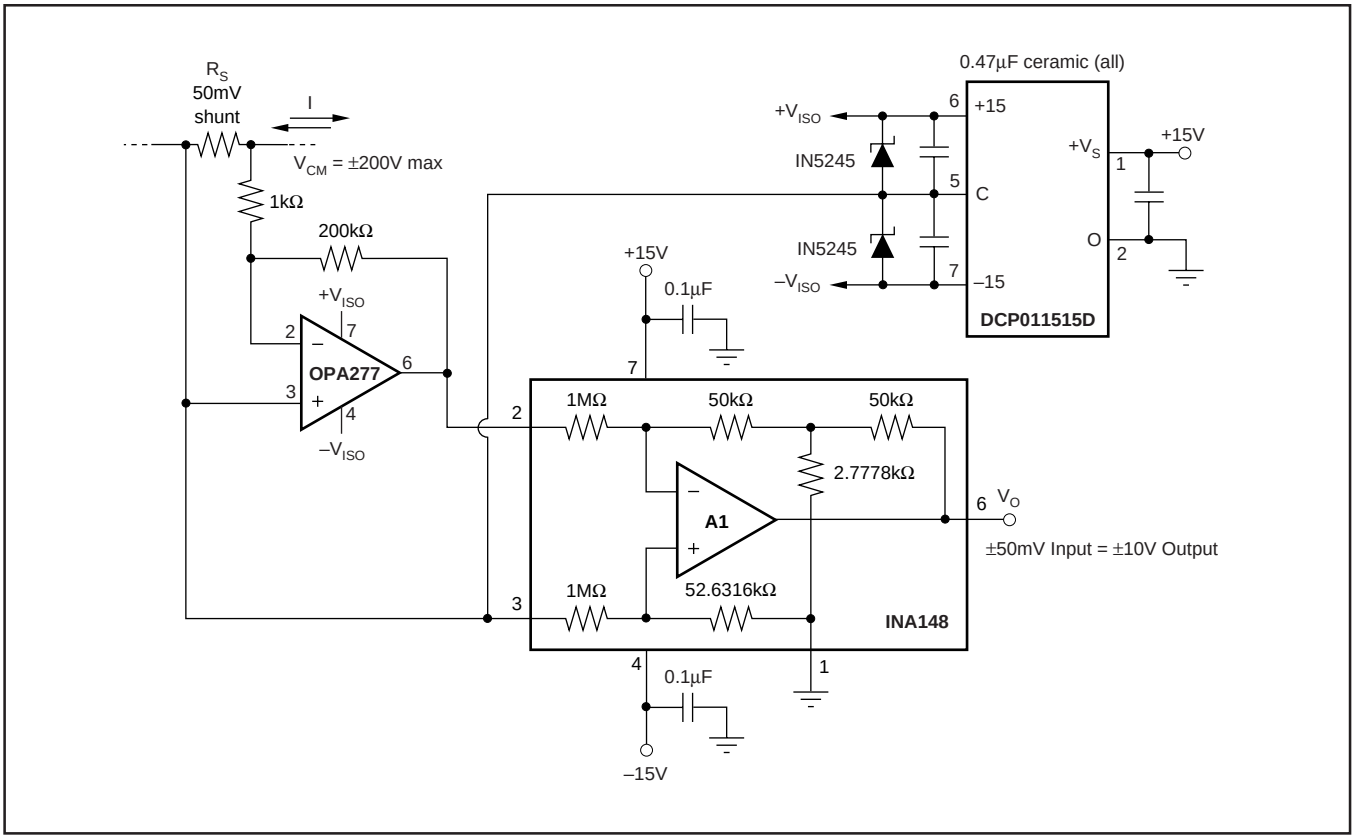


FIGURE 9. 50mV Current Shunt Amplifier with ±200V Common-Mode Voltage Range.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA148UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA	Samples
INA148UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA	Samples
INA148UA/2K5G4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA 148UA	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA148 :

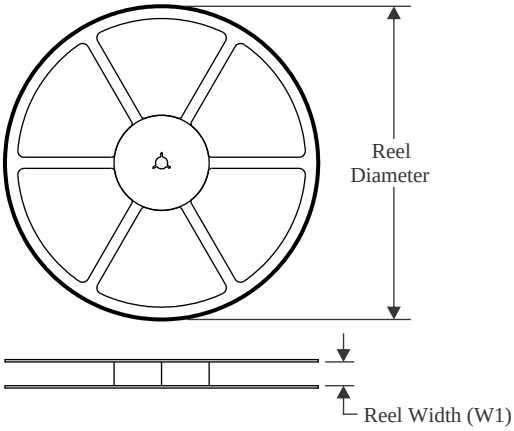
- Automotive : INA148-Q1

NOTE: Qualified Version Definitions:

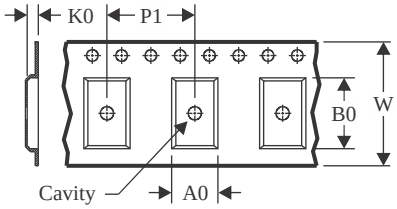
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

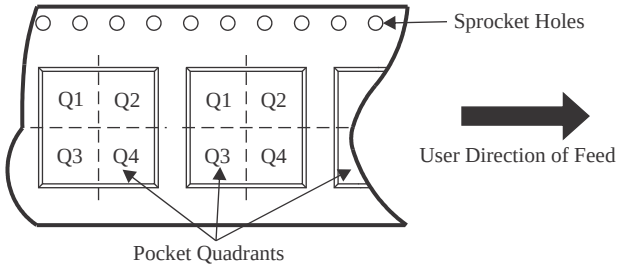


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

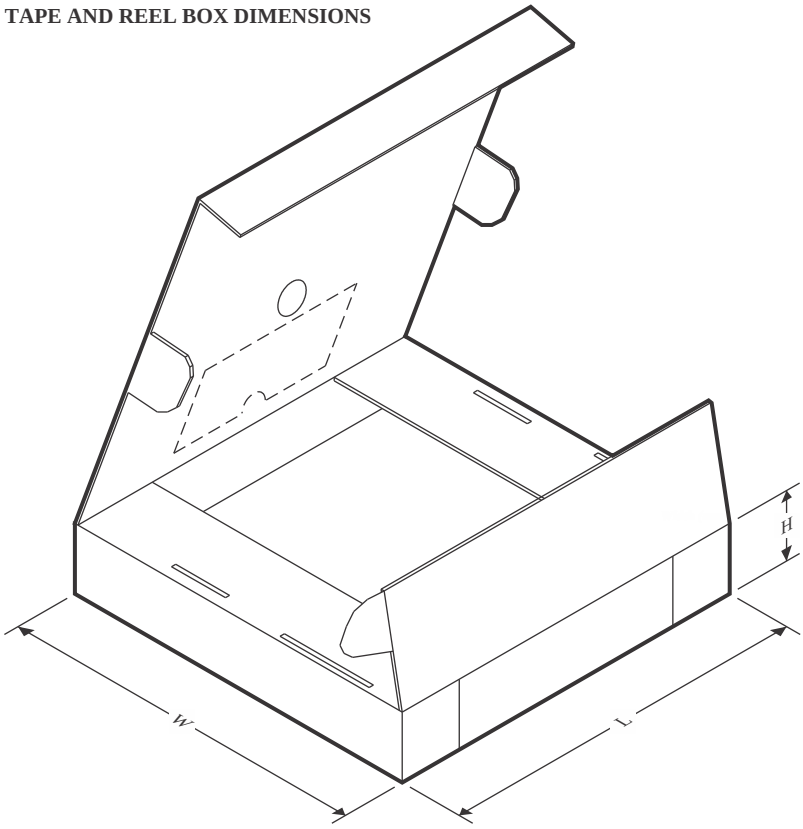
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA148UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

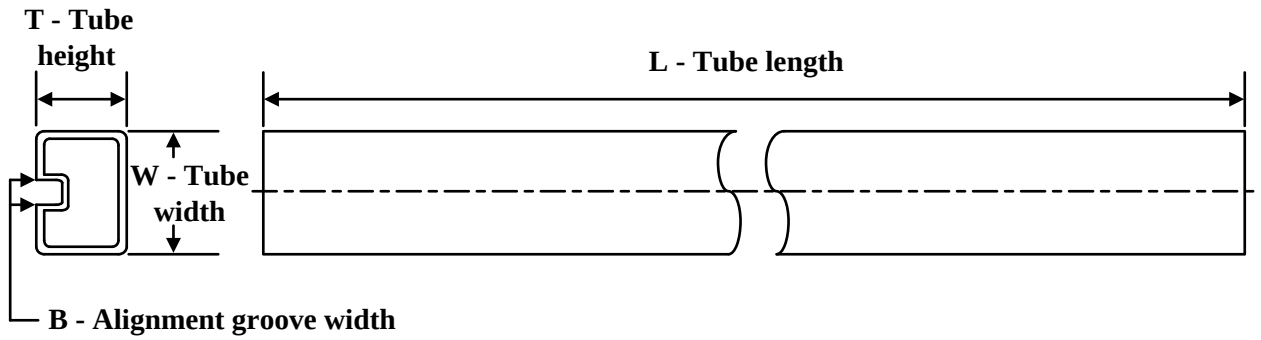
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA148UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA148UA	D	SOIC	8	75	506.6	8	3940	4.32

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