THE DATASHEET OF

INA126UA

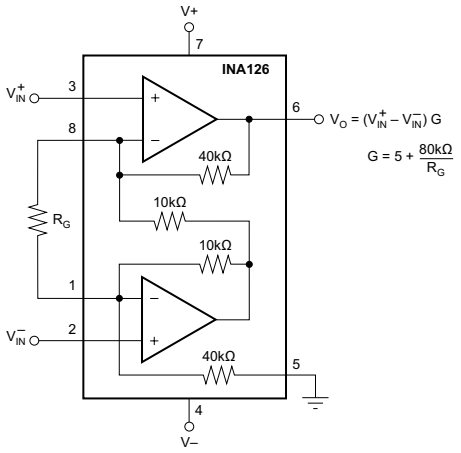
INAx126 MicroPower Instrumentation Amplifiers

1 Features

- Low quiescent current: 175 µA/channel
- Wide supply range: ±1.35 V to ±18 V
- Low offset voltage: 250-µV maximum
- Low offset drift: 3-µV/°C maximum
- Low noise: 35 nV/√Hz
- Low input bias current: 25-nA maximum
- Temperature range: –40°C to +85°C
- Multiple package options:
  - Single channel:
    - INA126P/PA 8-pin PDIP (P)
    - INA126U/UA 8-pin SOIC (D)
    - INA126E/EA 8-pin VSSOP (DGK)
  - Dual channels:
    - INA2126P/PA 16-pin PDIP (N)
    - INA2126U/UA 16-pin SOIC (D)
    - INA2126E/EA 16-pin SSOP (DBQ)

2 Applications

- Level transmitter
- Flow transmitter
- Multiparameter patient monitor
- Mixed module (AI, AO, DI, DO)
- AC charging (pile) station
- Infusion pump
- Electrocardiogram (ECG)



Simplified Schematic: INA126

3 Description

The INA126 and INA2126 (INAx126) are precision instrumentation amplifiers for accurate, low-noise, differential-signal acquisition. The two-op-amp design provides excellent performance with low quiescent current (175 µA/channel). These features combined with a wide operating voltage range of ±1.35 V to ±18 V make the INAx126 a great choice for portable instrumentation and data acquisition systems.

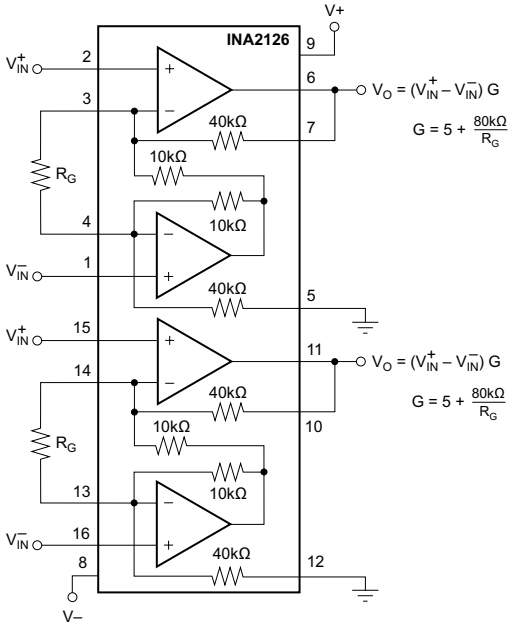
Gain can be set from 5 V/V to 10000 V/V with a single external resistor. Precision input circuitry provides low offset voltage (250 µV, maximum), low offset voltage drift (3 µV/°C, maximum), and excellent common-mode rejection.

All versions are specified for the –40°C to +85°C industrial temperature range.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
INA126	PDIP (8)	6.35 mm × 9.81 mm
	SOIC (8)	3.91 mm × 4.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
INA2126	PDIP (16)	6.35 mm × 19.30 mm
	SOIC (16)	3.91 mm × 9.90 mm
	SSOP (16)	3.90 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic: INA2126

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2015) to Revision C (December 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added dual supply specification to *Absolute Maximum Ratings*	5
• Deleted redundant operating temperature and input common mode voltage specifications in *Recommended Operating Conditions*	5
• Added dual supply and specified temperature specifications in *Recommended Operating Conditions*	5
• Added proper signs for PSRR and input bias current specifications in *Electrical Characteristics*	7
• Deleted V_O = 0 V test condition of common-mode voltage specification in *Electrical Characteristics*	7
• Changed common-mode voltage specification from ±11.25 V minimum, to –11.25 V minimum and 11.25 V maximum, in *Electrical Characteristics*	7
• Changed minimum CMRR specification for INA126U/E, INA2126E from 83 dB to 80 dB in *Electrical Characteristics*	7
• Added typical input bias current specification of ±10 nA for INA126PA/UA/EA and INA2126PA/UA/EA in *Electrical Characteristics*	7
• Changed current noise specifications in *Electrical Characteristics* from 60 fA/$\sqrt{\text{Hz}}$ to 160 fA/$\sqrt{\text{Hz}}$ for f = 1 kHz, and from 2 pApp to 7.3 pApp for f = 0.1 Hz to 10 Hz	7
• Changed test condition for short-circuit current specification in *Electrical Characteristics* from "Short circuit to ground" to "Continuous to V_S / 2" for clarity	7
• Changed short-circuit current specification in *Electrical Characteristics* from +10/-5 mA to ±5 mA	7
• Deleted redundant voltage range, operating temperature range, and specification temperature range specifications from *Electrical Characteristics*	7
• Changed Figures 6-7, 6-10, 6-13, 6-14, 6-15, 6-16, 6-17	9
• Added Figure 6-11	9

Changes from Revision A (August 2005) to Revision B (December 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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5 Pin Configuration and Functions

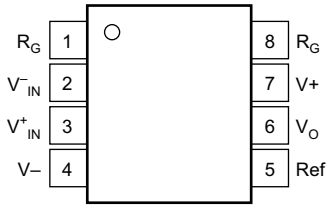

Figure 5-1. INA126: P (8-Pin PDIP), D (8-Pin SOIC), and DGK (8-Pin VSSOP) Packages, Top View

Table 5-1. Pin Functions: INA126

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 8	R_G	—	Gain setting pin. For gains greater than 5 place a gain resistor between pin 1 and pin 8.
2	$V–_{IN}$	I	Negative input
3	$V+_{IN}$	I	Positive input
4	V–	—	Negative supply
5	Ref	I	Reference input. This pin must be driven by a low impedance or connected to ground.
6	V_O	O	Output
7	V+	—	Positive supply

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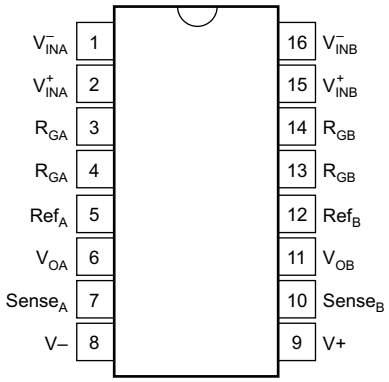

Figure 5-2. INA2126: N (16-Pin PDIP), D (16-Pin SOIC), and DBQ (16-Pin SSOP) Packages, Top View

Table 5-2. Pin Functions: INA2126

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$V–_{INA}$	I	Negative input for amplifier A
2	$V+_{INA}$	I	Positive input for amplifier A
3, 4	R_{GA}	—	Gain setting pin for amplifier A. For gains greater than 5 place a gain resistor between pin 3 and pin 4.
5	Ref_A	I	Reference input for amplifier A. This pin must be driven by a low impedance or connected to ground.
6	V_{OA}	O	Output of amplifier A
7	$Sense_A$	I	Feedback for amplifier A. Connect to VOA, amplifier A output.
8	V–	—	Negative supply
9	V+	—	Positive supply
10	$Sense_B$	I	Feedback for amplifier B. Connect to VOB, amplifier B output.
11	V_{OB}	O	Output of amplifier B
12	Ref_B	I	Reference input for amplifier B. This pin must be driven by a low impedance or connected to ground.
13, 14	R_{GB}	—	Gain setting pin for amplifier B. For gains greater than 5 place a gain resistor between pin 13 and pin 14.
15	$V+_{INB}$	I	Positive input for amplifier B
16	$V–_{INB}$	I	Negative input for amplifier B

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage dual supply, V_S = (V+) – (V–)		±18	V
	Supply voltage single supply, V_S = (V+) – (V–)		36	
	Input signal voltage(2)	(V–) – 0.7	(V+) + 0.7	V
	Input signal current(2)		10	mA
	Output short-circuit(3)	Continuous		
T_A	Operating Temperature	–55	125	°C
	Lead temperature (soldering, 10 s)		300	°C
T_{stg}	Storage Temperature	–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input signal voltage is limited by internal diodes connected to power supplies. See Input Protection.
(3) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	2.7	30	36	V
		Dual-supply	±1.35	±15	±18	
T_A	Specified temperature		–40		85	°C

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6.4 Thermal Information: INA126

THERMAL METRIC[1]		INA126			UNIT
		PDIP	SOIC	VSSOP	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.2	116.4	167.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.6	62.4	60.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	57.7	88.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.9	10.0	7.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.2	57.1	87.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: INA2126

THERMAL METRIC[1]		INA2126			UNIT
		PDIP	SOIC	SSOP	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.3	76.2	115.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	37.8	67.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	33.5	58.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.7	7.5	19.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	33.3	57.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.6 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 25 kΩ, V_{REF} = 0 V, and V_{CM} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage (RTI)	INA126P/U/E INA2126P/U/E			±100	±250	µV
		INA126PA/UA/EA INA2126PA/UA/EA			±150	±500	
	Offset voltage drift (RTI)	T_A = –40°C to +85°C	INA126P/U/E INA2126P/U/E		±0.5	±3	µV/°C
			INA126PA/UA/EA INA2126PA/UA/EA		±0.5	±5	
PSRR	Power-supply rejection ratio (RTI)	V_S = ±1.35 V to ±18 V	INA126P/U/E INA2126P/U/E		±5	±15	uV/V
			INA126PA/UA/EA INA2126PA/UA/EA		±5	±50	
	Input impedance				1 || 4		GΩ || pF
	Safe input voltage	R_S = 0 Ω		(V–) – 0.5		(V+) + 0.5	V
		R_S = 1 kΩ		(V–) – 10		(V+) + 10	
V_{CM}	Common-mode voltage[1]			–11.25	±11.5	11.25	V
	Channel seperation (dual)	G = 5, dc			130		dB
CMRR	Common-mode rejection ratio	R_S = 0 Ω, V_{CM} = ±11.25 V	INA126P INA2126P	83	94		dB
			INA126U/E INA2126U/E	80	94		
			INA126PA/UA/EA INA2126PA/UA/EA	74	83		
INPUT BIAS CURRENT							
I_B	Input bias current	INA126P/U/E INA2126P/U/E			±10	±25	nA
		INA126PA/UA/EA INA2126PA/UA/EA			±10	±50	
	Input bias current drift	T_A = –40°C to +85°C			±30		pA/°C
I_{OS}	Input offset current	INA126P/U/E INA2126P/U/E			±0.5	±2	nA
		INA126PA/UA/EA INA2126PA/UA/EA			±0.5	±5	nA
	Input offset current drift	T_A = –40°C to +85°C			±10		pA/°C
GAIN							
	Gain equation				5 + (80 kΩ / R_G)		V/V
G	Gain			5		10000	V/V
GE	Gain error	G = 5 , V_O = ±14 V	INA126P/U/E INA2126P/U/E		±0.02	±0.1	%
			INA126PA/UA/EA INA2126PA/UA/EA		±0.02	±0.18	
		G = 100, V_O = ±12 V	INA126P/U/E INA2126P/U/E		±0.2	±0.5	
			INA126PA/UA/EA INA2126PA/UA/EA		±0.2	±1	
	Gain drift[2]	T_A = –40°C to +85°C	G = 5		±2	±10	ppm/°C
			G = 100		±25	±100	
	Gain nonlinearity	G = 100, V_O = ±14 V			±0.002	±0.012	%

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6.6 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 25 kΩ, V_{REF} = 0 V, and V_{CM} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE							
e_N	Voltage noise	f = 1 kHz			35		nV/√Hz
		f = 100 Hz			35		
		f_B = 10 Hz			45		
		f_B = 0.1 Hz to 10 Hz			0.7		μV_{PP}
I_n	Current noise	f = 1 kHz			160		fA/√Hz
		f_B = 0.1Hz to 10Hz			7.3		pA_{PP}
OUTPUT							
	Positive output voltage swing			(V+) – 0.9	(V+) – 0.75		V
	Negative output voltage swing			(V–) + 0.95	(V–) + 0.8		V
I_{SC}	Short-circuit current	Continuous to V_S / 2			±5		mA
C_L	Load capacitance	Stable operation			1000		pF
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 5			200		kHz
		G = 100			9		
		G = 500			1.8		
SR	Slew rate	G = 5, V_O = ±10 V			0.4		V/µs
t_S	Settling time	To 0.01%, V_{STEP} = 10 V	G = 5		30		µs
			G = 100		160		
			G = 500		1500		
	Overload recovery	50% input overload			4		µs
POWER SUPPLY							
I_Q	Quiescent current (per channel)	I_O = 0 mA			±175	±200	µA

(1) Input voltage range of the instrumentation amplifier input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves.
(2) The values specified for G > 5 do not include the effects of the external gain-setting resistor, R_G.

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6.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

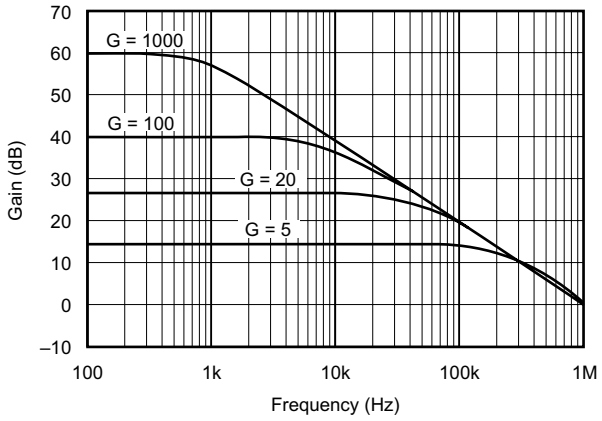


Figure 6-1. Gain vs Frequency

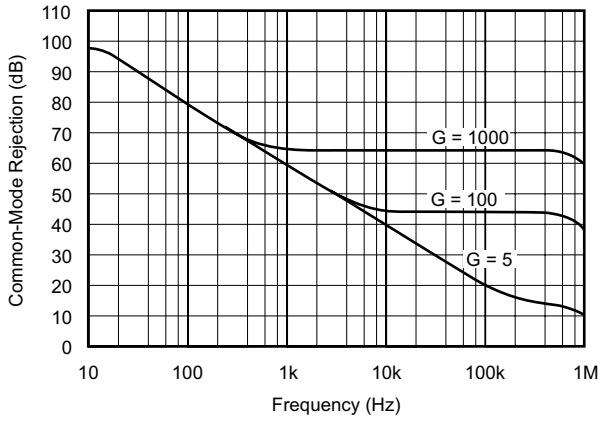


Figure 6-2. Common-Mode Rejection vs Frequency

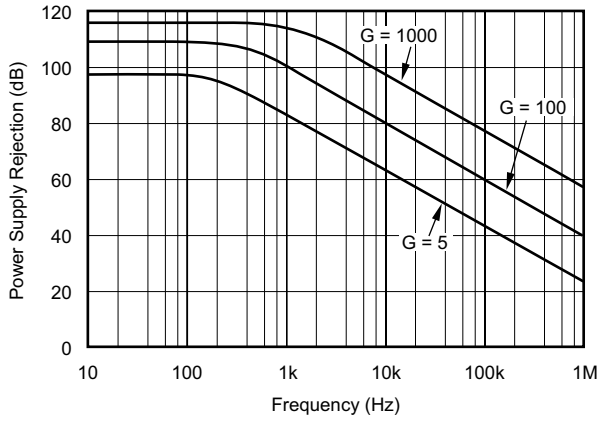


Figure 6-3. Positive Power Supply Rejection vs Frequency

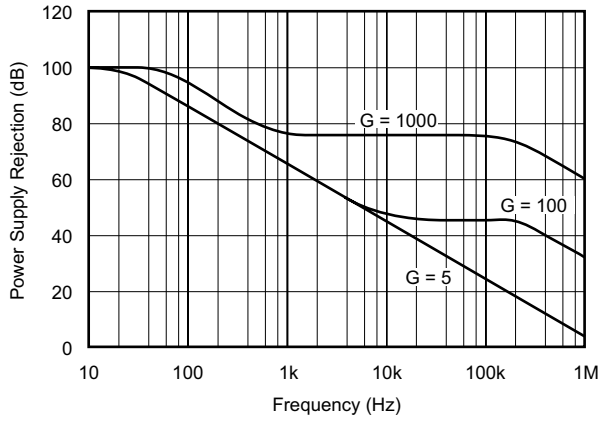
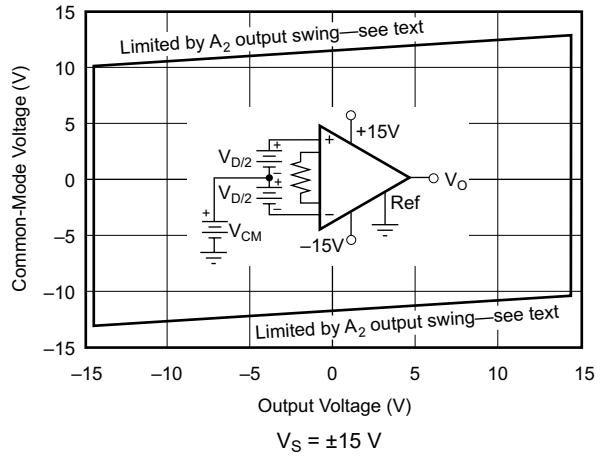
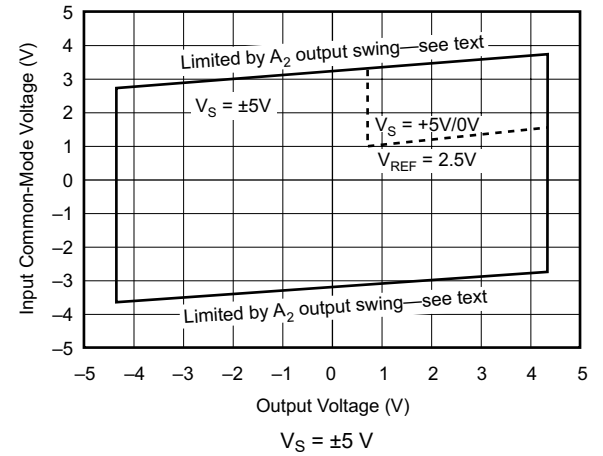


Figure 6-4. Negative Power Supply Rejection vs Frequency



V_S = ±15 V

Figure 6-5. Input Common-Mode Voltage Range vs Output Voltage



V_S = ±5 V

Figure 6-6. Input Common-Mode Voltage Range vs Output Voltage

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

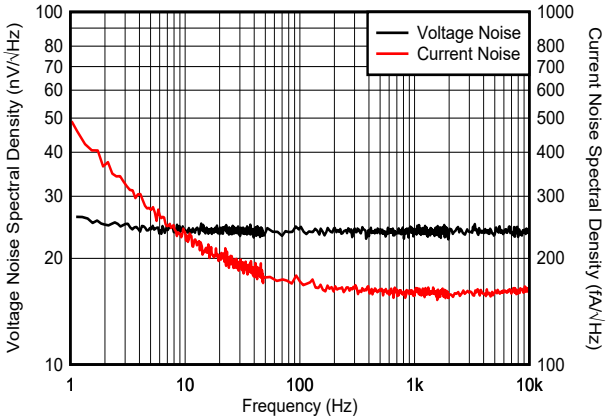

Figure 6-7. Input-Referred Noise vs Frequency

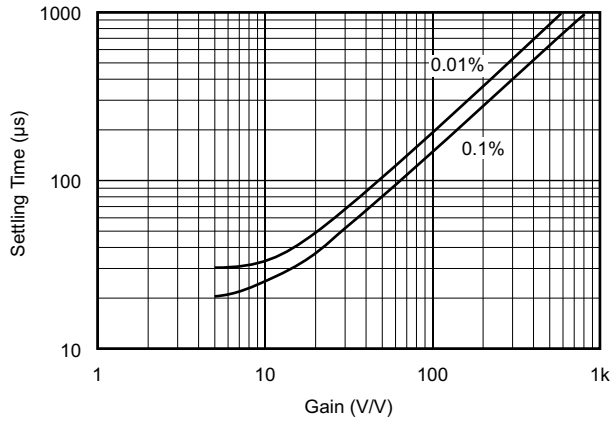

Figure 6-8. Settling Time vs Gain

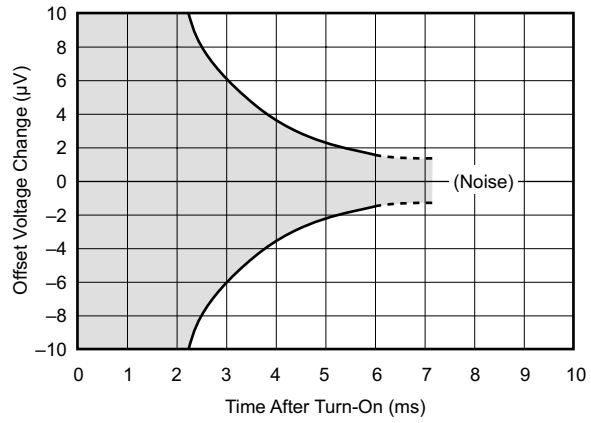

Figure 6-9. Input-Referred Offset Voltage WarmUp

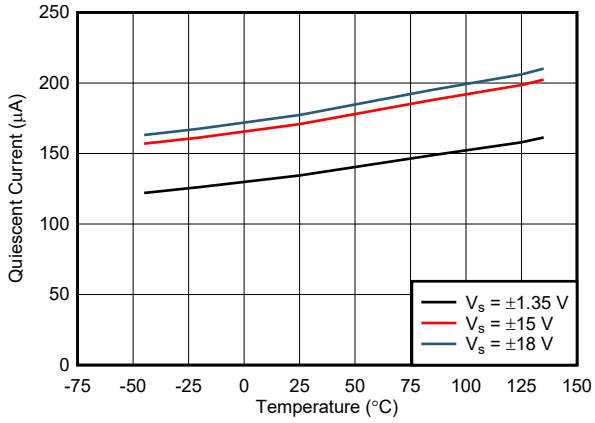

Figure 6-10. Quiescent Current vs Temperature

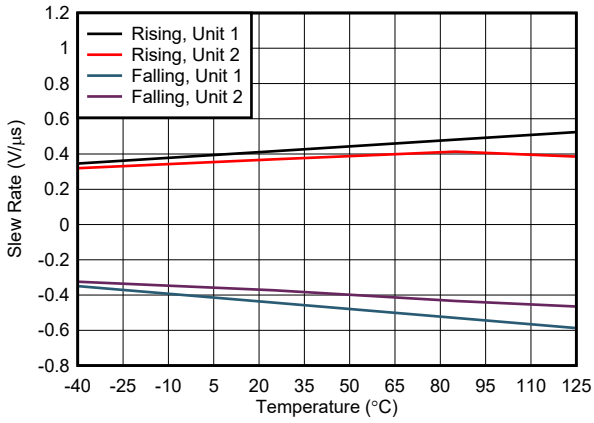

Figure 6-11. Slew Rate vs Temperature

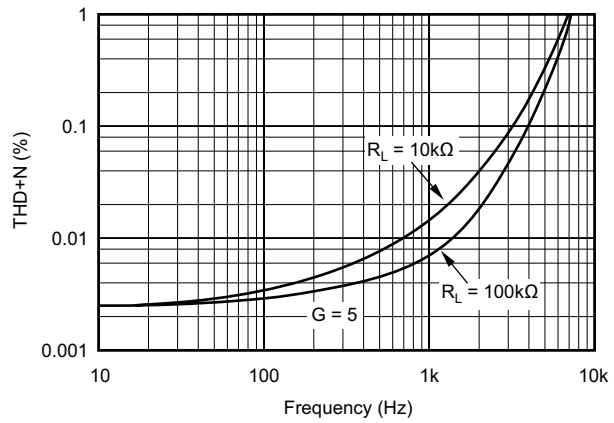

Figure 6-12. Total Harmonic Distortion + Noise vs Frequency

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6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V (unless otherwise noted)

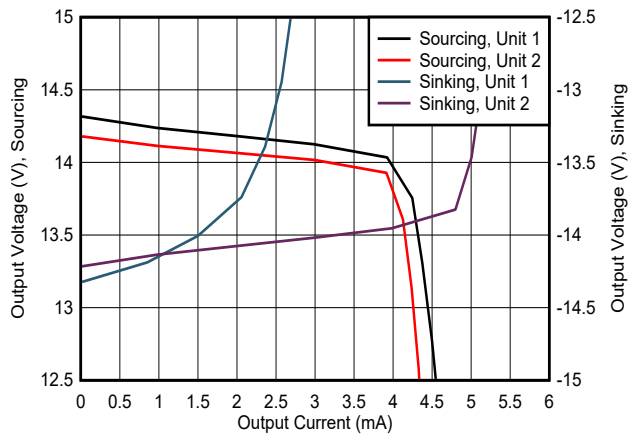
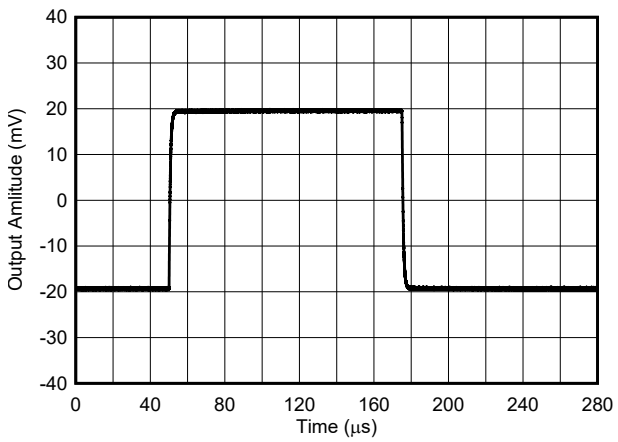
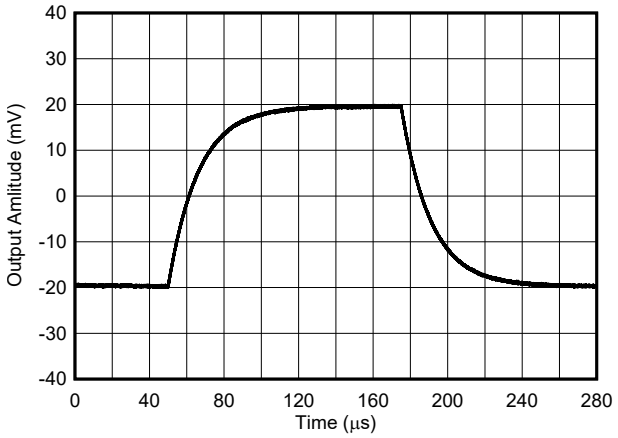


Figure 6-13. Output Voltage Swing vs Output Current



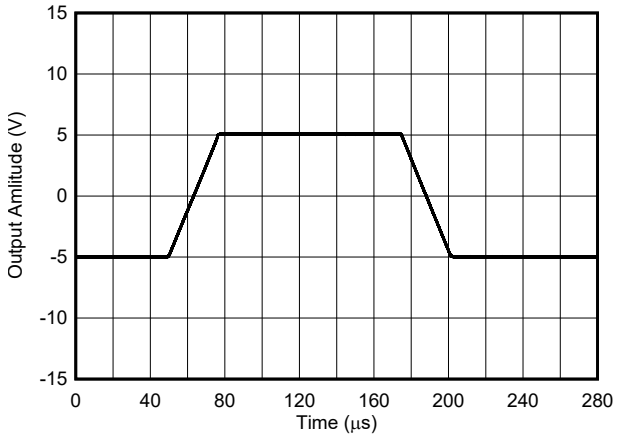
G = 5

Figure 6-14. Small-Signal Response



G = 100

Figure 6-15. Small-Signal Response



G = 5

Figure 6-16. Large-Signal Response

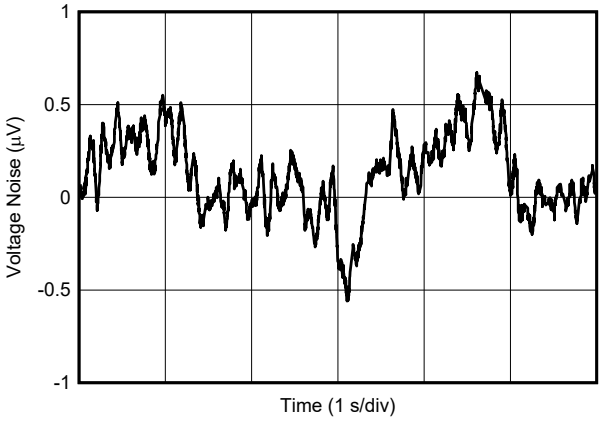


Figure 6-17. 0.1-Hz to 10-Hz Voltage Noise

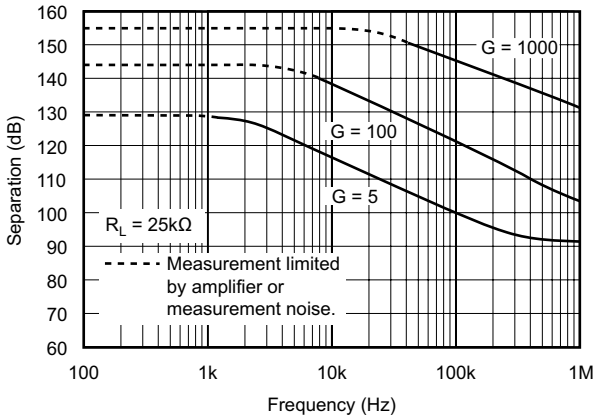


Figure 6-18. Channel Separation vs Frequency, RTI (Dual Version)

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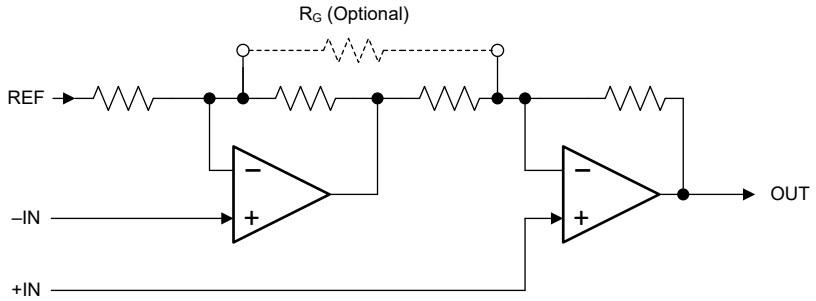
7 Detailed Description

7.1 Overview

The INAx126 use only two, rather than three, operational amplifiers, providing savings in power consumption. In addition, the input resistance is high and balanced, thus permitting the signal source to have an unbalanced output impedance.

A minimum circuit gain of 5 permits an adequate dc common-mode input range, as well as sufficient bandwidth for most applications.

7.2 Functional Block Diagram



7.3 Feature Description

The INAx126 are low-power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile two-operational-amplifier design and small size make the amplifiers an excellent choice for a wide range of applications. The two-op-amp topology reduces power consumption. A single external resistor sets any gain from 5 to 10,000. These devices operate with power supplies as low as ±1.35 V, and a quiescent current of 200 µA maximum.

7.4 Device Functional Modes

7.4.1 Single-Supply Operation

The INAx126 can be used on single power supplies from 2.7 V to 36 V. Use the output REF pin to level shift the internal output voltage into a linear operating condition. Ideally, connect the REF pin to a potential that is midsupply to avoid saturating the output of the amplifiers. See *Section 8.1* for information on how to adequately drive the reference pin.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INAx126 measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high input impedance make the INAx126 an excellent choice for a wide range of applications. The INAx126 can adjust the functionality of the output signals by setting the reference pin, giving additional flexibility that is practical for multiple configurations.

8.2 Typical Application

Figure 8-1 shows the basic connections required for operation of the INA126. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of 8 Ω in series with the Ref pin causes a typical device to degrade to approximately 80-dB CMR.

Figure 8-4 depicts a desired differential signal from a sensor at 1 kHz and 5 mV_{PP} superimposed on top of a 1-V_{PP}, 60-Hz common-mode signal (the 1-kHz signal can not be resolved in this scope trace). The FFT trace in Figure 8-5 shows the two signals. Figure 8-6 shows the clearly recovered differential signal at the output of the INA126 operating at a gain of 250. The FFT of Figure 8-7 shows the 60-Hz common-mode is no longer visible.

The dual version INA2126 has feedback-sense connections, $Sense_A$ and $Sense_B$, that must be connected to the respective output pins for proper operation. The sense connection can sense the output voltage directly at the load for best accuracy.

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G VALUE
5	NC	NC
10	16k	15.8k
20	5333	5360
50	1779	1780
100	842	845
200	410	412
500	162	162
1000	80.4	80.6
2000	40.1	40.2
5000	16.0	15.8
10000	8.0	7.87

NC: No Connection.

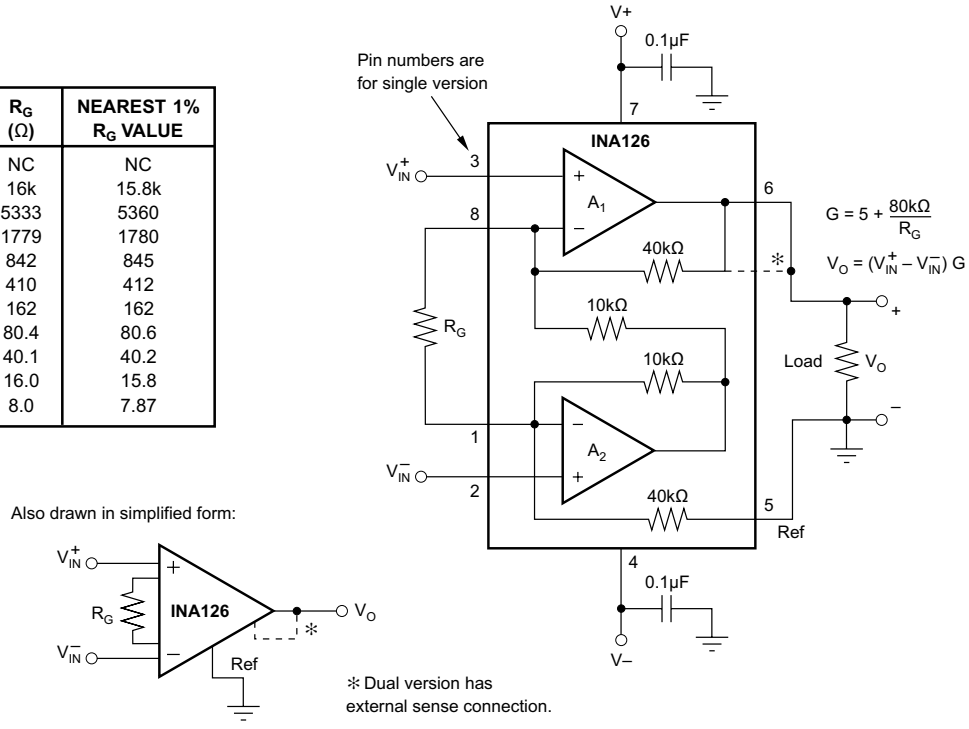

Figure 8-1. Basic Connections

8.2.1 Design Requirements

For the traces shown in Figure 8-2 and Figure 8-3:

- Common-mode rejection of at least 80 dB
- Gain of 250

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

Gain is set by connecting an external resistor, R_G:

$$g = 5 + 80\ k\Omega / R_G \quad (1)$$

Commonly used gains and R_G resistor values are shown in Figure 8-1.

The 80-kΩ term in Equation 1 comes from the internal metal-film resistors, which are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The R_G contribution to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error in gains of approximately 100 or greater.

8.2.2.2 Offset Trimming

The INAx126 family features low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 8-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref pin is added to the output signal. An operational amplifier buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

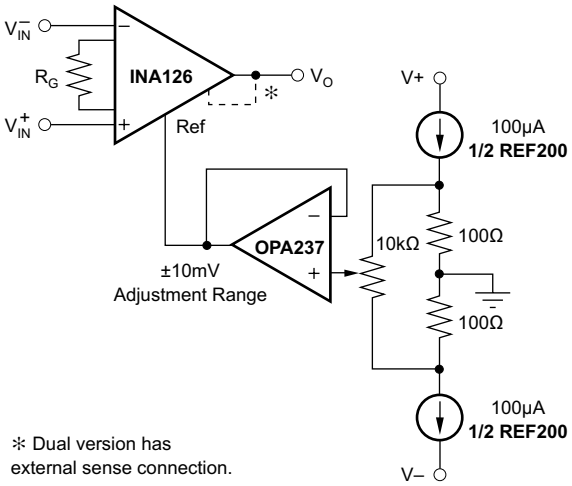

Figure 8-2. Optional Trimming of Output Offset Voltage

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8.2.2.3 Input Bias Current Return

The input impedance of the INAx126 is extremely high at approximately 10^9 Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is typically –10 nA (current flows out of the input pins). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 8-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 8-3). With higher source impedance, using two equal resistors provides a balanced input with the advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

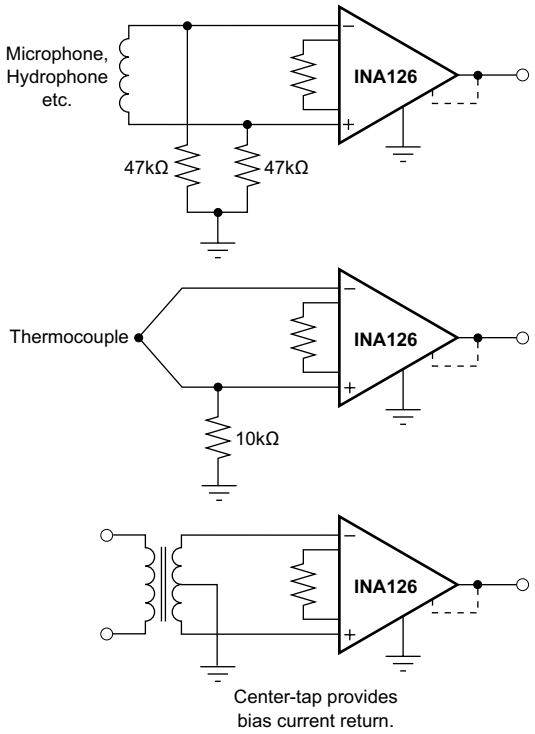

Figure 8-3. Providing an Input Common-Mode Current Path

8.2.2.4 Input Common-Mode Range

The input common-mode range of the INAx126 is shown in *Section 6.7*. The common-mode range is limited on the negative side by the output voltage swing of A_2, an internal circuit node that cannot be measured on an external pin. The output voltage of A_2 can be expressed as shown in Equation 2:

$$V_{O2} = 1.25\ V^-_{IN} - (V^+_{IN} - V^-_{IN})\ (10\ k\Omega/R_G) \quad (2)$$

where

- Voltages referred to Ref, pin 5

The internal op amp A_2 is identical to A_1, with an output swing typically limited to 0.7 V from the supply rails. When the input common-mode range is exceeded (A_2 output is saturated), A_1 can still be in linear operation and respond to changes in the noninverting input voltage. The output voltage, however, will be invalid.

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8.2.2.5 Input Protection

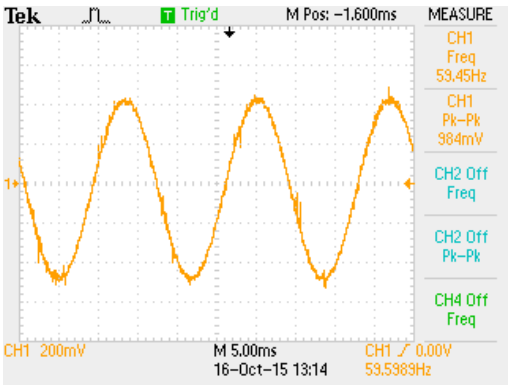
The inputs are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent the signal from exceeding the power supplies by more than approximately 0.7 V. If the signal-source voltage can exceed the power supplies, the source current should be limited to less than 10 mA. This limiting can generally be done with a series resistor. Some signal sources are inherently current-limited, and do not require limiting resistors.

8.2.2.6 Channel Crosstalk—Dual Version

The two channels of the INA2126 are completely independent, including all bias circuitry. At dc and low frequency, there is virtually no signal coupling between channels. Crosstalk increases with frequency and depends on circuit gain, source impedance, and signal characteristics.

As source impedance increases, careful circuit layout can help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Carefully balance the stray capacitance of each input to ground, and run the differential inputs of each channel parallel to each other, or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal that is rejected by the IA input.

8.2.3 Application Curves



Differential signal is too small to be seen

Figure 8-4. Common-mode Signal at INA126 Input

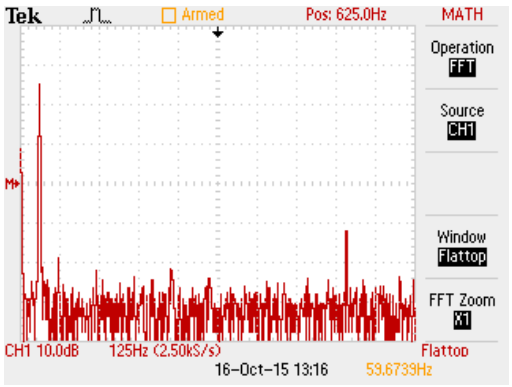


Figure 8-5. FFT of Signal in Previous Figure Shows Both the 60-Hz Common-mode Along With 5-kHz Differential Signal

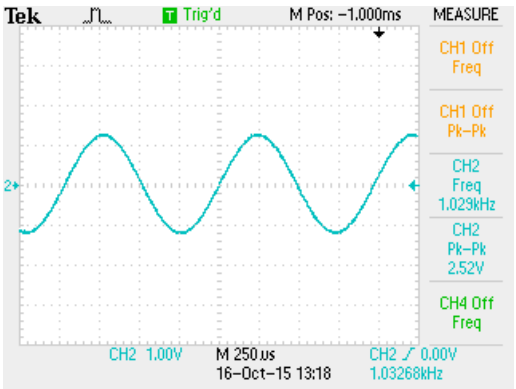


Figure 8-6. Recovered Differential Signal at the Output of the INA126 With a Gain of 250

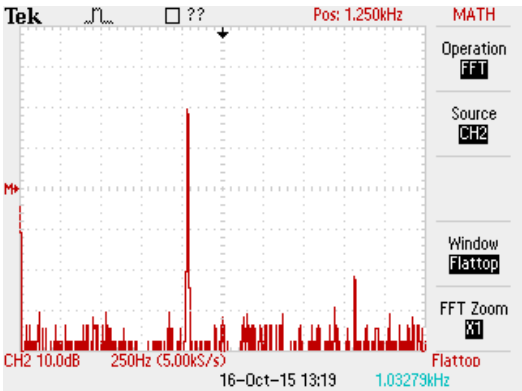


Figure 8-7. FFT of the INA126 Output Shows that the 60-Hz Common-mode Signal is Rejected

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9 Power Supply Recommendations

9.1 Low-Voltage Operation

The INAx126 can be operated on power supplies as low as ±1.35 V. Performance remains excellent with power supplies ranging from ±1.35 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range (see *Section 6.7*). Operation at low supply voltage requires careful attention to make sure that the common-mode voltage remains within the linear range (see Figure 6-5 and Figure 6-6).

The INAx126 operates from a single power supply with careful attention to input common-mode range, output voltage swing of both op amps, and the voltage applied to the Ref pin. Figure 9-1 shows a bridge amplifier circuit operated from a single 5-V power supply. The bridge provides an input common-mode voltage near 2.5 V, with a relatively small differential voltage.

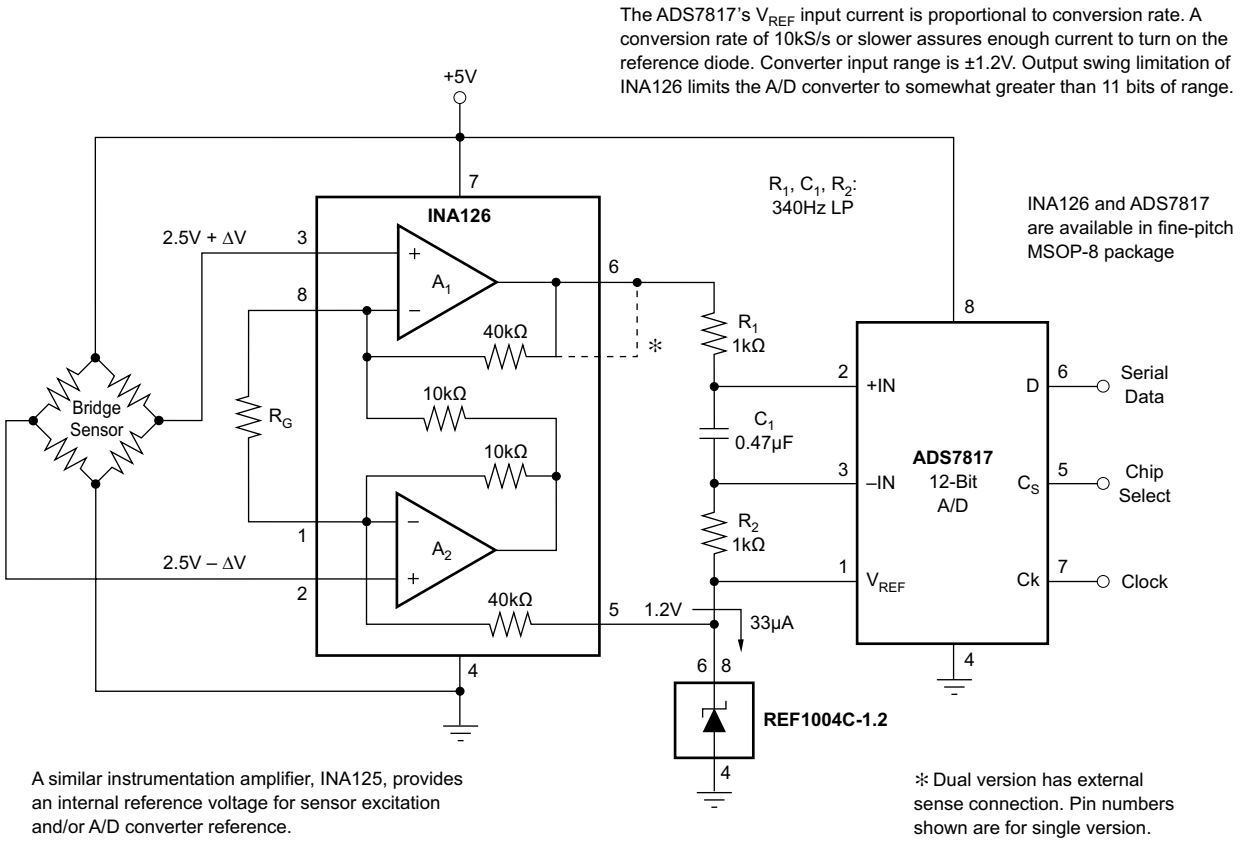

Figure 9-1. Bridge Signal Acquisition, Single 5-V Supply

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *PCB Design Guidelines For Reduced EMI*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 10-1, keep R_G close to the pins to minimize parasitic capacitance.
- Keep the traces as short as possible

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10.2 Layout Example

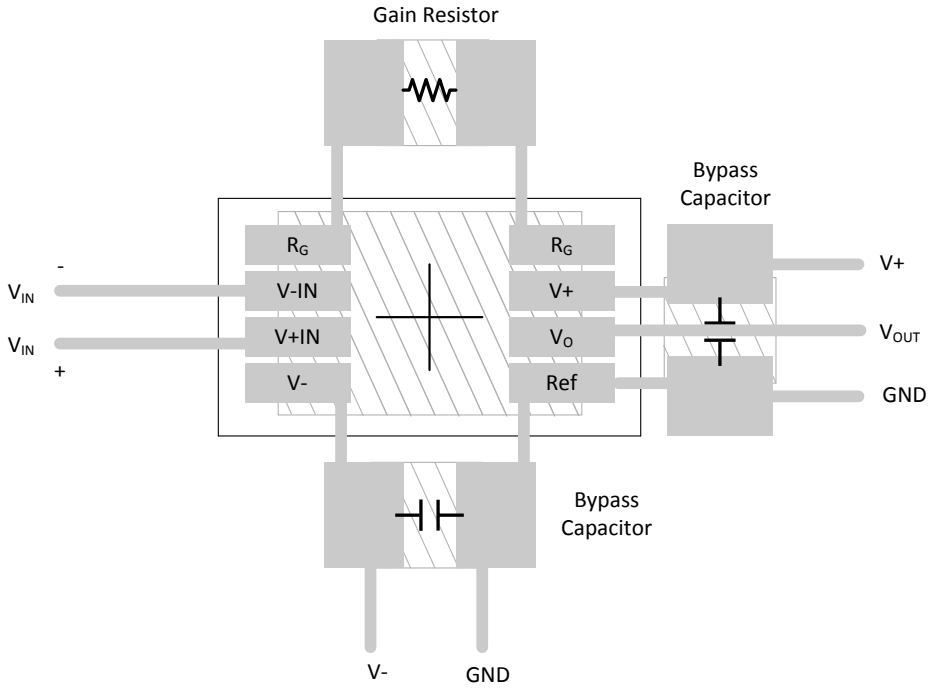

Figure 10-1. INA126 Layout Example

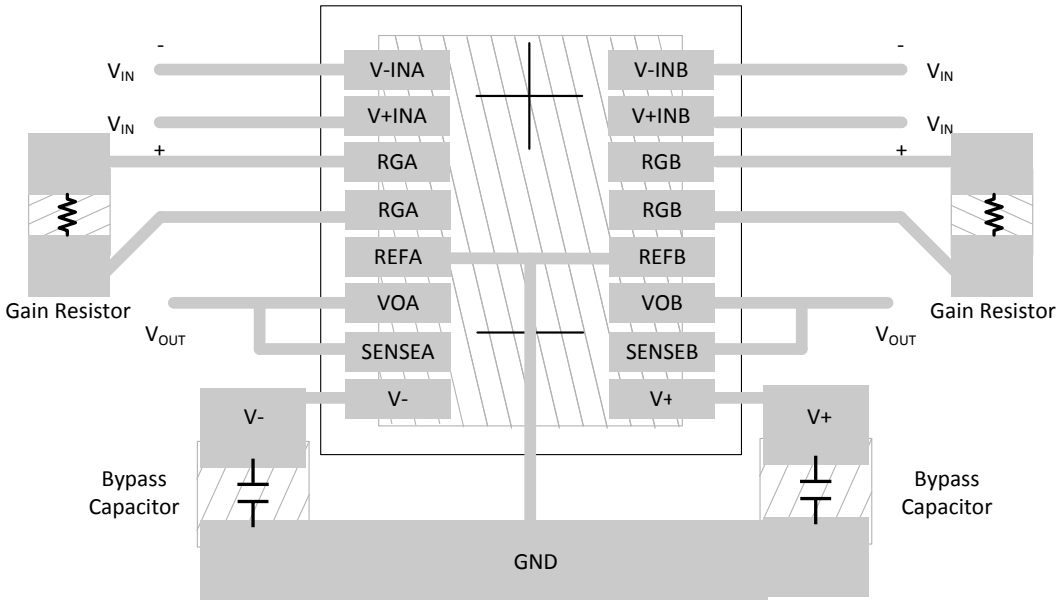

Figure 10-2. INA2126 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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PhotoMOS® is a registered trademark of Panasonic Corporation.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA126E/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A26	Samples
INA126E/250G4	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	A26	
INA126E/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR		A26	Samples
INA126EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR		A26	Samples
INA126EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR		A26	Samples
INA126EA/2K5G4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		A26	
INA126U	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		INA 126U	Samples
INA126U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		INA 126U	Samples
INA126UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		INA 126U A	Samples
INA126UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		INA 126U A	Samples
INA2126E/250	ACTIVE	SSOP	DBQ	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		INA 2126E	Samples
INA2126E/2K5	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 2126E	Samples
INA2126EA/250	ACTIVE	SSOP	DBQ	16	250	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126EA/2K5	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126U	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		INA2126U	Samples
INA2126UA	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	INA2126U A	Samples
INA2126UA/2K5	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2126U	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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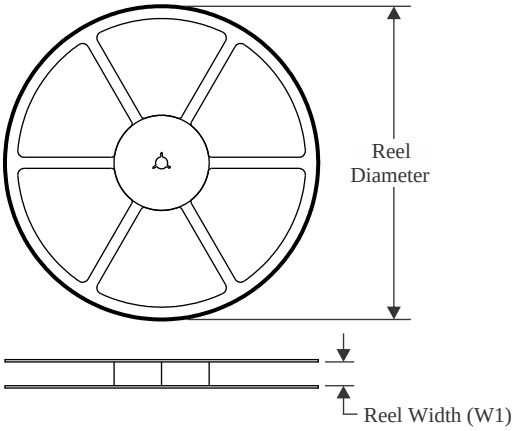
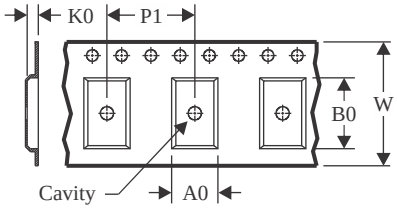
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

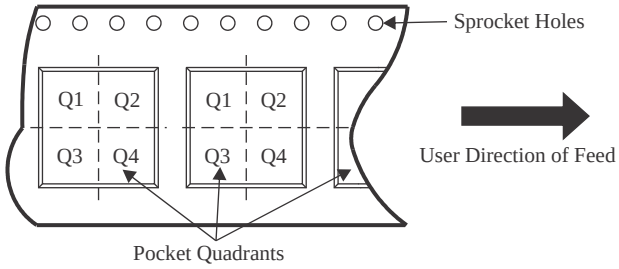


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

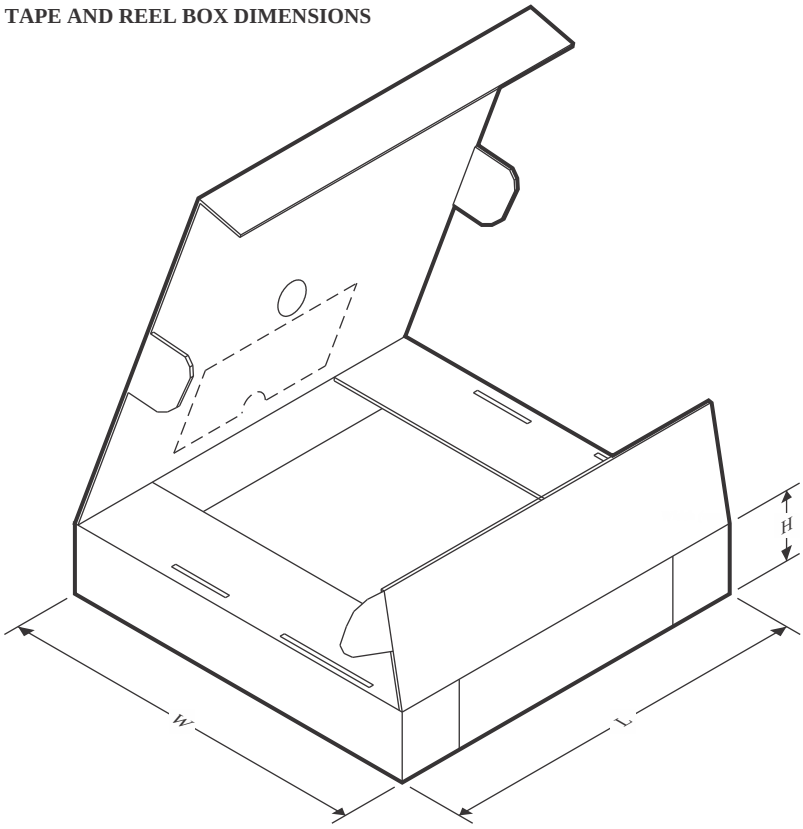


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA126E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA126UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2126E/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2126E/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2126E/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2126EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2126EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2126UA/2K5	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2126UA/2K5	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

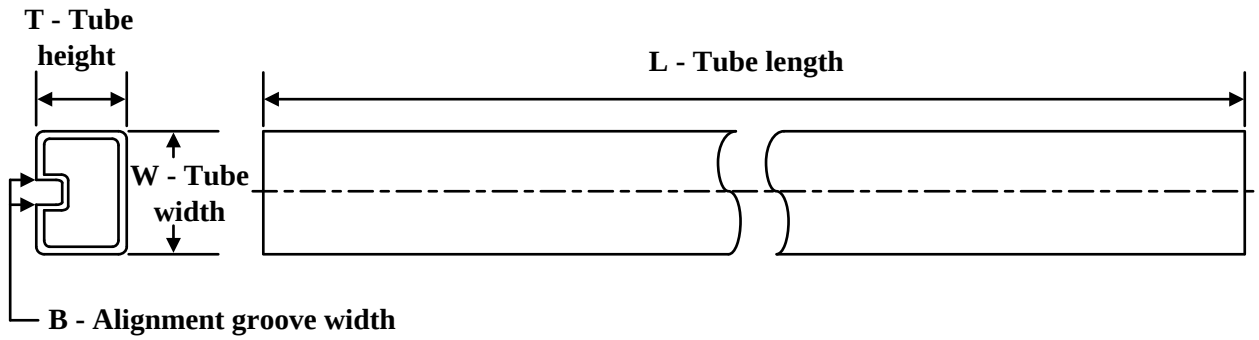
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

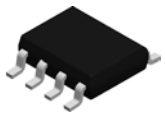
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA126E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA126E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA126E/2K5	VSSOP	DGK	8	2500	356.0	356.0	35.0
INA126E/2K5	VSSOP	DGK	8	2500	356.0	356.0	35.0
INA126EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA126EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA126EA/2K5	VSSOP	DGK	8	2500	356.0	356.0	35.0
INA126EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
INA126U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA126UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA2126E/250	SSOP	DBQ	16	250	210.0	185.0	35.0
INA2126E/2K5	SSOP	DBQ	16	2500	356.0	356.0	35.0
INA2126E/2K5	SSOP	DBQ	16	2500	356.0	356.0	35.0
INA2126EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
INA2126EA/2K5	SSOP	DBQ	16	2500	356.0	356.0	35.0
INA2126UA/2K5	SOIC	D	16	2500	356.0	356.0	35.0
INA2126UA/2K5	SOIC	D	16	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA126U	D	SOIC	8	75	506.6	8	3940	4.32
INA126UA	D	SOIC	8	75	506.6	8	3940	4.32
INA2126U	D	SOIC	16	40	506.6	8	3940	4.32
INA2126UA	D	SOIC	16	40	506.6	8	3940	4.32

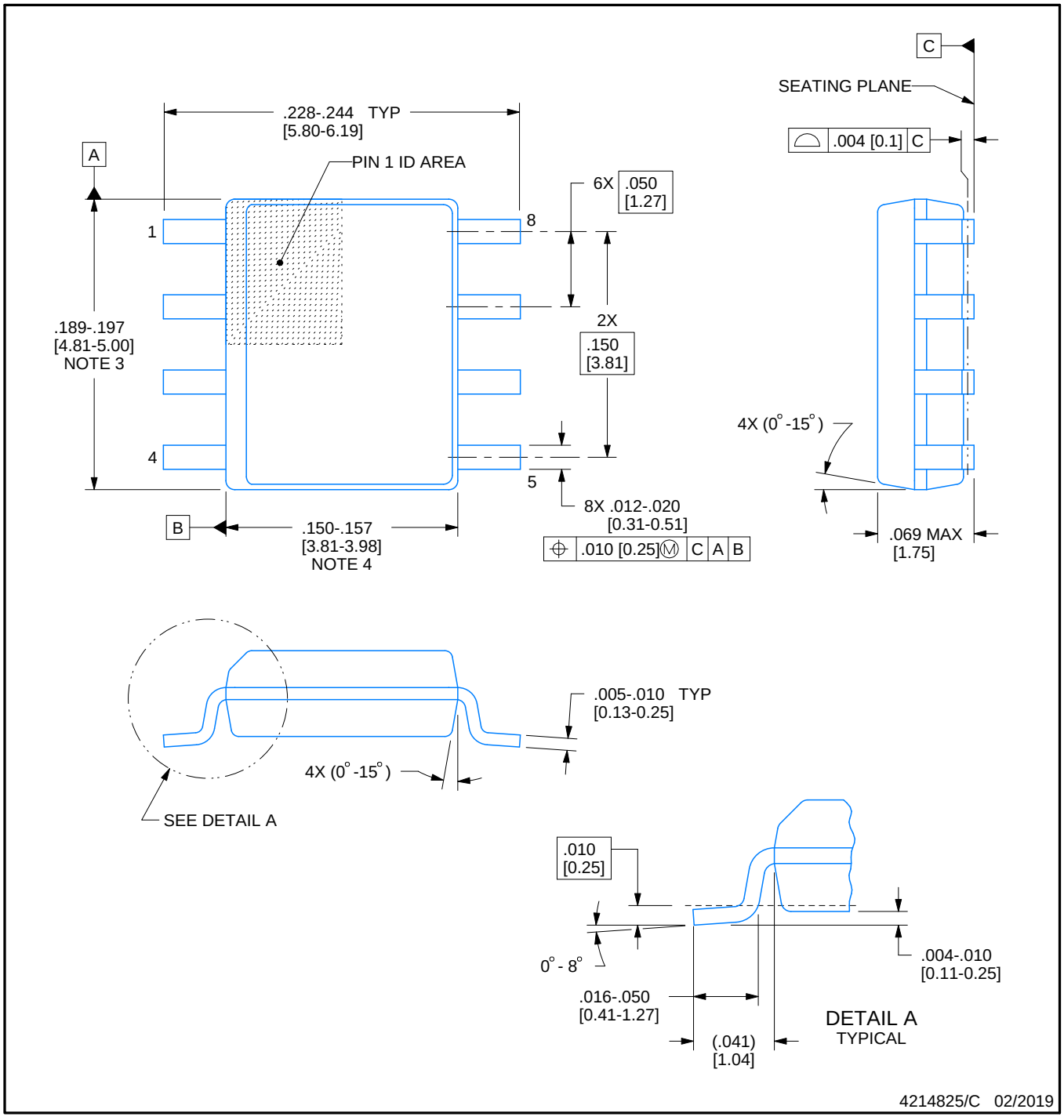


PACKAGE OUTLINE

D0008A

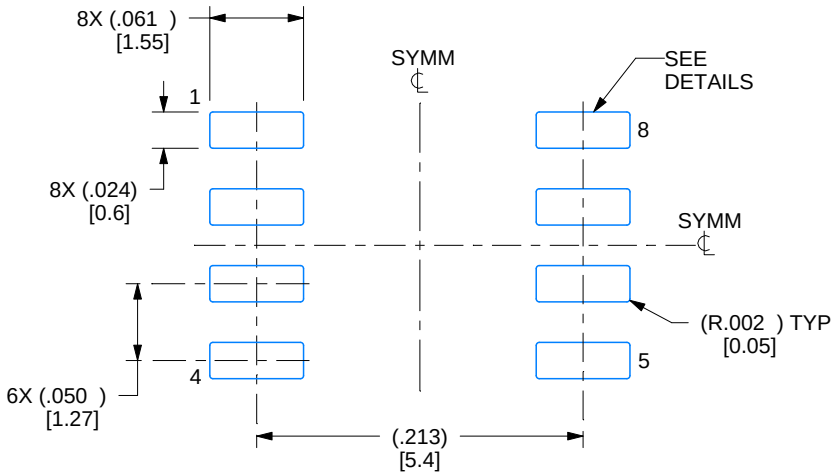
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

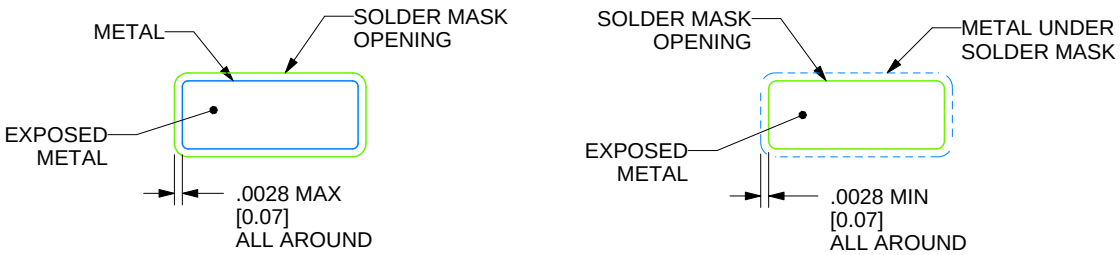


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

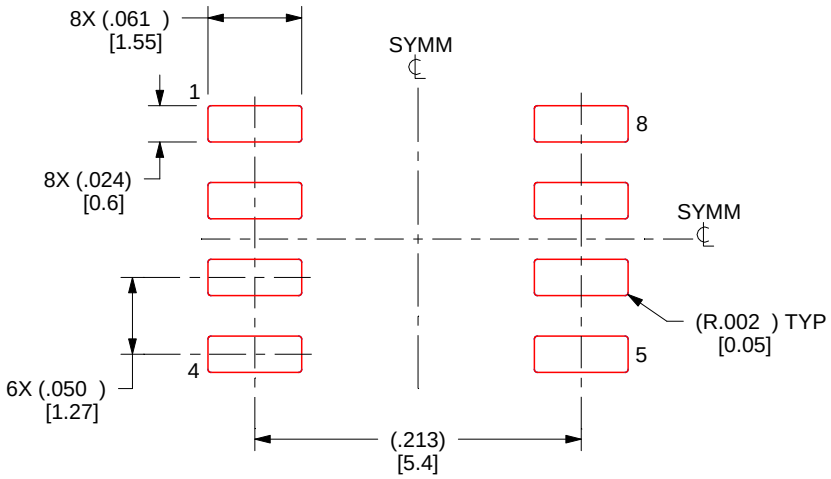
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

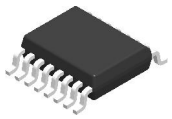


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

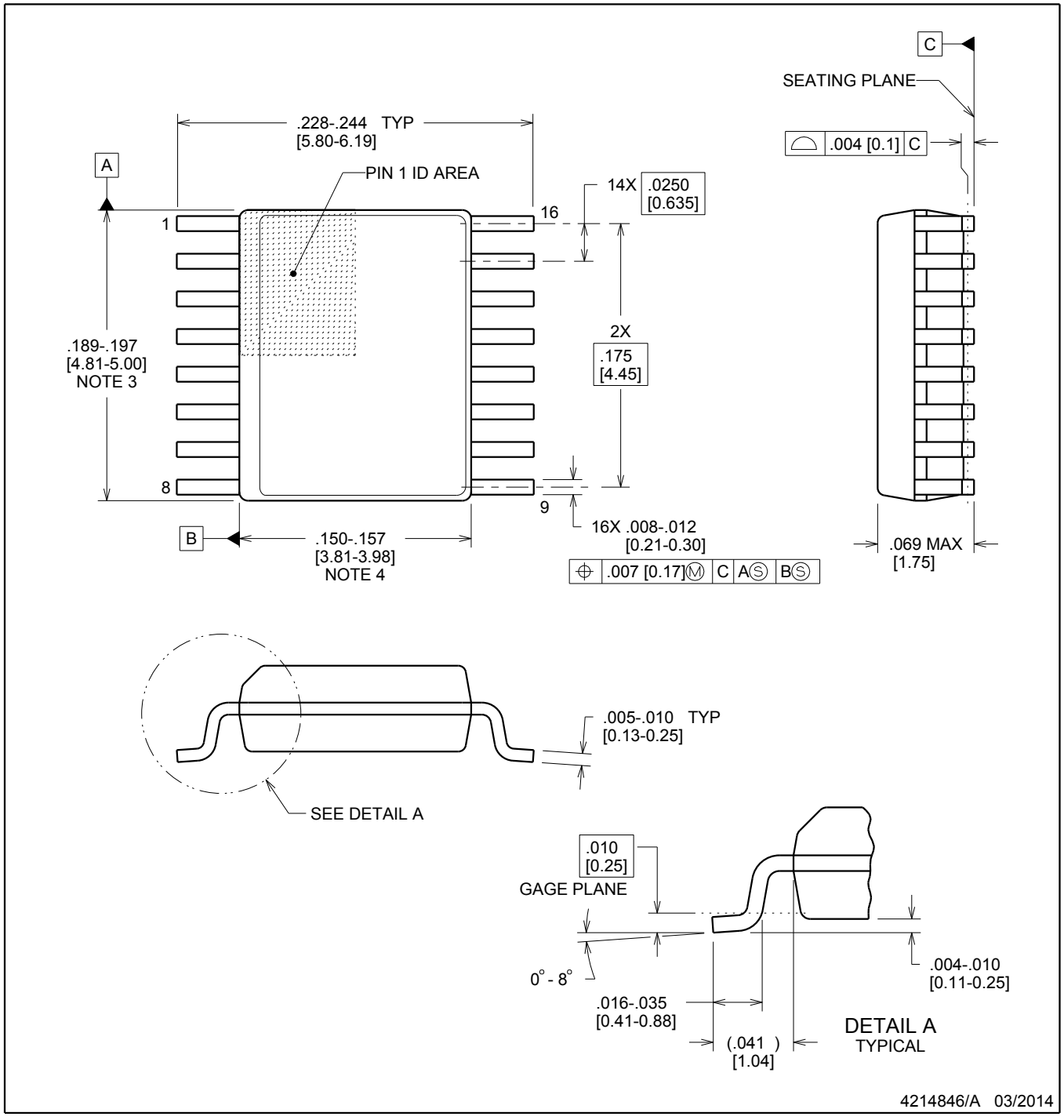


PACKAGE OUTLINE

DBQ0016A

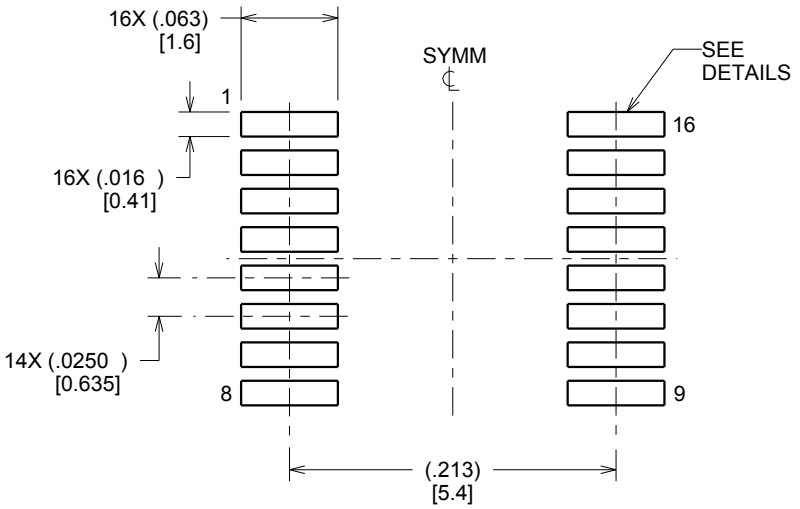
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

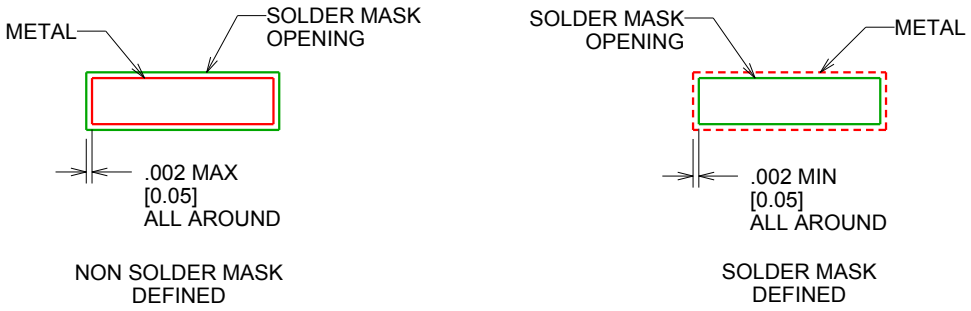


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

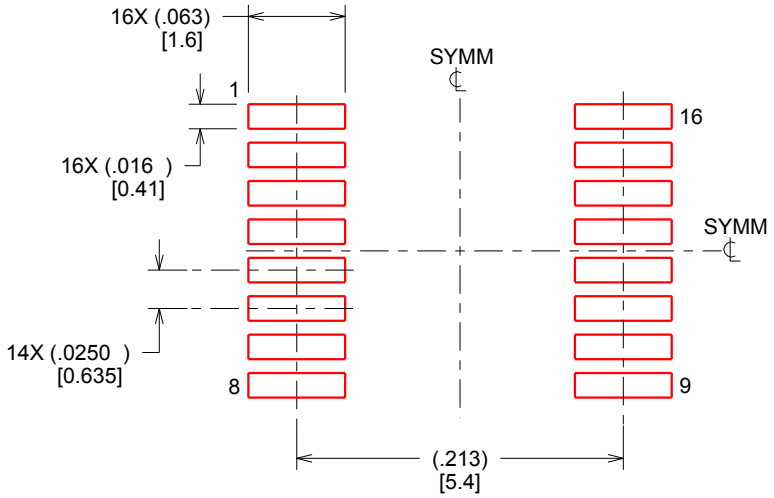
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

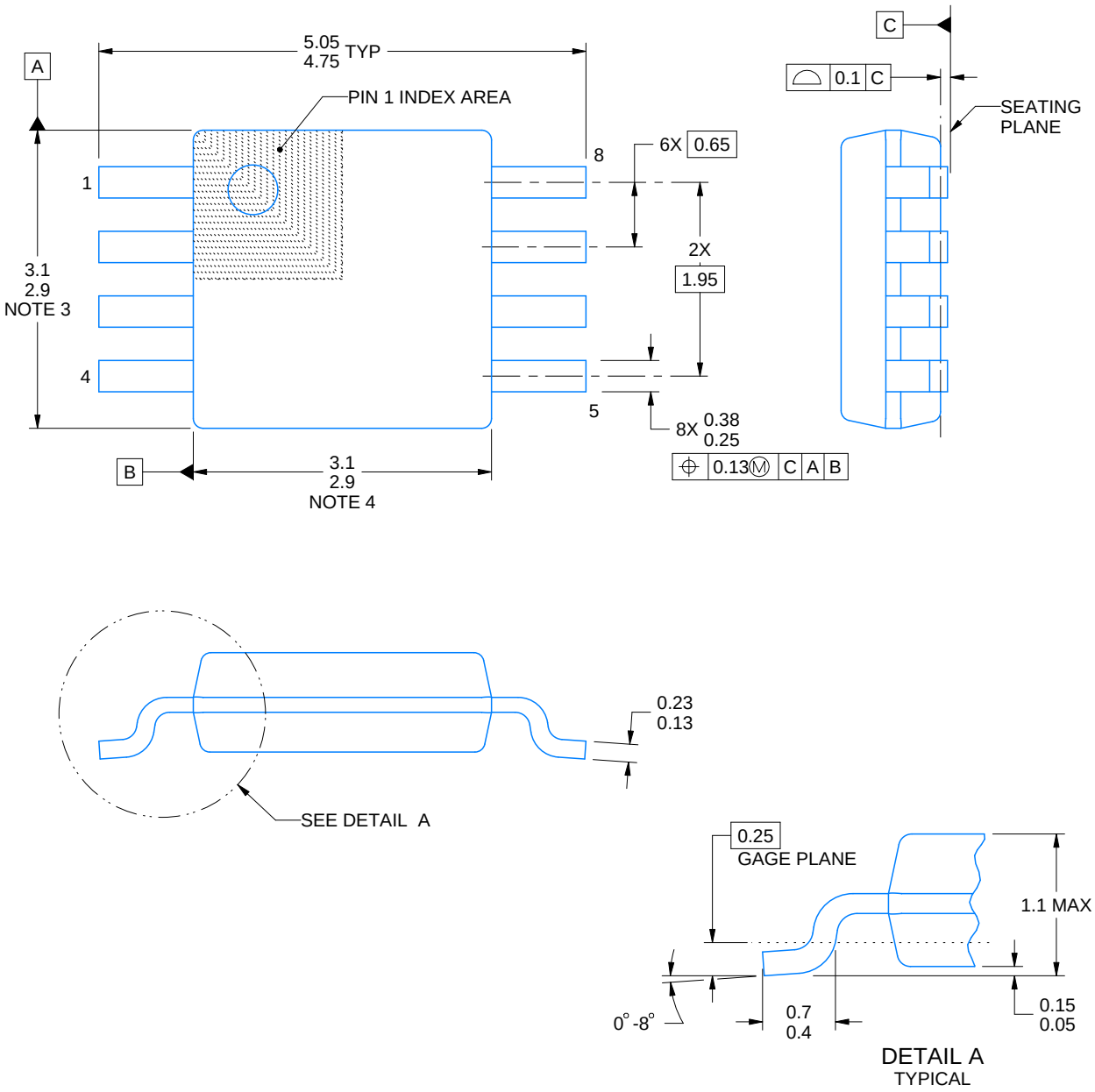
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

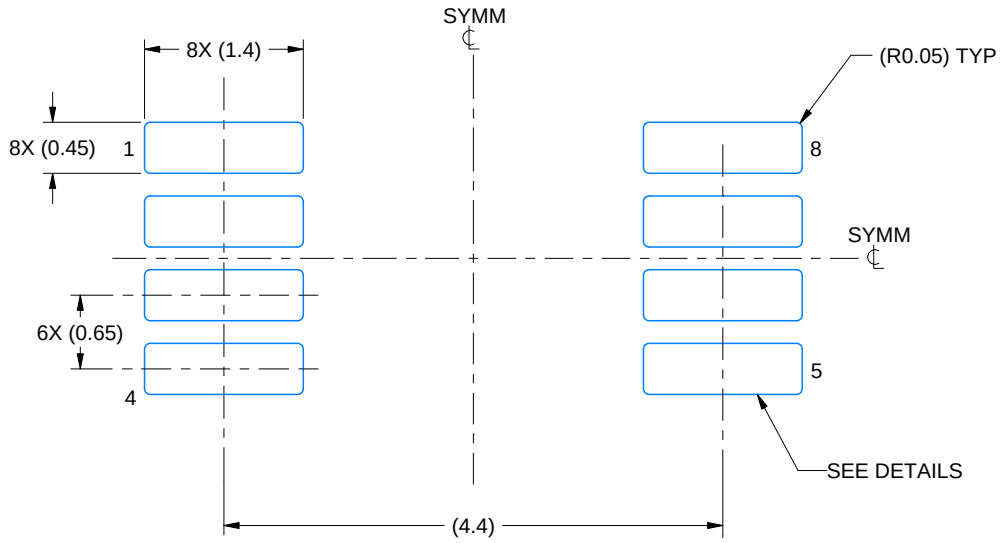
SMALL OUTLINE PACKAGE



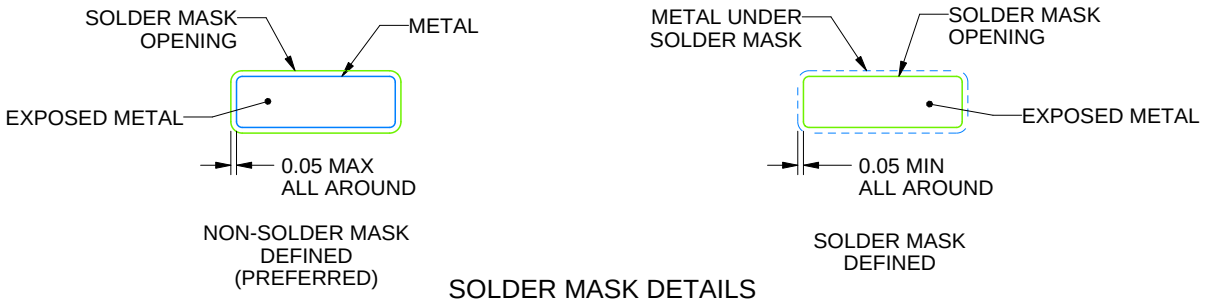
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

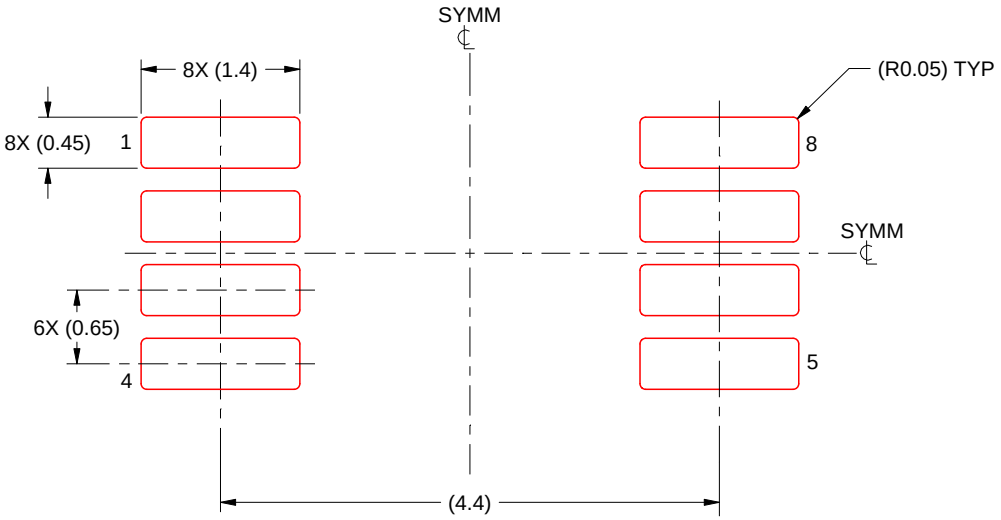


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



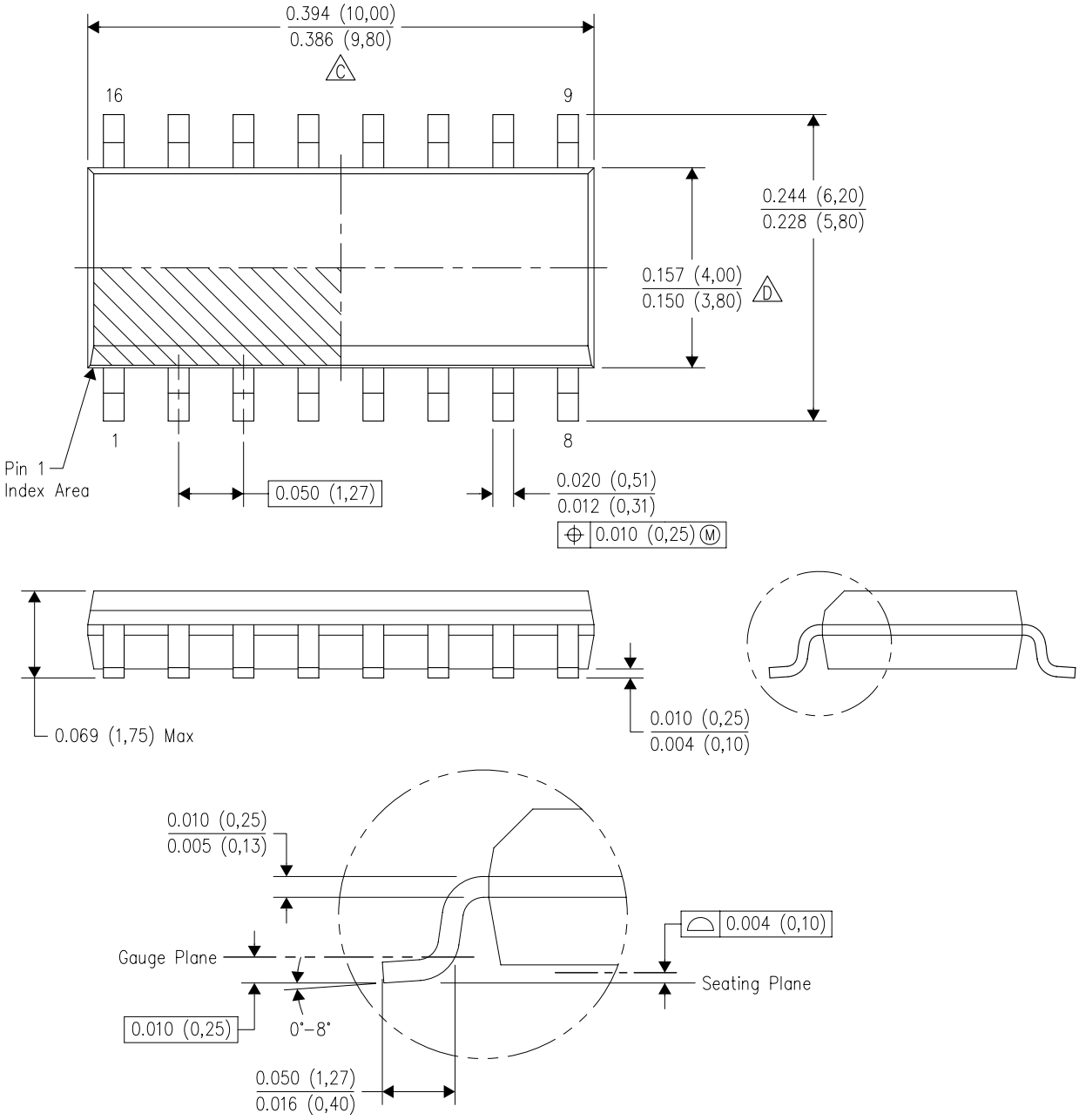
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

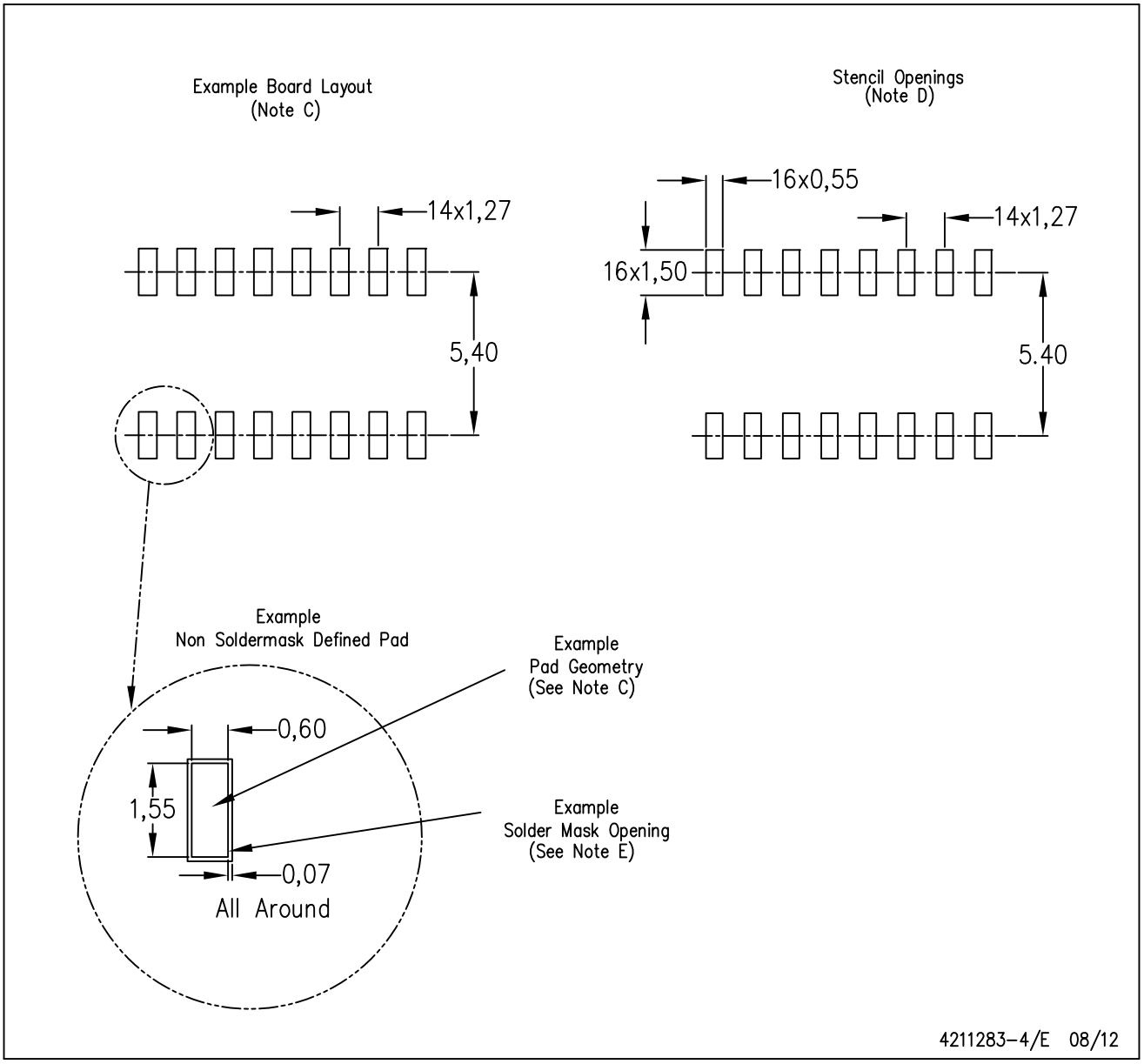
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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