THE DATASHEET OF

MAX5811PEUT+T

19-2270; Rev 1; 11/04

10-Bit, Low-Power, 2-Wire Interface, Serial, Voltage-Output DAC

General Description

The MAX5811 is a single, 10-bit voltage-output digital-to-analog converter (DAC) with an I²C™-compatible 2-wire interface that operates at clock rates up to 400kHz. The device operates from a single 2.7V to 5.5V supply and draws only 100µA at V_{DD} = 3.6V. A low-power power-down mode decreases current consumption to less than 1µA. The MAX5811 features three software-selectable power-down output impedances: 100kΩ, 1kΩ, and high impedance. Other features include an internal precision Rail-to-Rail® output buffer and a power-on reset (POR) circuit that powers up the DAC in the 100kΩ power-down mode.

The MAX5811 features a double-buffered I²C-compatible serial interface that allows multiple devices to share a single bus. All logic inputs are CMOS-logic compatible and buffered with Schmitt triggers, allowing direct interfacing to optocoupled and transformer-isolated interfaces. The MAX5811 minimizes digital noise feedthrough by disconnecting the clock (SCL) signal from the rest of the device when an address mismatch is detected.

The MAX5811 is specified over the extended temperature range of -40°C to +85°C and is available in a space-saving 6-pin SOT23 package. Refer to the MAX5812 data sheet for the 12-bit version.

Applications

Digital Gain and Offset Adjustments

Programmable Voltage and Current Sources

Programmable Attenuation

VCO/Varactor Diode Control

Low-Cost Instrumentation

Battery-Operated Equipment

Features

- **Ultra-Low Supply Current**
  100µA at V_{DD} = 3.6V
  130µA at V_{DD} = 5.5V
- **300nA Low-Power Power-Down Mode**
- **Single 2.7V to 5.5V Supply Voltage**
- **Fast 400kHz I²C-Compatible 2-Wire Serial Interface**
- **Schmitt-Trigger Inputs for Direct Interfacing to Optocouplers**
- **Rail-to-Rail Output Buffer Amplifier**
- **Three Software-Selectable Power-Down Output Impedances**
  100kΩ, 1kΩ, and High Impedance
- **Read-Back Mode for Bus and Data Checking**
- **Power-On Reset to Zero**
- **Miniature 6-Pin SOT23 Package**

Ordering Information

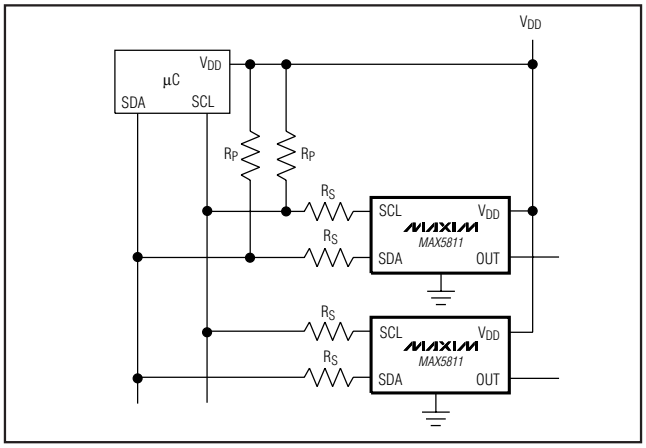
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX5811LEUT-T	-40°C to +85°C	6 SOT23-6	AAYS
MAX5811MEUT-T	-40°C to +85°C	6 SOT23-6	AAYU
MAX5811NEUT-T	-40°C to +85°C	6 SOT23-6	AAYW
MAX5811PEUT-T	-40°C to +85°C	6 SOT23-6	AAYY

Functional Diagram appears at end of data sheet.

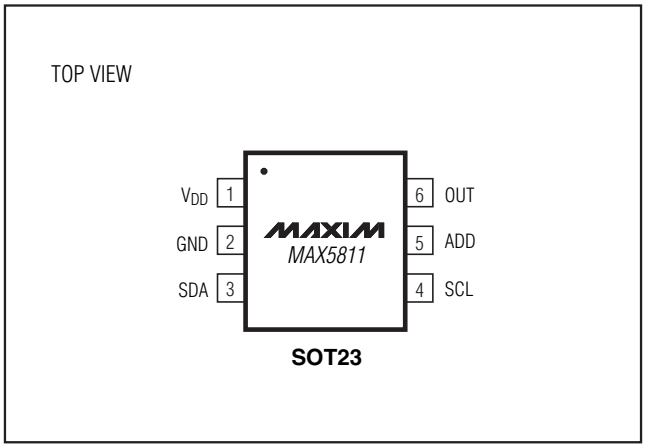
Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

I²C is a trademark of Philips Corp.

Typical Operating Circuit



Pin Configuration



10-Bit Low Power 2-Wire Interface Serial, Voltage-Output DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SCL, SDA to GND .....-0.3V to +6V
OUT, ADD to GND .....-0.3V to V_{DD} + 0.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 9.1mW above +70°C).....727mW

Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 2)						
Resolution	N		10			Bits
Integral Nonlinearity	INL	(Note 3)		±0.5	±4	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)			±0.5	LSB
Zero-Code Error	ZCE	Code = 000 hex, V_{DD} = 2.7V		±6	±40	mV
Zero-Code Error Tempco				2.3		ppm/°C
Gain Error	GE	Code = 3FF hex		-0.8	-3	%FS
Gain-Error Tempco				0.26		ppm/°C
DAC OUTPUT						
Output Voltage Range		No load (Note 4)	0		V_{DD}	V
DC Output Impedance		Code = 200 hex		1.2		Ω
Short-Circuit Current		V_{DD} = 5V, V_{OUT} = full scale (short to GND)		42.2		mA
		V_{DD} = 3V, V_{OUT} = full scale (short to GND)		15.1		
Wake-Up Time		V_{DD} = 5V		8		µs
		V_{DD} = 3V		8		
DAC Output Leakage Current		Power-down mode = high impedance, V_{DD} = 5.5V, V_{OUT} = V_{DD} or GND		±0.1	±1	µA
DIGITAL INPUTS (SCL, SDA)						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Hysteresis			0.05 x V_{DD}			V
Input Leakage Current		Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Input Capacitance				6		pF
DIGITAL OUTPUT (SDA)						
Output Logic Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
Three-State Leakage Current	I_L	Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Three-State Output Capacitance				6		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, GND = 0, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.5		V/µs
Voltage-Output Settling Time		To 1/2LSB code 100 hex to 300 hex or 300 hex to 100 hex (Note 5)		4	12	µs
Digital Feedthrough		Code = 000 hex, digital inputs from 0 to V_{DD}		0.2		nV-s
Digital-to-Analog Glitch Impulse		Major-carry transition (code = 1FF hex to 200 hex and 200 hex to 1FF hex)		12		nV-s
POWER SUPPLIES						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No Load		All digital inputs at 0 or V_{DD} = 3.6V		100	170	
		All digital inputs at 0 or V_{DD} = 5.5V		130	190	
Power-Down Supply Current		All digital inputs at 0 or V_{DD} = 5.5V		0.3	1	µA
TIMING CHARACTERISTICS (Figure 1)						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus-Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD,STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Repeated START Setup Time	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_r	(Note 5)	0		300	ns
SDA and SCL Receiving Fall Time	t_f	(Note 5)	0		300	ns
SDA Transmitting Fall Time	t_f	(Note 5)	$20 + 0.1C_b$		250	ns
STOP Condition Setup Time	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_b	(Note 5)			400	pF
Maximum Duration of Suppressed Pulse Widths	t_{SP}		0		50	ns

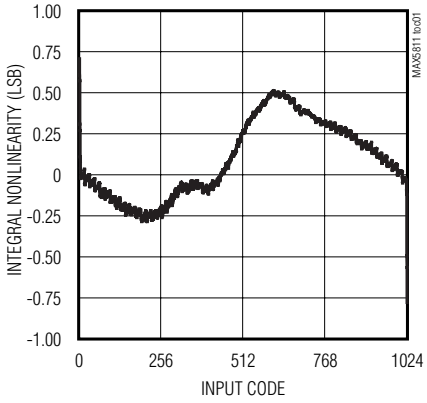
Note 1: All devices are 100% production tested at T_A = +25°C and are guaranteed by design for T_A = T_{MIN} to T_{MAX}.
Note 2: Static specifications are tested with the output unloaded.
Note 3: Linearity is guaranteed from codes 29 to 995.
Note 4: Offset and gain error limit the FSR.
Note 5: Guaranteed by design. Not production tested.

10-Bit Low Power 2-Wire Interface Serial, Voltage-Output DAC

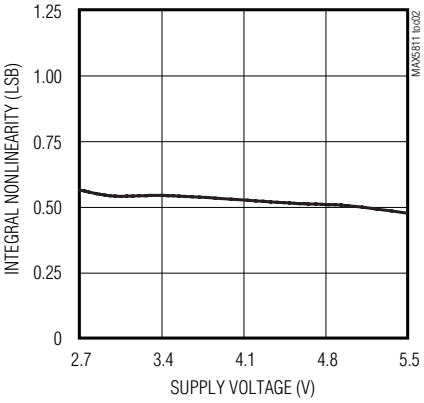
Typical Operating Characteristics

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

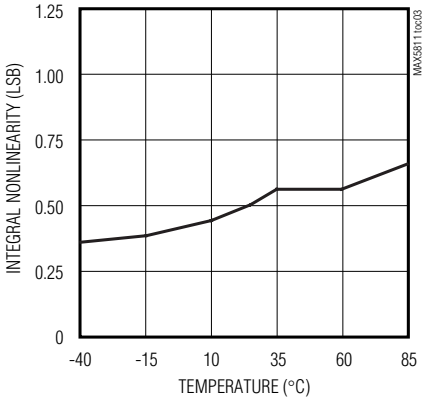
INTEGRAL NONLINEARITY vs. INPUT CODE



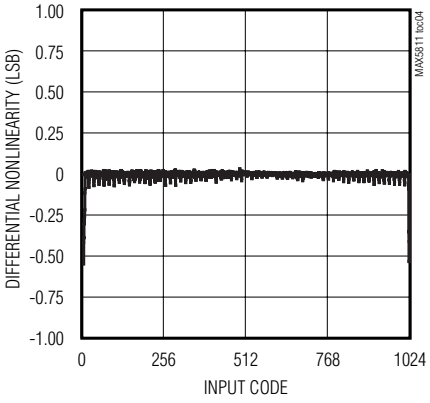
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



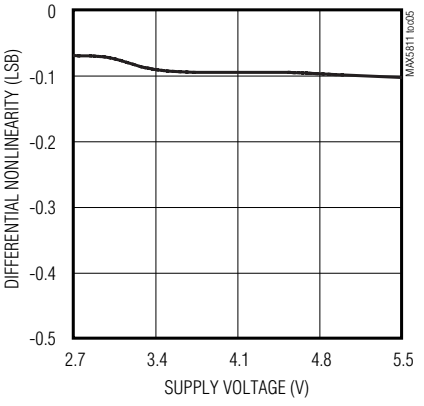
INTEGRAL NONLINEARITY vs. TEMPERATURE



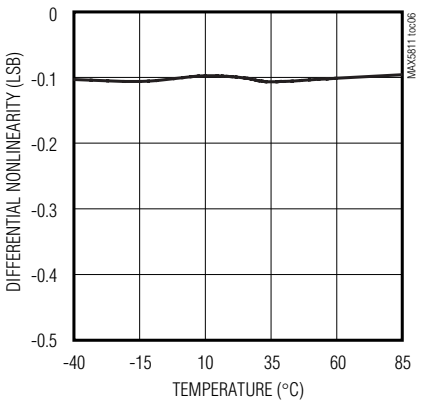
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



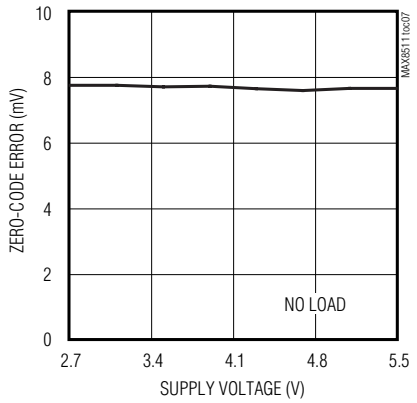
DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



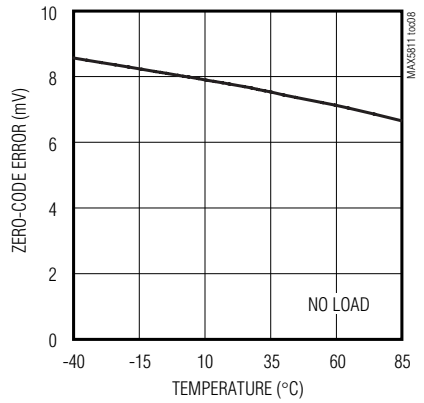
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



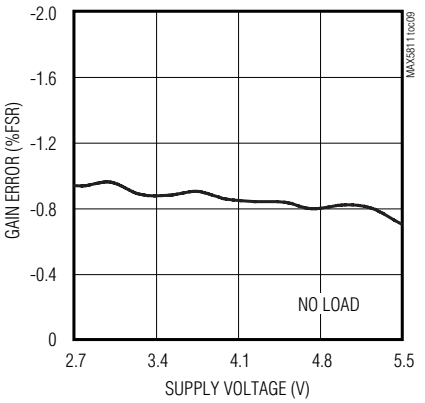
ZERO-CODE ERROR vs. SUPPLY VOLTAGE



ZERO-CODE ERROR vs. TEMPERATURE



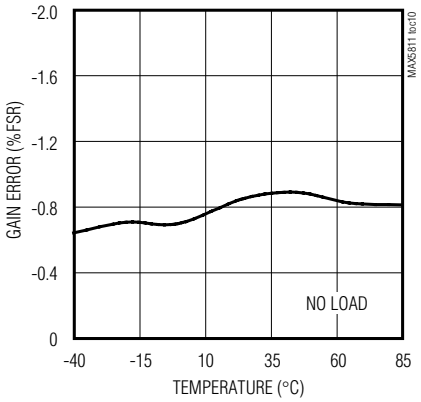
GAIN ERROR vs. SUPPLY VOLTAGE



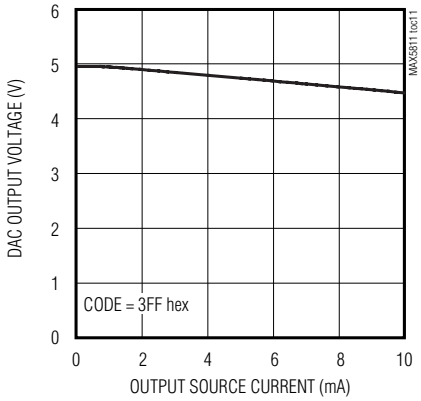
Typical Operating Characteristics (continued)

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

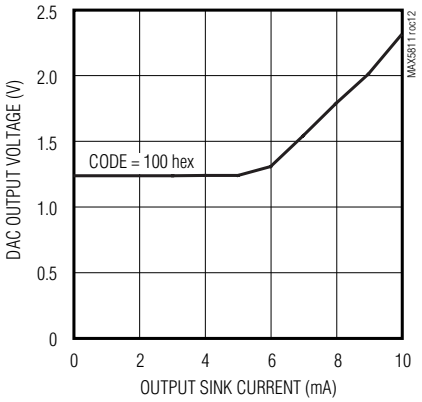
GAIN ERROR vs. TEMPERATURE



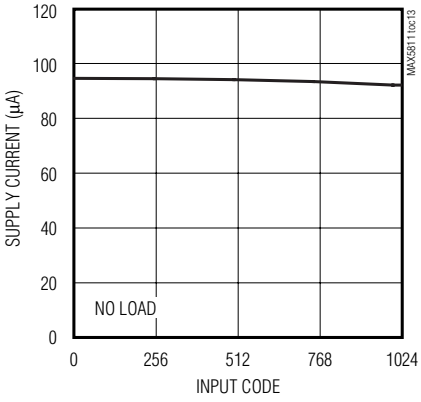
DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (NOTE 6)



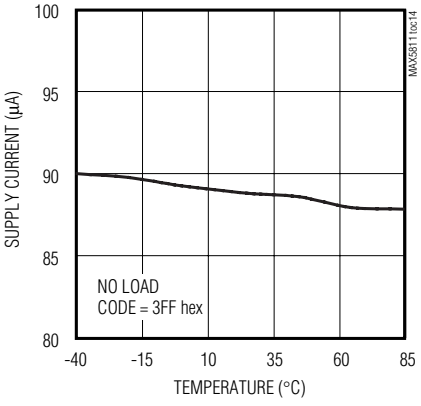
DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT (NOTE 6)



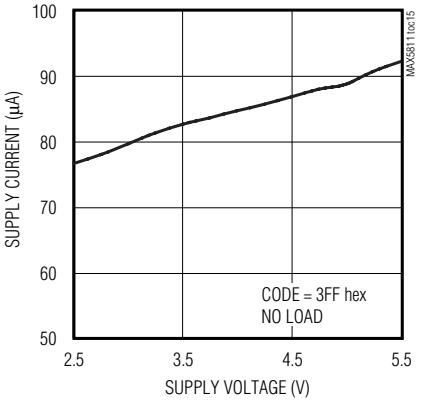
SUPPLY CURRENT vs. INPUT CODE



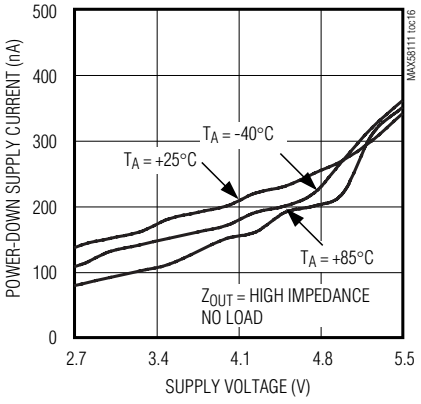
SUPPLY CURRENT vs. TEMPERATURE



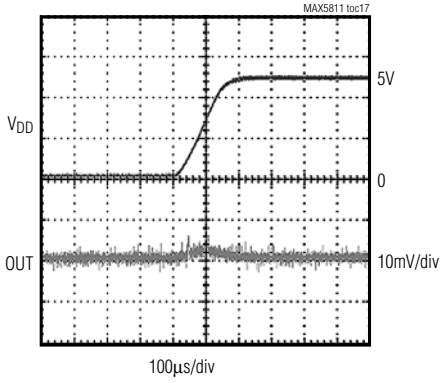
SUPPLY CURRENT vs. SUPPLY VOLTAGE



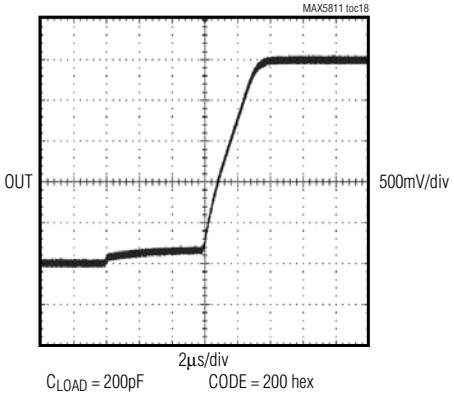
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



POWER-UP GLITCH



EXITING SHUTDOWN

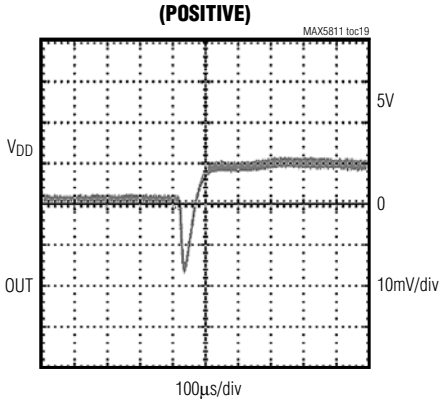


10-Bit Low Power 2-Wire Interface Serial, Voltage-Output DAC

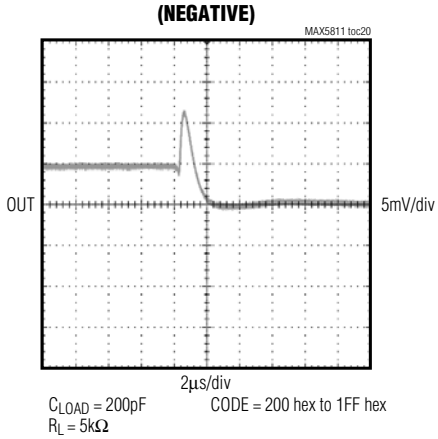
Typical Operating Characteristics (continued)

(V_{DD} = +5V, R_L = 5kΩ, T_A = +25°C.)

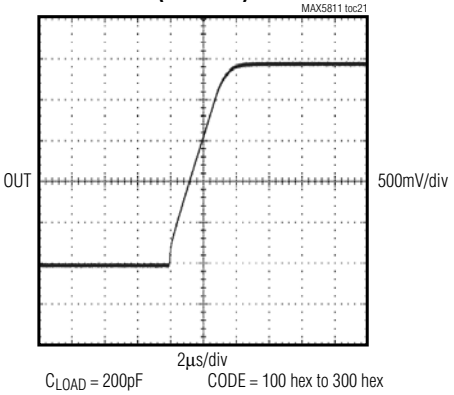
MAJOR-CARRY TRANSITION (POSITIVE)



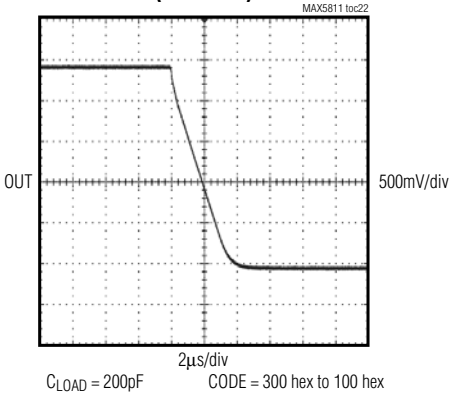
MAJOR-CARRY TRANSITION (NEGATIVE)



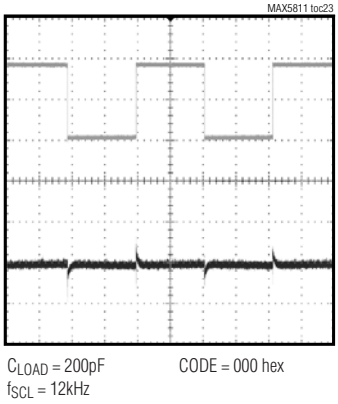
SETTLING TIME (POSITIVE)



SETTLING TIME (NEGATIVE)



DIGITAL FEEDTHROUGH



Note 6: The ability to drive loads less than 5kΩ is not implied.

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power Supply and DAC Reference Input
2	GND	Ground
3	SDA	Bidirectional Serial Data I/O
4	SCL	Serial Clock Line
5	ADD	Address Select. A logic high sets the address LSB to 1, a logic low sets the address LSB to 0.
6	OUT	Analog Output

Detailed Description

The MAX5811 is a 10-bit, voltage-output DAC with an I²C/SMBus-compatible 2-wire interface. The device consists of a serial interface, power-down circuitry, input and DAC registers, a 10-bit resistor string DAC, unity-gain output buffer, and output resistor network. The serial interface decodes the address and control bits, routing the data to either the input or DAC register. Data can be directly written to the DAC register immediately updating the device output, or can be written to the input register without changing the DAC output. Both registers retain data as long as the device is powered.

DAC Operation

The MAX5811 uses a segmented resistor string DAC architecture, which saves power in the overall system and guarantees output monotonicity. The MAX5811's input coding is straight binary, with the output voltage given by the following equation:

$$V_{OUT} = \frac{V_{REF} \times (D)}{2^N}$$

where N = 10 (bits), and D = the decimal value of the input code (0 to 1023).

Output Buffer

The MAX5811 analog output is buffered by a precision, unity-gain follower that slews at about 0.5V/µs. The buffer output swings rail-to-rail, and is capable of driving 5kΩ in parallel with 200pF. The output settles to ±0.5LSB within 4µs.

Power-On Reset

The MAX5811 features an internal POR circuit that initializes the device upon power-up. The DAC registers are set to zero scale and the device is powered-down with the output buffer disabled and the output pulled to GND through the 100kΩ termination resistor. Following power-up, a wake-up command must be initiated before any conversions are performed.

Power-Down Modes

The MAX5811 has three software-controlled low-power power-down modes. All three modes disable the output buffer and disconnect the DAC resistor string from V_{DD}, reducing supply current draw to 300nA. In power-down mode 0, the device output is high impedance. In power-down mode 1, the device output is internally pulled to GND by a 1kΩ termination resistor. In power-down mode 2, the device output is internally pulled to GND by a 100kΩ termination resistor. Table 1 shows the power-down mode command words.

Upon wake-up, the DAC output is restored to its previous value. Data is retained in the input and DAC registers during power-down mode.

Digital Interface

The MAX5811 features an I²C/SMBus-compatible 2-wire interface consisting of a serial data line (SDA) and

Table 1. Power-Down Command Bits

POWER-DOWN COMMAND BITS		MODE/FUNCTION
PD1	PD0	
0	0	Power-up device. DAC output restored to previous value.
0	1	Power-down mode 0. Power-down device with output floating.
1	0	Power-down mode 1. Power-down device with output terminated with 1kΩ to GND.
1	1	Power-down mode 2. Power-down device with output terminated with 100kΩ to GND.

10-Bit Low Power 2-Wire Interface Serial, Voltage-Output DAC

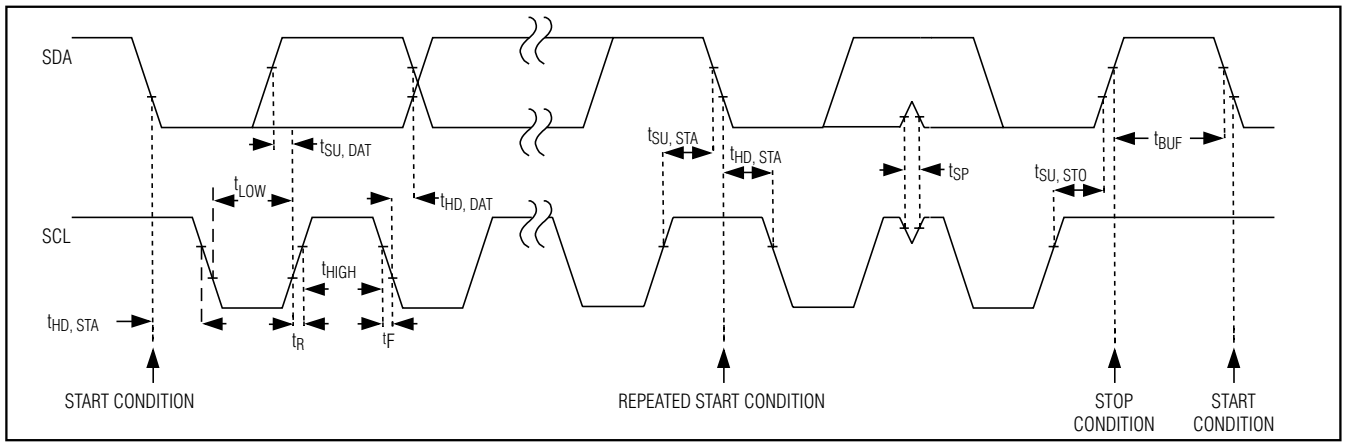


Figure 1. 2-Wire Serial Interface Timing Diagram

a serial clock line (SCL). The MAX5811 is SMBus compatible within the range of V_{DD} = 2.7V to 3.6V. SDA and SCL facilitate bidirectional communication between the MAX5811 and the master at rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX5811 is a transmit/receive slave-only device, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX5811 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (S_r) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX5811 SDA and SCL drivers are open-drain outputs, requiring a pullup resistor (500Ω or greater) to generate a logic high voltage (see *Typical Operating Circuit*). Series resistors R_S are optional. These series resistors protect the input stages of the MAX5811 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see *START and STOP Conditions*). SDA and SCL idle high when the I²C bus is not busy.

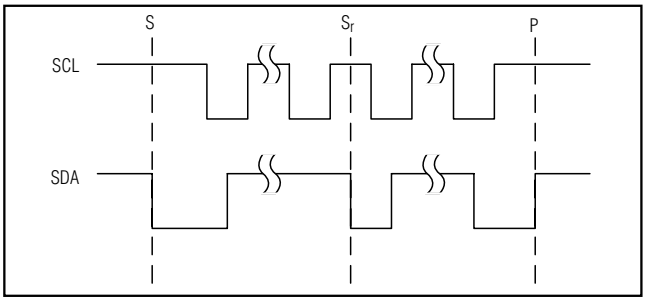


Figure 2. START/STOP Conditions

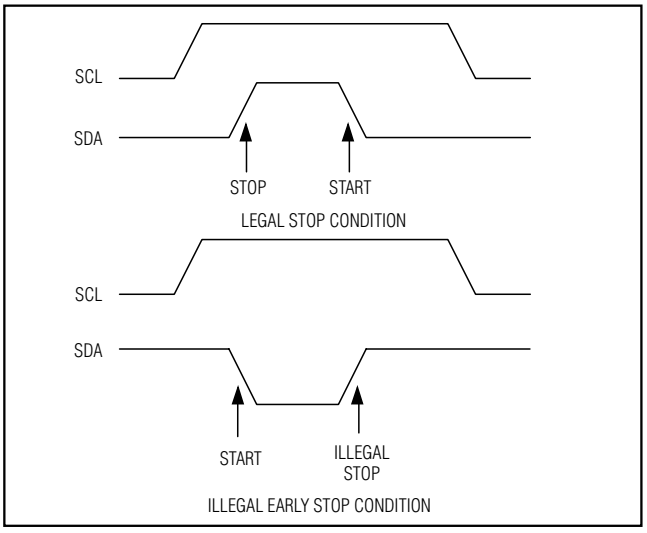


Figure 3. Early STOP Condition

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-

low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX5811. The master terminates transmission by issuing a not acknowledge followed by a STOP condition (*see Acknowledge Bit*). The STOP condition frees the bus. If a repeated START condition (Sr) is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect address is detected, the MAX5811 internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

Early STOP Conditions

The MAX5811 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 3). This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP conditions.

Repeated START Conditions

A REPEATED START (S_r) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation. S_r may also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX5811 serial interface supports continuous write operations with or without an S_r condition separating them. Continuous read operations require S_r conditions because of the change in direction of data flow.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. ACK is always generated by the receiving device. The MAX5811 generates an ACK when receiving an address or data by pulling SDA low during the ninth clock period. When transmitting data, the MAX5811 waits for the receiving device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address (Figure 4). When idle, the MAX5811 waits for a START condition followed by its slave address. The serial interface compares each address value bit by bit, allowing the interface to power down immediately if an incorrect address is detected. The LSB of the address word is the Read/$\overline{\text{Write}}$ (R/$\overline{W}$) bit. R/$\overline{W}$ indicates whether the master is writing to or reading from the MAX5811 (R/$\overline{W}$ = 0 selects the write condition, R/$\overline{W}$ = 1 selects the read condition). After receiving the proper address, the MAX5811 issues an ACK by pulling SDA low for one clock cycle.

Table 2. MAX5811 I²C Slave Addresses

PART	V_{ADD}	DEVICE ADDRESS (A_6...A_0)
MAX5811L	GND	0010 000
MAX5811L	V_{DD}	0010 001
MAX5811M	GND	0010 010
MAX5811M	V_{DD}	0010 011
MAX5811N	GND	0110 100
MAX5811N	V_{DD}	0110 101
MAX5811P	GND	1010 100
MAX5811P	V_{DD}	1010 101

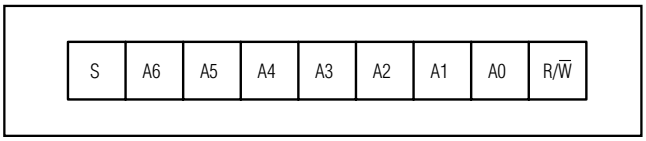


Figure 4. Slave Address Byte Definition

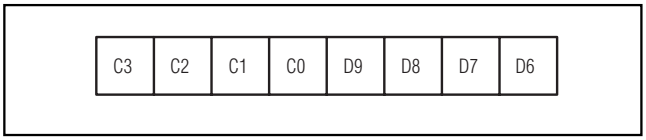


Figure 5. Command Byte Definition

The MAX5811 has eight different factory/user-programmed addresses (Table 2). Address bits A6 through A1 are preset, while A0 is controlled by ADD. Connecting ADD to GND sets A0 = 0. Connecting ADD to V_{DD} sets A0 = 1. This feature allows up to eight MAX5811s to share the same bus.

Write Data Format

In write mode (R/$\overline{W}$ = 0), data that follows the address byte controls the MAX5811 (Figure 5). Bits C3–C0 configure the MAX5811 (Table 3). Bits D9–D0 are DAC data. Bits S1 and S0 are sub-bits and are always zero. Input and DAC registers update on the falling edge of SCL during the acknowledge bit. Should the write cycle be prematurely aborted, data is not updated and the

10-Bit Low Power 2-Wire Interface Serial, Voltage-Output DAC

Table 3. Command Byte Definitions

SERIAL DATA INPUT							FUNCTION
C3	C2	C1	C0	D9/PD1*	D8/PD0*	D7-D6	
1	1	0	0	DAC DATA	DAC DATA	DAC DATA	Load DAC with new data from the following data byte and update DAC output simultaneously as soon as data is available from the serial bus. The DAC and input registers are updated with the new data.
1	1	0	1	DAC DATA	DAC DATA	DAC DATA	Load input register with data from the following data byte. DAC output remains unchanged.
1	1	1	0	DAC DATA	DAC DATA	DAC DATA	Load input register with data from the following data byte. Update DAC output to the previously stored data.
1	1	1	1	X	X	XX	Update DAC output from input register. The device ignores any new data.
1	0	X	X	X	X	XX	Read data request. Data bits are ignored. The contents of the DAC register are available on the bus.
0	1	X	X	0	0	XX	Power up the device.
0	1	X	X	0	1	XX	Power-down mode 0. Power down device with output floating.
0	1	X	X	1	0	XX	Power-down mode 1. Power down device with output terminated with 1kΩ to GND.
0	1	X	X	1	1	XX	Power-down mode 2. Power down device with output terminated with 100kΩ to GND.

**When C3 = 0 and C2 = 1, data bits D9 and D8 write to the power-down registers (PD1 and PD0).*
X = Don't care.

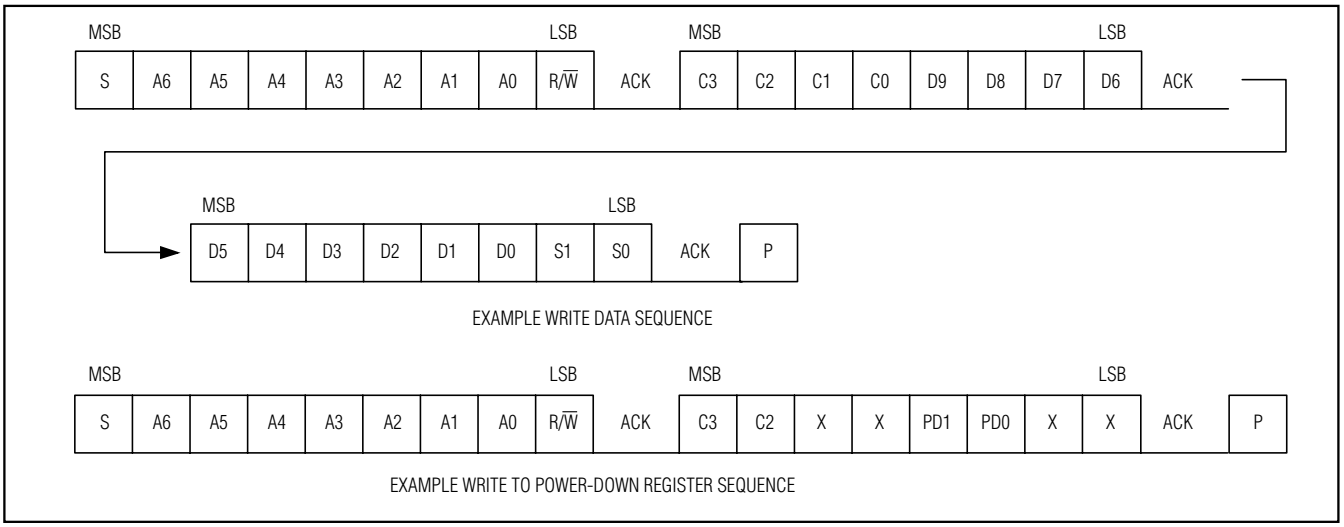


Figure 6. Example Write Command Sequences

write cycle must be repeated. Figure 6 shows two example write data sequences.

Read Data Format

In read mode (R/$\overline{W}$ = 1), the MAX5811 writes the contents of the DAC register to the bus. The direction of

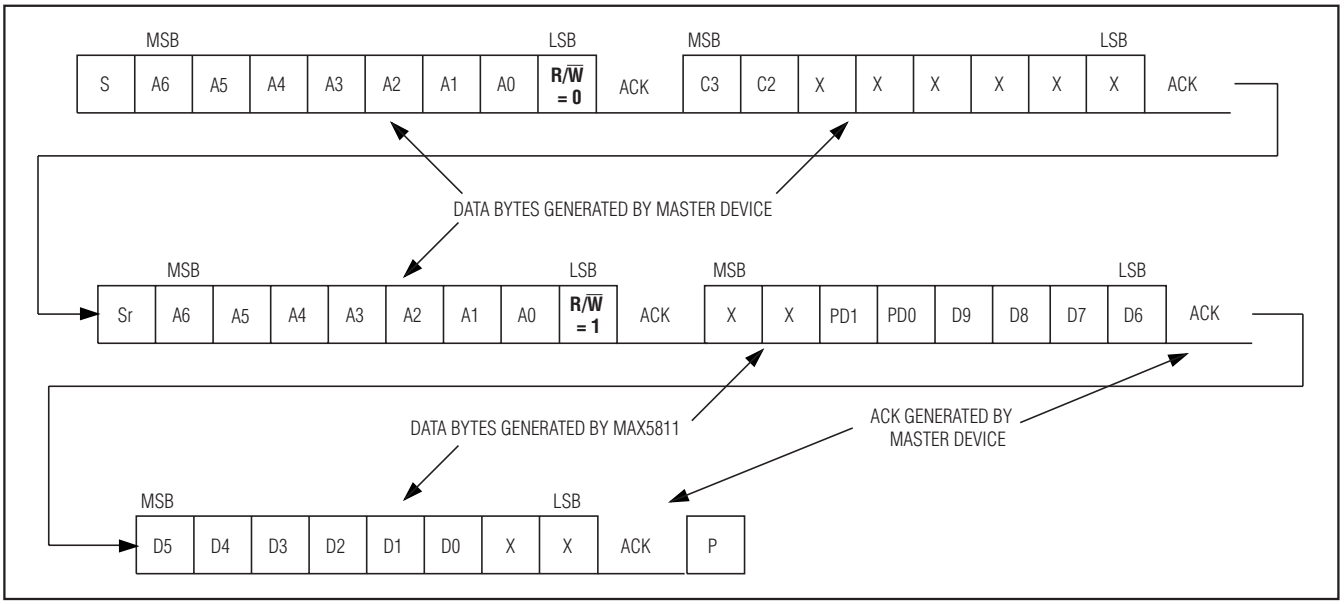


Figure 7. Read Word Data Sequence

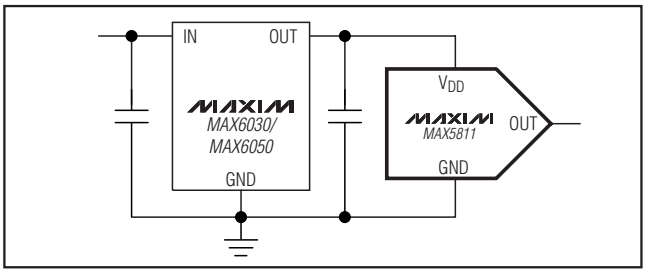


Figure 8. Powering the MAX5811 from an External Reference

data flow reverses following the address acknowledge by the MAX5811. The device transmits the first byte of data, waits for the master to acknowledge, then transmits the second byte. Figure 7 shows an example read data sequence.

I²C Compatibility

The MAX5811 is compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the ninth clock pulse. The *Typical Operating Circuit* shows a typical I²C application. The communication protocol supports the standard I²C 8-bit communications. The general call address is ignored. The MAX5811 address is compatible with the 7-bit I²C addressing protocol only. No 10-bit address formats are supported.

Digital Feedthrough Suppression

When the MAX5811 detects an address mismatch, the serial interface disconnects the SCL signal from the core circuitry. This minimizes digital feedthrough caused by the SCL signal on a static output. The serial interface reconnects the SCL signal once a valid START condition is detected.

Applications Information

Powering the Device from an External Reference

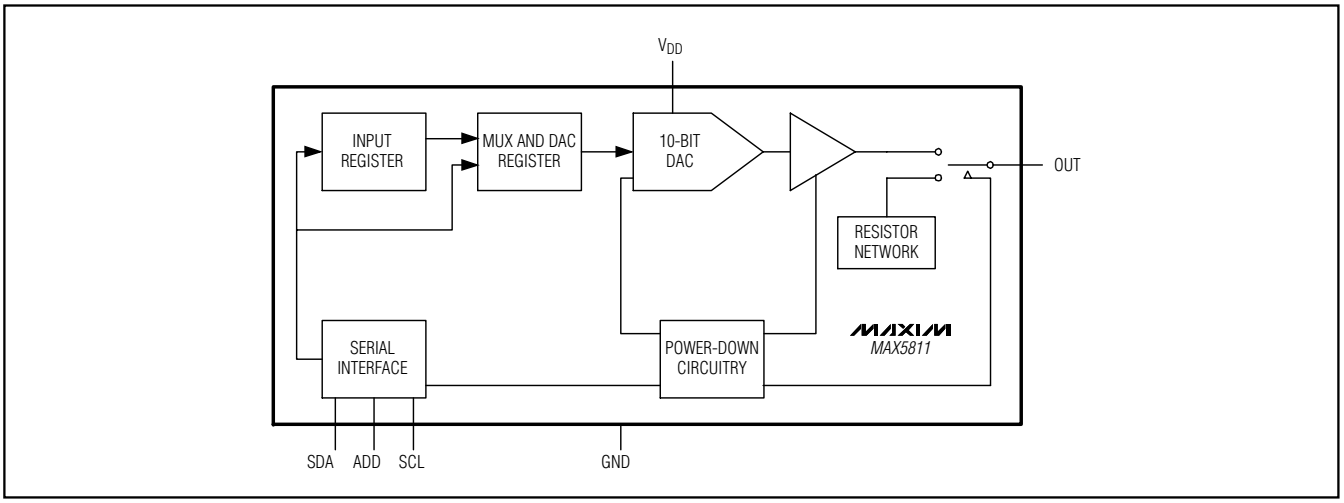
The MAX5811 uses the V_{DD} as the DAC voltage reference. Any power-supply noise is directly coupled to the device output. The circuit in Figure 8 uses a precision voltage reference to power the MAX5811, isolating the device from any power-supply noise. Powering the MAX5811 in such a manner greatly improves overall performance, especially in noisy systems. The MAX6030 (3V, 75ppm/°C) or the MAX6050 (5V, 75ppm/°C) precision voltage references are ideal choices due to the low power requirements of the MAX5811.

Digital Inputs and Interface Logic

The MAX5811 2-wire digital interface is I²C and SMBus compatible. The two digital inputs (SCL and SDA) load the digital input serially into the DAC. Schmitt-trigger buffered inputs allow slow-transition interfaces such as

10-Bit Low Power 2-Wire Interface Serial, Voltage-Output DAC

Functional Diagram



optocouplers to interface directly to the device. The digital inputs are compatible with CMOS logic levels.

Power-Supply Bypassing and Ground Management

Careful PC board layout is important for optimal system performance. Keep analog and digital signals separate to reduce noise injection and digital feedthrough. Use a ground plane to ensure that the ground return from GND to the power-supply ground is short and low impedance. Bypass V_{DD} with a 0.1µF capacitor to ground as close to the device as possible.

Selector Guide

PART	ADDRESS
MAX5811LEUT	0010 00X
MAX5811MEUT	0010 01X
MAX5811NEUT	0110 10X
MAX5811PEUT	1010 10X

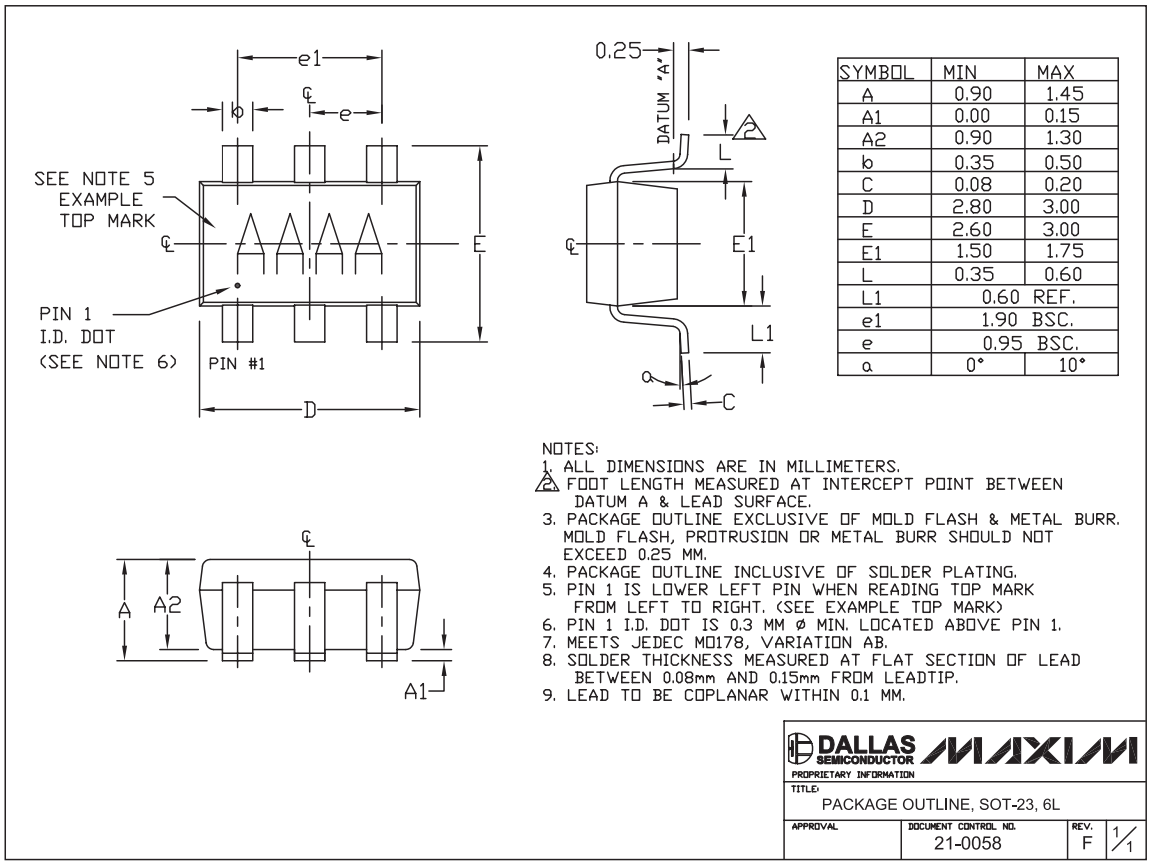
Chip Information

TRANSISTOR COUNT: 7172

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF.	
e1	1.90 BSC.	
e	0.95 BSC.	
α	0°	10°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	F	1/1

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MAX5811PEUT+T on WIN SOURCE
- Maxim Integrated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management