THE DATASHEET OF

MAX9101EUK+T

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+1.0V Micropower SOT23 Comparators

MAX9100/MAX9101

General Description

The MAX9100/MAX9101 micropower comparators are optimized for single-cell systems, and are fully specified for operation from a single supply of 1.0V to 5.5V. This ultra-low voltage operation, 5µA quiescent current consumption, and small footprint make the MAX9100/MAX9101 ideal for use in battery-powered systems. A wide-input common-mode range that includes the negative rail and rail-to-rail output swing allows almost all of the power supply to be used for signal voltage. In addition, propagation delay is less than 4µs, and rise and fall times are 100ns.

The MAX9100 features a push-pull CMOS output stage that sinks and sources current with large internal output drivers that allow rail-to-rail output swings with loads up to 5mA.The MAX9101 has an open-drain output stage that makes it suitable for mixed-voltage designs.

The MAX9100/MAX9101 are available in tiny SOT23-5 packages.

Applications

- Single-Cell Systems
- Pagers
- Closed Sensor Applications
- Battery-Powered Instrumentation
- Portable Electronic Equipment
- Portable Communication Devices

Features

- Ultra-Low Voltage: Guaranteed Down to 1.0V
- Low Quiescent Current: 5µA
- Optimized for Single-Cell Battery-Powered Systems
- Wide Input Common-Mode Range
- CMOS Rail-to-Rail Output Swing (MAX9100)
- Open-Drain Output (MAX9101)
- 4µs Propagation Delay
- High Output Drive Capability: 5mA Sink and Source (MAX9100)
- No Output Phase Reversal for Overdriven Inputs
- Available in Tiny SOT23-5 Package

Ordering Information

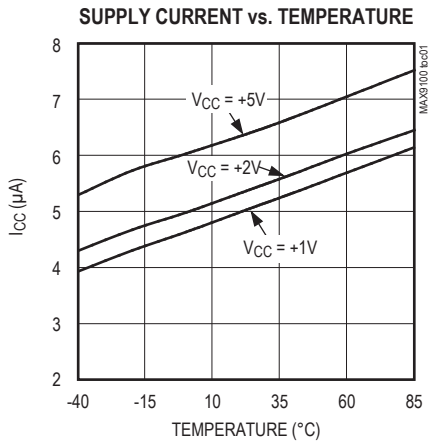
PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX9100EUK+T	5 SOT23-5	ADOR	U5-1
MAX9100ESA	8 SO	—	S8-2
MAX9101EUK+T	5 SOT23-5	ADOS	U5-1
MAX9101ESA	8 SO	—	S8-2

Note: *All devices specified for over -40°C to +85°C operating temperature range.*

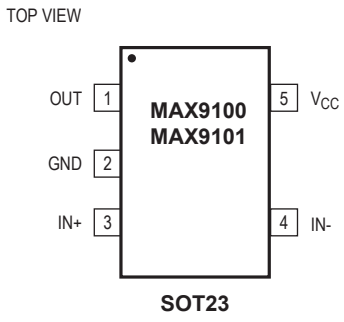
+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Typical Operating Characteristic



Pin Configurations



Pin Configurations continued at end of data sheet.

19-1808; Rev 2; 1/26

Absolute Maximum Ratings

Supply Voltage (V_{CC} to GND) ..... -0.3V to +6V
IN+ or IN- to GND..... -0.3V to (V_{CC} + 0.3V)
Current Into Input Pins..... ±20mA
Output Voltages to GND
MAX9100..... -0.3V to (V_{CC} + 0.3V)
MAX9101..... -0.3V to +6V
Output Short-Circuit Duration (to V_{CC} or GND)..... Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin Plastic SOT23
(derate 7.3mW/°C above +70°C)..... 571mW
8-Pin Plastic SO
(derate 5.88mW/°C above +70°C)..... 471mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +1.2V to +5.5V, V_{CM} = 0V, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from the PSRR tests	1.0		5.5	V
Supply Current	I_{CC}	V_{CC} = +1V, T_A = +25ºC		5.0	8.0	µA
		V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}		6.0	13.0	
Input Offset Voltage	V_{OS}	T_A = +25°C		±3	±10	mV
		T_A = T_{MIN} to T_{MAX}			±20	
Input Hysteresis	V_{HYST}			±2		mV
Input Offset Current	I_{OS}	V_{CC} = +5.5V, T_A = +25ºC		±0.1	±5	nA
		V_{CC} = +5.5V, T_A = T_{MIN} to T_{MAX}			±10	
Input Bias Current	I_B	V_{CC} = +5.5V, T_A = +25ºC		±5	±15	nA
		V_{CC} = +5.5V, T_A = T_{MIN} to T_{MAX}			±30	
Input Resistance	R_{IN}	Differential mode		200		MΩ
		Common mode		65		
Input Common-Mode Voltage Range (Note 2)	V_{CM}	Inferred from CMRR test	0		V_{CC} -0.2	V
Common-Mode Rejection Ratio (Note 3)	CMRR	T_A = +25ºC	54	68		dB
		T_A = T_{MIN} to T_{MAX}	46			
Power-Supply Rejection Ratio	PSRR	1.0V ≤ V_{CC} ≤ 1.5V, T_A = +25ºC	54	66		dB
		1.5V ≤ V_{CC} ≤ 5.5V, T_A = -40ºC to +85°C	56	68		
Output-Voltage High (MAX9100)	V_{CC} - V_{OH}	V_{CC} = +5.0V, I_{SOURCE} = 5mA		90	180	mV
		V_{CC} = +1.2V, I_{SOURCE} = 0.5mA		60	120	
		V_{CC} = +1.0V, I_{SOURCE} = 0.1mA, T_A = +25ºC		25	75	
Output-Voltage Low	V_{OL}	V_{CC} = +5.0V, I_{SINK} = 5mA		100	180	mV
		V_{CC} = +1.2V, I_{SINK} = 0.5mA		45	120	
		V_{CC} = +1.0V, I_{SINK} = 0.5mA, T_A = +25ºC		15	75	

Electrical Characteristics (continued)

(V_{CC} = +1.2V to +5.5V, V_{CM} = 0V, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

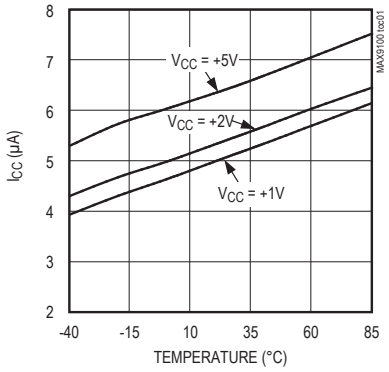
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{SC}	Sourcing (MAX9100)	V_{CC} = +5.0V		25		mA
			V_{CC} = +1.2V		3		
		Sinking	V_{CC} = +5.0V		28		
			V_{CC} = +1.2V		3		
Output Open-Drain Leakage Current (MAX9101)	I_{LKG}	V_{CC} = +5.5V			0.02	0.2	µA
Power-Up Time	t_{PU}				250		ns
Input Capacitance	C_{IN}				3		pF
Output Rise Time (MAX9100)	t_{rise}	C_L = 15pF			100		ns
Output Fall Time (Note 4)	t_{fall}	C_L = 15pF			100		ns
Propagation Delay (Note 5)	t_{pd+}	$V_{OVERDRIVE}$ = 50mV, V_{CC} = +5.0V			3.4		µs
	t_{pd-}	$V_{OVERDRIVE}$ = 50mV, V_{CC} = +5.0V			4.5		
	t_{pd+}	$V_{OVERDRIVE}$ = 50mV, V_{CC} = +1.0V			3.3		
	t_{pd-}	$V_{OVERDRIVE}$ = 50mV, V_{CC} = +1.0V			3.7		

Note 1: All specifications are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Operation with V_{CM} up to V_{CC} is possible with reduced accuracy. See the *Input Stage Circuitry and Rail-to-Rail Operation* section.
Note 3: Tested over the specified Input Common-Mode Voltage Range and with V_{CC} = +5.5V.
Note 4: Specified with C_L = 15pF for MAX9100/MAX9101, and with R_{PULLUP} = 5kΩ for MAX9101.
Note 5: Input overdrive is defined above and beyond the offset voltage and hysteresis of the comparator input.

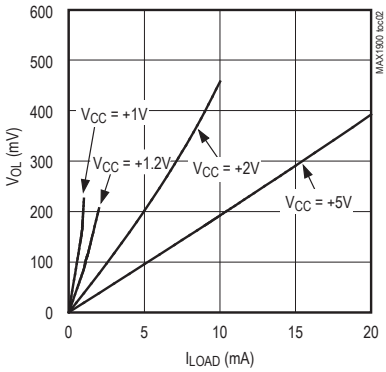
Typical Operating Characteristics

(V_{CC} = +5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

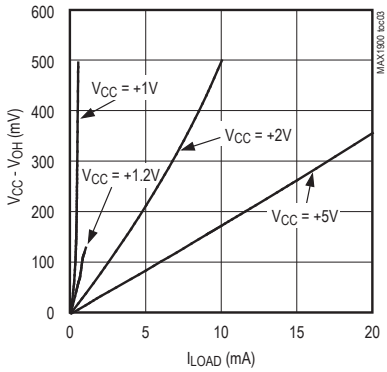
SUPPLY CURRENT vs. TEMPERATURE



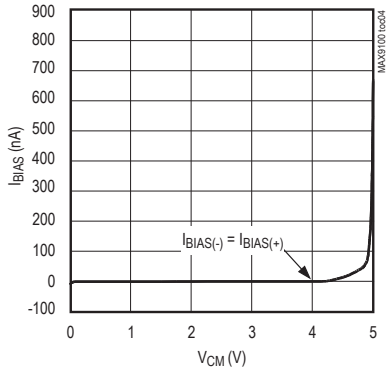
OUTPUT-VOLTAGE LOW vs. SINK CURRENT



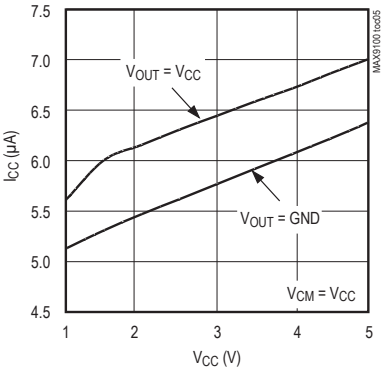
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT



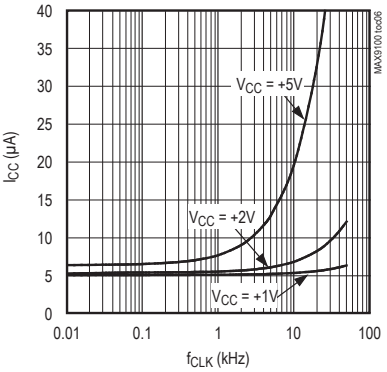
INPUT BIAS CURRENT vs. V_{CM}



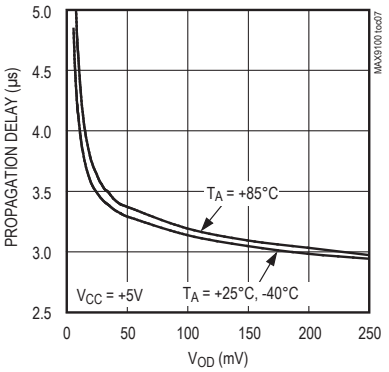
SUPPLY CURRENT vs. SUPPLY VOLTAGE



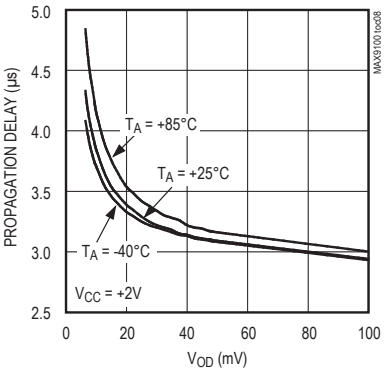
SUPPLY CURRENT vs. OUTPUT TRANSITION FREQUENCY



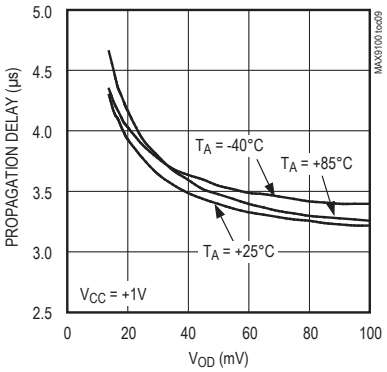
PROPAGATION DELAY (tpd+) vs. INPUT OVERDRIVE



PROPAGATION DELAY (tpd+) vs. INPUT OVERDRIVE



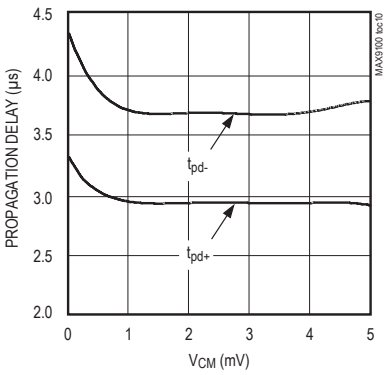
PROPAGATION DELAY (tpd)+ vs. INPUT OVERDRIVE



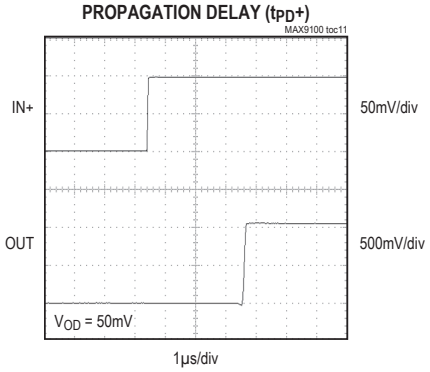
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

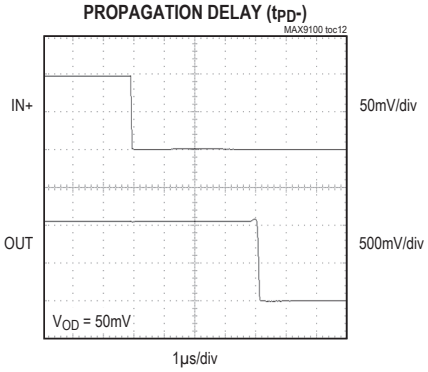
PROPAGATION DELAY vs. V_{CM}



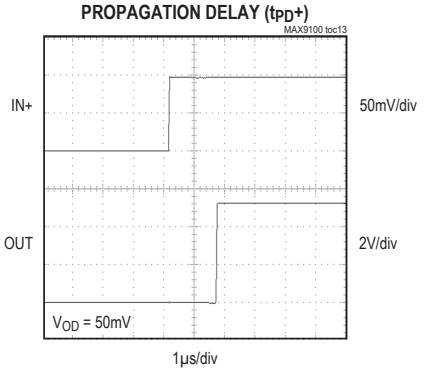
PROPAGATION DELAY (t_{PD}+)



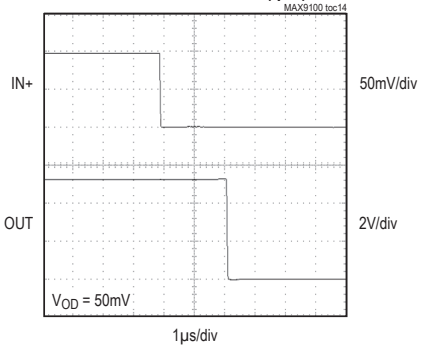
PROPAGATION DELAY (t_{PD}-)



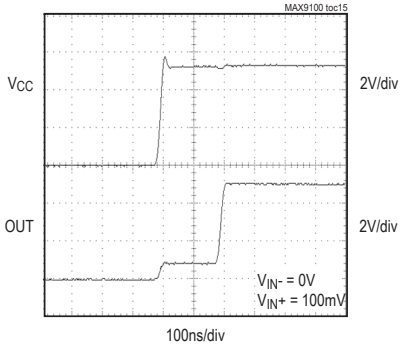
PROPAGATION DELAY (t_{PD}+)



PROPAGATION DELAY (tpd-)



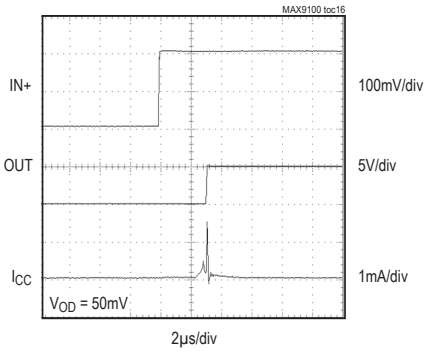
POWER-UP DELAY



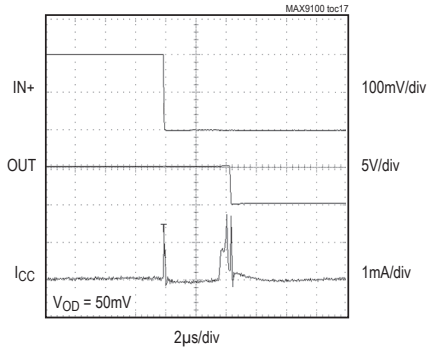
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

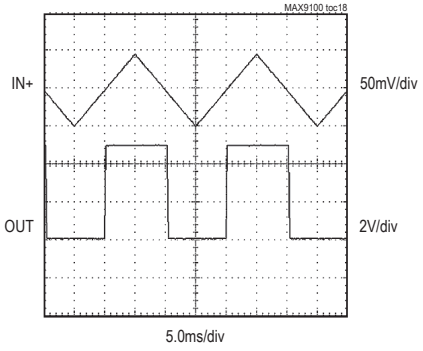
SWITCHING CURRENT, OUTPUT RISING



SWITCHING CURRENT, OUTPUT FALLING



RESPONSE TO SLOW TRIANGLE WAVEFORM



Pin Description

PIN		NAME	FUNCTION
SOT23-5	SO-8		
1	6	OUT	Comparator Output
2	4	GND	Ground
3	3	IN+	Noninverting Input
4	2	IN-	Inverting Input
—	1, 5, 8	N.C.	No Connection
5	7	V_{CC}	Positive Supply Voltage

Detailed Description

The MAX9100/MAX9101 are low-power and ultra-low single-supply voltage comparators. They have an operating supply voltage range between +1.0V to +5.5V and consume only 5µA of quiescent supply current, while achieving 4µs propagation delay.

Input Stage Circuitry and Rail-to-Rail Operation

The devices' input common-mode range is fully specified from 0 to (V_{CC} - 0.2V), although full rail-to-rail input range is possible with degraded performance. These comparators may operate at any differential input voltage within these limits. Input bias current is typically ±5nA if the input voltage is within the specified common-mode range. Comparator inputs are protected from overvoltage by internal diodes connected to the supply rails. As the input voltage exceeds the supply rails, these diodes become forward biased and begin to conduct. Consequently, bias currents increase exponentially as the input voltage exceeds the supply rails.

True rail-to-rail input operation is also possible. For input common-mode voltages from V_{CC} - 0.2V to V_{CC}, the input bias current will typically increase to 800nA. Additionally, the supply current will typically increase to 7µA. Otherwise, the device functions as within the specified common-mode range. See graphs in the *Typical Operating Characteristics*.

Output Stage Circuitry

The MAX9100/MAX9101 contain a unique output stage capable of rail-to-rail operation. Many comparators consume orders of magnitude more current during switching than during steady-state operation. However, with this family of comparators, the supply-current change during an output transition is extremely small. The *Typical Operating Characteristics* graph Supply Current vs. Output Transition Frequency shows the minimal supply-current increase as the output switching frequency approaches 100kHz. This characteristic reduces the requirement for power-supply filter capacitors to reduce glitches created by comparator switching currents. This feature increases battery life in portable applications.

Push-Pull Output (MAX9100)

The MAX9100 has a push-pull CMOS output. The output stage swings rail-to-rail under no-load conditions. External load drive capability varies with supply voltage.

Open-Drain Output (MAX9101)

The MAX9101 has an open-drain output, which can be pulled up to +6.0V above ground independent of the supply voltage. This is typically used with an external pullup resistor, facilitating interface between mixed logic voltages. Alternatively, multiple open-drain comparator outputs can be connected in a wired-OR configuration.

Applications Information

Low-Voltage Operation: V_{CC} = 1V

The minimum operating voltage is +1.0V. At lower supply voltages, the input common-mode range remains rail-to-rail, but the comparator's output drive capability is reduced and propagation delay increases (see the *Typical Operating Characteristics*).

Internal Hysteresis

Hysteresis increases the comparators' noise margin by increasing the upper threshold and decreasing the lower threshold (Figure 1). This hysteresis prevents the comparator from providing multiple poles when driven with a very-slow-changing signal.

Additional Hysteresis

These comparators have 1.0mV internal hysteresis. Additional hysteresis can be generated with two resistors using positive feedback (Figure 2). Use the following procedure to calculate resistor values:

1) Calculate the trip points of the comparator using these formulas:

$$V_{TH} = V_{REF} + \left(\frac{(V_{CC} - V_{REF})R2}{R1+R2}\right)$$

$$V_{TL} = V_{REF}\left(1 - \frac{R2}{R1+R2}\right)$$

V_{TH} is the threshold voltage at which the comparator switches its output from high to low as V_{IN} rises above the trip point. V_{TL} is the threshold voltage at which the comparator switches its output from low to high as V_{IN} drops below the trip point.

2) The hysteresis band will be:

$$V_{HYS} = V_{TH} - V_{TL} = V_{CC}\left(\frac{R2}{R1+R2}\right)$$

3) In this example, let V_{CC} = +5V and V_{REF} = +2.5V:

$$V_{TH} = 2.5 + 2.5\left(\frac{R2}{R1+R2}\right)$$

and

$$V_{TL} = 2.5\left(1 - \frac{R2}{R1+R2}\right)$$

4) Select R2. In this example, we will choose 1kΩ.

5) Select V_{HYS}. In this example, we will choose 50mV.

6) Solve for R1:

$$V_{HYS} = V_{CC}\left(\frac{R2}{R1+R2}\right)$$

$$0.050 = 5\left(\frac{1000}{R1+1000}\right)$$

where R1 ≈ 100kΩ, V_{TH} = 2.525V, and V_{TL} = 2.475V.

Board Layout and Bypassing

A power-supply bypass capacitor is not normally required, but 100nF bypass capacitors can be used when the supply impedance is high or when the supply leads are long. Minimize signal lead lengths to reduce stray capacitance between the input and output that might cause instability.

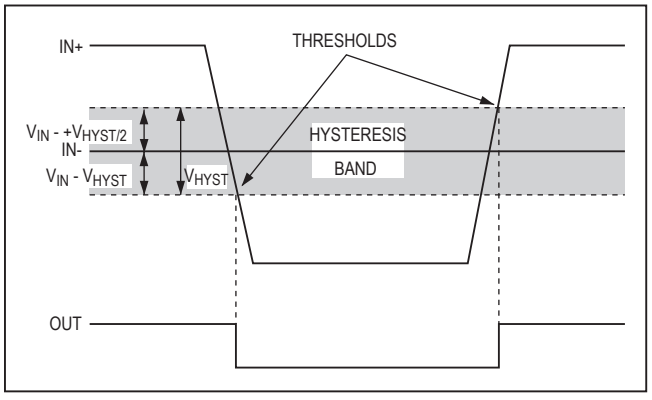


Figure 1. Threshold Hysteresis Band

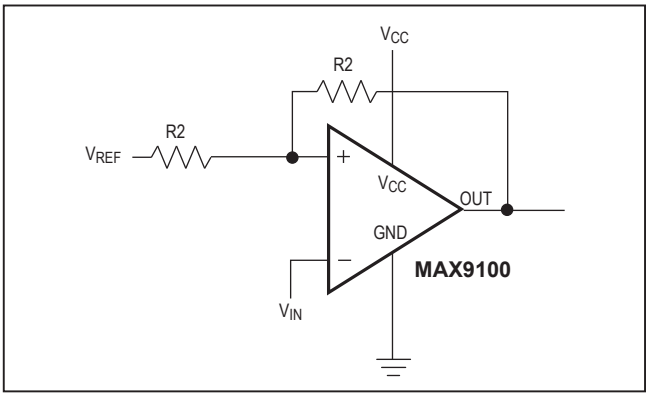


Figure 2. Additional Hysteresis (MAX9100)

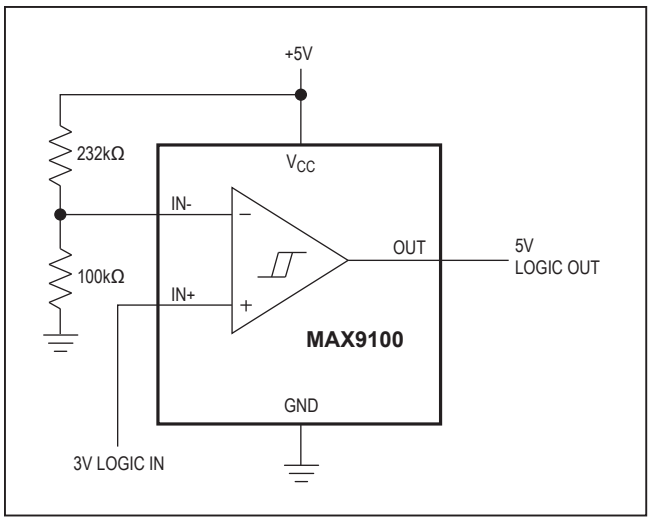


Figure 3. MAX9100 Logic-Level Translator

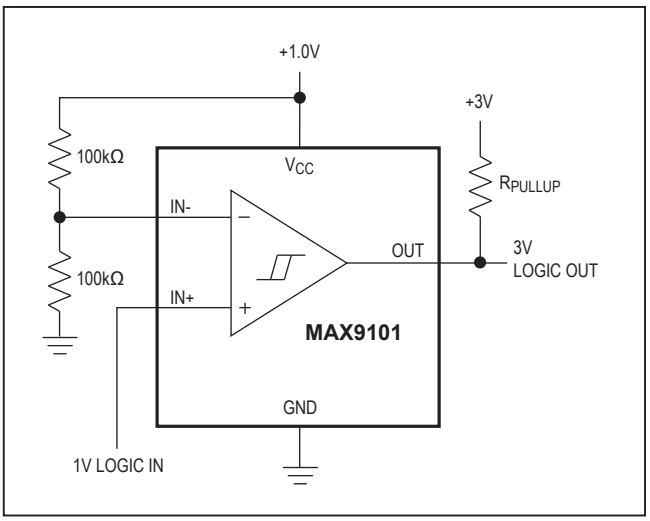


Figure 4. MAX9101 Logic-Level Translator

Typical Application

Logic-Level Translator

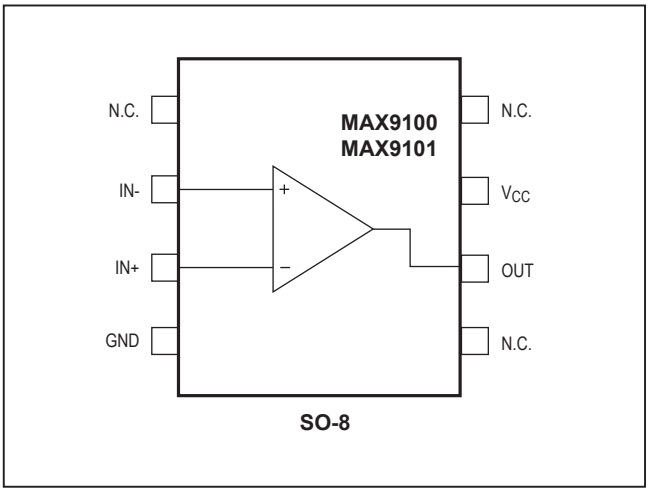
3V to 5V

Figure 3 shows an application that converts 3V logic levels to 5V logic levels. The push-pull output MAX9100 is powered by the +5V supply voltage, and the inverting input is biased to +1.5V with two resistors. This configuration allows a full 5V swing at the output, maximizing the noise margin of the receiving circuit.

1V to 3V

Figure 4 shows an application that converts 1V logic levels to 3V logic levels. The MAX9101 is powered by the +1V supply voltage, and the pullup resistor for the output is connected to the +3V supply voltage. The inverting input is biased to +0.5V with two resistors.

Pin Configurations (continued)



SO-8

Chip Information

TRANSISTOR COUNT: 393

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/00	Initial release	—
1	1/07	Add input current ratings to ABS MAX table	2
2	1/26	Updated *Ordering Information* table	1

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