



**THE DATASHEET OF  
NLV74LCX138DR2G**



# Low-Voltage CMOS 3-to-8 Decoder/Demultiplexer With 5 V-Tolerant Inputs

## MC74LCX138

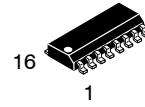
The MC74LCX138 is a high performance, 3-to-8 decoder/demultiplexer operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX138 inputs to be safely driven from 5 V devices. The MC74LCX138 is suitable for memory address decoding and other TTL level bus-oriented applications.

The MC74LCX138 high-speed 3-to-8 decoder/demultiplexer accepts three binary weighted inputs (A0, A1, A2) and, when enabled, provides eight mutually exclusive active-LOW outputs ( $\overline{O0}$ – $\overline{O7}$ ). The LCX138 features three Enable inputs, two active-LOW ( $\overline{E1}$ ,  $\overline{E2}$ ) and one active-HIGH (E3). All outputs will be HIGH unless  $\overline{E1}$  and  $\overline{E2}$  are LOW, and E3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LCX138 devices and one inverter (see Figure 1). The LCX138 can be used as an 8-output demultiplexer by using one of the active-LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

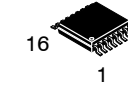
Current drive capability is 24 mA at the outputs at 3 V.

### Features

- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability at 3 V
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model >2000 V
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

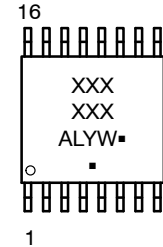
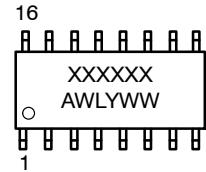


SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F

### MARKING DIAGRAMS



- A = Assembly Location
- WL, L = Wafer Lot
- Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

# MC74LCX138

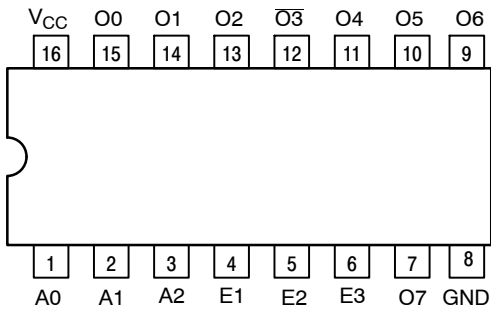


Figure 1. Pinout: 16-Lead (Top View)

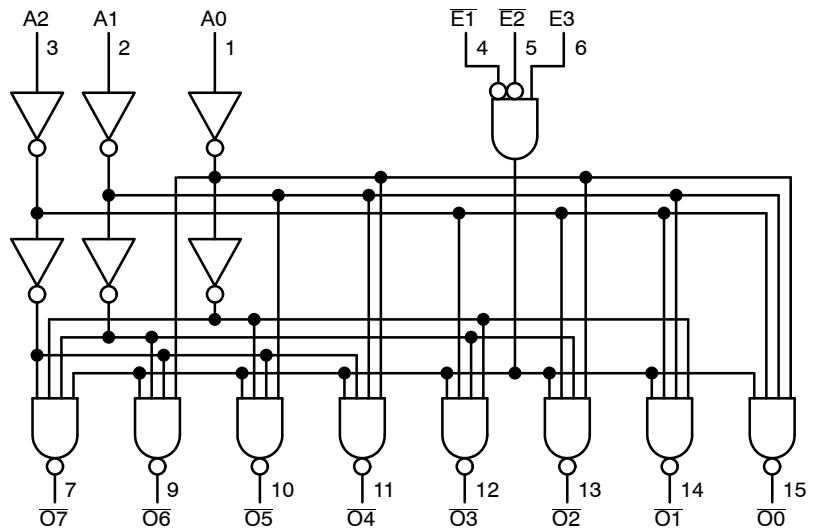


Figure 2. Logic Diagram

## PIN NAMES

Pins	Function
A0-A2	Address Inputs
E1-E2	Enable Inputs
E3	Enable Input
O0-O7	Outputs

## TRUTH TABLE

Inputs						Outputs							
E1	E2	E3	A0	A1	A2	O0	O1	O2	O3	O4	O5	O6	O7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level

L = Low Voltage Level

X = High or Low Voltage Level and Transitions are Acceptable

For I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

# MC74LCX138

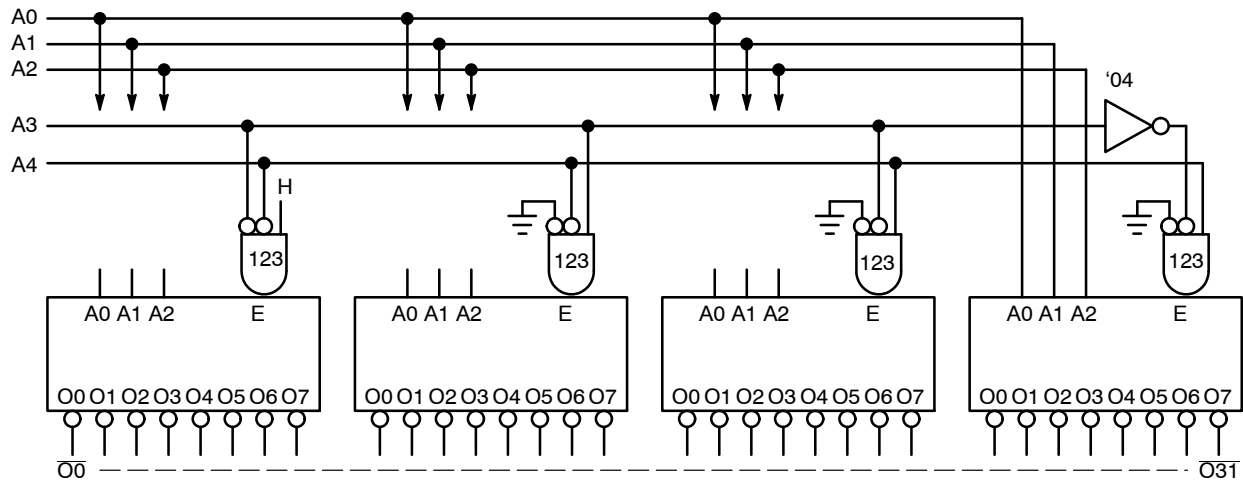


Figure 3. Expansion to 1-of-32 Decoding

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage	-0.5 to +6.5	V	
$V_I$	DC Input Voltage (Note 1)	-0.5 to +6.5	V	
$V_O$	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
$I_{IK}$	DC Input Diode Current	$V_I < GND$	-50	mA
$I_{OK}$	DC Output Diode Current	$V_O < GND$	-50	mA
$I_O$	DC Output Source/Sink Current		$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin		$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature, 1 mm from Case for 10 secs		260	$^{\circ}C$
$T_J$	Junction Temperature Under Bias		+150	$^{\circ}C$
$\theta_{JA}$	Thermal Resistance (Note 1)	SOIC-16 WQFN-16 TSSOP-16	126 114 159	$^{\circ}C/W$
$P_D$	Power Dissipation in Still Air at 25 $^{\circ}C$	SOIC-16 WQFN-16 TSSOP-16	995 1094 787	mW
MSL	Moisture Sensitivity		Level 1	-
$F_R$	Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in	-
$V_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- $I_O$  absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
- HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

# MC74LCX138

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating	1.65	3.3	5.5	V
		Data Retention Only	1.5	3.3	5.5	
V <sub>I</sub>	Digital Input Voltage	0	–	5.5	V	
V <sub>O</sub>	Output Voltage	Active Mode (High or Low State)	0	–	V <sub>CC</sub>	V
		Tri-State Mode	0	–	5.5	
		Power Down Mode (V <sub>CC</sub> = 0 V)	0	–	5.5	
T <sub>A</sub>	Operating Free-Air Temperature	–40	–	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Rate	V <sub>CC</sub> = 1.65 V to 1.95 V	0	–	20	nS/V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0	–	20	
		V <sub>I</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0	–	10	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	–	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = –40 °C to +85 °C		T <sub>A</sub> = –40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V <sub>CC</sub>	–	0.65 x V <sub>CC</sub>	–	V
			2.3 – 2.7	1.7	–	1.7	–	
			3.0 – 3.6	2.0	–	2.0	–	
			4.5 – 5.5	0.70 x V <sub>CC</sub>	–	0.70 x V <sub>CC</sub>	–	
V <sub>IL</sub>	LOW Level Input Voltage		1.65 – 1.95	–	0.35 x V <sub>CC</sub>	–	0.35 x V <sub>CC</sub>	V
			2.3 – 2.7	–	0.7	–	0.7	
			3.0 – 3.6	–	0.8	–	0.8	
			4.5 – 5.5	–	0.30 x V <sub>CC</sub>	–	0.30 x V <sub>CC</sub>	
V <sub>OH</sub>	High-Level Output Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = –100 μA I <sub>OH</sub> = –4 mA I <sub>OH</sub> = –8 mA I <sub>OH</sub> = –12 mA I <sub>OH</sub> = –16 mA I <sub>OH</sub> = –24 mA I <sub>OH</sub> = –32 mA	1.65 to 5.5	V <sub>CC</sub> – 0.1	–	V <sub>CC</sub> – 0.1	–	V
			1.65	1.29	–	1.29	–	
			2.3	1.8	–	1.8	–	
			2.7	2.2	–	2.2	–	
			3.0	2.4	–	2.4	–	
			3.0	2.2	–	2.2	–	
			4.5	3.7	–	3.7	–	
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 32 mA	1.65 to 5.5	–	0.1	–	0.1	V
			1.65	–	0.24	–	0.24	
			2.3	–	0.3	–	0.3	
			2.7	–	0.4	–	0.4	
			3.0	–	0.4	–	0.4	
			3.0	–	0.55	–	0.55	
			4.5	–	0.6	–	0.6	
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>I</sub> = 5.5 V or V <sub>O</sub> = 5.5 V	0	–	10	–	10	μA

# MC74LCX138

## DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40 °C to +85 °C		T <sub>A</sub> = -40 °C to +125 °C		Unit
				Min	Max	Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = 5.5 V or GND	3.6	-	10	-	10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V	2.3 to 3.6	-	500	-	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = -40 °C to +85 °C		T <sub>A</sub> = -40 °C to +125 °C		Unit
				Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, A <sub>n</sub> to $\bar{O}_n$	See Figures 4 and 5	1.65 to 1.95	-	11.5	-	11.5	ns
			2.3 to 2.7	-	7.2	-	7.2	
			2.7	-	7.0	-	7.0	
			3.0 to 3.6	-	6.0	-	6.0	
			4.5 to 5.5	-	5.0	-	5.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, E <sub>1</sub> , E <sub>2</sub> to $\bar{O}_n$	See Figures 4 and 5	1.65 to 1.95	-	12.0	-	12.0	ns
			2.3 to 2.7	-	8.4	-	8.4	
			2.7	-	7.5	-	7.5	
			3.0 to 3.6	-	6.5	-	6.5	
			4.5 to 5.5	-	5.5	-	5.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, E <sub>3</sub> to $\bar{O}_n$	See Figures 4 and 5	1.65 to 1.95	-	11.5	-	11.5	ns
			2.3 to 2.7	-	7.2	-	7.2	
			2.7	-	7.0	-	7.0	
			3.0 to 3.6	-	6.0	-	6.0	
			4.5 to 5.5	-	5.0	-	5.0	
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 5)		1.65 to 1.95	-	-	-	-	ns
			2.3 to 2.7	-	-	-	-	
			2.7	-	-	-	-	
			3.0 to 3.6	-	1.0	-	1.0	
			4.5 to 5.5	-	-	-	-	

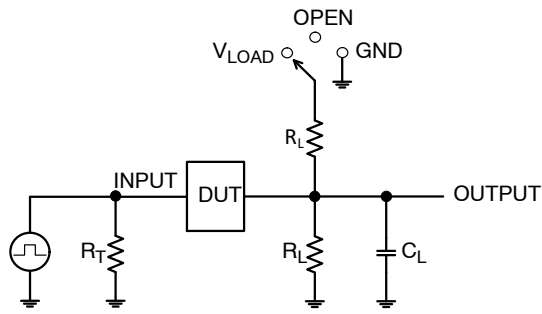
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	25	pF

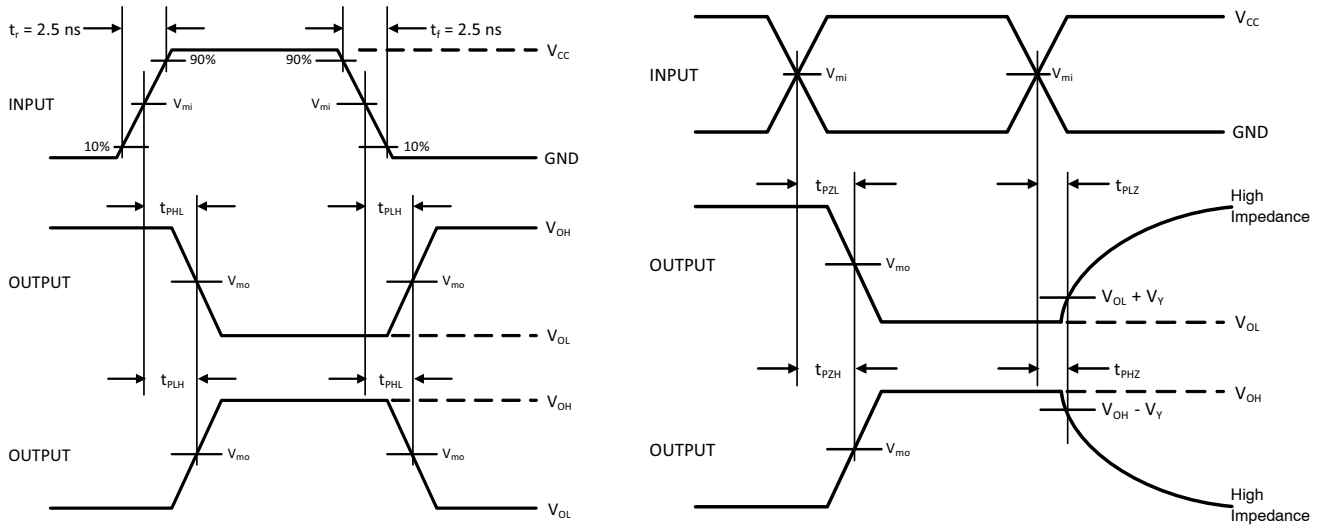
# MC74LCX138



$C_L$  includes probe and jig capacitance  
 $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1$  MHz

Test	Switch Position
$t_{PLH} / t_{PHL}$	Open
$t_{PLZ} / t_{PZL}$	$V_{LOAD}$
$t_{PHZ} / t_{PZH}$	GND

Figure 4. Test Circuit



$V_{CC}, V$	$R_L, \Omega$	$C_L, pF$	$V_{LOAD}$	$V_m, V$	$V_Y, V$
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	$V_{CC}/2$	0.3

Figure 5. Switching Waveforms

# MC74LCX138

## ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74LCX138DR2G	LCX138	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LCX138DR2G-Q*	LCX138	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LCX138DTG	LCX 138	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74LCX138DTR2G	LCX 138	TSSOP-16 (Pb-Free)	2500 Tape & Reel

## DISCONTINUED (Note 6)

NLV74LCX138DR2G*	LCX138	SOIC-16 (Pb-Free)	2500 Tape & Reel
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<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

6. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).

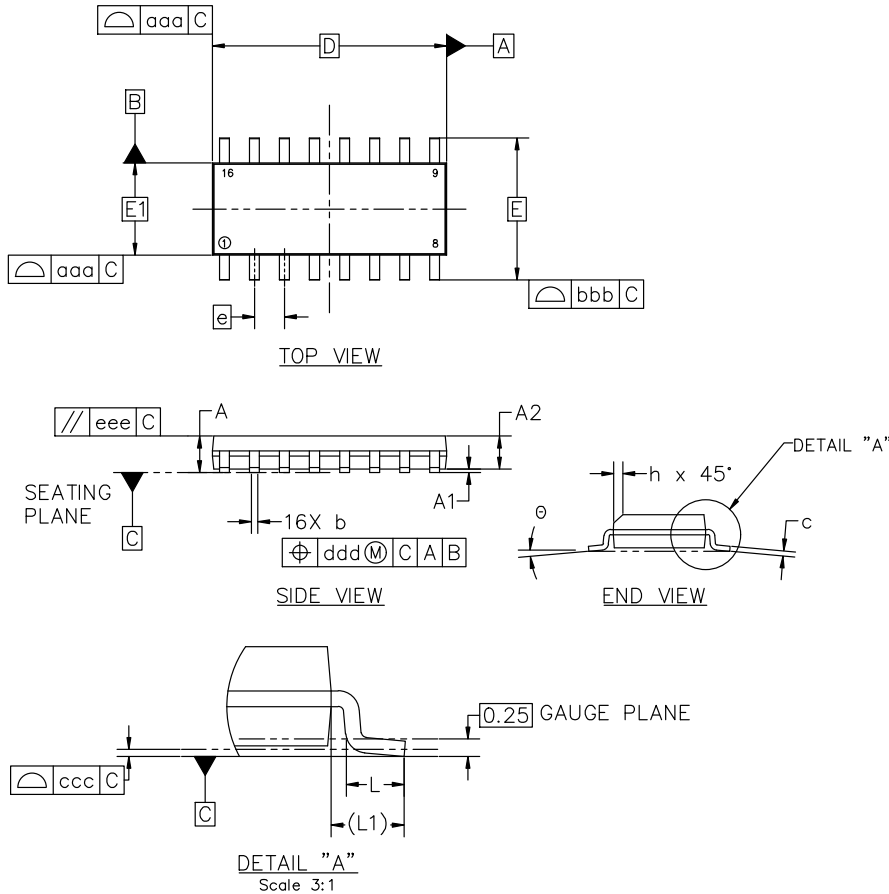


**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

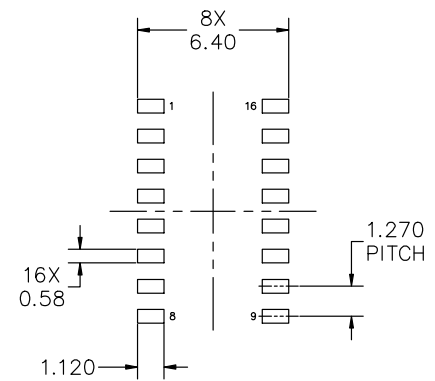
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

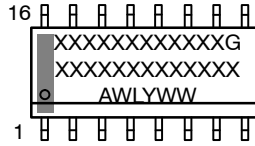
<b>DOCUMENT NUMBER:</b>	<b>98ASB42566B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.37 1.27P</b>	<b>PAGE 1 OF 2</b>

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**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

DATE 18 OCT 2024

**GENERIC  
MARKING DIAGRAM\***



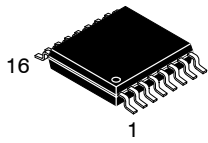
XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR  2. BASE  3. EMITTER  4. NO CONNECTION  5. EMITTER  6. BASE  7. COLLECTOR  8. COLLECTOR  9. BASE  10. EMITTER  11. NO CONNECTION  12. EMITTER  13. BASE  14. COLLECTOR  15. EMITTER  16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE  2. ANODE  3. NO CONNECTION  4. CATHODE  5. CATHODE  6. NO CONNECTION  7. ANODE  8. CATHODE  9. CATHODE  10. ANODE  11. NO CONNECTION  12. CATHODE  13. CATHODE  14. NO CONNECTION  15. ANODE  16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1  2. BASE, #1  3. EMITTER, #1  4. COLLECTOR, #1  5. COLLECTOR, #2  6. BASE, #2  7. EMITTER, #2  8. COLLECTOR, #2  9. COLLECTOR, #3  10. BASE, #3  11. EMITTER, #3  12. COLLECTOR, #3  13. COLLECTOR, #4  14. BASE, #4  15. EMITTER, #4  16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1  2. COLLECTOR, #1  3. COLLECTOR, #2  4. COLLECTOR, #2  5. COLLECTOR, #3  6. COLLECTOR, #3  7. COLLECTOR, #4  8. COLLECTOR, #4  9. BASE, #4  10. EMITTER, #4  11. BASE, #3  12. EMITTER, #3  13. BASE, #2  14. EMITTER, #2  15. BASE, #1  16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1  2. DRAIN, #1  3. DRAIN, #2  4. DRAIN, #2  5. DRAIN, #3  6. DRAIN, #3  7. DRAIN, #4  8. DRAIN, #4  9. GATE, #4  10. SOURCE, #4  11. GATE, #3  12. SOURCE, #3  13. GATE, #2  14. SOURCE, #2  15. GATE, #1  16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE  2. CATHODE  3. CATHODE  4. CATHODE  5. CATHODE  6. CATHODE  7. CATHODE  8. CATHODE  9. ANODE  10. ANODE  11. ANODE  12. ANODE  13. ANODE  14. ANODE  15. ANODE  16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH  2. COMMON DRAIN (OUTPUT)  3. COMMON DRAIN (OUTPUT)  4. GATE P-CH  5. COMMON DRAIN (OUTPUT)  6. COMMON DRAIN (OUTPUT)  7. COMMON DRAIN (OUTPUT)  8. SOURCE P-CH  9. SOURCE P-CH  10. COMMON DRAIN (OUTPUT)  11. COMMON DRAIN (OUTPUT)  12. COMMON DRAIN (OUTPUT)  13. GATE N-CH  14. COMMON DRAIN (OUTPUT)  15. COMMON DRAIN (OUTPUT)  16. SOURCE N-CH</p>	

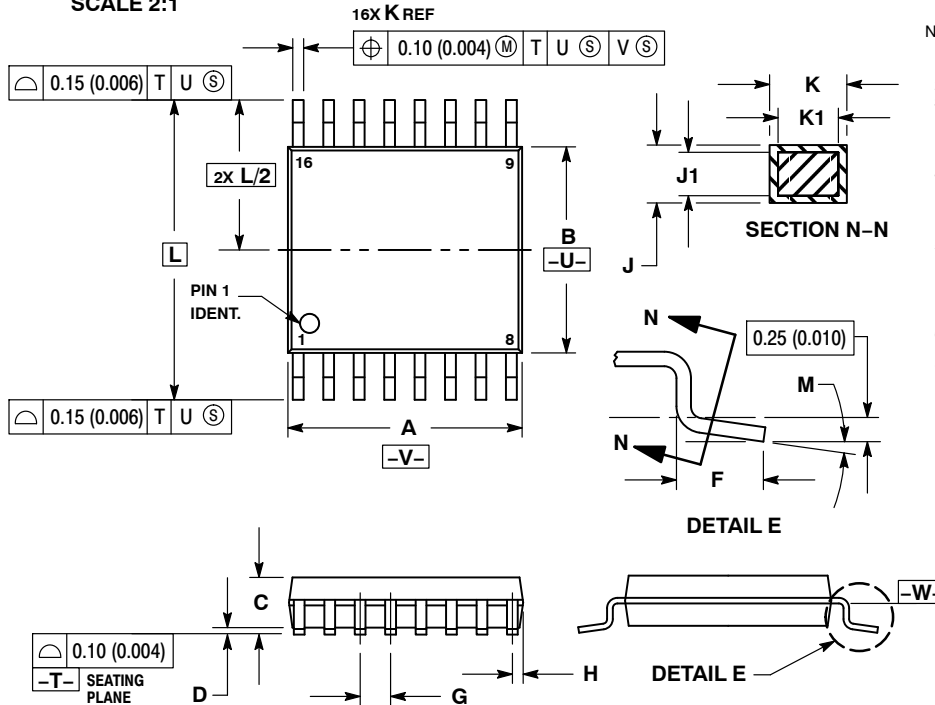
<b>DOCUMENT NUMBER:</b>	<b>98ASB42566B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.37 1.27P</b>	<b>PAGE 2 OF 2</b>

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TSSOP-16 WB  
CASE 948F  
ISSUE B

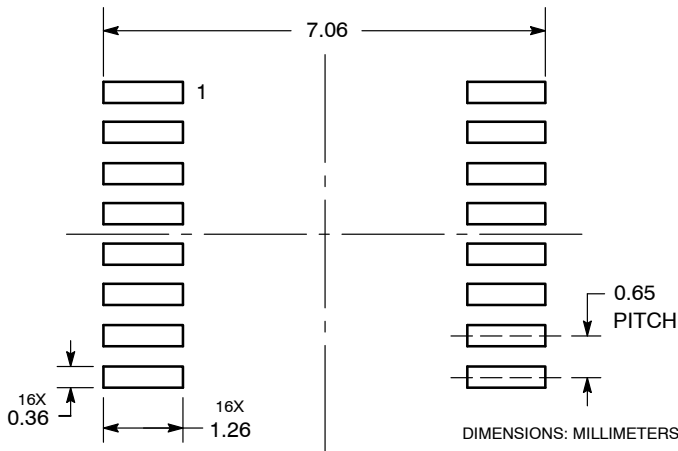
DATE 19 OCT 2006



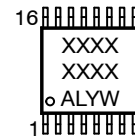
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

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