



**THE DATASHEET OF
CY62147EV18LL-45BVXI**



4-Mbit (256K x 16) Static RAM

Features

- **Very high speed: 45 ns**
- **Wide voltage range: 1.65V–2.25V**
- **Pin-compatible with CY62147DV18**
- **Ultra low standby power**
 - Typical standby current: 1 μ A
 - Maximum standby current: 7 μ A
- **Ultra-low active power**
 - Typical active current: 2 mA @ f = 1 MHz
- **Ultra low standby power**
- **Easy memory expansion with $\overline{\text{CE}}$, and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in a 48-ball Pb-free VFBGA package**

Functional Description^[1]

The CY62147EV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device

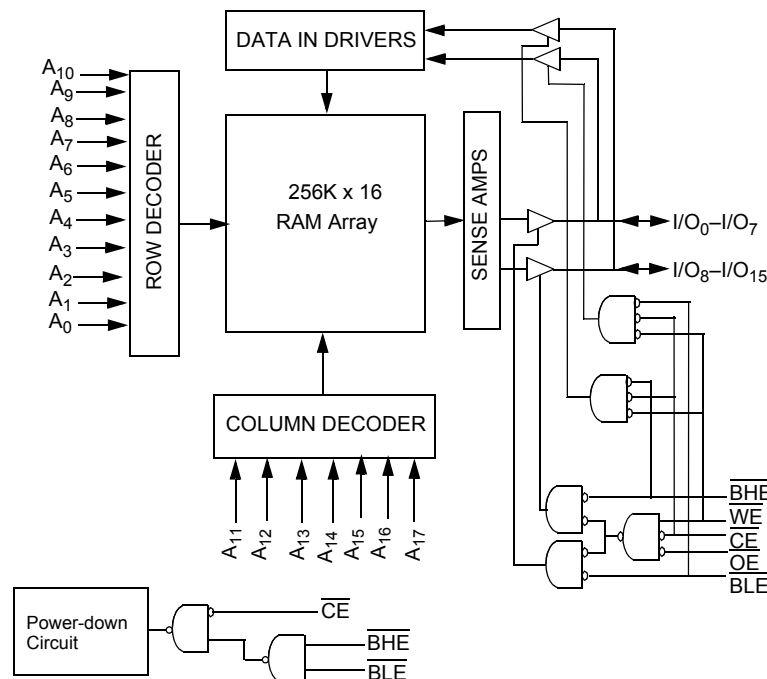
also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{\text{CE}}$ HIGH or both BLE and BHE are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{\text{CE}}$ HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and WE LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62147EV18 is available in a 48-ball VFBGA package.

Logic Block Diagram

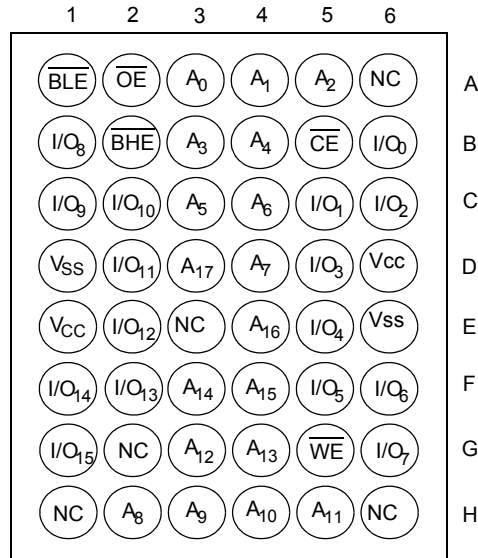


Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2, 3]

**48-ball VFBGA Pinout
Top View**



Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
					f = 1MHz		f = f _{max}			
Min.	Typ. ^[4]	Max.	Typ. ^[4]	Max.	Typ. ^[4]	Max.	Typ. ^[4]	Max.		
CY62147EV18-45LL	1.65	1.8	2.25	45	2	2.5	15	20	1	7

Notes:

- NC pins are not connected on the die.
- Pins H1, G2, and H6 in the VFBGA package are address expansion pins for 8 Mb, 16 Mb and 32 Mb, respectively.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to + 150°C
 Ambient Temperature with Power Applied -55°C to + 125°C
 Supply Voltage to Ground Potential -0.2V to + 2.45V ($V_{CCMAX} + 0.2V$)
 DC Voltage Applied to Outputs in High-Z State^[5,6] -0.2V to 2.45V ($V_{CCMAX} + 0.2V$)

DC Input Voltage^[5,6] -0.2V to 2.45V ($V_{CCMAX} + 0.2V$)
 Output Current into Outputs (LOW) 20 mA
 Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current > 200mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[7]
CY62147EV18	Industrial	-40°C to +85°C	1.65V to 2.25V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns			Unit
			Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA V _{CC} = 1.65V	1.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA V _{CC} = 1.65V			0.2	V
V _{IH}	Input HIGH Voltage	V _{CC} = 1.65V to 2.25V	1.4		V _{CC} + 0.2V	V
V _{IL}	Input LOW Voltage	V _{CC} = 1.65V to 2.25V	-0.2		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC(max)} = 2.25V I _{OUT} = 0 mA CMOS levels		15	20	mA
		f = 1 MHz V _{CC(max)} = 2.25V		2	2.5	mA
I _{SB1}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$ f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)		1	7	μA
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0		1	7	μA

Capacitance (for all Packages)^[8]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output Capacitance		10	pF

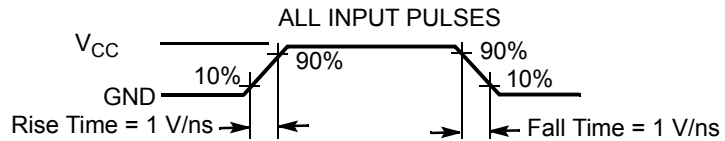
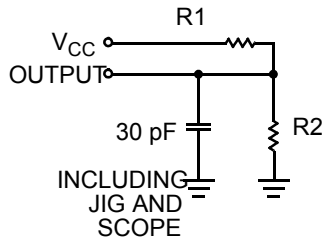
Note:

5. V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
6. V_{IH(max)} = V_{CC} + 0.5V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{cc(min)} and 200 μs wait time after V_{cc} stabilization.
8. Tested initially and after any design or process changes that may affect these parameters.

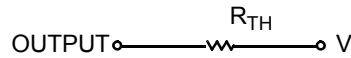
Thermal Resistance

Parameter	Description	Test Conditions	VFBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient) ^[8]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case) ^[8]		10	°C/W

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

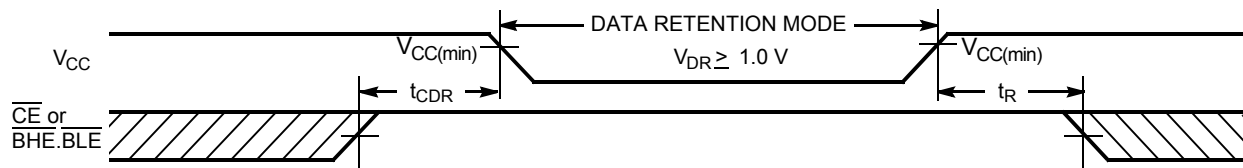


Parameters	1.80V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$ $CE \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0.5	3	μA
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform^[10]



Notes:

- 9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100 \mu s$ or stable at $V_{CC(min.)} \geq 100 \mu s$.
- 10. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics (Over the Operating Range) ^[11]

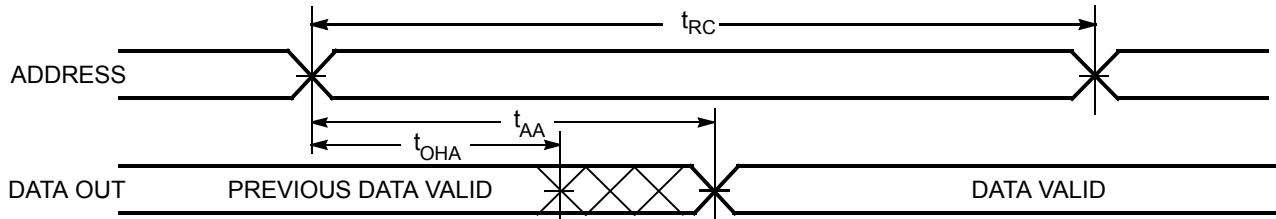
Parameter	Description	45 ns		Unit
		Min.	Max.	
Read Cycle				
t _{RC}	Read Cycle Time	45		ns
t _{AA}	Address to Data Valid		45	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		45	ns
t _{DOE}	\overline{OE} LOW to Data Valid		22	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[12]	5		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[12, 13]		18	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[12]	10		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[12, 13]		18	ns
t _{PU}	\overline{CE} LOW to Power-up	0		ns
t _{PD}	\overline{CE} HIGH to Power-down		45	ns
t _{DBE}	$\overline{BLE/BHE}$ LOW to Data Valid		45	ns
t _{LZBE}	$\overline{BLE/BHE}$ LOW to Low Z ^[12]	10		ns
t _{HZBE}	$\overline{BLE/BHE}$ HIGH to HIGH Z ^[12, 13]		18	ns
Write Cycle^[14]				
t _{WC}	Write Cycle Time	45		ns
t _{SCE}	\overline{CE} LOW to Write End	35		ns
t _{AW}	Address Set-up to Write End	35		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-up to Write Start	0		ns
t _{PWE}	\overline{WE} Pulse Width	35		ns
t _{BW}	$\overline{BLE/BHE}$ LOW to Write End	35		ns
t _{SD}	Data Set-up to Write End	25		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	\overline{WE} LOW to High-Z ^[12, 13]		18	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z ^[12]	10		ns

Notes:

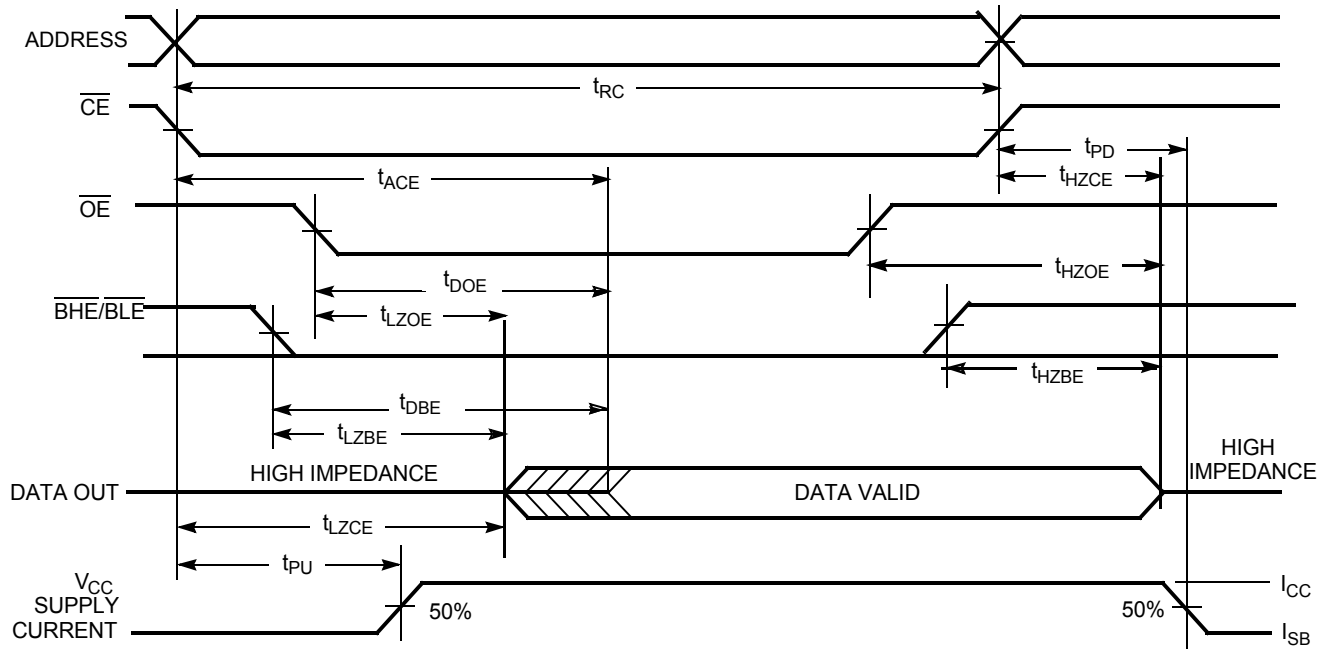
11. Test conditions for all parameters other than three-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
13. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state
14. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)^[15, 16]



Read Cycle No. 2 (\overline{OE} Controlled)^[16, 17]

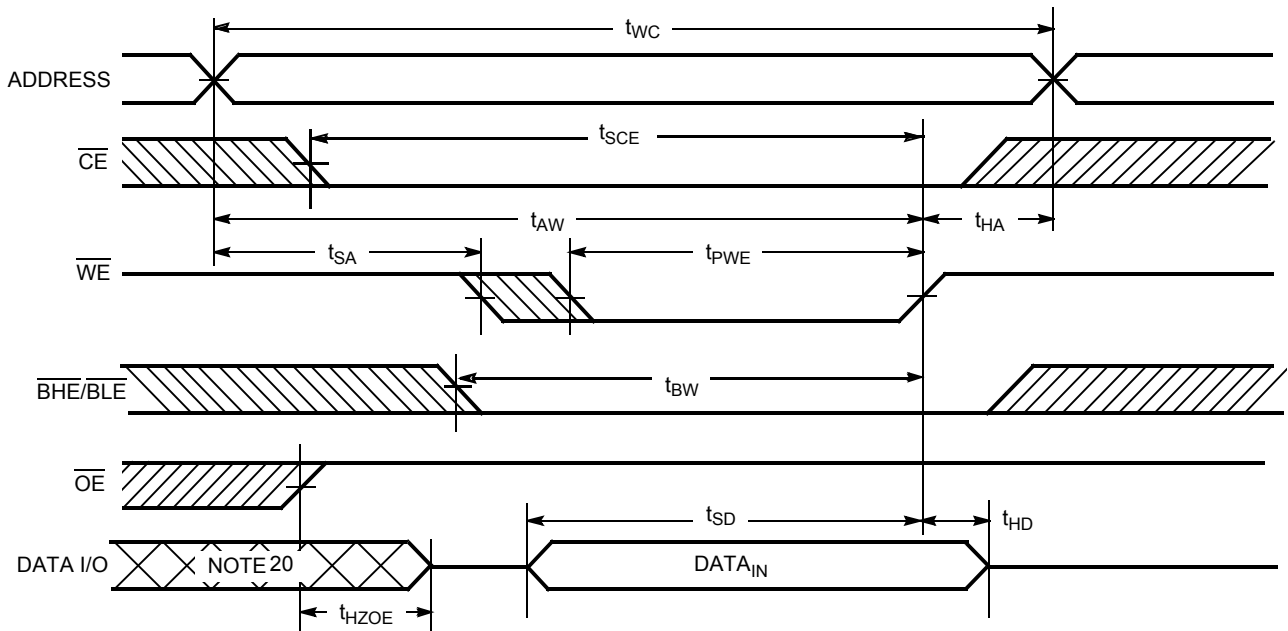


Notes:

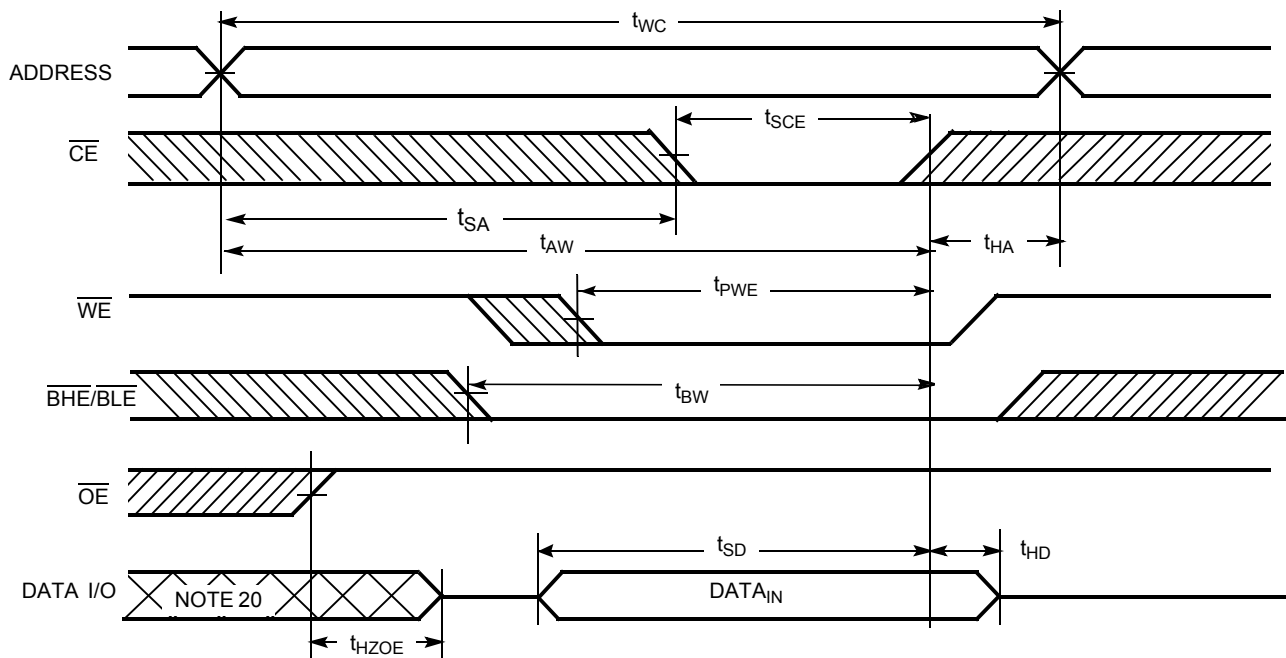
- 15. The device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
- 16. \overline{WE} is HIGH for read cycle.
- 17. Address valid prior to or coincident with \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{WE} Controlled)^[14, 18, 19]



Write Cycle No. 2 (\overline{CE} Controlled)^[14, 18, 19]

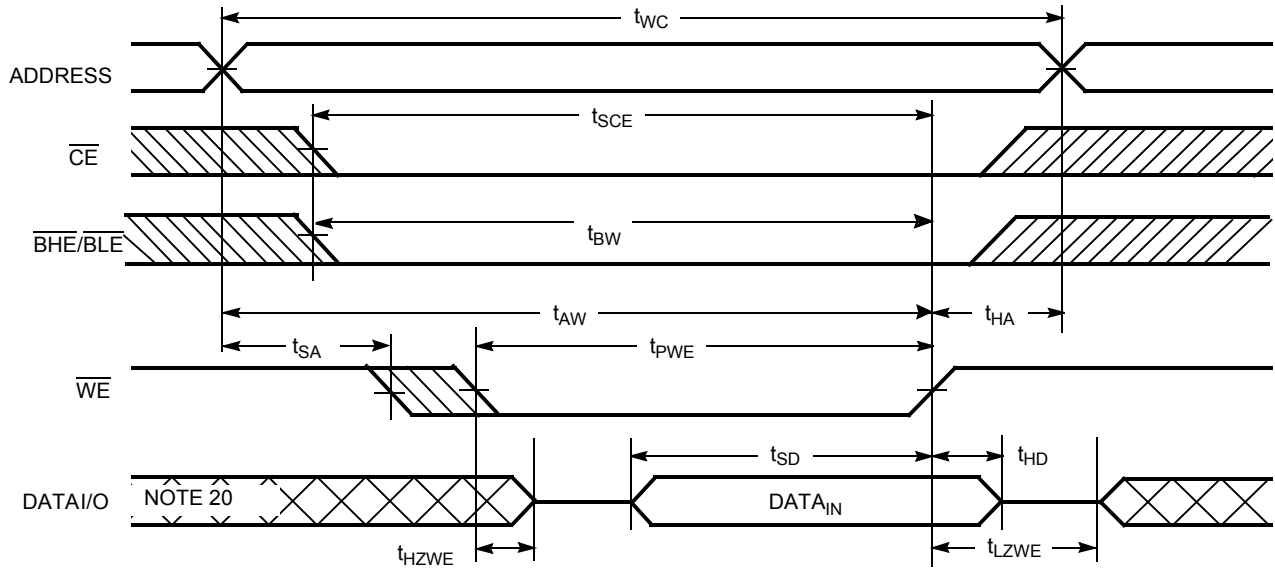


Notes:

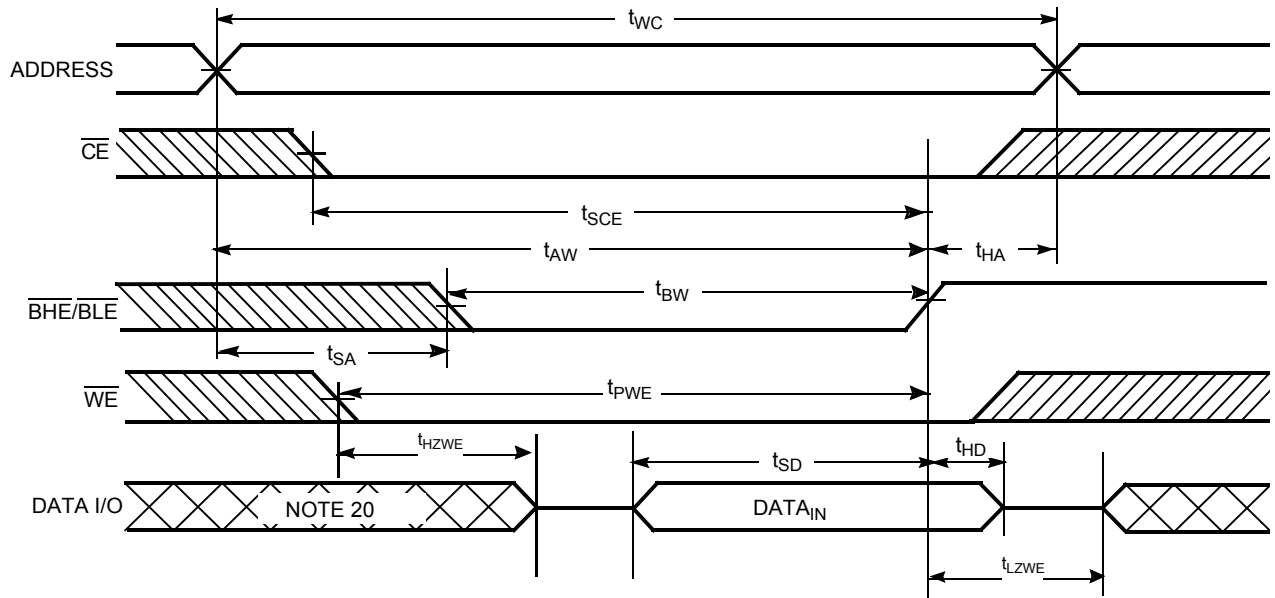
- 18. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 19. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
- 20. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[19]



Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[19]



Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

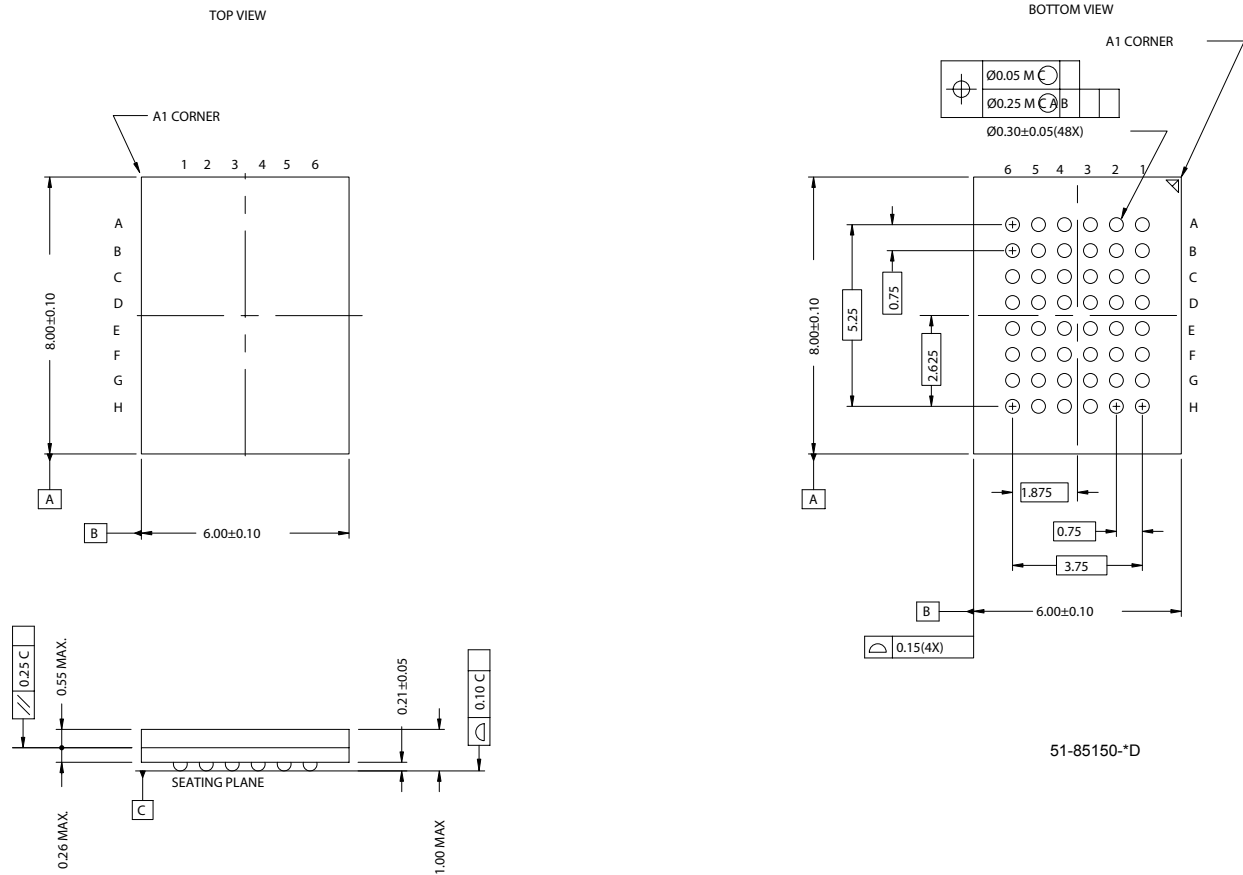
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147EV18LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array Pb-Free	Industrial

Please contact your local Cypress sales representative for availability of other parts

Package Diagram

48-pin VFBGA (6 x 8 x 1 mm) (51-85150)





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Document History Page

Document Title: CY62147EV18 MoBL2™ 4-Mbit (256K x 16) Static RAM				
Document Number: 38-05441				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201580	01/08/04	AJU	New Data Sheet
*A	247009	See ECN	SYT	<p>Changed from Advance Information to Preliminary</p> <p>Moved Product Portfolio to Page 2</p> <p>Changed V_{CCMax} from 2.20 to 2.25 V</p> <p>Changed V_{CC} stabilization time in footnote #8 from 100 μs to 200 μs</p> <p>Removed Footnote #15 (t_{LZBE}) from Previous Revision</p> <p>Changed I_{CCDR} from 2.0 μA to 2.5 μA</p> <p>Changed typo in Data Retention Characteristics (t_R) from 100 μs to t_{RC} ns</p> <p>Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin</p> <p>Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin</p> <p>Changed t_{SCE} and t_{BW} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin</p> <p>Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin</p> <p>Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin</p> <p>Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin</p> <p>Changed Ordering Information to include Pb-Free Packages</p>
*B	414820	See ECN	ZSD	<p>Changed from Preliminary to Final</p> <p>Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed 35ns Speed Bin</p> <p>Removed "L" version of CY62147EV18</p> <p>Changed ball E3 from DNU to NC</p> <p>Changed I_{CC} (Typ) value from 1.5 mA to 2 mA at $f=1$ MHz</p> <p>Changed I_{CC} (Max) value from 2 mA to 2.5 mA at $f=1$ MHz</p> <p>Changed I_{CC} (Typ) value from 12 mA to 15 mA at $f=f_{max}$</p> <p>Changed I_{SB1} and I_{SB2} Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA.</p> <p>Extended undershoot limit to -2V in footnote #5</p> <p>Changed I_{CCDR} Max. from 2.5 μA to 3 μA.</p> <p>Added I_{CCDR} typical value.</p> <p>Changed t_{LZOE} from 3 ns to 5 ns</p> <p>Changed t_{LZCE}, t_{LZBE} and t_{LZWE} from 6 ns to 10 ns</p> <p>Changed t_{HZCE} from 22 ns to 18 ns</p> <p>Changed t_{PWE} from 30 ns to 35 ns.</p> <p>Changed t_{SD} from 22 ns to 25 ns.</p> <p>Updated the package diagram 48-pin VFBGA from *B to *D</p> <p>Updated the ordering information table and replaced Package Name column with Package Diagram</p>

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