



**THE DATASHEET OF  
CAV93C86YE-GT3**



# EEPROM Serial 16-Kb Microwire - Automotive Grade 1

## CAV93C86



SOIC-8  
V SUFFIX  
CASE 751BD



TSSOP-8  
Y SUFFIX  
CASE 948AL

### Description

The CAV93C86 is an EEPROM Serial 16-Kb Microwire Automotive Grade 1 device, which is configured as either registers of 16 bits (ORG pin at  $V_{CC}$ ) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAV93C86 is manufactured using onsemi's advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin SOIC and TSSOP packages.

### Features

- Automotive AEC-Q100 Grade 1 ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) Qualified
- High Speed Operation: 2 MHz
- Low Power CMOS Technology
- 2.5 V to 5.5 V Operation
- Selectable x8 or x16 Memory Organization
- Self-timed Write Cycle with Auto-clear
- Hardware and Software Write Protection
- Power-up Inadvertent Write Protection
- Sequential Read
- Program Enable (PE) Pin
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-pin SOIC and TSSOP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free, and RoHS Compliant

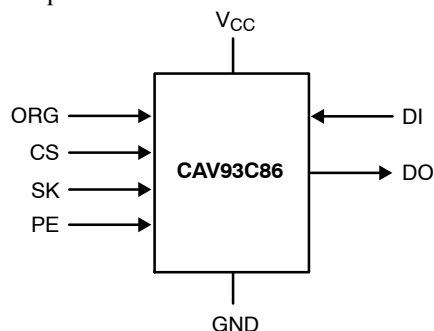
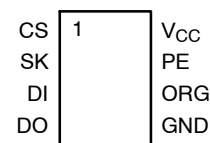


Figure 1. Functional Symbol

**Note:** When the ORG pin is connected to  $V_{CC}$ , the x16 organization is selected. When it is connected to ground, the x8 pin is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the x16 organization.

### PIN CONFIGURATION



SOIC (V) and TSSOP (Y)

### PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
$V_{CC}$	Power Supply
GND	Ground
ORG	Memory Organization
PE	Program Enable

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The DC input voltage on any pin should not be lower than  $-0.5\text{ V}$  or higher than  $V_{CC} + 0.5\text{ V}$ . During transitions, the voltage on any pin may undershoot to no less than  $-1.5\text{ V}$  or overshoot to no more than  $V_{CC} + 1.5\text{ V}$ , for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

Symbol	Parameter	Min	Units
$N_{END}$ (Note 3)	Endurance	1,000,000	Program / Erase Cycles
$T_{DR}$	Data Retention	100	Years

- These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- Block Mode,  $V_{CC} = 5\text{ V}$ ,  $25^\circ\text{C}$ .

**Table 3. D.C. OPERATING CHARACTERISTICS**

( $V_{CC} = +2.5\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
$I_{CC1}$	Supply Current (Write)	Write, $V_{CC} = 5.0\text{ V}$		2	mA
$I_{CC2}$	Supply Current (Read)	Read, DO open, $f_{SK} = 2\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$		500	$\mu\text{A}$
$I_{SB1}$	Standby Current (x8 Mode)	$V_{IN} = \text{GND or } V_{CC}$ $CS = \text{GND, ORG} = \text{GND}$		5	$\mu\text{A}$
$I_{SB2}$	Standby Current (x16 Mode)	$V_{IN} = \text{GND or } V_{CC}$ $CS = \text{GND, ORG} = \text{Float or } V_{CC}$		3	$\mu\text{A}$
$I_{LI}$	Input Leakage Current	$V_{IN} = \text{GND to } V_{CC}$		2	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{OUT} = \text{GND to } V_{CC}$ $CS = \text{GND}$		2	$\mu\text{A}$
$V_{IL1}$	Input Low Voltage	$4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$	-0.1	0.8	V
$V_{IH1}$	Input High Voltage	$4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$	2	$V_{CC} + 1$	V
$V_{IL2}$	Input Low Voltage	$1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$	0	$V_{CC} \times 0.2$	V
$V_{IH2}$	Input High Voltage	$1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} + 1$	V
$V_{OL1}$	Output Low Voltage	$4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$ , $I_{OL} = 2.1\text{ mA}$		0.4	V
$V_{OH1}$	Output High Voltage	$4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$ , $I_{OH} = -400\text{ }\mu\text{A}$	2.4		V
$V_{OL2}$	Output Low Voltage	$1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$ , $I_{OL} = 1\text{ mA}$		0.2	V
$V_{OH2}$	Output High Voltage	$1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 4. PIN CAPACITANCE** (Note 4)

Symbol	Test	Conditions	Min	Typ	Max	Units
$C_{OUT}$	Output Capacitance (DO)	$V_{OUT} = 0\text{ V}$			5	pF
$C_{IN}$	Input Capacitance (CS, SK, DI, ORG)	$V_{IN} = 0\text{ V}$			5	pF

# CAV93C86

**Table 5. POWER-UP TIMING** (Notes 4, 5)

Symbol	Parameter	Max	Units
t <sub>PUR</sub>	Power-up to Read Operation	1	ms
t <sub>PUW</sub>	Power-up to Write Operation	1	ms

**Table 6. A.C. TEST CONDITIONS**

Input Rise and Fall Times	≤ 50 ns		
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V	
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V	
Input Pulse Voltages	0.2 V <sub>CC</sub> to 0.7 V <sub>CC</sub>	1.8 V ≤ V <sub>CC</sub> ≤ 4.5 V	
Timing Reference Voltages	0.5 V <sub>CC</sub>	1.8 V ≤ V <sub>CC</sub> ≤ 4.5 V	
Output Load	Current Source I <sub>OLmax</sub> /I <sub>OHmax</sub> ; CL = 100 pF		

4. These parameters are tested initially and after a design or process change that affects the parameter.
5. t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated.
6. The input levels and timing reference points are shown in the “A.C. Test Conditions” table.

**Table 7. A.C. CHARACTERISTICS**

(V<sub>CC</sub> = +2.5 V to +5.5 V, TA = -40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
t <sub>CSS</sub>	CS Setup Time	50		ns
t <sub>CSH</sub>	CS Hold Time	0		ns
t <sub>DIS</sub>	DI Setup Time	100		ns
t <sub>DIH</sub>	DI Hold Time	100		ns
t <sub>PD1</sub>	Output Delay to 1		0.25	μs
t <sub>PD0</sub>	Output Delay to 0		0.25	μs
t <sub>HZ</sub> (Note 7)	Output Delay to High-Z		100	ns
t <sub>EW</sub>	Program/Erase Pulse Width		5	ms
t <sub>CSMIN</sub>	Minimum CS Low Time	0.25		μs
t <sub>SKHI</sub>	Minimum SK High Time	0.25		μs
t <sub>SKLOW</sub>	Minimum SK Low Time	0.25		μs
t <sub>SV</sub>	Output Delay to Status Valid		0.25	μs
SK <sub>MAX</sub>	Maximum Clock Frequency	DC	2000	kHz

7. This parameter is tested initially and after a design or process change that affects the parameter.

**Table 8. INSTRUCTION SET**

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A10-A0	A9-A0			Read Address AN- A0
ERASE	1	11	A10-A0	A9-A0			Clear Address AN- A0
WRITE	1	01	A10-A0	A9-A0	D7-D0	D15-D0	Write Address AN- A0
EWEN	1	00	11XXXXXXXXXX	11XXXXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXXXX	00XXXXXXXXXX			Write Disable
ERAL	1	00	10XXXXXXXXXX	10XXXXXXXXXX			Clear All Addresses
WRAL	1	00	01XXXXXXXXXX	01XXXXXXXXXX	D7-D0	D15-D0	Write All Addresses

## DEVICE OPERATION

The CAV93C86 is a 16,384-bit nonvolatile memory intended for use with industry standard microprocessors. The CAV93C86 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 13-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 14-bit instructions control the reading, writing and erase operations of the device. The CAV93C86 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 10-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations).

**Note:** *The Write, Erase, Write all and Erase all instructions require PE = 1. If PE is left floating, 93C86 is in Program Enabled mode. For Write Enable and Write Disable instruction PE = don't care.*

## Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAV93C86 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

After the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

## Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C86 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

# CAV93C86

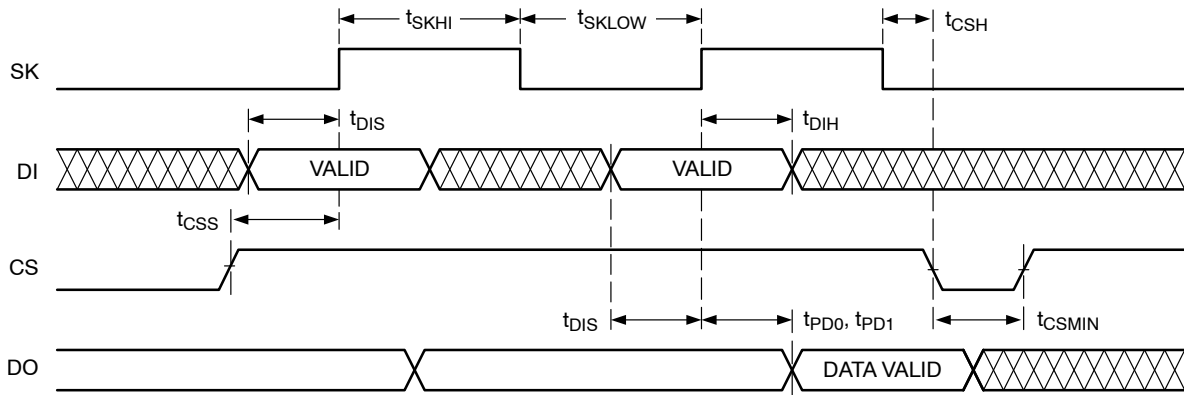


Figure 2. Synchronous Data Timing

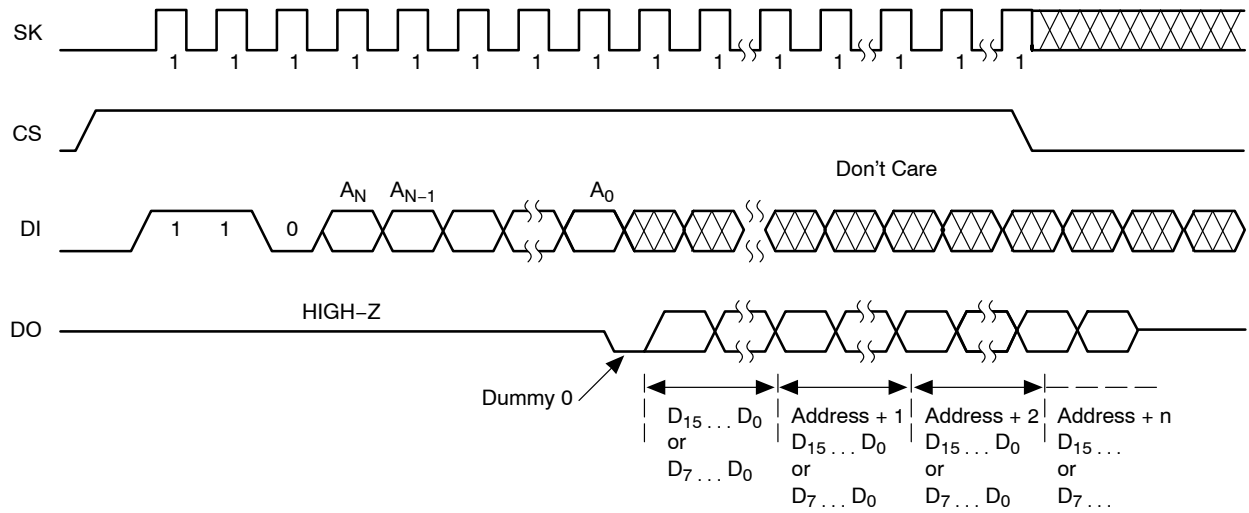


Figure 3. Read Instruction Timing

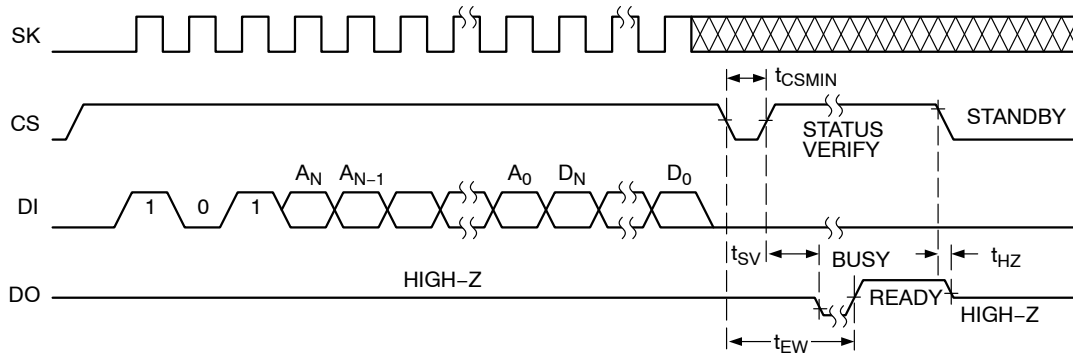


Figure 4. Write Instruction Timing

# CAV93C86

## Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C86 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

## Erase/Write Enable and Disable

The CAV93C86 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAV93C86 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

## Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C86 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

## Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAV93C86 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

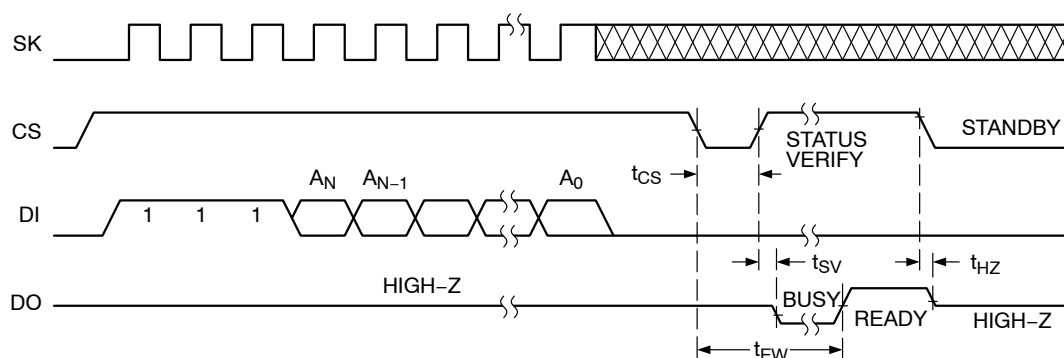


Figure 5. Erase Instruction Timing

## ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAV93C86VE-GT3	93C86D	SOIC-8, JEDEC	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAV93C86YE-GT3	M86D	TSSOP-8	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. All packages are RoHS-compliant (Lead-free, Halogen-free).

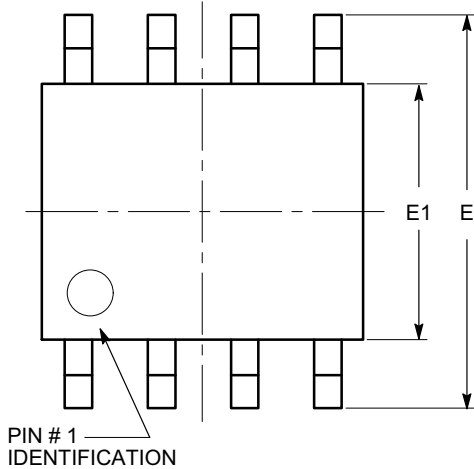
9. The standard lead finish is NiPdAu.

10. For additional package and temperature options, please contact your nearest onsemi Sales office.

11. For detailed information and a breakdown of device nomenclature and numbering systems, please see the onsemi Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)

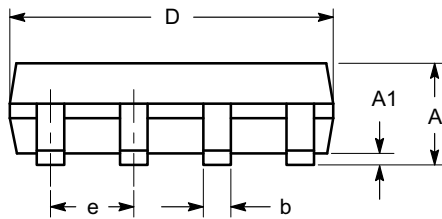
**SOIC-8, 150 mils**  
CASE 751BD  
ISSUE O

DATE 19 DEC 2008

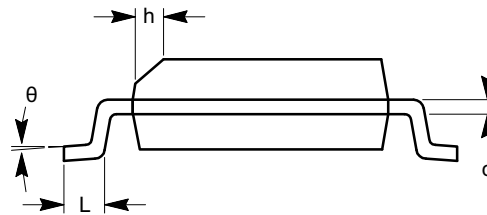


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



**SIDE VIEW**



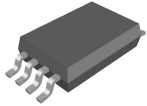
**END VIEW**

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

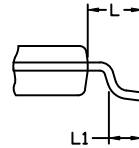
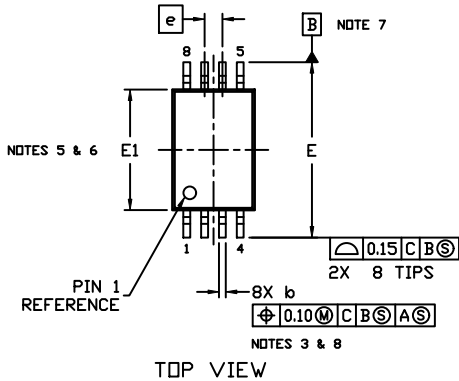
<b>DOCUMENT NUMBER:</b>	<b>98AON34272E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8, 150 MILS</b>	<b>PAGE 1 OF 1</b>

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



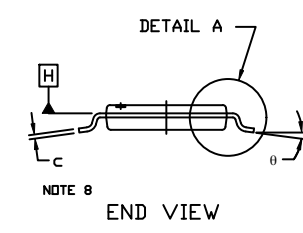
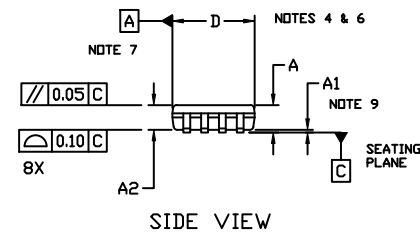
TSSOP8, 4.4x3.0, 0.65P  
CASE 948AL  
ISSUE A

DATE 20 MAY 2022



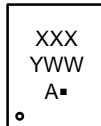
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



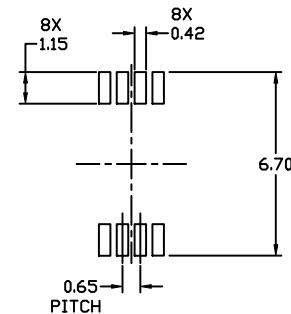
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code
- Y = Year
- WW = Work Week
- A = Assembly Location
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT\*

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

DOCUMENT NUMBER:	98AON34428E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP8, 4.4X3.0, 0.65P	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View CAV93C86YE-GT3 on WIN SOURCE](#)
- ⊖ [ON Semiconductor Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management