THE DATASHEET OF

PI6CFGL402BLIEX

PI6CFGL402B

Low Power PCIe 3.0 Clock Generator with 4 HCSL Outputs

Features

- PCIe® 3.0, 2.0 and 1.0 complaint
- LVDS compatible outputs
- Supply voltage of 3.3V ±5%
- 25MHz crystal or clock input frequency
- Low power consumption with independent output power supply 1.05V to 3.3V
- Jitter 40ps cycle-to-cycle (typ)
- Spread of -0.5%, -1.0%, -1.5%, and no spread
- Industrial temperature range
- Spread Bypass option available
- Spread and frequency selection via external pins
- Packaging: (Pb-free and Green)

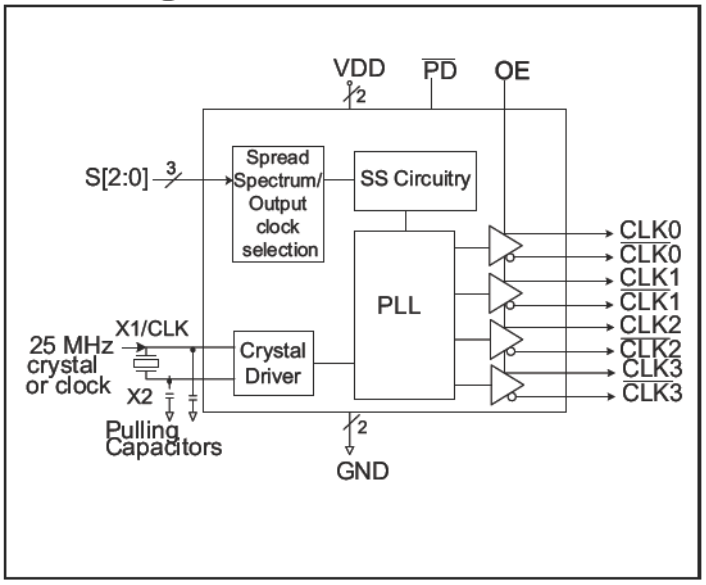
  →20-pin, 173-mil wide TSSOP

Description

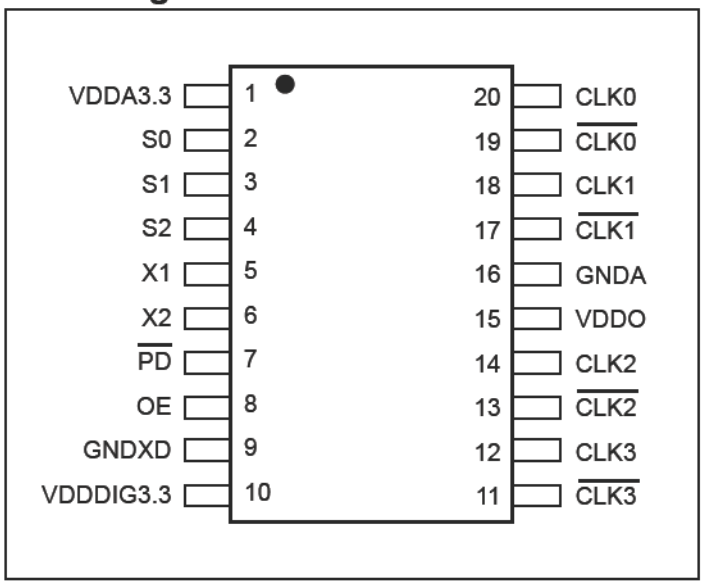
The PI6CFGL402B is a spread spectrum clock generator compliant to PCI Express® 3.0 and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce Electromagnetic Interference (EMI).

The PI6CFGL402B provides four differential (HCSL) or LVDS spread spectrum outputs. The PI6CFGL402B is configured to select spread and clock selection. Using Pericom's patented Phase-Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces four pairs of differential outputs (HCSL) at 100MHz and 200MHz clock frequencies. It also provides spread selection of -0.5%, -1.0%, -1.5%, and no spread.

Block Diagram



Pin Configuration



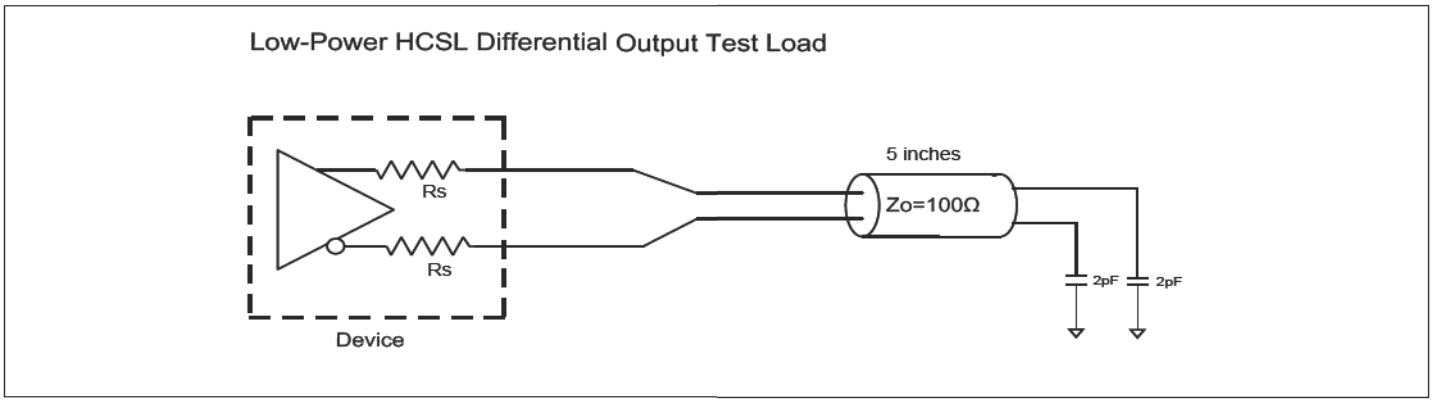
Pin Description

Pin #	Pin Name	I/O Type	Description
1	VDDA3.3	Power	3.3V power for PLL core.
2	S0	Input	Spread Spectrum Select pin #0. See Spread Selection Table. Internal pull-up resistor.
3	S1	Input	Spread Spectrum Select pin #1. See Spread Selection Table. Internal pull-up resistor.
4	S2	Input	Spread Spectrum Select pin #2. See Spread Selection Table. Internal pull-up resistor.
5	X1	Input	Crystal connection.
6	X2	Output	Crystal connection.
7	$\overline{PD}$	Input	Power down. Internal pull-up resistor.
8	OE	Input	Output enable. Tri-states output (High=enable outputs); Low=disable outputs). Internal pull-up resister.
9	GNDXD	Power	Connect to digital circuit ground.
10	VDDDIG3.3	Power	3.3V digital power.
11	$\overline{CLK3}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 3. LOW when output is disabled.
12	CLK3	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 3. LOW when output is disabled.
13	$\overline{CLK2}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 2. LOW when output is disabled.
14	CLK2	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 2. LOW when output is disabled.
15	VDDO	Power	Output power supply, nominal 1.8V, range 1.05V~3.3V.
16	GNDA	Power	Output and Analog circuit ground
17	$\overline{CLK1}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 1. LOW when output is disabled.
18	CLK1	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 1. LOW when output is disabled.
19	$\overline{CLK0}$	Output	Selectable 100/200 MHz Spread Spectrum differential compliment output clock 0. LOW when output is disabled.
20	CLK0	Output	Selectable 100/200 MHz Spread Spectrum differential true output clock 0. LOW when output is disabled.

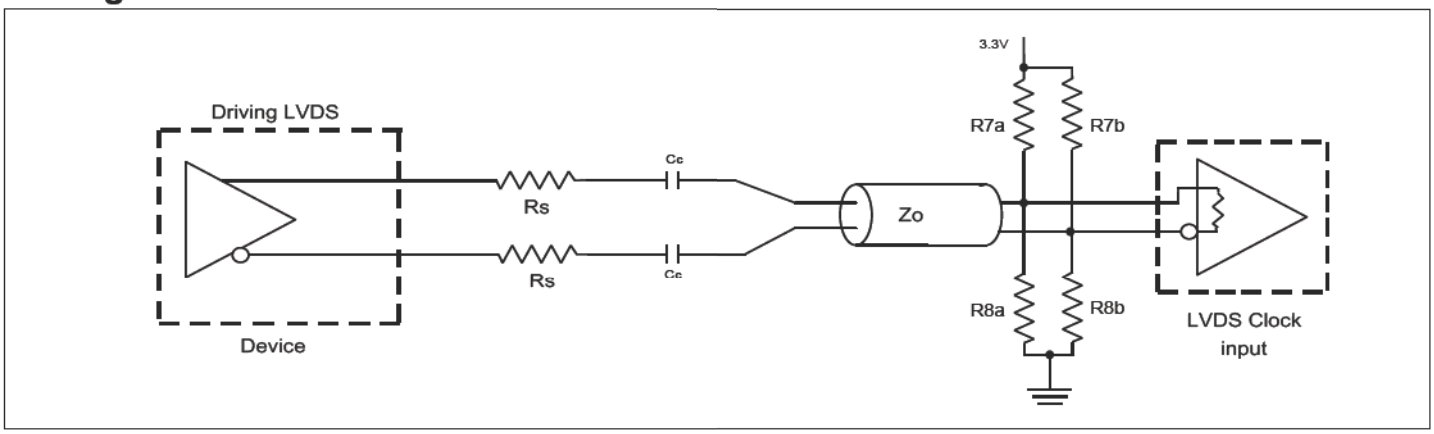
Table 2: Spread Selection Table

S2	S1	S0	Spread %	Spread Type	Output Frequency
0	0	0	-0.5	Down	100
0	0	1	-1.0	Down	100
0	1	0	-1.5	Down	100
0	1	1	No Spread	Not Applicable	100
1	0	0	-0.5	Down	200
1	0	1	-1.0	Down	200
1	1	0	-1.5	Down	200
1	1	1	No Spread	Not Applicable	200

Test Loads



Driving LVDS



Driving LVDS inputs with the PI6CFGL402B

Component	Value	
	Receiver has termination	Receiver does not have termination
R7a, R7b	10K Ω	140 Ω
R8a, R8b	5.6K Ω	75 Ω
Cc	0.1 uF	0.1 uF
Vcm	1.2 volts	1.2 volts

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential.....4.6V
All Inputs and Output.....-0.5V toV_{DD}+0.5V
Ambient Operating Temperature..... -40 to +85°C
Storage Temperature..... –65°C to +150°C
Junction Temperature ..... 125°C
Soldering Temperature.....260°C
ESD Protection (Input) .....2000V(HBM)

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics–Current Consumption

(T_A = -40~85°C; Supply Voltage VDD = 3.3V +/-10%; VDDO = 1.8V +/-10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
I_{DDOP}	Operating Supply Current[1]	Total power consumption, All outputs active @100MHz			60	mA

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions (T_A = -40~85°C; Supply Voltage VDD = 3.3V +/-10%; VDDO = 1.8V +/-10%, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
V_{DDX}	Supply Voltage[1]	Supply voltage for core, analog	3.0	3.3	3.6	V
V_{DDO}	Supply Voltage[1]	Supply voltage outputs	1.65	1.8	2.0	V
V_{IH}	Input High Voltage[1]	OE, S0, S1, SS0, SS1	0.65 V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage[1]	OE, S0, S1, SS0, SS1	-0.3		0.35 V_{DD}	V
I_{IN}	Input Current[1]	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD (exclude XTAL pin)	-5		5	uA
I_{INP}		Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA
Fin	Input Frequency[1]	XTAL, or X1 input	23	25	27	MHz
Lpin	Pin Inductance[1]				7	nH
C_{IN}	Capacitance[1,4]	Logic Inputs, except DIF_IN	1.5		5	pF
C_{INDIF_IN}		DIF_IN differential clock inputs	1.5		2.7	pF
COUT		Output pin capacitance			6	pF

Symbol	Parameters	Condition	Min.	Type	Max.	Units
T_{STAB}	Clk Stabilization[1,2]	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.6	1	ms
f_{MODIN}	Input SS Modulation Frequency[1]	Allowable Frequency (Triangular Modulation)	30	31.500	33	kHz
t_{OE}	Output Enable Time[1]	All outputs			10	µs
t_{OT}	Output Disable Time[1]	All outputs			10	µs
t_{STABLE}	From power-up to V_{DD} = 3.3V[1]	From Power-up V_{DD} = 3.3V		3.0		ms
t_{SPREAD}	Setting period after spread change[1]	Setting period after spread change		3.0		ms

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Control input must be monotonic from 20% to 80% of input swing. Input Frequency Capacitance
3. Time from deassertion until outputs are >200 mV
4. DIF_IN input

Electrical Characteristics–CLK 0.7V Low Power HCSL Outputs (T_A = -40~85°C; Supply Voltage VDD = 3.3V +/-10%; VDDO = 1.8V +/-10%; 100MHz output frequency, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Max.	Units
Trf	Slew rate[1,2,3]		1.1	2	4.5	V/ns
V_{HIGH}	Voltage High[1]	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660		900	mV
V_{LOW}	Voltage Low[1]		-150		150	mV
Vmax	Max Voltage[1]	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV
Vmin	Min Voltage[1]		-300			mV
Vswing	Vswing[1,2]	Scope averaging off	300			mV
Vcross_abs	Crossing Voltage (abs)[1,5]	Scope averaging off	250		550	mV
Δ-Vcross	Crossing Voltage (var)[1,6]	Scope averaging off			140	mV
t_{DC}	Duty Cycle[1]	Measured differentially, PLL Mode	45		55	%
t_{skew}	Skew, Output to Output[1]	V_T = 50%			50	ps
$t_{jcyc-cyc}$	Jitter, Cycle to cycle[1,2]	PLL mode			50	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production.
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.
4. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
5. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
6. The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Phase Jitter Parameters

(T_A = -40~85°C; Supply Voltage VDD = 3.3V +/-10%; VDDO = 1.8V +/-10%; 100MHz output frequency, See Test Loads for Loading Conditions)

Symbol	Parameters	Condition	Min.	Type	Industry Limit	Units
$t_{jphPCIeG1}$	Phase Jitter, PCI Express	PCIe Gen 1[1,2,3,5]		25	86	ps (p-p)
$t_{jphPCIeG2}$		PCIe Gen 2 Low Band 10kHz < f < 1.5MHz[1,2,5]		0.9	3	ps (rms)
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)[1,2,5]		1.6	3.1	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)[1,2,4,5]		0.36	1	ps (rms)

Notes:

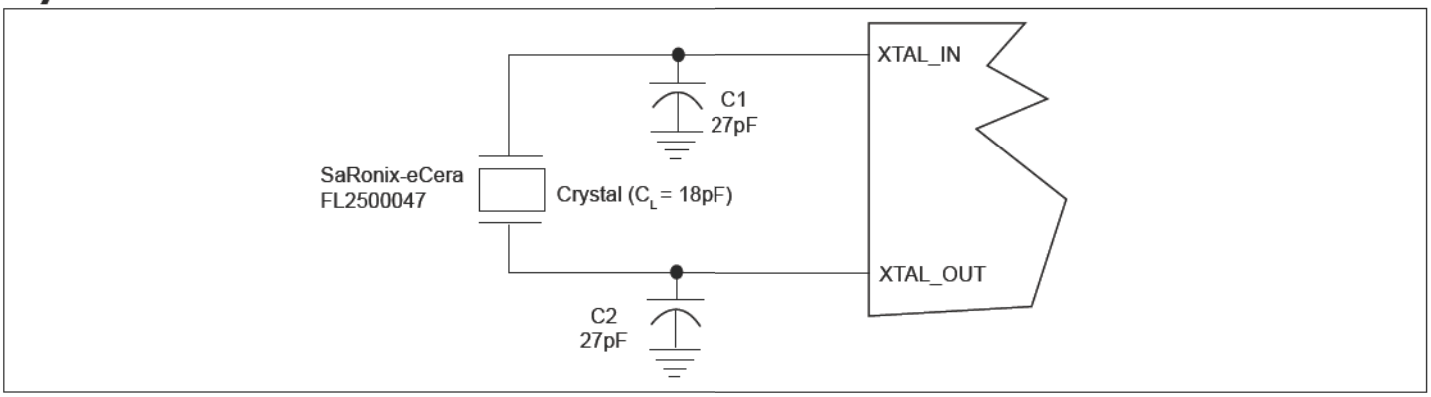
1. Guaranteed by design and characterization, not 100% tested in production.
2. See http://www.pcisig.com for complete specs.
3. Sample size of at least 100k cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.
4. Calculated from Intel-supplied Clock Jitter Tool.
5. Applies to all different outputs.

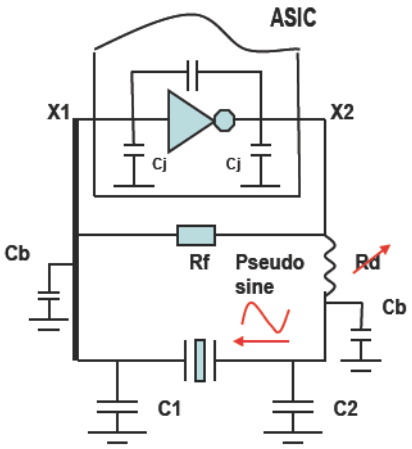
Application Notes

Crystal circuit connection

The following diagram shows crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 27pF, C2= 27pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit





CL= crystal spec. loading cap.

Cj = chip in/output cap. (3~5pF)

Cb = PCB trace/via cap. (2~4pF)

C1,2 = load cap. components

Rd = drive level res. (100Ω)

Final choose/trim C1=C2=2 *CL - (Cb +Cj) for the target +/-ppm
Example: C1=C2=2*(18pF) – (4pF+5pF)=27pF

Recommended Crystal Specification

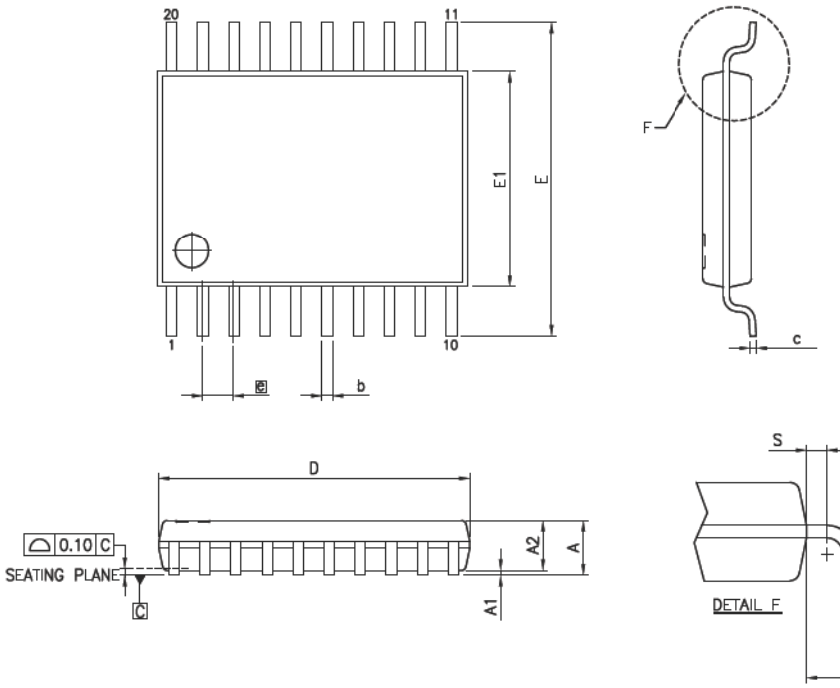
Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

Packaging Mechanical: 20-pin TSSOP (L)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E		6.40 BSC	
e		0.65 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC MO-153F/AC
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity — DATE: 05/03/12

DESCRIPTION: 20-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1311 — REVISION: F

12-0373

Ordering Information(1-3)

Ordering Code	Package Code	Description
PI6CFGL402BLIE	L	20-Pin, 173mil Wide (TSSOP)

Note:
1. Thermal characteristics and package top marking information can be found at http://www.pericom.com/packaging/
2. E = lead-free and green packaging
3. Adding an X suffix = tape/reel

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