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LPC112x

32-bit ARM Cortex-M0 microcontroller; 64 kB flash and 8 kB SRAM; 12-bit ADC

Rev. 1 — 24 February 2015 Product data sheet

1. General description

The LPC112x are a ARM Cortex-M0 based, low-cost 32-bit MCU family, designed for 8/16-bit microcontroller applications, offering performance, low power, simple instruction set and memory addressing together with reduced code size compared to existing 8/16-bit architectures.

The LPC112x operate at CPU frequencies of up to 50 MHz.

The peripheral complement of the LPC112x includes 64 kB of flash memory, 8 kB of data memory, one Fast-mode Plus I^2C-bus interface, three RS-485/EIA-485 UARTs, two SSP interfaces, four general purpose counter/timers, a 12-bit ADC, and up to 38 general purpose I/O pins.

2. Features and benefits

- System:
  - ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-Maskable Interrupt (NMI) input selectable from several input sources.
  - Serial Wire Debug.
  - System tick timer.
- Memory:
  - 64 kB on-chip flash programming memory.
  - 256 byte page erase function.
  - 8 kB SRAM.
  - In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- Digital peripherals:
  - Up to 38 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors. A configurable open-drain mode is supported.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current output driver (20 mA) on one pin.
  - High-current sink drivers (20 mA) on two I^2C-bus pins in Fast-mode Plus.
  - Four general purpose counter/timers with up to six capture inputs and up to 13 match outputs.
  - Programmable windowed WDT.
- Analog peripherals:
  - 12-bit ADC with 2 Msamples/s and eight channels.

- Serial interfaces:
  - Three UARTs with fractional baud rate generation, internal FIFO, and RS-485 support. One UART with modem control.
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call.
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Available as LQFP48 package.

3. Applications

- eMetering
- Alarm systems
- Lighting
- White goods

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1125JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1124JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

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4.1 Ordering options

Table 2. Ordering options

Type number	Flash	Total SRAM	UART RS-485	I^2C/ Fast+	SSP	ADC channels	GPIO	Package
LPC1125JBD48/303	64 kB	8 kB	3	1	2	8	38	LQFP48
LPC1124JBD48/303	32 kB	8 kB	3	1	2	8	38	LQFP48

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5. Block diagram

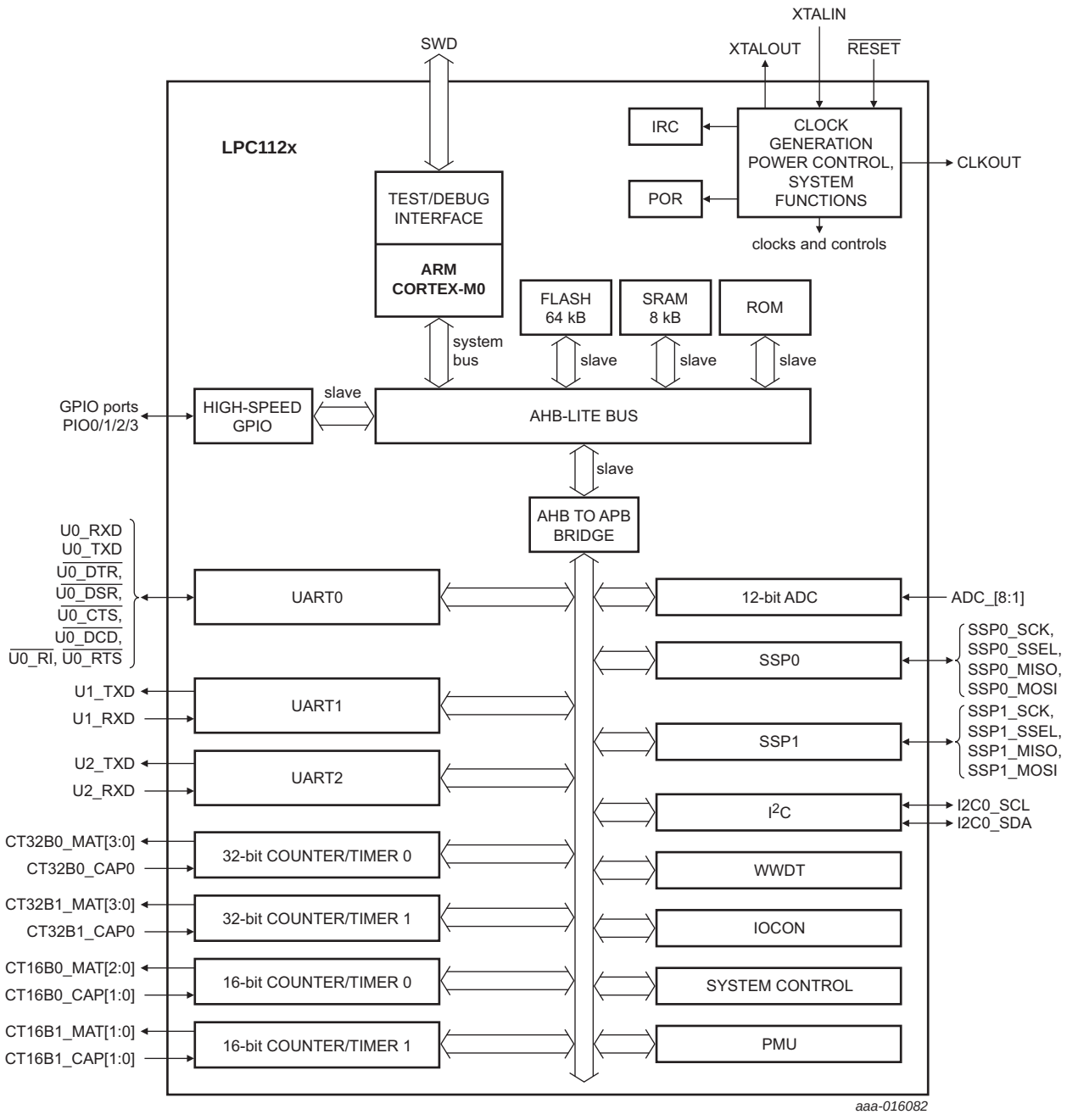

Fig 1. LPC112x block diagram

6. Pinning information

6.1 Pinning

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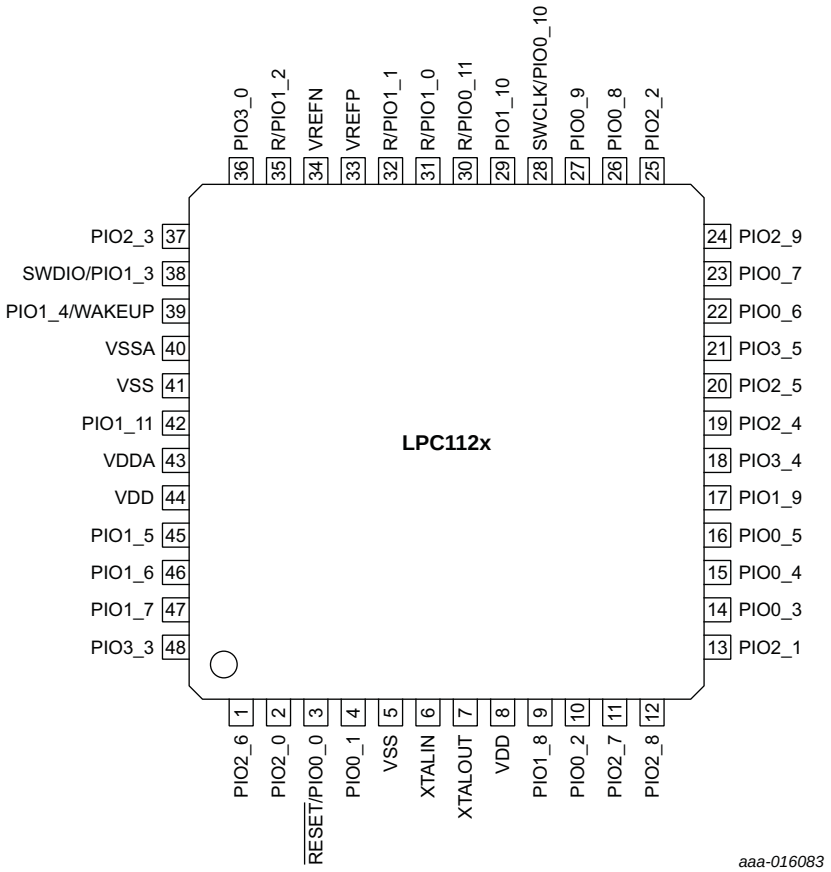

Fig 2. LQFP48 package

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6.2 Pin description

Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
$\overline{\text{RESET}}$/PIO0_0	3	[8]	I; PU	yes	I	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
					I/O	**PIO0_0 —** General purpose port 0 input/output 0.
PIO0_1	4	[6]	I; PU	yes	I/O	**PIO0_1 —** General purpose port 0 input/output 1. A LOW level on this pin during reset starts the ISP command handler.
					O	**CLKOUT —** Clock output.
					O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2	10	[6]	I; PU	yes	I/O	**PIO0_2 —** General purpose port 0 input/output 2.
					I/O	**SSP0_SSEL —** Slave select for SSP0.
					I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
					I	**ADC_PIN_TRIG0 —** ADC pin trigger input 0.
PIO0_3	14	[6]	I; PU	yes	I/O	**PIO0_3 —** General purpose port 0 input/output 3.
					-	**R —** Reserved.
					-	**R —** Reserved.
					I	**U2_RXD —** Receiver input for UART2.
PIO0_4	15		I; IA	yes	I/O	**PIO0_4 —** General purpose port 0 input/output 4.
					I/O	**I2C0_SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5	16	[7]	I; IA	yes	I/O	**PIO0_5 —** General purpose port 0 input/output 5.
					I/O	**I2C0_SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6	22	[6]	I; PU	yes	I/O	**PIO0_6 —** General purpose port 0 input/output 6.
					-	**R —** Reserved.
					I/O	**SSP0_SCK —** Serial clock for SSP0.
					O	**U1_TXD —** Transmitter output for UART1.
PIO0_7	23	[5]	I; PU	yes	I/O	**PIO0_7 —** General purpose port 0 input/output 7. High-current output driver.
					I	**$\overline{\text{U0_CTS}}$ —** Clear To Send input for UART0.
					I	**ADC_PIN_TRIG1 —** ADC pin trigger input 1.
					I	**U1_RXD —** Receiver input for UART1.
PIO0_8	26	[6]	I; PU	yes	I/O	**PIO0_8 —** General purpose port 0 input/output 8.
					I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	**R —** Reserved.
					I	**ADC_PIN_TRIG2 —** ADC pin trigger input 2.

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Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
PIO0_9	27	[6]	I; PU	yes	I/O	**PIO0_9 —** General purpose port 0 input/output 9.
					I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
					O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	**R —** Reserved.
					I	**ADC_PIN_TRIG3 —** ADC pin trigger input 3.
SWCLK/PIO0_10	28	[6]	I; PU	yes	I/O	**SWCLK —** Serial wire clock.
					I/O	**PIO0_10 —** General purpose port 0 input/output 10.
					I/O	**SSP0_SCK —** Serial clock for SSP0.
					O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11	30	[3]	I; PU	yes	I	**R —** Reserved. Configure for an alternate function in the IOCON block.
					I/O	**PIO0_11 —** General purpose port 0 input/output 11.
					AI	**ADC_7 —** A/D converter, input 7.
					O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
R/PIO1_0	31	[3]	I; PU	yes	I	**R —** Reserved. Configure for an alternate function in the IOCON block.
					I/O	**PIO1_0 —** General purpose port 1 input/output 0.
					AI	**ADC_6 —** A/D converter, input 6.
					I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1	32	[3]	O; PU	no	O	**R —** Reserved. Configure for an alternate function in the IOCON block.
					I/O	**PIO1_1 —** General purpose port 1 input/output 1.
					AI	**ADC_5 —** A/D converter, input 5.
					O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2	35	[3]	I; PU	no	I	**R —** Reserved. Configure for an alternate function in the IOCON block.
					I/O	**PIO1_2 —** General purpose port 1 input/output 2.
					AI	**ADC_4 —** A/D converter, input 4.
					O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3	38	[3]	I; PU	no	I/O	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin.
					I/O	**PIO1_3 —** General purpose port 1 input/output 3.
					AI	**ADC_3 —** A/D converter, input 3.
					O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.

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Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
PIO1_4/ WAKEUP	39	[4]	I; PU	no	IO	**PIO1_4 —** General purpose port 1 input/output 4. General-purpose digital input/output pin. This pin also serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
					AI	**ADC_2 —** A/D converter, input 2.
					O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5	45	[6]	I; PU	no	I/O	**PIO1_5 —** General purpose port 1 input/output 5.
					O	**$\overline{\text{U0_RTS}}$ —** Request To Send output for UART0.
					I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6	46	[6]	I; PU	no	I/O	**PIO1_6 —** General purpose port 1 input/output 6.
					I	**U0_RXD —** Receiver input for UART0. In ISP mode, connect to UART.
					O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7	47	[6]	I; PU	no	I/O	**PIO1_7 —** General purpose port 1 input/output 7.
					O	**U0_TXD —** Transmitter output for UART0. In ISP mode, connect to UART.
					O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8	9	[6]	I; PU	no	I/O	**PIO1_8 —** General purpose port 1 input/output 8.
					I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
					-	**R —** Reserved.
					O	**U2_TXD —** Transmitter output for U2.
PIO1_9	17	[6]	I; PU	no	I/O	**PIO1_9 —** General purpose port 1 input/output 9.
					O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
					I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.I
PIO1_10	29	[3]	I; PU	no	I/O	**PIO1_10 —** General purpose port 1 input/output 10.
					AI	**ADC_8 —** A/D converter, input 8.
					O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
PIO1_11	42	[3]	I; PU	no	I/O	**PIO1_11 —** General purpose port 1 input/output 11.
					AI	**ADC_1 —** A/D converter, input 1.
					I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
PIO2_0	2	[6]	I; PU	no	IO	**PIO2_0 —** General purpose port 2 input/output 0.
					O	**$\overline{\text{U0_DTR}}$ —** Data Terminal Ready output for UART0.
					I/O	**SSP1_SSEL —** Slave Select for SSP1.
					I	**ADC_PIN_TRIG4 —** ADC pin trigger input 4.
PIO2_1	13	[6]	I; PU	no	I/O	**PIO2_1 —** General purpose port 2 input/output 1.
					I	**$\overline{\text{U0_DSR}}$ —** Data Set Ready input for UART0.
					I/O	**SSP1_SCK —** Serial clock for SSP1.

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Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
PIO2_2	25	[6]	I; PU	no	I/O	**PIO2_2 —** General purpose port 2 input/output 2.
					I	**U0_DCD —** Data Carrier Detect input for UART0.
					I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
PIO2_3	37	[6]	I; PU	no	I/O	**PIO2_3 —** General purpose port 2 input/output 3.
					I	**U0_RI —** Ring Indicator input for UART0.
					I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
PIO2_4	19	[6]	I; PU	no	I/O	**PIO2_4 —** General purpose port 2 input/output 4.
					O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					I/O	**SSP1_SSEL —** Slave Select for SSP1.
PIO2_5	20	[6]	I; PU	no	I/O	**PIO2_5 —** General purpose port 2 input/output 5.
					O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO2_6	1	[6]	I; PU	no	I/O	**PIO2_6 —** General purpose port 2 input/output 6.
					O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO2_7	11	[6]	I; PU	no	I/O	**PIO2_7 —** General purpose port 2 input/output 7.
					O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I	**U0_RXD —** Receiver input for UART0.
PIO2_8	12	[6]	I; PU	no	I/O	**PIO2_8 —** General purpose port 2 input/output 8.
					I	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					O	**U0_TXD —** Transmitter output for UART0.
PIO2_9	24	[6]	I; PU	no	I/O	**PIO2_9 —** General purpose port 2 input/output 9.
					I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO2_10	-	[6]	I: PU	no	I/O	**PIO2_10 —** General purpose port 2 input/output 10.
PIO3_0	36	[6]	I; PU	no	I/O	**PIO3_0 —** General purpose port 3 input/output 0.
					O	**U0_DTR —** Data Terminal Ready output for UART0.
					O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					O	**U0_TXD —** Transmitter Output for UART0.
PIO3_2	-	[6]	I; PU	no	I/O	**PIO3_2 —** General purpose port 3 input/output 2.
					I	**U0_DCD —** Data Carrier Detect input for UART0.
					O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					I/O	**SSP1_SCK —** Serial clock for SSP1.
PIO3_3	48	[6]	I; PU	no	I/O	**PIO3_3 —** General purpose port 3 input/output 3.
					I	**U0_RI —** Ring Indicator input for UART0.
					I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO3_4	18	[6]	I; PU	no	I/O	**PIO3_4 —** General purpose port 3 input/output 4.
					I	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
					I	**U0_RXD —** Receiver input for UART0.
PIO3_5	21	[6]	I; PU	no	I/O	**PIO3_5 —** General purpose port 3 input/output 5.
					I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					O	**U0_TXD —** Transmitter output for UART0.

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Table 3. Pin description

Symbol	LQFP48		Reset state [1]	Start logic wake-up pin	Type	Description
XTALIN	6	[2]	-	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7	[2]	-	-	-	Output from the oscillator amplifier.
VREFP	33		-	-	-	Positive reference voltage for the ADC.
VREFN	34		-	-	-	Negative reference voltage for the ADC.
V_{DD}	8; 44		-	-	-	3.3 V supply voltage to the internal regulator and the external rail.
V_{DDA}	43		-	-	-	Analog supply voltage.
V_{SSA}	40		-	-	-	Analog ground.
V_{SS}	5; 41		-	-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 27).

[4] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled (see Figure 27). In deep power-down mode, this pin serves as the wake-up pin.

[5] High-current output driver. Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 27).

[6] Standard digital I/O pin. Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 27).

[7] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 28 for the reset pad configuration.

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7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.2 On-chip flash program memory

The LPC112x contain up to 64 kB of on-chip flash memory.

7.3 On-chip SRAM

The LPC112x contain a total of 8 kB on-chip static RAM memory.

7.4 Memory map

The LPC112x incorporate several distinct memory regions, shown in the following figures. Figure 3 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

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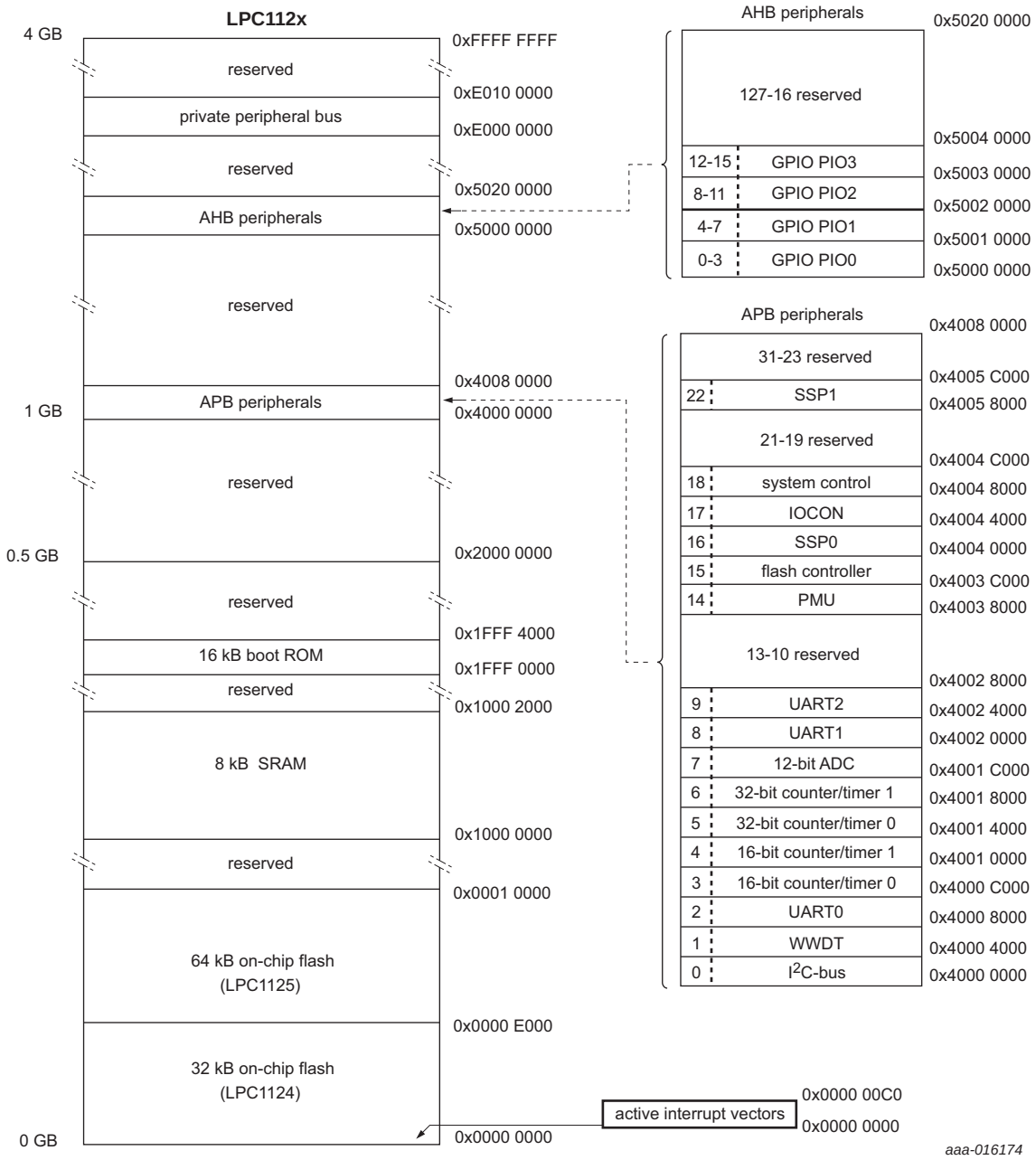

Fig 3. LPC112x memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

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- On the LPC112x, the NVIC supports 32 vectored interrupts including up to 13 inputs to the start logic from individual GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 40 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC112x use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of 38 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset with the exception of the I^2C-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCON block for each GPIO pin (except for pins PIO0_4 and PIO0_5).
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled in the IOCON block.
- Programmable open-drain mode.

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7.8 UART

The LPC112x contain three UARTs.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.9 SSP controller

The LPC112x contains two SSP controllers.

The SSP controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.9.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.

7.10 I^2C-bus serial I/O controller

The LPC112x contains one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the

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capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I^2C-interface is a standard I^2C-bus compliant interface with open-drain pins. The I^2C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- The I^2C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are internal connections to the 16-bit timer match outputs, five external pins, and the ARM TXEV interrupt.

The ADC includes a hardware threshold compare function with zero-crossing detection.

7.11.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of 2 Msamples/s.
- Input multiplexing among 8 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- Burst conversion mode for single or multiple inputs.

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7.12 General purpose external event counter/timers

The LPC112x include two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes up to two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.12.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.13 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.14 Windowed WatchDog Timer

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.14.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

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- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.15 Clocking and power control

7.15.1 Crystal oscillators

The LPC112x include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC112x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 4 for an overview of the LPC112x clock generation.

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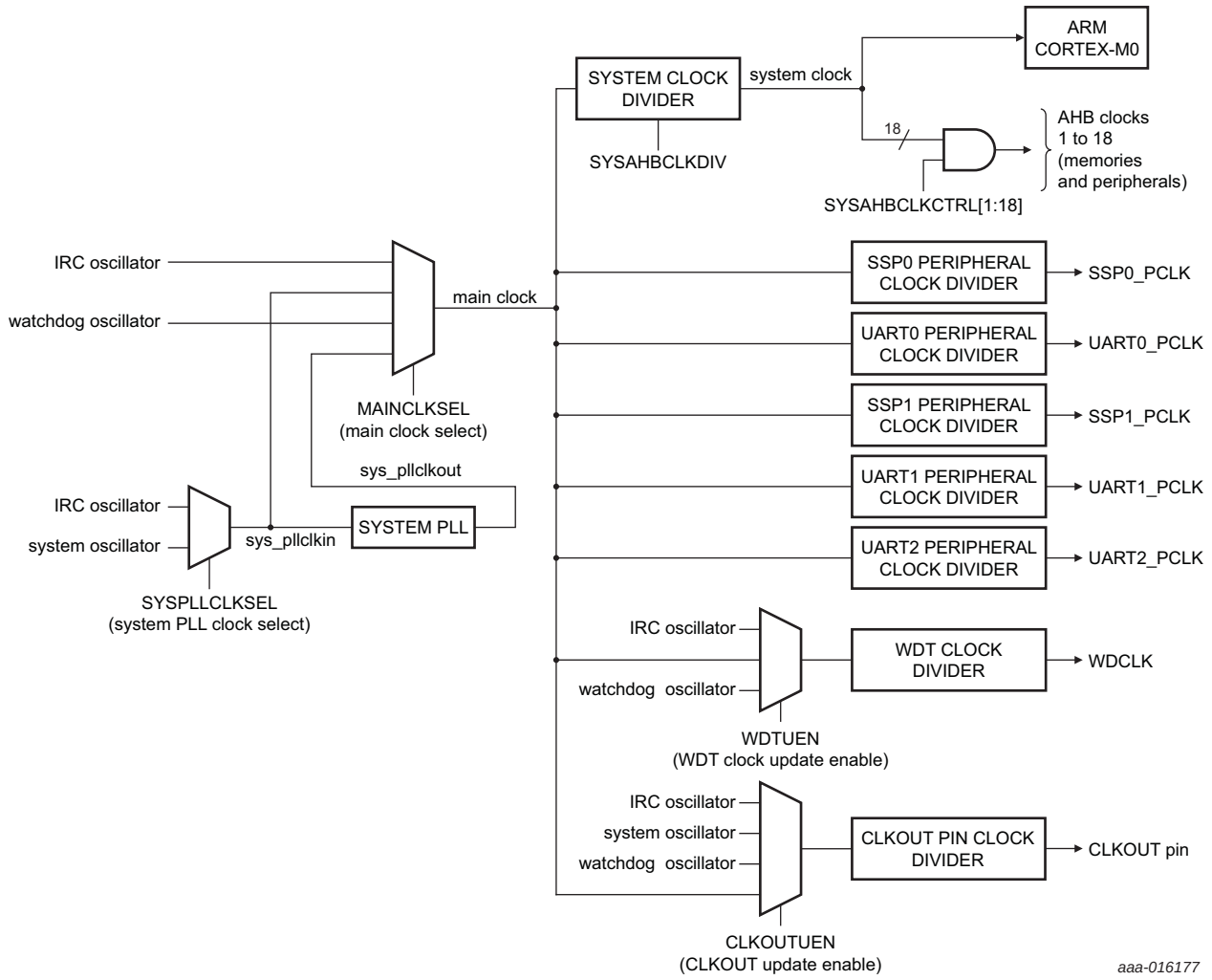

Fig 4. LPC112x clock generation block diagram

7.15.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the LPC112x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.15.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

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7.15.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 %.

7.15.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The PLL output frequency must be lower than 100 MHz. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.15.3 Clock output

The LPC112x features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.15.4 Wake-up process

The LPC112x begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the system oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.15.5 Power control

The LPC112x support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.15.5.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC112x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.

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- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.15.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.15.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 13 pins total serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.15.5.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC112x can wake up from Deep power-down mode via the WAKEUP pin.

A LOW-going pulse as short as 50 ns wakes up the part from Deep power-down mode.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The RESET pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.16 System control

7.16.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

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7.16.2 Reset

Reset has four sources on the LPC112x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.16.3 Brownout detection

The LPC112x includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

7.16.4 Code security (Code Read Protection - CRP)

This feature of the LPC112x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC111x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.

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CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the *LPC112x user manual*.

7.16.5 APB interface

The APB peripherals are located on one APB bus.

7.16.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.16.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.16.1).

7.17 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	–0.5	+4.6	V
V_{DDA}	analog supply voltage		[2]	–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[5][2]	–0.5	+5.5	V
		5 V tolerant open-drain pins PIO0_4 and PIO0_5	[2][4]	–0.5	+5.5	V
V_{IA}	analog input voltage	pin configured as analog input	[2] [3]	–0.5	4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[6]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[7]		+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended, and proper operation is not guaranteed. The conditions for functional operation are specified in Table 6.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 6) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] See Table 6 for maximum operating voltage.

[4] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] Including voltage on outputs in 3-state mode.

[6] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C)
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 5. Thermal resistance value (C/W): ±15 %

LQFP48	
θja	
JEDEC (4.5 in × 4 in)	
0 m/s	82.1
1 m/s	73.7
2.5 m/s	68.2
8-layer (4.5 in × 3 in)	
0 m/s	115.2
1 m/s	94.7
2.5 m/s	86.3
θjc	29.6
θjb	34.2

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10. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
V_{DDA}	analog supply voltage			2.4	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
Power consumption in low-current mode[11]							
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 1 MHz V_{DD} = 3.3 V	[2][3][5][6][7]	-	0.7	-	mA
		system clock = 6 MHz V_{DD} = 3.3 V	[2][3][5][6][7]	-	1.0	-	mA
		system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4][6][7]	-	1.5	-	mA
		system clock = 50 MHz V_{DD} = 3.3 V	[2][3][6][7][8]	-	6.0	-	mA
		Sleep mode; system clock = 12 MHz V_{DD} = 3.3 V	[2][3][4][6][7]	-	0.8	-	mA
		system clock = 50 MHz V_{DD} = 3.3 V	[2][3][4][6][7]	-	2.4	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[2][3][9]	-	1.8	8	µA
		T_{amb} = 105 °C		-	-	65	µA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[2][10]	-	220	900	nA
		T_{amb} = 105 °C		-	-	3.5	µA
Standard port pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[17]	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10[17]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[17]	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD} \geq 1.8$ V	[12][14]	0	-	5.0	V

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Table 6. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −4 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −3 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.8 V ≤ V_{DD} ≤ 3.6 V		−3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 1.8 V ≤ V_{DD} ≤ 3.6 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		−15	−50	−85	µA
		1.8 V ≤ V_{DD} < 2.0 V		−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[17]	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10[17]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[17]	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} ≥ 1.8 V	[12] [14]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V

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Table 6. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OH} = -20\ mA$		$V_{DD} - 0.5$	-	-	V
		$1.8\ V \le V_{DD} < 2.5\ V$; $I_{OH} = -12\ mA$		$V_{DD} - 0.5$	-	-	V
V_{OL}	LOW-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OL} = 4\ mA$		-	-	0.4	V
		$1.8\ V \le V_{DD} < 2.5\ V$; $I_{OL} = 3\ mA$		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.5\ V$; $2.5\ V \le V_{DD} \le 3.6\ V$		20	-	-	mA
		$1.8\ V \le V_{DD} < 2.5\ V$		12	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4\ V$ $2.5\ V \le V_{DD} \le 3.6\ V$		4	-	-	mA
		$1.8\ V \le V_{DD} < 2.5\ V$		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[15]	-	-	50	mA
I_{pd}	pull-down current	$V_I = 5\ V$		10	50	150	µA
I_{pu}	pull-up current	$V_I = 0\ V$ $2.0\ V \le V_{DD} \le 3.6\ V$		−15	−50	−85	µA
		$1.8\ V \le V_{DD} < 2.0\ V$		−10	−50	−85	µA
		$V_{DD} < V_I < 5\ V$		0	0	0	µA
I^2C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4\ V$; I^2C-bus pins configured as standard mode pins $2.5\ V \le V_{DD} \le 3.6\ V$		3.5	-	-	mA
		$1.8\ V \le V_{DD} < 2.5\ V$		3	-	-	
I_{OL}	LOW-level output current	$V_{OL} = 0.4\ V$; I^2C-bus pins configured as Fast-mode Plus pins $2.5\ V \le V_{DD} \le 3.6\ V$		20	-	-	mA
		$1.8\ V \le V_{DD} < 2.5\ V$		16	-	-	

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Table 6. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{LI}	input leakage current	$V_I = V_{DD}$	[16]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

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Table 6. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Pin capacitance							
C_{io}	input/output capacitance	pins configured for analog function		-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)		-	-	2.5	pF
		pins configured as GPIO		-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SSP0/1 disabled in system configuration block.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[10] WAKEUP pin pulled HIGH externally.

[11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[12] Including voltage on outputs in 3-state mode.

[13] V_{DD} supply voltage must be present.

[14] 3-state outputs go into 3-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To V_{SS}.

[17] Characterized on samples. Not tested in production.

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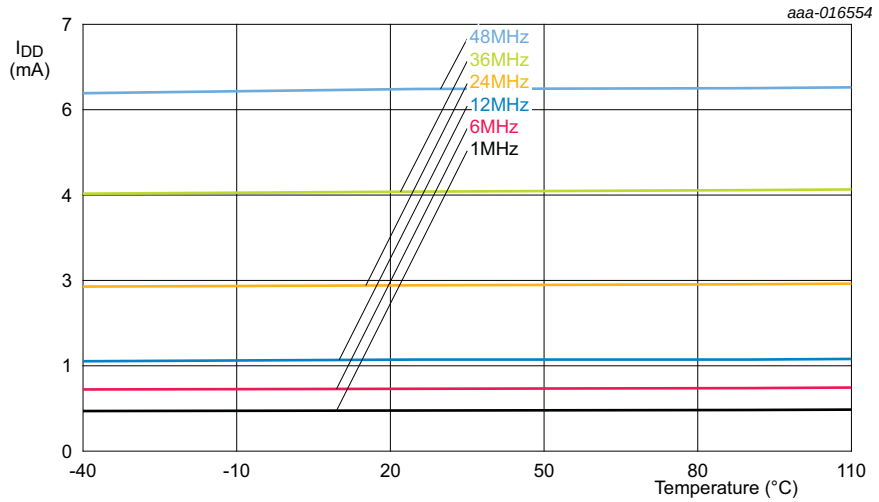
10.1 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC112x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

3 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz - 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 5. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

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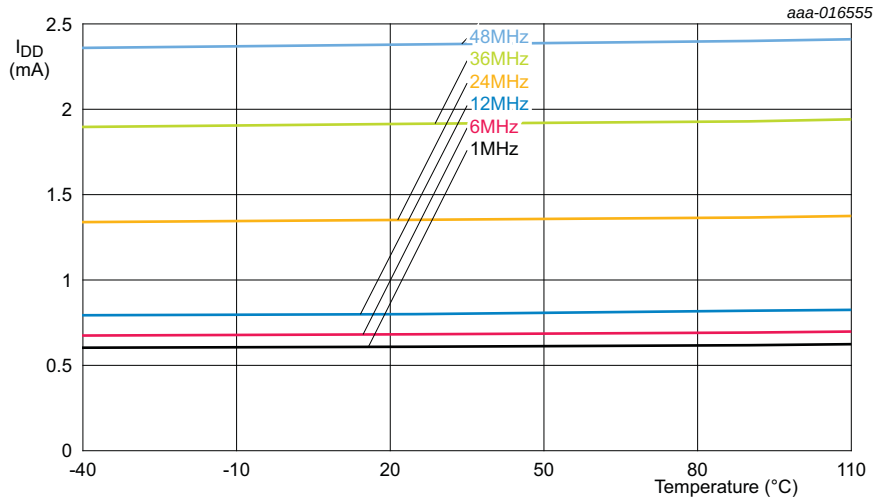

Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

3 MHz - 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz - 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 6. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

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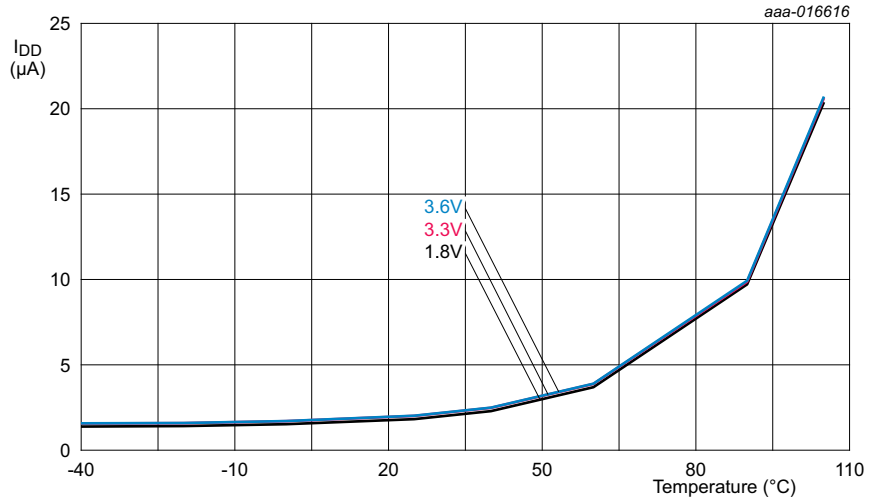

Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 7. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

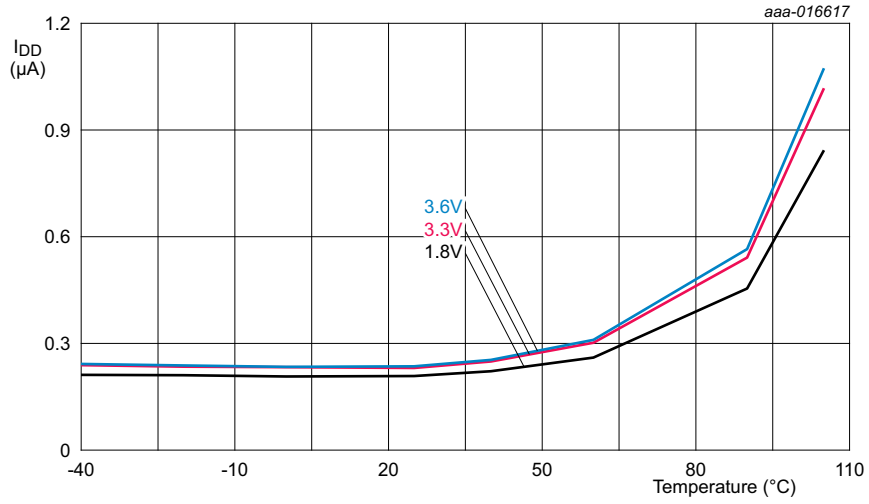

Fig 8. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

10.2 CoreMark data

Remark: All CoreMark data were taken with the Keil uVision v. 5.1.0 tool.

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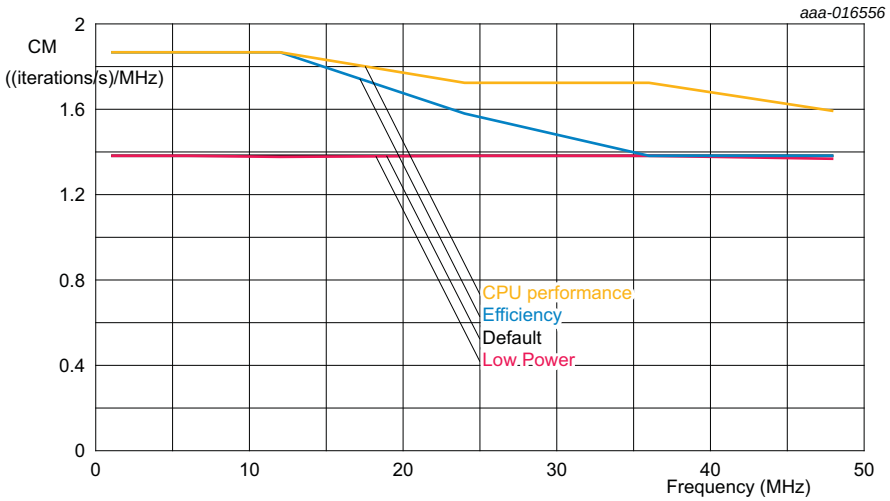
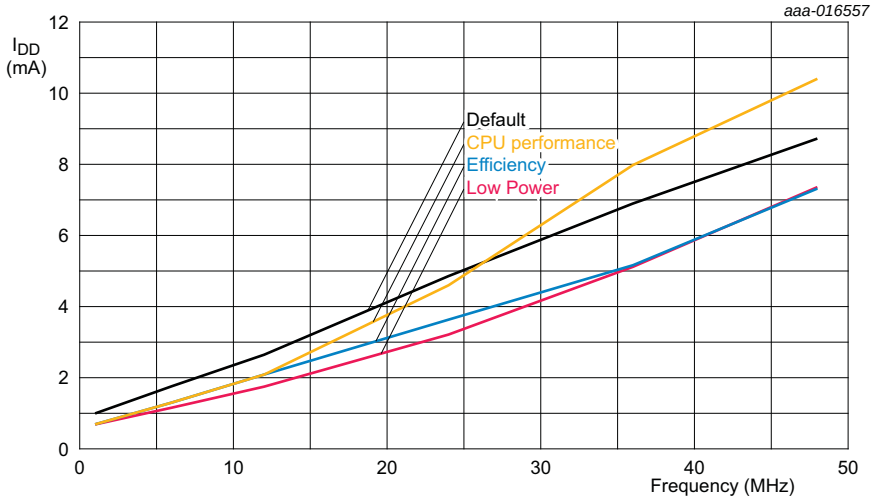


V_{DD} = 3.3 V; T = 25 °C; active mode; typical samples.

Fig 9. CoreMark score for different Power API modes



V_{DD} = 3.3 V; T = 25 °C; active mode; typical samples. System oscillator enabled; main clock derived from external clock signal; PLL and SYSAHBCLKDIV enabled for frequencies > 20 MHz.

Fig 10. CoreMark current consumption for different power modes using external clock

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10.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 7. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.212	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.1928	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.002	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.0686	-	
ADC	-	0.0532	0.2074	
CLKOUT	-	0.0104	0.0392	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.0266	0.1028	
CT16B1	-	0.025	0.0956	
CT32B0	-	0.026	0.0998	
CT32B1	-	0.0246	0.0956	
GPIO	-	0.2252	0.8754	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.0324	0.1262	
I2C	-	0.0384	0.1484	
ROM	-	0.017	0.0658	
SSP0	-	0.0482	0.187	
SSP1	-	0.048	0.1862	
UART0	-	0.0862	0.334	
UART1	-	0.0836	0.3236	
UART2	-	0.0818	0.3176	
WWDT	-	0.039	0.1964	Main clock selected as clock source for the WDT.

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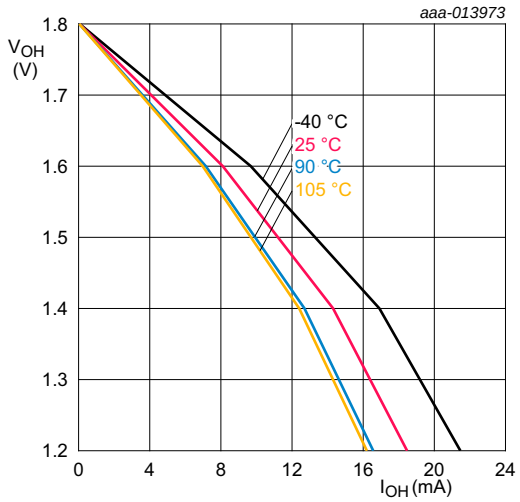
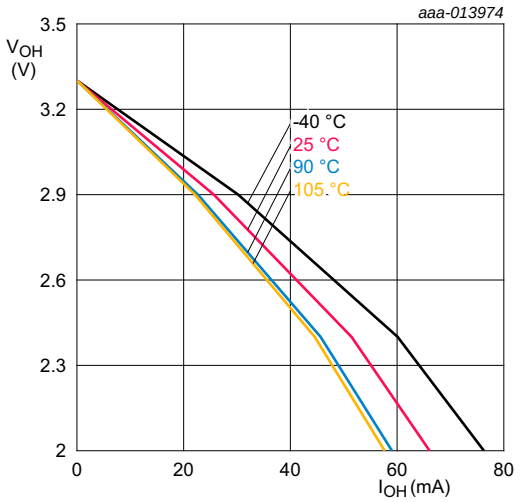
10.4 Electrical pin characteristics

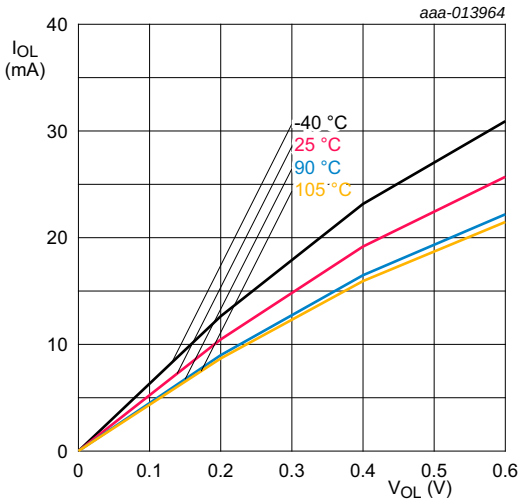


Conditions: V_{DD} = 1.8 V; on pin PIO0_7.

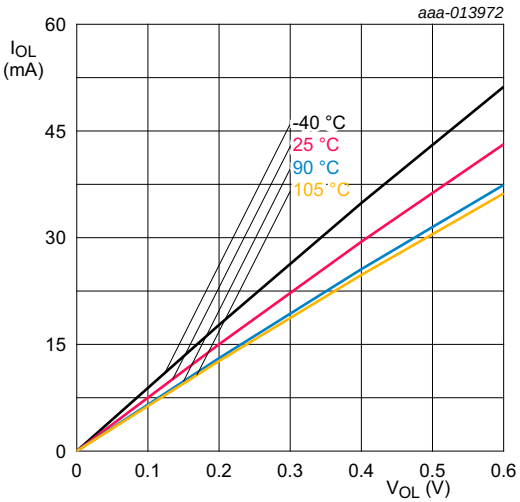


Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 11. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 1.8 V; on pins PIO0_4 and PIO0_5.



Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 12. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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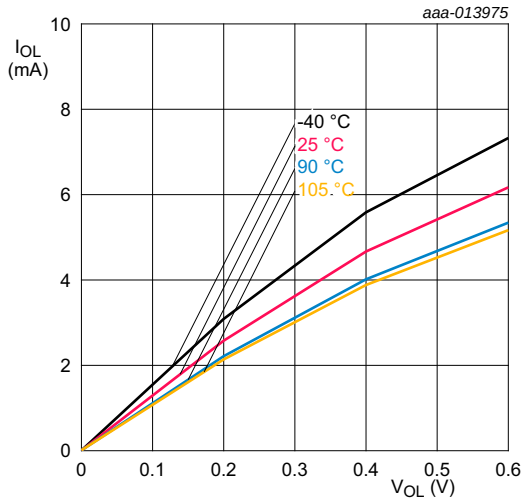
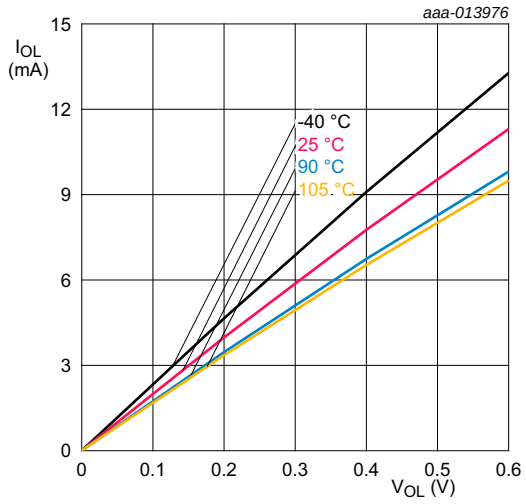
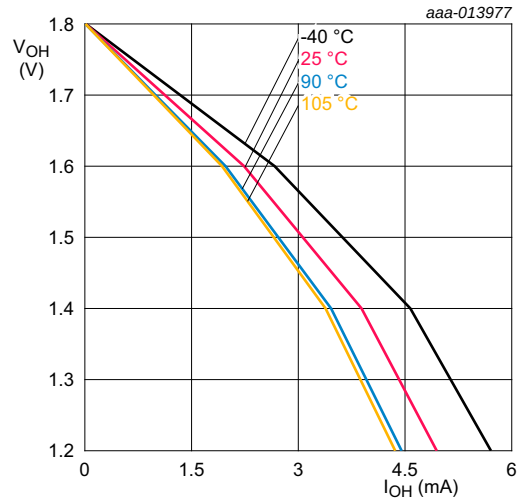


Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_7.

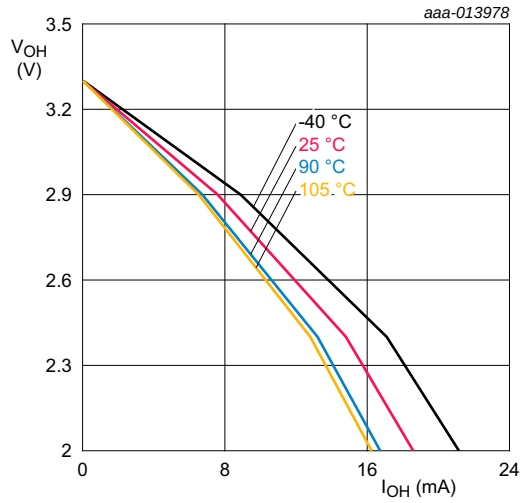


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_7.

Fig 13. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 14. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

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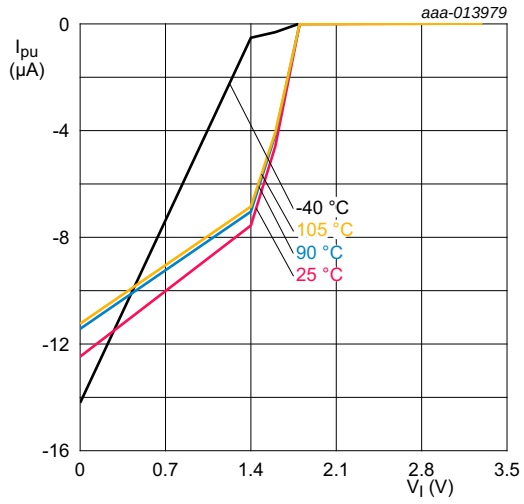
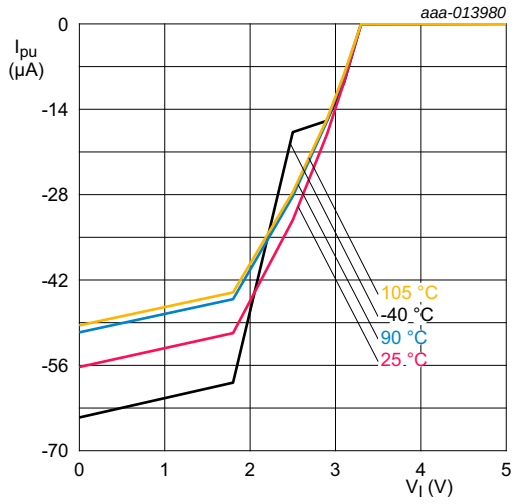
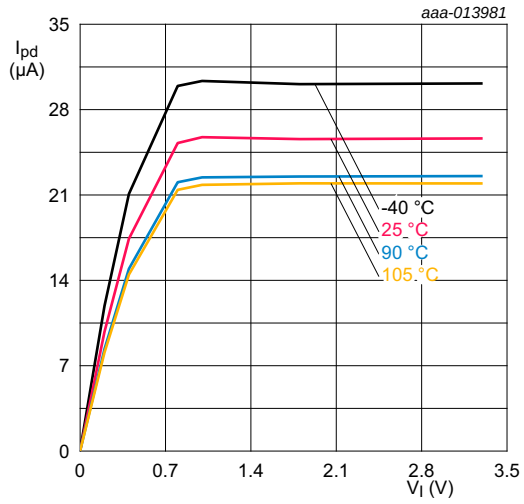


Conditions: V_{DD} = 1.8 V; standard port pins.

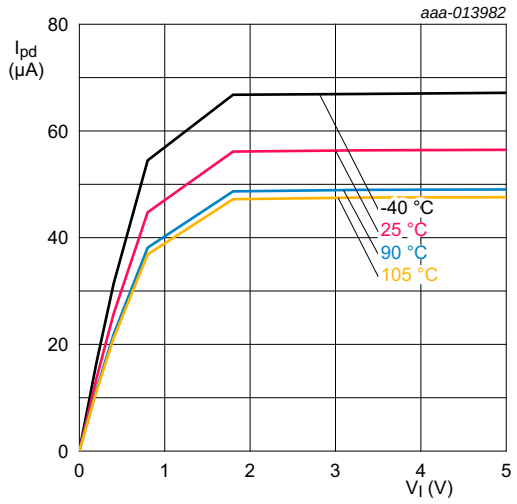


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 15. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 16. Typical pull-down current I_{PD} versus input voltage V_I

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11. Dynamic characteristics

11.1 Flash memory

Table 8. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

11.2 External clock

Table 9. Dynamic characteristic: external clock

T_{amb} = −40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency	1	-	25	MHz
$T_{cy(clk)}$	clock cycle time	40	-	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

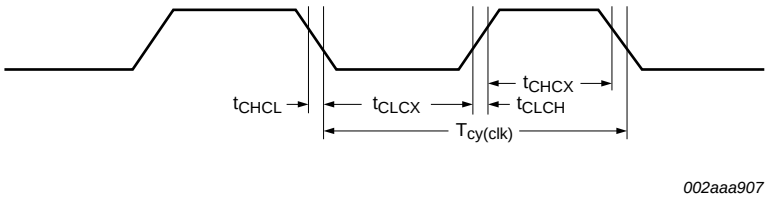

Fig 17. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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11.3 Internal oscillators

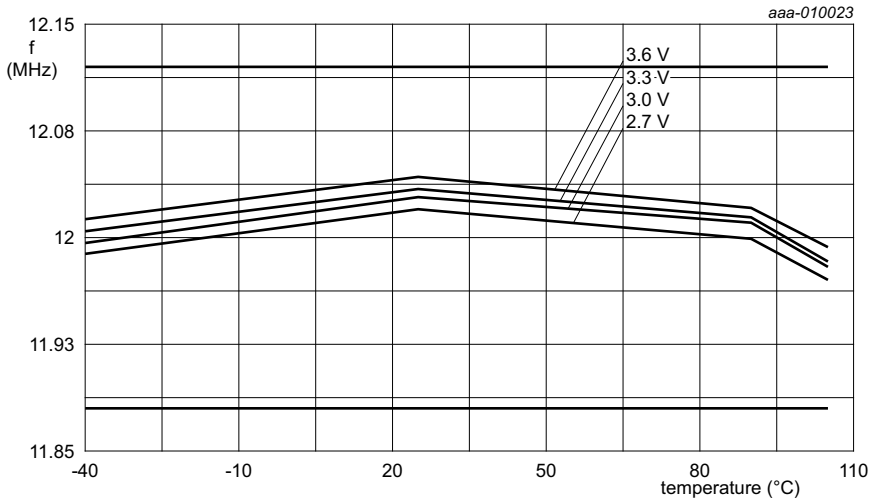
Table 10. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1 %	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2.5 %	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 18. Typical Internal RC oscillator frequency versus temperature

Table 11. Dynamic characteristics: WatchDog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; [2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register [2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the *LPC112x user manual.*

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11.4 I/O pins

Table 12. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

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11.5 I²C-bus

Table 13. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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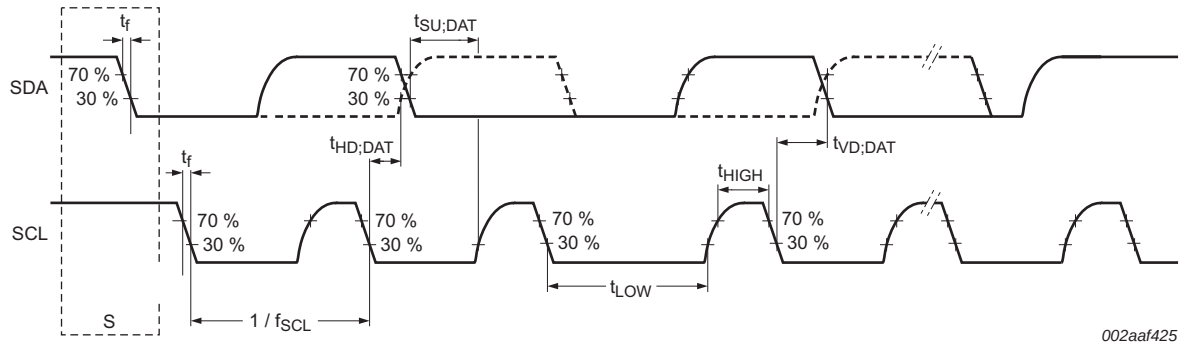

Fig 19. I²C-bus pins clock timing

11.6 SSP interfaces

Table 14. Dynamic characteristics of SSP pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40			ns
t_{DS}	data set-up time	in SPI mode 2.4 V ≤ V_{DD} ≤ 3.6 V	[2]	20	-	-	ns
		2.0 V ≤ V_{DD} < 2.4 V	[2]	25			ns
		1.8 V ≤ V_{DD} < 2.0 V	[2]	29	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SSP slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	3 × $T_{cy(PCLK)}$ + 4	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	3 × $T_{cy(PCLK)}$ + 11	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	2 × $T_{cy(PCLK)}$ + 5	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SSP bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] T_{amb} = −40 °C to 105 °C.

[3] $T_{cy(clk)}$ = 12 × $T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: V_{DD} = 3.3 V.

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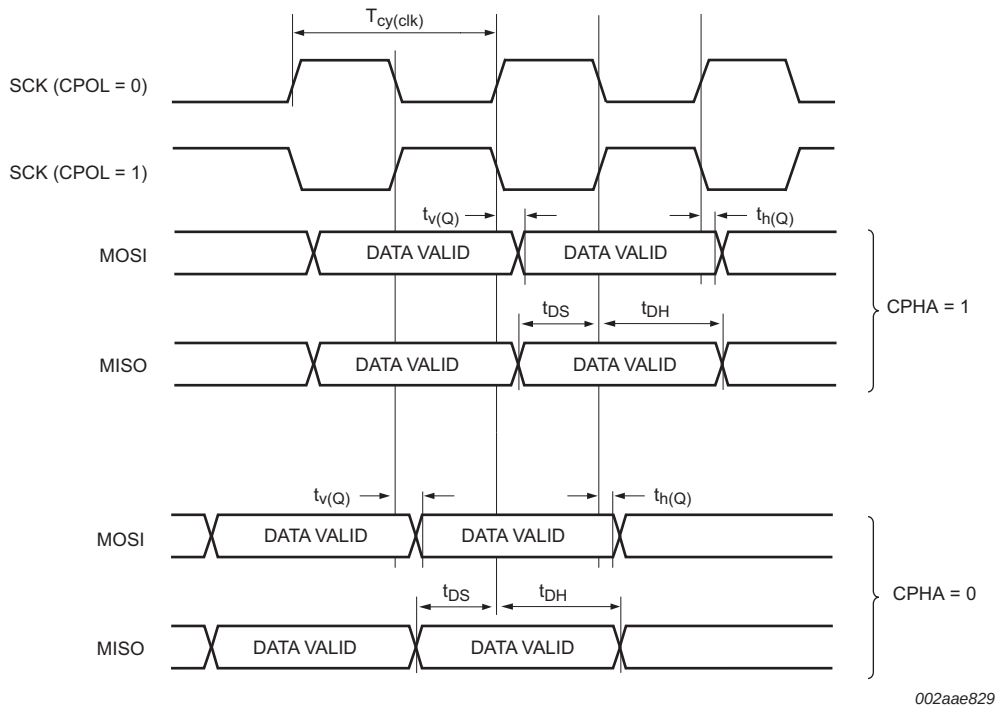

Pin names SCK, MISO, and MOSI refer to pins for both SSP peripherals, SSP0 and SSP1.

Fig 20. SSP master timing in SPI mode

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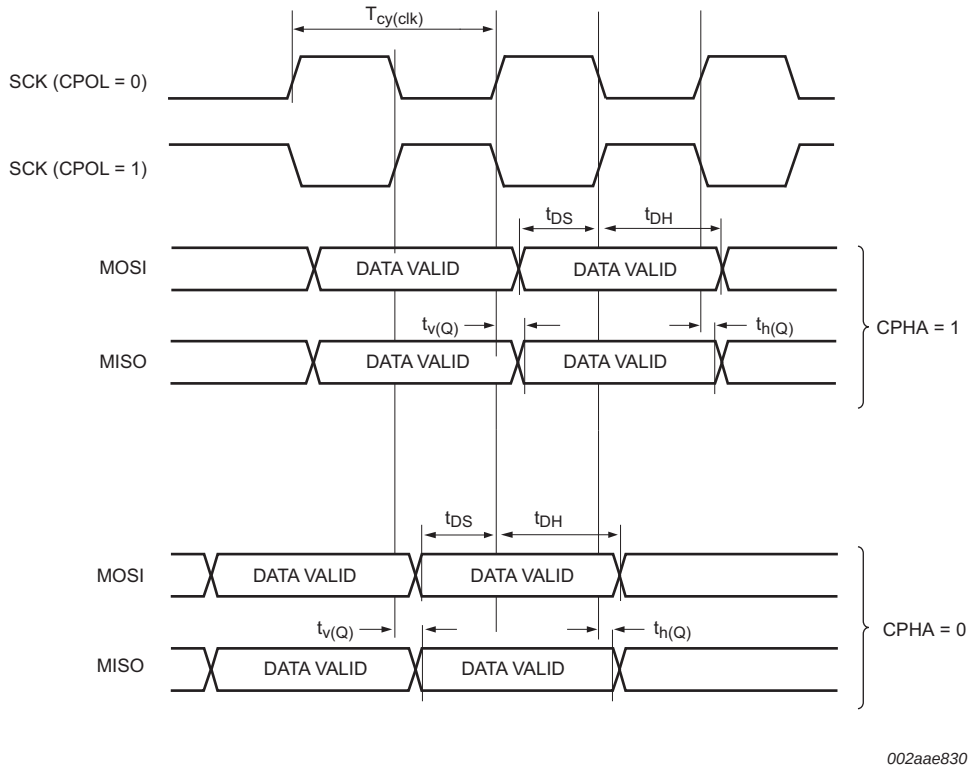

Pin names SCK, MISO, and MOSI refer to pins for both SSP peripherals, SSP0 and SSP1.

Fig 21. SSP slave timing in SPI mode

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12. Analog characteristics

12.1 BOD static characteristics

Table 15. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC111x user manual*.

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12.2 12-bit ADC

Table 16. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DDA}; V_{SSA} = 0; VREFN = V_{SSA}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage		[1]	0		V_{DDA}	V
C_{ia}	analog input capacitance			-		2.5	pF
$f_{clk(ADC)}$	ADC clock frequency	$V_{DDA} \geq 2.7$ V	[8]			50	MHz
		$V_{DDA} \geq 2.4$ V	[9]			25	MHz
f_s	sampling frequency	$V_{DDA} \geq 2.7$ V	[8]	-		2	Msamples/s
		$V_{DDA} \geq 2.4$ V	[9]	-		1	Msamples/s
E_D	differential linearity error		[2]	-	+/- 2	-	LSB
$E_{L(adj)}$	integral non-linearity		[3]	-	+/- 2	-	LSB
E_O	offset error		[4]	-	+/- 3	-	LSB
$V_{err(fs)}$	full-scale error voltage	2 Msamples/s	[5]	-	+/- 0.12	-	%
		1 Msamples/s			+/- 0.07	-	%
Z_i	input impedance	f_s = 2 Msamples/s	[6][7]	0.1		-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 22.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 22.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 22.

[5] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 22.

[6] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0.32 pF.

[7] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 6 for C_{io}.

[8] In the ADC TRM register, set VRANGE = 0 (default).

[9] In the ADC TRM register, set VRANGE = 1.

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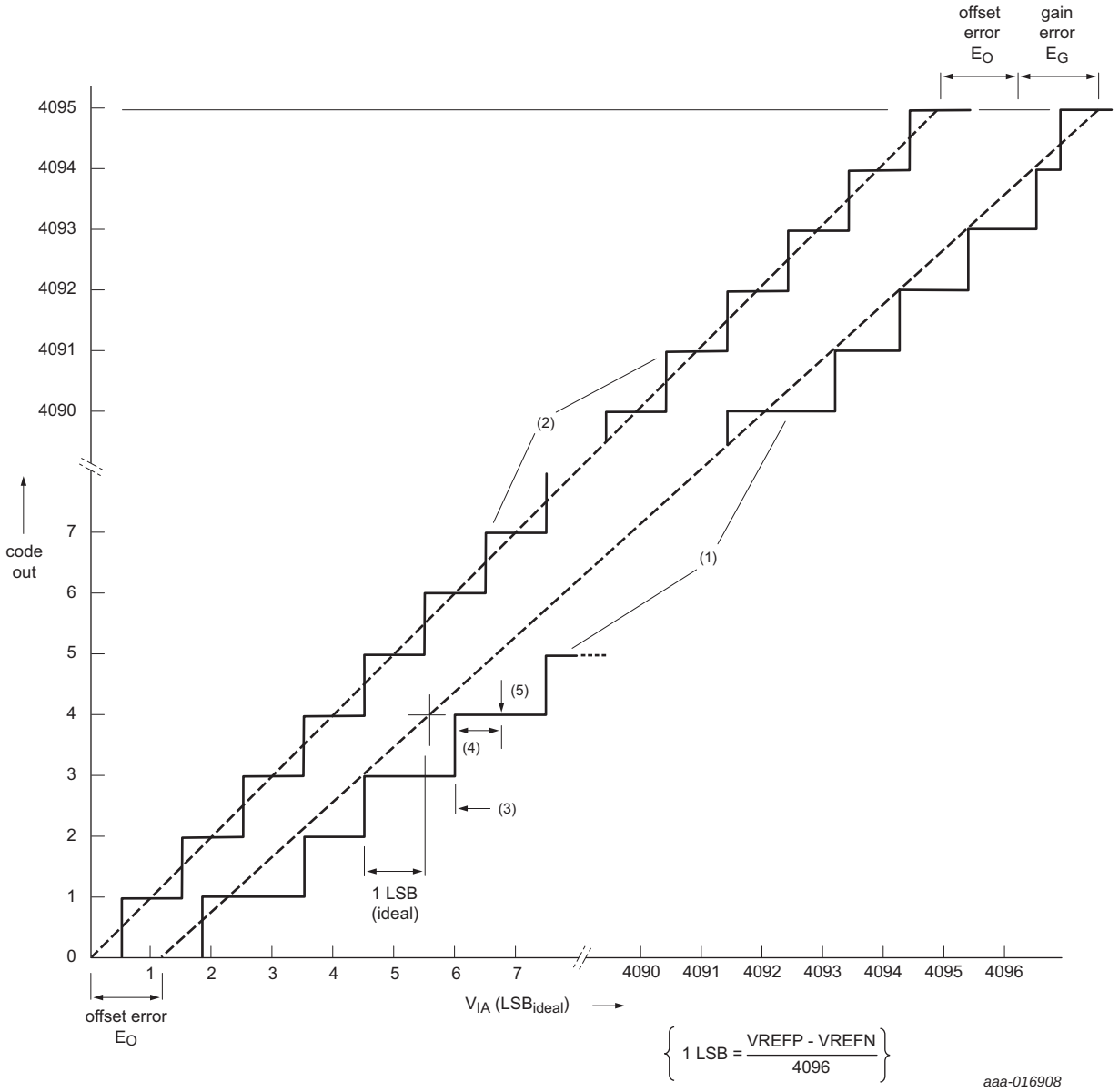

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 22. 12-bit ADC characteristics

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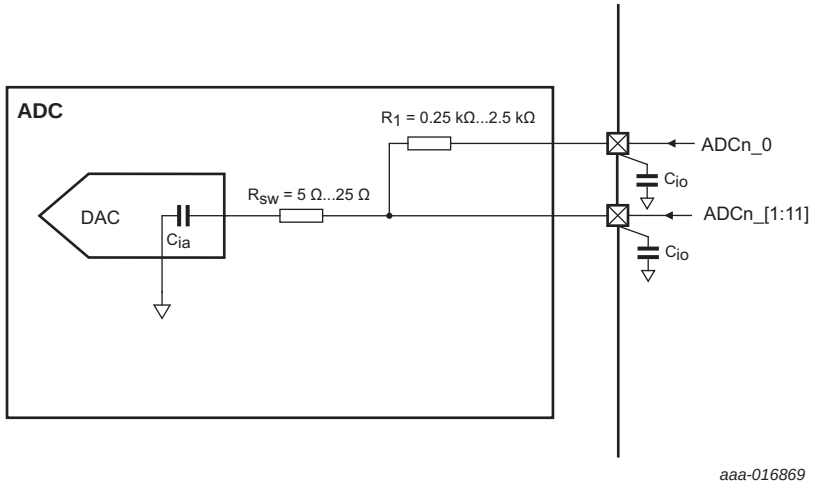

Fig 23. ADC input impedance

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13. Application information

13.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 6:

- The ADC input trace must be short and as close as possible to the LPC112x chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

13.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

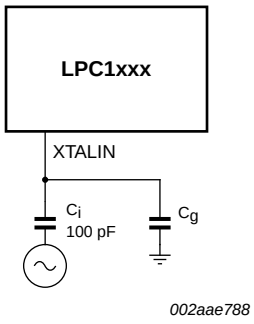

Fig 24. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 24), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 25 and in Table 17 and Table 18. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 25 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 17).

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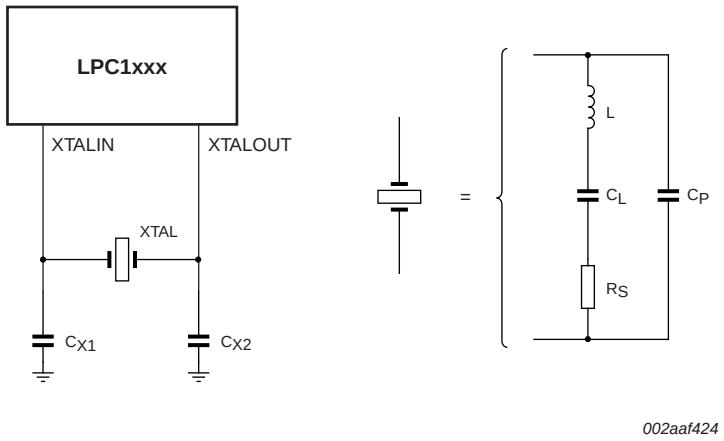

Fig 25. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 17. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

13.3 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

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order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{X1} and C_{X2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

13.4 Connecting power, clocks, and debug functions

Figure 26 shows the basic board connections used to power the LPC112x and provide debug capabilities via the serial wire port.

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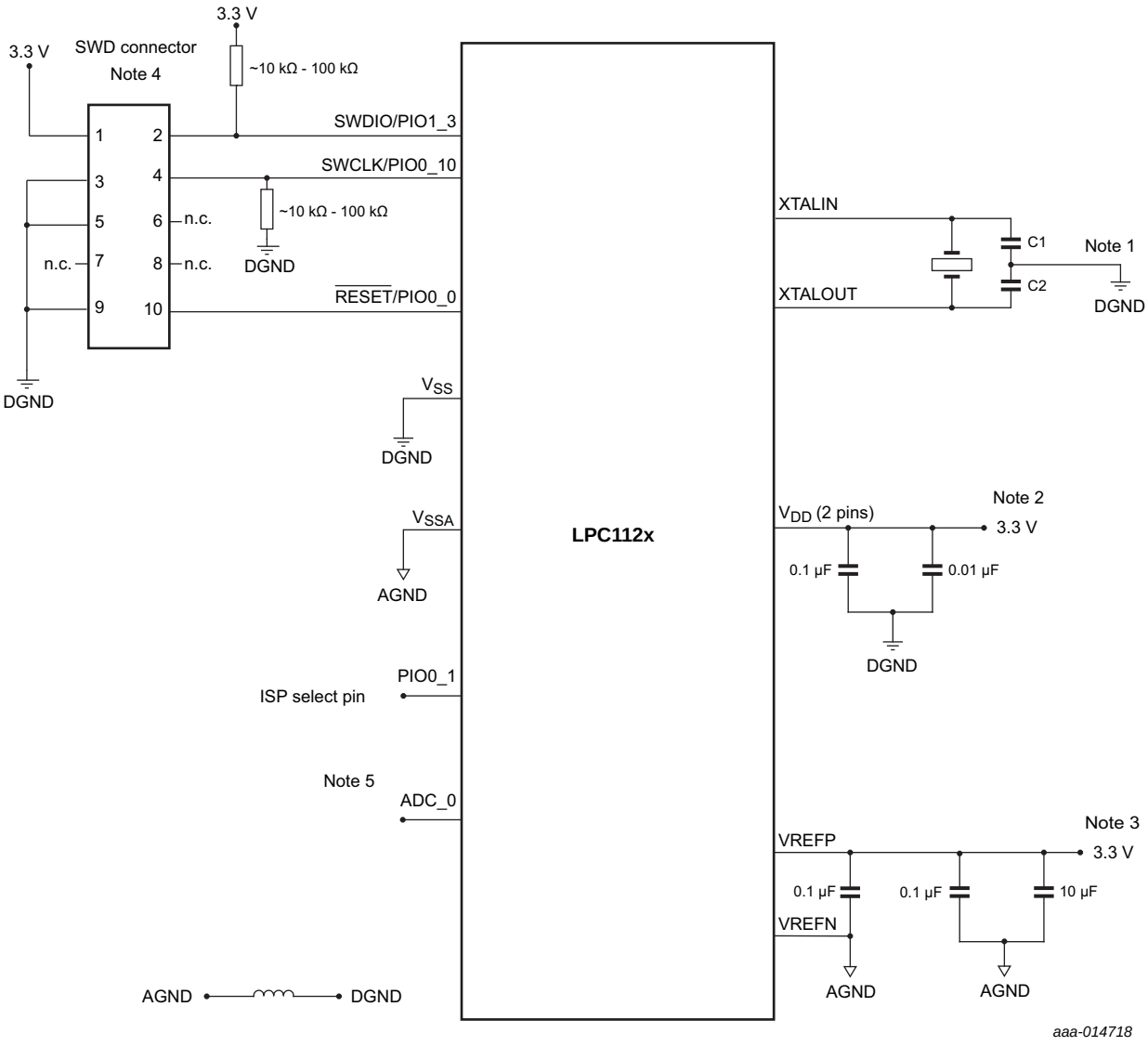

(1) See Section 13.2 “XTAL input” for the values of C1 and C2.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DD} pins. The 10 µF bypass capacitor filters the power line. Tie VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 4.

Fig 26. Power, clock, and debug connections

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13.5 Termination of unused pins

Table 19 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 19. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_0	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether Deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

13.6 Pin states in different power modes

Table 20. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_4, PIO0_5 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
PIO1_4/ WAKEUP	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

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13.7 Standard I/O pad configuration

Figure 27 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital output: Pseudo open-drain mode enable/disabled.
- Analog input.

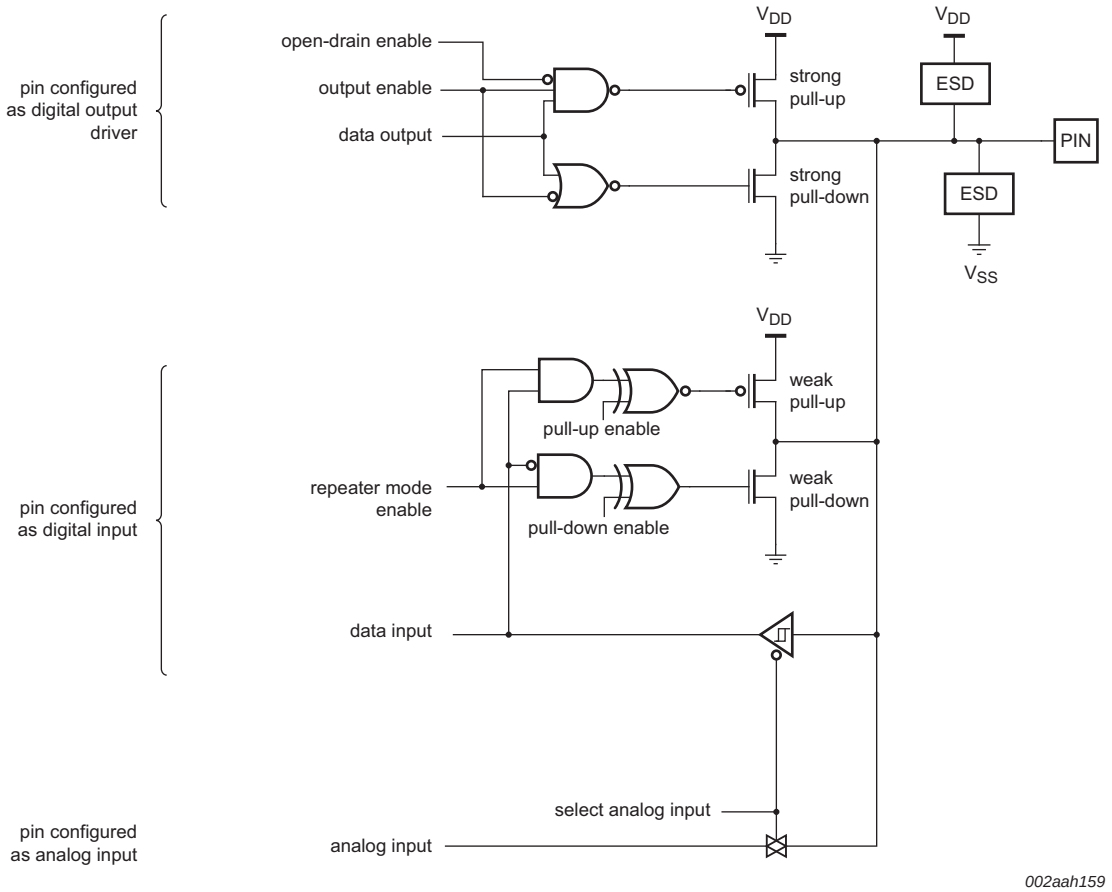

Fig 27. Standard I/O pad configuration

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13.8 Reset pad configuration

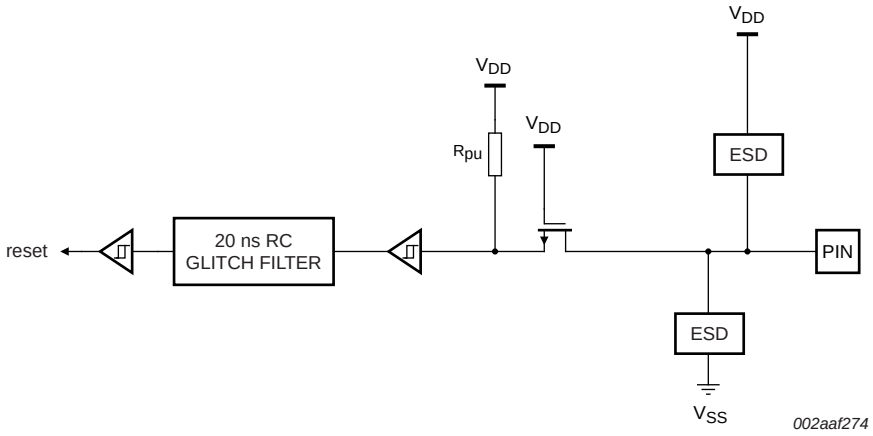

Fig 28. Reset pad configuration

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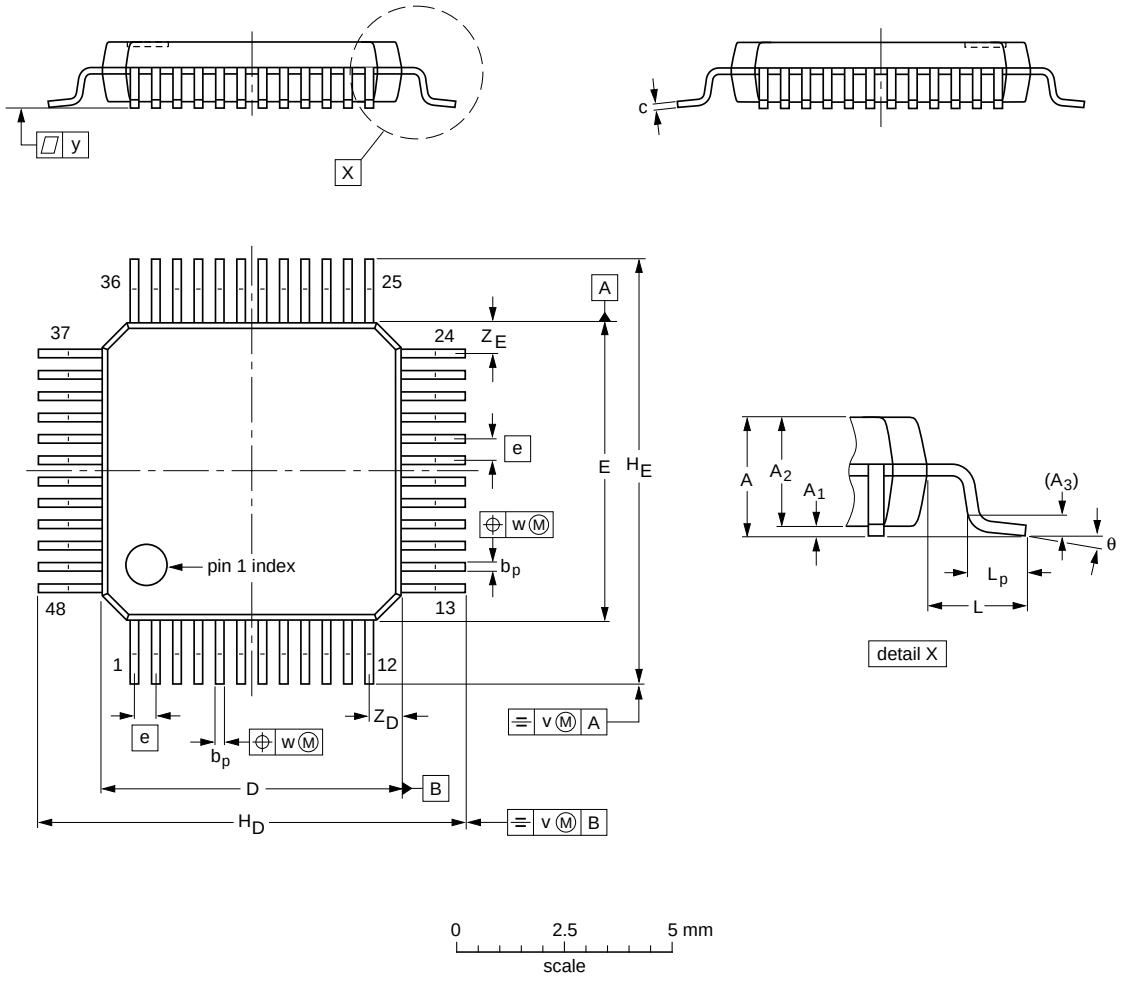
14. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 29. LQFP48 package outline

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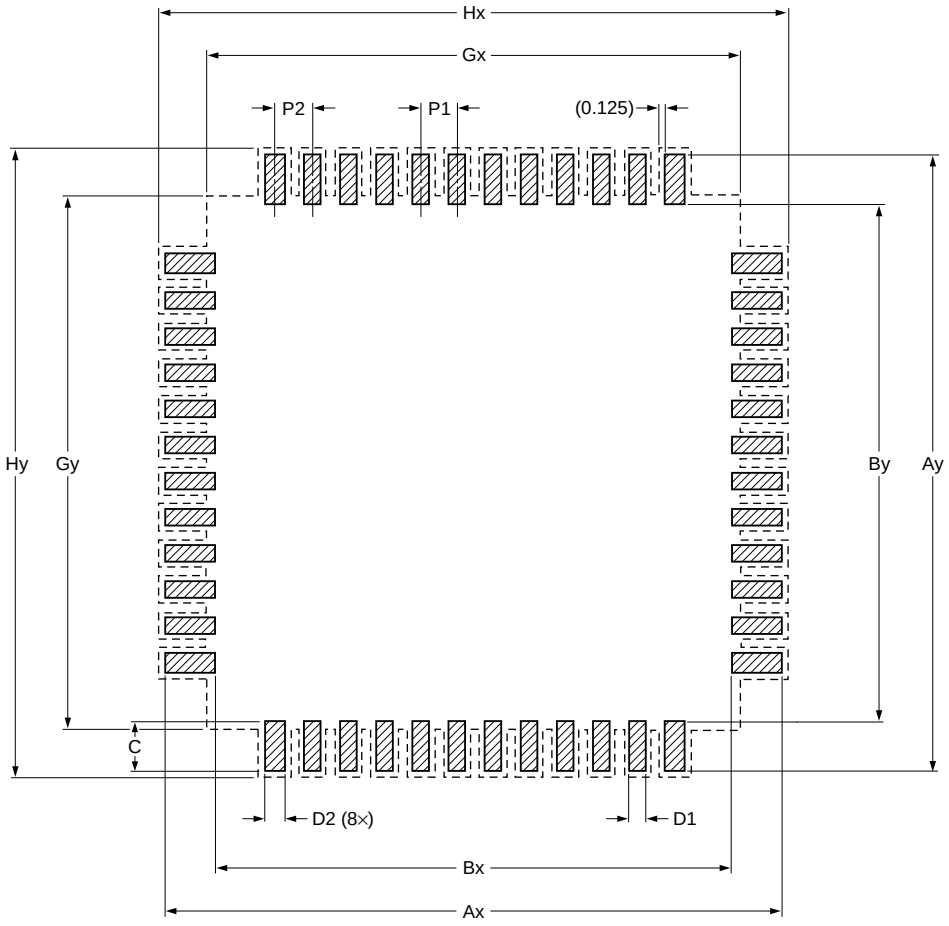
15. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 30. Reflow soldering of the LQFP48 package

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16. Abbreviations

Table 21. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

17. References

[1] User manual UM10839.

[2] Errata sheet ES_LPC112x.

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

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18. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC112x v.1.0	20150224	Product data sheet	-	-

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19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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