THE DATASHEET OF

PCA9509PDP,118

PCA9509P

Low Power Level Translating I^{2}C-Bus/SMBus Repeater

Rev. 5.1 — 3 July 2025 **Product data sheet**

Document information

Information	Content
Keywords	PCA9509P, Repeater, I^{2}C, SMBus, I^{2}C Repeater, Dual Supply
Abstract	The PCA9509P is a level translating I^{2}C-bus/SMBus repeater with two voltage supplies that enables processor low voltage 2-wire serial bus to interface with standard I^{2}C-bus or SMBus I/O

1 General description

The PCA9509P is a level translating I^2C-bus/SMBus repeater with two voltage supplies that enables processor low voltage 2-wire serial bus to interface with standard I^2C-bus or SMBus I/O. While retaining all the operating modes and features of the I^2C-bus system during the level shifts, it also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, therefore enabling the I^2C-bus or SMBus maximum capacitance of 400 pF on the higher voltage side. Port A allows a voltage range from 0.8 V to 2.0 V and is overvoltage tolerant. Port B allows a voltage range from 2.3 V to 5.5 V and is overvoltage tolerant. Both port A and port B SDA and SCL pins are high-impedance when the PCA9509P is unpowered.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses an offset LOW which prevents bus lock-up and allows the bidirectional nature of the device. The output pulldown on the port A internal buffer LOW is set for approximately $0.2V_{CC(A)}$, while the input threshold of the internal buffer is set about $0.1V_{CC(A)}$ lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pulldown on the port B drives a hard LOW and the input level is set at 0.3 of SMBus or I^2C-bus voltage level which enables port B to connect to any other I^2C-bus devices or buffer.

The PCA9509P drivers are not enabled unless $V_{CC(A)}$ is above 0.7 V and $V_{CC(B)}$ is above 1.7 V. The enable (EN) pin can also be used to turn on and turn off the drivers under system control. Caution must be observed to change only the state of the EN pin when the bus is idle.

1.1 Selection recommendations

The PCA9509P must be used if an external A-port pullup resistor is required to adjust current for noise margin considerations or to reduce operating current consumption. See Table 1 for the comparison.

Table 1. Device selection recommendation

Concern	Recommended device	
	PCA9509	PCA9509P
A-port — lowest voltage	1.0 V	0.85 V
A-port — current source[1]	Yes — 1 mA	No — external pullup
Operating current[2]	< 6.1 mA	< 0.95 mA
Standby current EN = LOW	< 2 mA	< 22 μA max.

[1] The PCA9509 current mirrors do not shut down when the device is disabled, allowing instant turn-on, but at the cost of the higher standby current. The PCA9509P current mirrors are turned off when disabled for lowest standby power consumption, but sufficient delay (10 μs) after enable is needed before resuming operation.

[2] Operating currents do not include the current consumed by the external pull-ups on the B-port or the external pull-ups on the A-port of the PCA9509P.

2 Features and benefits

- Bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- Voltage level translation from port A (0.8 V to 2.0 V) to port B (2.3 V to 5.5 V)
- No internal current source on A port to reduce current consumption for portable applications
- Active HIGH enable input disables current mirrors to reduce standby power
- Open-drain inputs/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I^2C-bus devices and multiple controllers
- Powered-off high-impedance I^2C-bus pins
- Operating supply voltage range of 0.8 V to 2.0 V on port A, 2.3 V to 5.5 V on port B
- All pins are 5 V tolerant with respect to ground pin
- 0 Hz to 400 kHz clock frequency
  Remark: The maximum system operating frequency can be less than 400 kHz because of the delays added by the repeater.
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8, XQFN8

3 Ordering information

Table 2 describes the ordering information for PCA9509P.

Table 2. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9509PDP	9509P	TSSOP8	Plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9509PGM	9PX[1]	XQFN8	Plastic, thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2

[1] 'X' changes based on the date code.

3.1 Ordering options

Table 3 describes the ordering options for PCA9509P.

Table 3. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9509PDP	PCA9509PDP,118	TSSOP8	Reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = -40 °C to +85 °C
PCA9509PGM	PCA9509PGM,125	XQFN8	Reel 7" Q3/T4 *standard mark	4000	T_{amb} = -40 °C to +85 °C

4 Functional diagram

Figure 1 shows the labeled block diagram of PCA9509P.

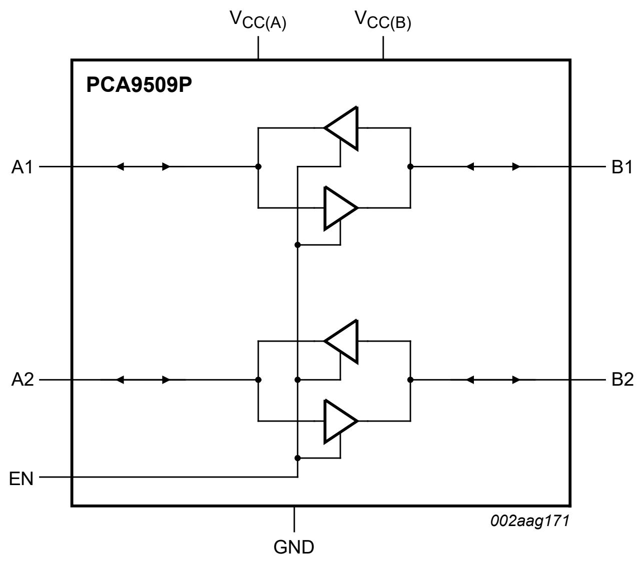


Figure 1. Functional diagram of PCA9509P

5 Pinning information

This section provides the pin configuration and description of PCA9509P.

5.1 Pinning

Figure 2 shows the pin configuration of PCA9509P.

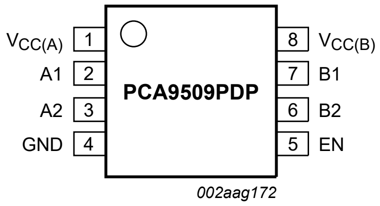


Figure 2. Pin configuration for TSSOP8

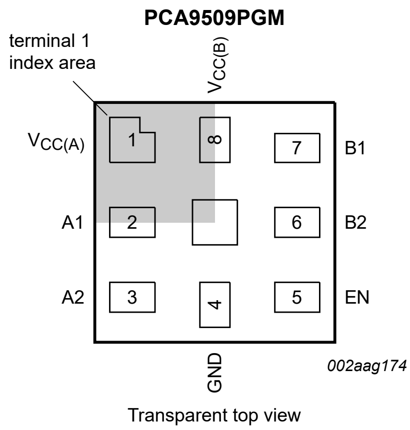


Figure 3. Pin configuration for XQFN8

5.2 Pin description

Table 4 provides detailed description of various pins on PCA9509P.

Table 4. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	Port A power supply
A1[1]	2	Port A (lower voltage side)
A2[1]	3	Port A (lower voltage side)
GND	4	Ground (0 V)
EN	5	Enable input (active HIGH)
B2[1]	6	Port B (SMBus/I^{2}C-bus side)
B1[1]	7	Port B (SMBus/I^{2}C-bus side)
$V_{CC(B)}$	8	Port B power supply

[1] Port A and port B can be used for either SCL or SDA.

6 Functional description

Refer to Figure 1.

The PCA9509P enables I^2C-bus or SMBus translation down to $V_{CC(A)}$ as low as 0.8 V without degradation of system performance. The PCA9509P contains 2 bidirectional open-drain buffers designed to support up-translation/down-translation between the low voltage and 3.3 V SMBus or 5 V I^2C-bus. The port A and port B I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered.

The PCA9509P includes a power up circuit that keeps the output drivers turned off until the $V_{CC(B)}$ is above 1.7 V and the $V_{CC(A)}$ is above 0.7 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power up. After power up and with the EN pin HIGH, a LOW level on port A (below approximately $0.15V_{CC(A)}$) turns on the corresponding port B driver (either SDA or SCL) and drives port B down to about 0 V. When port A rises above approximately $0.15V_{CC(A)}$, the port B pulldown driver is turned off and the external pullup resistor pulls the pin HIGH. When port B falls first and goes below $0.3V_{CC(B)}$, the port A driver is turned on, and port A pulls down to $0.2V_{CC(A)}$ (typical). The port B pulldown is not enabled unless the port A voltage goes below V_{IL}. If the port A low voltage goes below V_{IL}, the port B pulldown driver is enabled until port A rises above approximately $0.15V_{CC(A)}$ (V_{IL}), then port B, if not externally driven LOW, rises, being pulled up by the external pullup resistor. When port B voltage rises above 50 % of $V_{CC(B)}$, port A continues to rise being pulled up by an external pullup resistor.

Remark: Ground offset between the PCA9509P ground and the ground of devices on port A of the PCA9509P must be avoided.

The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V has an output resistance of 133 Ω or less (R = E / I). Such a driver shares enough current with the port A output pulldown of the PCA9509P to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{IL} can be as low as 80 mV at cold temperatures and the low end of the current distribution, the maximum ground offset must not exceed 40 mV.

Bus repeaters that use an output offset are not interoperable with the port A of the PCA9509P as their output LOW levels are not recognized by the PCA9509P as a LOW. If the PCA9509P is placed in an application where the V_{IL} of port A of the PCA9509P does not go below its V_{IL}, the port B does not go LOW.

Port B provides normal I^2C-bus voltage levels and is interoperable with all I^2C-bus targets, controllers, and repeaters.

6.1 Enable

The EN pin is active HIGH and allows the user to select when the repeater is active. This can be used to isolate a badly behaved target on power up until after the system power up reset. It should never change state during an I^2C-bus operation because disabling during a bus operation hangs the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled. The EN also puts the PCA9509P in a standby condition to reduce power consumption.

The enable pin must only change state when the bus and the repeater port are in an idle state to prevent system failures.

Because the enable pin (EN) can put the PCA9509P in Standby mode, and when in standby the current mirrors are turned OFF to save power, the recovery from the disabled/standby state is slow so that the current mirrors can return to full current before the channels are enabled.

Remark: The system design must allow sufficient time after STOP before disabling the PCA9509P so that both sides of the SDA and SCL channels are HIGH. It must also allow sufficient time before the START such that the channel is disabled before the SDA goes LOW. The PCA9509P should only be enabled during a bus idle state and there must also be sufficient time allowed before the START such that the PCA9509P is fully active before the falling edge of the SDA that defines a START.

6.2 I²C-bus systems

As with the standard I²C-bus system, pullup resistors are required to provide the logic at HIGH levels. The size of these pullup resistors depends on the system. Port A is designed to work with the size of pullup resistor' as required to meet rise time requirements but minimize current consumption. Port B is designed to work with Standard-mode and Fast-mode I²C-bus devices in addition to SMBus devices. Standard-mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices and multiple controllers are possible. Under certain conditions, higher termination currents can be used (when all currents are > 3 mA).

6.3 Edge rate control

The PCA9509P includes circuitry that slows down the falling edge of both the A side and B side open-drain output pull-downs. This slowdown reduces system noise and undershoot when the signal reflects off the end of the bus. The slew rate control circuit limits the maximum slew rate, and is relatively insensitive to the load capacitance, the bus high voltage and to the pullup value. The rising edge slew rate on the A side and B side is controlled by the RC time constant of the bus pull-up resistor and the bus capacitance, which are system level considerations and not under the control of the PCA9509P. The pullup resistors must be chosen based on the total bus capacitance to result in a reasonable rising edge transition time that is less than the maximum allowed rise time, and slow enough not to make system level noise problems, and to make the A side low voltage less than V_{IL}.

6.4 Bus pull-up resistor selection

The AC test load for the PCA9509P is 1.35 kΩ and 50 pF total capacitance. This results in a rise time of approximately 60 ns. The 1.35 kΩ resistor is chosen to provide a little less than 3 mA in a 3.3 V application so it is compatible with Standard-mode I²C-bus devices and Fast-mode devices. The B side output pull-down is a strong driver and is capable of sinking Fast-mode Plus (Fm+) currents, however the pullup must be sized for the weakest part in the system, so if Standard-mode I²C-bus parts are present on the B side, the pullup must be limited to less than 3 mA. If only Fm+ parts are used on the B side, the maximum pullup current can be up to 30 mA. The pullup resistor should always be sized to provide less than the rated pull-up current for the weakest part on the bus under the maximum bus voltage expected in the system. When the bus capacitance is high, the current must be set near the maximum current drive for the weakest part. However, if the bus capacitance is low a lower current/higher resistor value must be used to keep the rise time from getting so fast that it causes problems. The A side pull-up resistor must be selected to keep the LOW-level voltage at the A side input below $0.1V_{CC(A)}$.

6.4.1 Port A pullup resistor sizing

When selecting the pullup resistor for the A side of the PCA9509P, there are several considerations and limitations from both the PCA9509P and the other parts on the A-side bus that must be considered.

6.4.1.1 Minimum resistor size

The first limitation is that for the PCA9509P to recognize a LOW on the A side, the voltage level must be below $0.1V_{CC(A)}$ including ground offset. This and the drive strength of the parts driving the less than $0.1V_{CC(A)}$ level define the minimum resistor value that can be used based on the other parts on the A-side bus. There is also a limit of 4 mA maximum current that can be applied to the PCA9509P A side when it is LOW. For example, if the part driving the PCA9509P A side is rated at 3 mA at 0.4 V (and it is a MOS part) and assuming that $V_{CC(A)}$ = 0.8 V, then the part has an effective output resistance of 0.4 V / 3 mA = 133 Ω, so the maximum current is 0.08 V / 133 Ω = ~600 μA, so the maximum pullup current is 600 μA. And for $V_{CC(A)}$ = 0.8 V the minimum resistance is 0.72 V / 600 μA = 1.2 kΩ. If the part providing the $0.1V_{CC(A)}$ has a low output resistance, then the current is limited to 4 mA by the PCA9509P, and for $V_{CC(A)}$ = 0.8 V the minimum pullup resistance would be 0.64 V / 4 mA = 160 Ω. Since the ground offset is never zero, the minimum resistor value must be increased accordingly.

6.4.1.2 Maximum resistance sizing

The pullup resistor on the A side of the PCA9509P should be chosen to provide at least 100 μA of pull-up current. So, for $V_{CC(A)}$ = 0.8 V the maximum resistor value looks like 0.64 V / 100 μA = 6.4 kΩ.

6.4.1.3 Rise time constraints

In addition to the current minimum and maximum considerations, the RC time constant of the A-side bus must be considered. It is recommended that the RC time constant be chosen so that it is greater than 60 ns to control the size of the bounce that results when a driver on the A side turns off that was driving a $<0.1V_{CC(A)}$ level and before the offset output driver in the PCA9509P can turn on and hold the voltage to $\sim 0.2V_{CC(A)}$. The maximum RC time constant is limited by the I^2C-bus family specification for maximum rise time between $0.3V_{CC(A)}$ and $0.7V_{CC(A)}$ (400 ns for Fast mode and 1000 ns for Standard mode operation). Although the maximum current and maximum rise time limits predict an allowable capacitance well above the 400 pF I^2C-bus family specification, this is not likely to be possible in a typical I^2C-bus system since there is so little voltage margin for the V_{IL} of the PCA9509P ground offset is more likely to limit the effective capacitance than current drive capability because high-capacitance buses tend to be physically large and large size tends to result in larger ground-offset voltages, which must be severely limited to be successful at a bus voltage of 1 V and below.

7 Application design-in information

A typical application is shown in Figure 4. In this example, the CPU is running on a 0.9 V I2C-bus while the target is connected to a 3.3 V bus. Both buses run at 400 kHz. Controller devices can be placed on either bus.

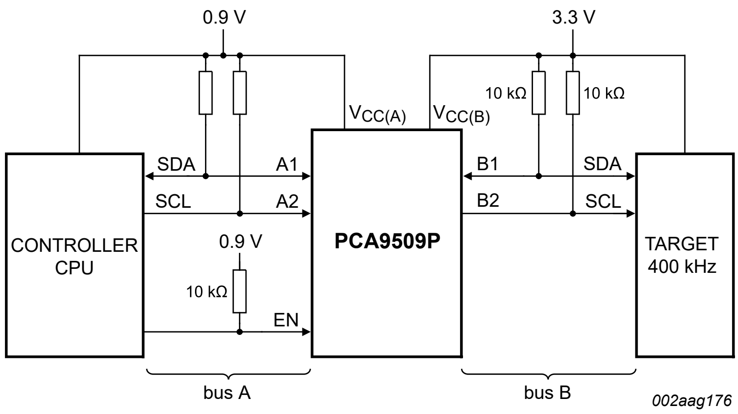


Figure 4. Typical application

When port B of the PCA9509P is pulled LOW by a driver on the I2C-bus, a CMOS hysteresis input detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about $0.2V_{CC(A)}$. When port A of the PCA9509P falls, a comparator detects the falling edge when it falls below $0.15V_{CC(A)}$ and causes the internal driver on port B to turn on and pull the port B pin down to ground. To illustrate what would be seen in a typical application, refer to Figure 5 and Figure 6. If the bus controller in Figure 4 writes to the target through the PCA9509P, waveforms shown in Figure 5 would be observed on the B bus. This looks like a normal I2C-bus transmission.

On the A bus side of the PCA9509P, the clock and data lines are driven by the controller and swing nearly to ground. After the eighth clock pulse, the target replies with an ACK that causes a LOW on the A side equal to the V_{OL} of the PCA9509P, which the controller recognizes as a LOW. It is important to note that any arbitration or clock stretching events require that the LOW level on the A bus side at the input of the PCA9509P (V_{IL}) is below $0.1V_{CC(A)}$ to be recognized by the PCA9509P and then transmitted to the B bus side.

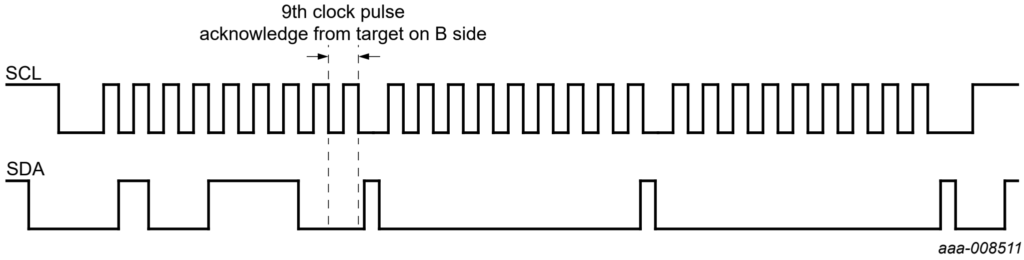


Figure 5. Bus B SMBus/I2C-bus waveform

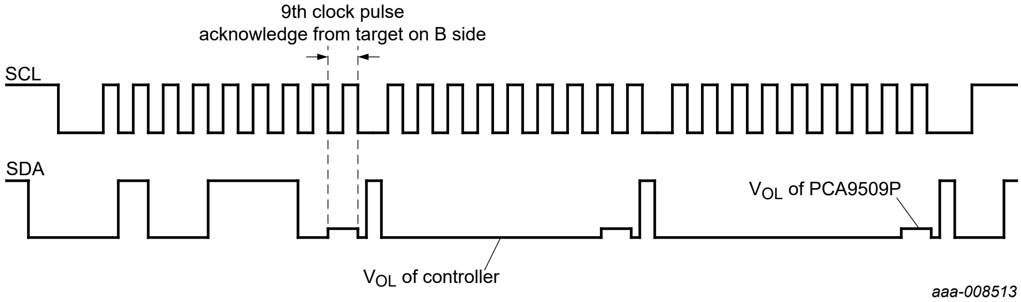


Figure 6. Bus A lower voltage waveform

8 Limiting values

Table 5 describes the limiting values of PCA9509P.

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Note	Min	Max	Unit
$V_{CC(B)}$	Supply voltage port B			-0.5	+6.0	V
$V_{CC(A)}$	Supply voltage port A			-0.5	+6.0	V
$V_{I/O}$	Voltage on an input/output pin	Port A	[1]	-0.5	+6.0	V
		Port B; enable pin (EN)	[1]	-0.5	+6.0	V
$I_{I/O}$	Input/output current			-	±20	mA
I_{OL}	LOW-level output current	A-side I/O active LOW		-	20	mA
		B-side I/O active LOW		-	40	mA
I_I	Input current			-	±20	mA
P_{tot}	Total power dissipation			-	100	mW
T_{stg}	Storage temperature			-65	+150	°C
T_{amb}	Ambient temperature	Operating in free air		-40	+85	°C
T_j	Junction temperature			-	+125	°C
T_{sp}	Solder point temperature	10 s max.		-	300	°C

[1] With I/O pins OFF. If active, see I_{OL}.

9 Static characteristics

Table 6 describes the typical static characteristics of PCA9509P.

Table 6. Static characteristics

GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Note	Min	Typ[1]	Max	Unit
Supplies							
$V_{CC(B)}$	Supply voltage port B			2.3	-	5.5	V
$V_{CC(A)}$	Supply voltage port A			0.8[2]	-	2.0	V
$I_{CC(A)}$	Supply current port A	All port A static HIGH or LOW		2	5	16	µA
$I_{CC(B)}$	Supply current port B	All port B static HIGH		200	500	850	µA
		All port B static LOW		200	510	950	µA
$I_{CC(B)stb}$	Standby port B supply current	EN = LOW		0.5	1.5	10	µA
Input and output of port A (A1 to A2)							
V_{IH}	HIGH-level input voltage	Port A		$0.2V_{CC(A)}$	-	5.5	V
V_{IL}	LOW-level input voltage			-0.5	-	$+0.1V_{CC(A)}$	V
V_{IK}	Input clamping voltage	I_L = -18 mA		-1.5	-	-0.5	V
I_{LI}	Input leakage current	$V_I = V_{CC(A)}$; EN = HIGH; B1 = HIGH		-10	-	+10	µA
		EN = GND		-1	-	+1	µA
V_{OL}	LOW-level output voltage	$V_{CC(A)}$ = 0.8 V to 2.0 V; I_{load} = 100 µA	[3]	-	$0.2V_{CC(A)}$	$0.25V_{CC(A)}$	V
$V_{OL}-V_{IL}$	Difference between LOW-level output and LOW-level input voltage		[4]	-	$0.05V_{CC(A)}$	-	mV
C_{io}	Input/output capacitance	Disabled		-	7	10	pF
Input and output of port B (B1 to B2)							
V_{IH}	HIGH-level input voltage	Port B		$0.7V_{CC(B)}$	-	5.5	V
V_{IL}	LOW-level input voltage	Port B		-0.5	-	$+0.3V_{CC(B)}$	V
V_{IK}	Input clamping voltage	I_L = -18 mA		-1.5	-	-0.5	V
I_{LI}	Input leakage current	V_I = 3.6 V with An input HIGH		-1.0	-	+1.0	µA

Table 6. Static characteristics...*continued*

GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Note	Min	Typ[1]	Max	Unit
I_{IL}	LOW-level input current	V_I = 200 mV; $V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 2.0 V; port A = 1.35 kΩ pullup to $V_{CC(A)}$		-10	-	+10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	0.1	0.2	V
		I_{OL} = 30 mA at $V_{CC(B)}$ = 3.0 V		-	0.2	0.5	V
C_{io}	Input/output capacitance	Disabled		-	3	5	pF
Enable							
V_{IL}	LOW-level input voltage			-0.5	-	+0.2$V_{CC(A)}$	V
V_{IH}	HIGH-level input voltage			0.8$V_{CC(A)}$	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V; $V_{CC(B)}$ = 3.6 V; $V_{CC(A)}$ = 1.1 V		-10	-	+1	µA
I_{LI}	Input leakage current	V_I = $V_{CC(A)}$		-1	-	+1	µA
C_i	Input capacitance	V_I = 3.0 V		-	2	3	pF

[1] Typical values with $V_{CC(A)}$ = 1.1 V, $V_{CC(B)}$ = 3.3 V.

[2] Care must be taken to minimize the resistance in series with the ground pin of the PCA9509P to the ground reference point of the $V_{CC(A)}$ supply because there is only 80 mV margin between the power good threshold and the 0.8 V minimum supply voltage at cold temperature (-40 °C). Because the B-side I_{OL} of up to 30 mA flows through the resistance causing a voltage drop that effectively reduces the $V_{CC(A)}$ to chip ground voltage and when $V_{CC(A)}$ is less than the power good voltage ~0.72 V, the PCA9509P is disabled. For example, if the resistance is 1.4 Ω, then 1.4 Ω × 60 mA = 84 mV and 0.8 V - 0.084 V = 0.716 V, which is less than the power good threshold, so the PCA9509P disables when both outputs drive LOW.

[3] As long as the chip ground is common with the input ground reference the driver resistance can be as large as 120 Ω. However, ground offset rapidly decreases the maximum allowed driver resistance.

[4] Guaranteed by design.

10 Dynamic characteristics

Table 7 describes the dynamic characteristics of PCA9509P.

Table 7. Dynamic characteristics

$V_{CC(A)}$ = 0.8 V to 2.0 V; $V_{CC(B)}$ = 2.3 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Note	Min	Typ[2]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	Port B to port A	[1]	70	110	180	ns
t_{PHL}	HIGH to LOW propagation delay	Port B to port A	[1]	104	156	270	ns
SR_f	Falling slew rate	Port A; 0.7$V_{CC(A)}$ to 0.3$V_{CC(A)}$	[1]	0.007	0.015	0.036	V/ns
t_{PLH}	LOW to HIGH propagation delay	Port A to port B	[1]	-72	-110	-175	ns
t_{PLH2}	LOW to HIGH propagation delay 2	Port A to port B; measured from 0.15$V_{CC(A)}$ on port A to 0.5$V_{CC(B)}$ on port B	[1]	61	98	266	ns
t_{PHL}	HIGH to LOW propagation delay	Port A to port B	[1]	52	89	226	ns
SR_f	Falling slew rate	Port B; 0.7$V_{CC(B)}$ to 0.3$V_{CC(B)}$	[1]	0.02	0.05	0.1	V/ns

Table 7. Dynamic characteristics...*continued*

$V_{CC(A)}$ = 0.8 V to 2.0 V; $V_{CC(B)}$ = 2.3 V to 5.5 V; GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Note	Min	Typ[2]	Max	Unit
t_{en}	Enable time	EN HIGH to enabled	[3]	10	-	-	μs
t_{dis}	Disable time	EN LOW to disabled	[3]	300	-	-	ns

[1] Load capacitance = 50 pF; load resistance on port B = 1.35 kΩ. Port A = 1.35 kΩ, and an input falling slew rate of 0.05 V/ns.
[2] Typical values were measured with $V_{CC(A)}$ = 1.1 V, $V_{CC(B)}$ = 3.3 V at T_{amb} = 25 °C.
[3] Enable pin (EN) should only change state when the bus and the repeater port are in an idle state. That is, the t_{en} must be considered the set-up time before START and t_{dis} must be considered the hold time after STOP.

10.1 AC waveforms

This section shows the AC waveforms.

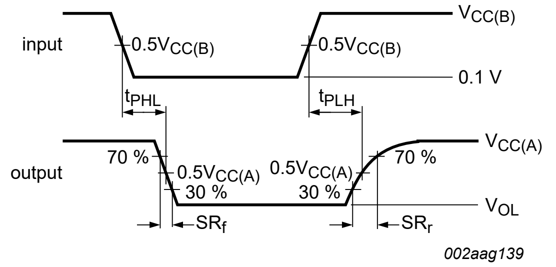


Figure 7. Propagation delay times and slew rate; port B to port A

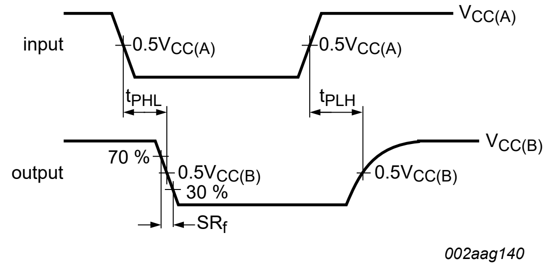


Figure 8. Propagation delay times and slew rate; port A to port B

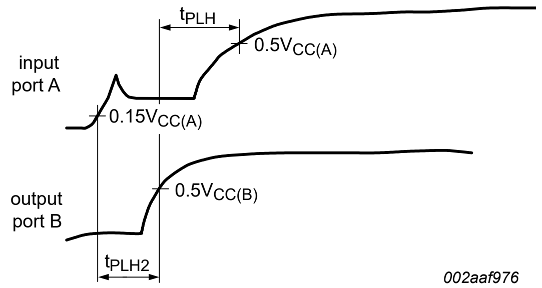
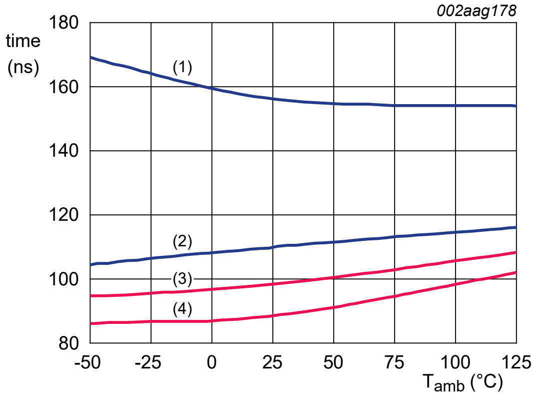


Figure 9. Propagation delay from the port A's external driver switching off to port B LOW-to-HIGH transition; port A to port B

10.2 Performance curves

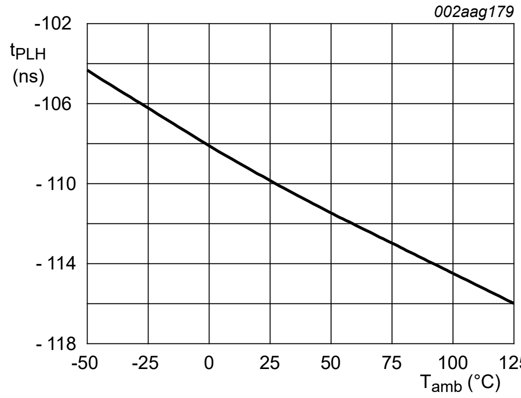
This section details the performance characteristics through graphical curves.



$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V

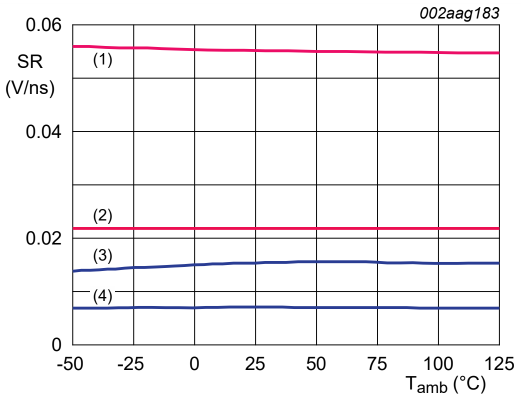
1. Port A t_{PHL}
2. Port A t_{PLH}
3. Port B t_{PLH2}
4. Port B t_{PHL}

Figure 10. Typical propagation delay versus ambient temperature



$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V

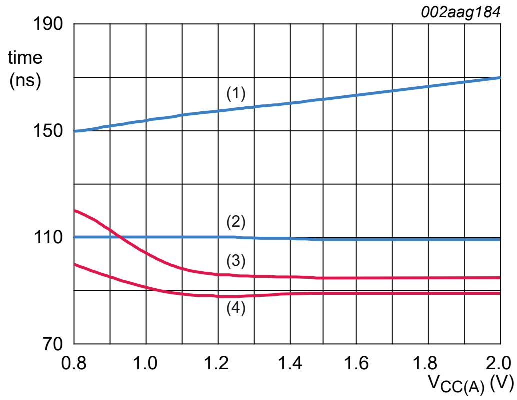
Figure 11. Typical port B LOW to HIGH propagation delay versus ambient temperature



$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V

1. Slew rate of falling signal, port B
2. Slew rate of rising signal, port B
3. Slew rate of falling signal, port A
4. Slew rate of rising signal, port A

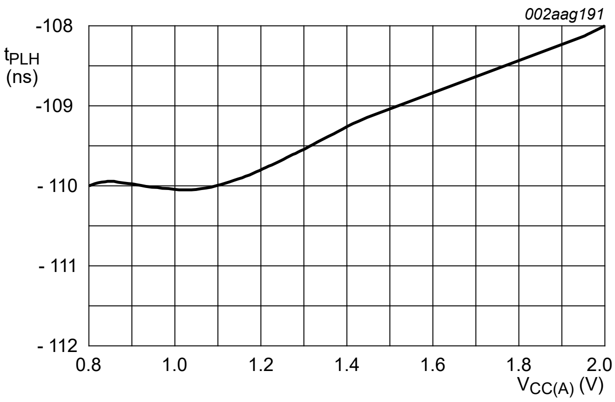
Figure 12. Typical slew rate versus ambient temperature



T_{amb} = 27 °C; $V_{CC(B)}$ = 3.3 V

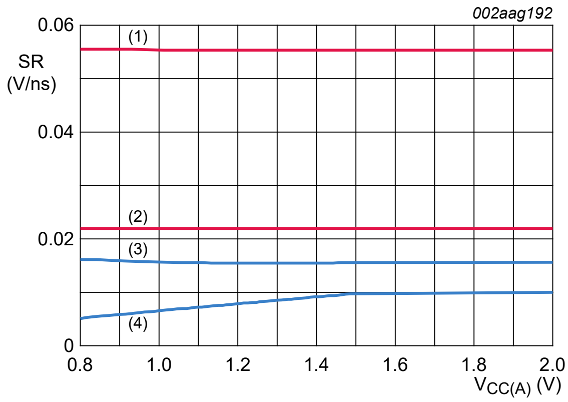
1. Port A t_{PHL}
2. Port A t_{PLH}
3. Port B t_{PLH2}
4. Port B t_{PHL}

Figure 13. Typical propagation delay versus port A supply voltage



T_{amb} = 27 °C; $V_{CC(B)}$ = 3.3 V

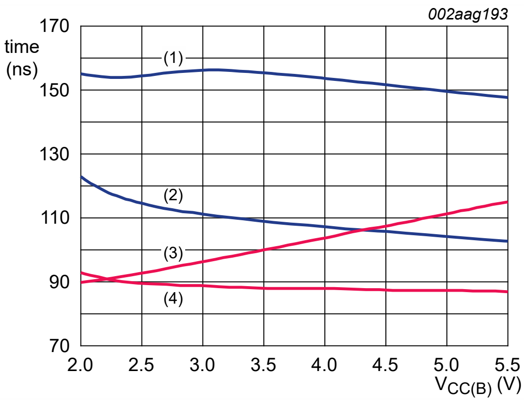
Figure 14. Typical port B LOW to HIGH propagation delay versus port A supply voltage



T_{amb} = 27 °C; $V_{CC(B)}$ = 3.3 V

1. Slew rate of falling signal, port B
2. Slew rate of rising signal, port B
3. Slew rate of falling signal, port A
4. Slew rate of rising signal, port A

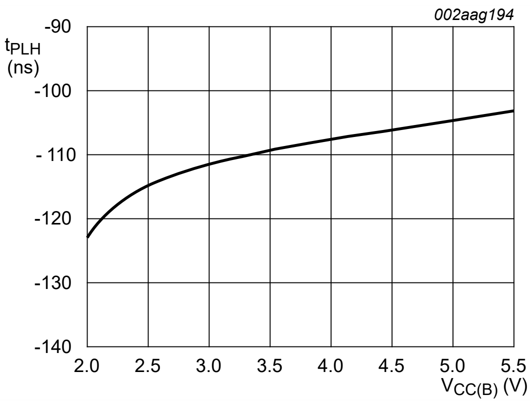
Figure 15. Typical slew rate versus port A supply voltage



T_{amb} = 27 °C; $V_{CC(A)}$ = 1.1 V

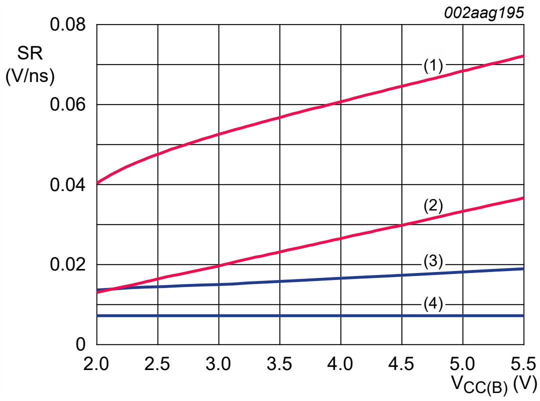
1. Port A t_{PHL}
2. Port A t_{PLH}
3. Port B t_{PLH2}
4. Port B t_{PHL}

Figure 16. Typical propagation delay versus port B supply voltage



T_{amb} = 27 °C; $V_{CC(A)}$ = 1.1 V

Figure 17. Typical port B LOW to HIGH propagation delay versus port B supply voltage



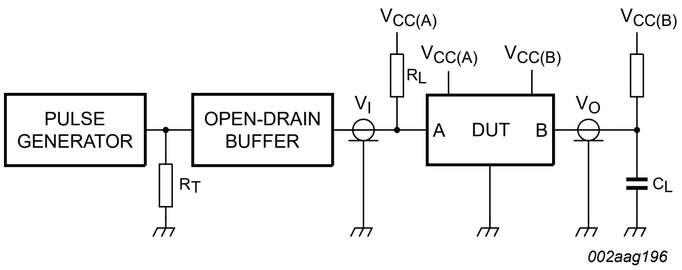
T_{amb} = 27 °C; $V_{CC(A)}$ = 1.1 V

1. Slew rate of falling signal, port B
2. Slew rate of rising signal, port B
3. Slew rate of falling signal, port A
4. Slew rate of rising signal, port A

Figure 18. Typical slew rate versus port B supply voltage

11 Test information

Figure 19 and Figure 20 illustrate the test circuits for open-drain outputs from A to B and from B to A, respectively.

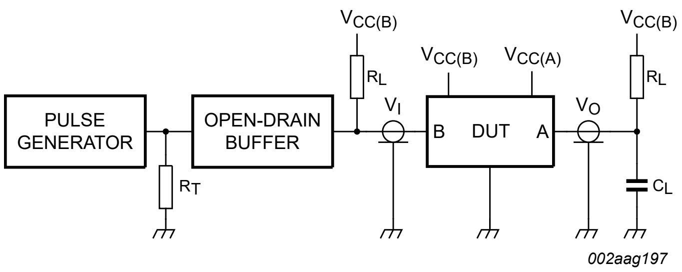


R_L = load resistor; 1.35 kΩ

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance must be equal to Z_o of pulse generators

Figure 19. Test circuit for open-drain outputs A to B



R_L = load resistor; 1.35 kΩ

C_L = load capacitance includes jig and probe capacitance; 50 pF

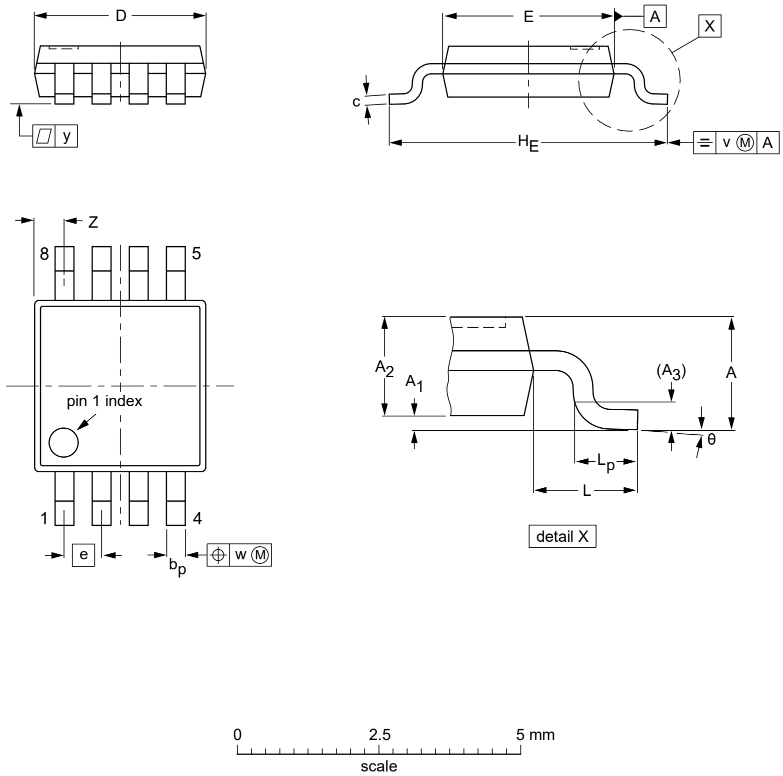
R_T = termination resistance must be equal to Z_o of pulse generators

Figure 20. Test circuit for open-drain outputs B to A

12 Package outline

Figure 21 and Figure 22 show the package outline for PCA9509P.

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

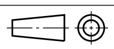
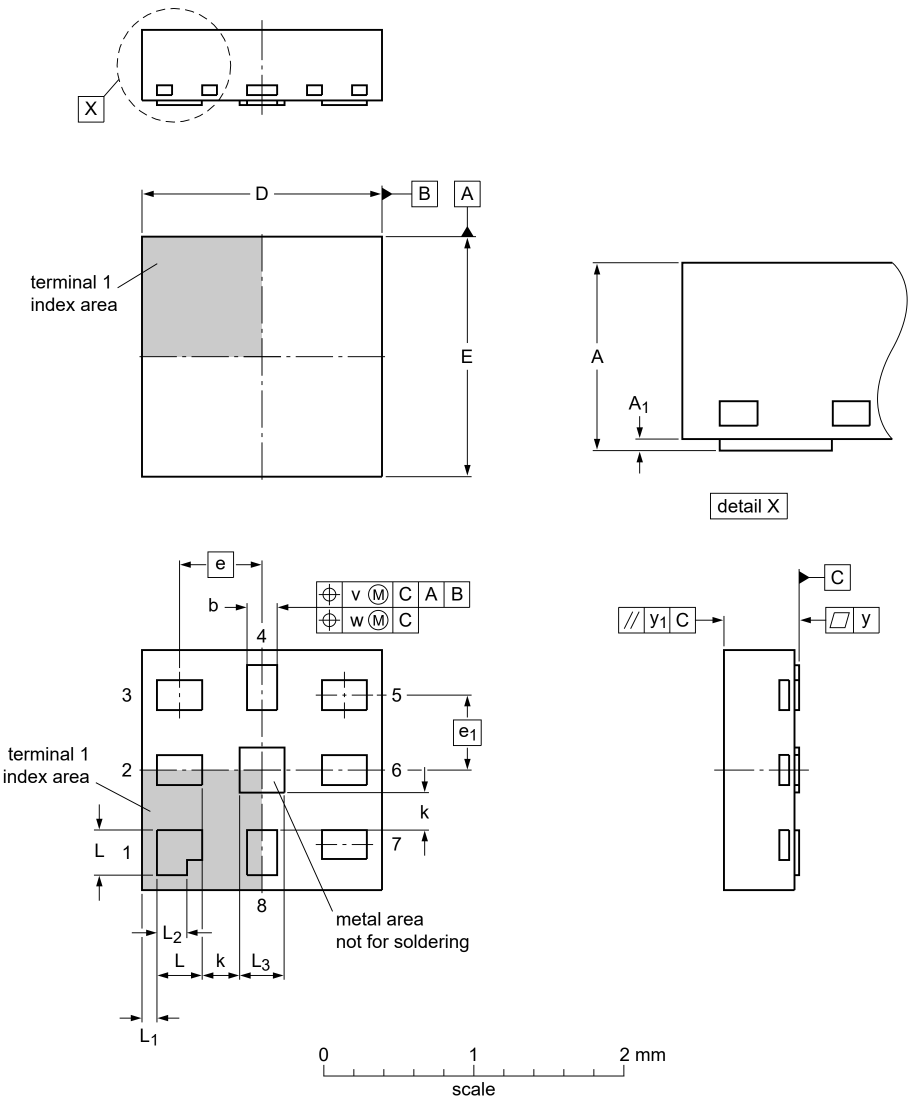
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Figure 21. Package outline SOT505-1 (TSSOP8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit[1]		A	A_1	b	D	E	e	e_1	k	L	L_1	L_2	L_3	v	w	y	y_1
	max	0.5	0.05	0.25	1.65	1.65				0.35	0.15	0.25	0.35				
mm	nom			0.20	1.60	1.60	0.55	0.5		0.30	0.10	0.20	0.30	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.2	0.25	0.05	0.15	0.25				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References IEC	JEDEC	JEITA		European projection	Issue date
SOT902-2	- - -	MO-255	- - -			~~16-07-14~~ 16-11-08

Figure 22. Package outline SOT902-2 (XQFN8)

13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and Table 9

Table 8. SnPb eutectic process (from J-STD-020D)

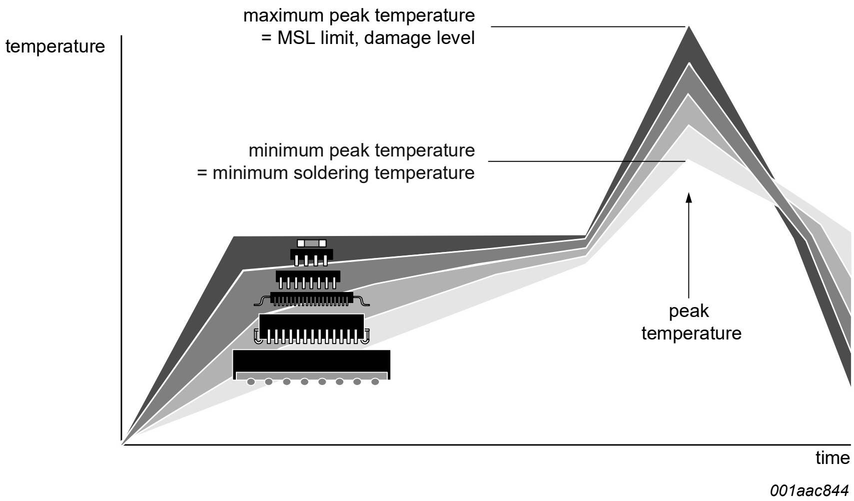
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.



MSL: Moisture Sensitivity Level

Figure 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

14 Soldering: PCB footprints

This section covers the PCB design guidelines for soldering the PCA9509P.

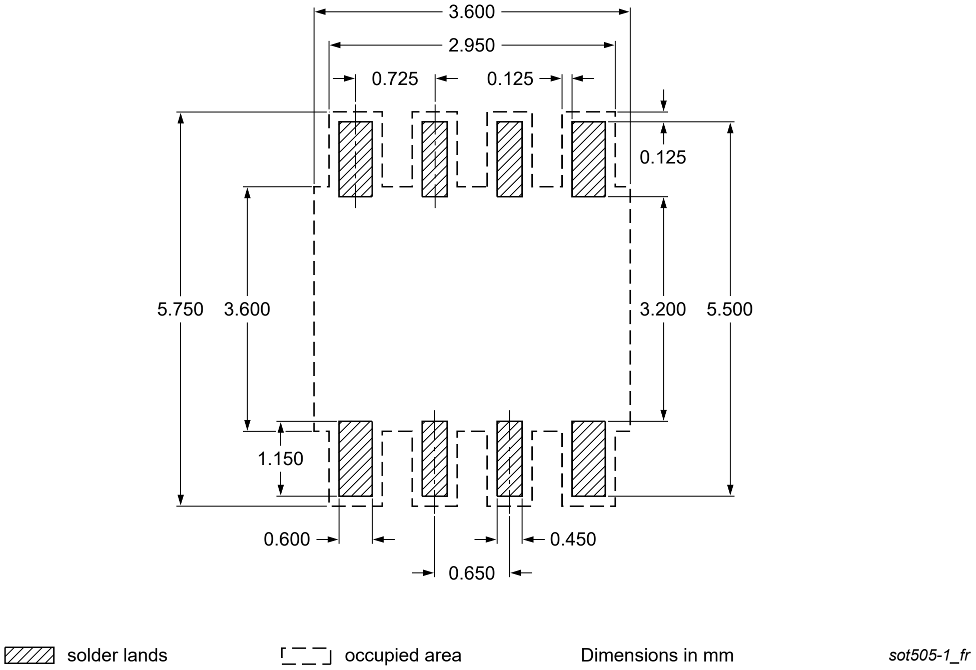
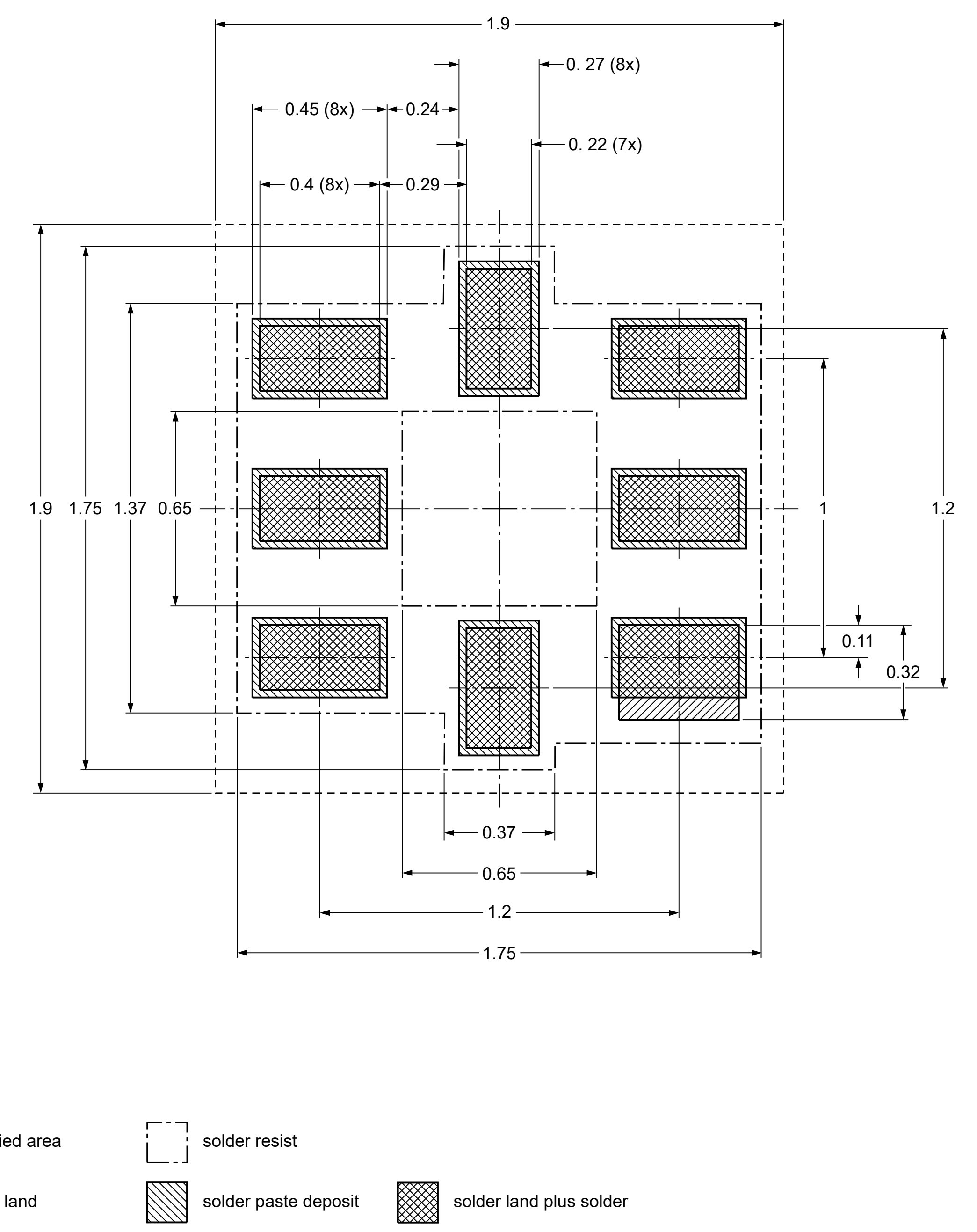


Figure 24. PCB footprint for SOT505-1 (TSSOP8); reflow soldering

Footprint information for reflow soldering of XQFN8 package **SOT902-2**



Dimensions in mm

Issue date ~~15-06-19~~ 15-06-23

sot902-2_fr

Figure 25. PCB footprint for SOT902-2 (XQFN8); reflow soldering

15 Acronyms

Table 10 lists acronyms used in this document.

Table 10. Acronyms

Acronym	Description
CDM	Charged-device model
CMOS	Complementary metal-oxide semiconductor
CPU	Central processing unit
ESD	Electrostatic discharge
HBM	Human body model
I/O	Input/output
I^2C-bus	Inter-integrated circuit bus
NMOS	Negative-channel metal-oxide semiconductor
RC	Resistor-capacitor network
SMBus	System management bus
SDA	Serial data line
SCL	Serial clock line

16 Revision history

Table 11 summarizes revisions to this document.

Table 11. Revision history

Document ID	Release date	Description
PCA9509P v.5.1	03 July 2025	Updated as per CIN# 202507003I: • Made some editorial changes • Updated the Table 2 and Table 3 with PCA9509PGM in place of PCA950PGM
PCA9509P v.5.0	18 July 2022	Updated as per CIN# 202206023I: • Table 6: Changed PCA9509P max V_{IH} specification to clearly indicate port A, port B and Enable pins are overvoltage tolerant to 5.5 V. There is no change to device or test coverage, only to data sheet values • Removed all references, including associated text, to PCA9509 A • The terms "master" and "slave" are deprecated and have been replaced with "controller" and "target" respectively in accordance with NXP's inclusive language project
PCA9509P v.4.0	18 May 2018	Product data sheet
PCA9509P v.3.0	19 July 2013	Product data sheet
PCA9509P v.2.0	15 May 2013	Product data sheet
PCA9509P v.1.0	14 August 2012	Product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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