



**THE DATASHEET OF
IDTCV174CPVG**





PROGRAMMABLE FLEXPC CLOCK FOR P4 PROCESSOR

IDTCV174C

FEATURES:

- Compliant with Intel CK505
- Power management control suitable for low power applications
- One high precision PLL for CPU/SRC/PCI, SSC and N programming
- One high precision PLL for SRC/PCI, SSC and N programming
- One high precision PLL for 96MHz/48MHz
- Push-pull IOs for differential outputs
- Support spread spectrum modulation, -0.5 down spread and others
- Support SMBus block read/write, index read/write
- Selectable output strength
- Smooth transition for N programming
- Available in SSOP and TSSOP packages

KEY SPECIFICATIONS:

- CPU/SRC CLK cycle to cycle jitter < 85ps
- PCI CLK cycle to cycle jitter < 500ps

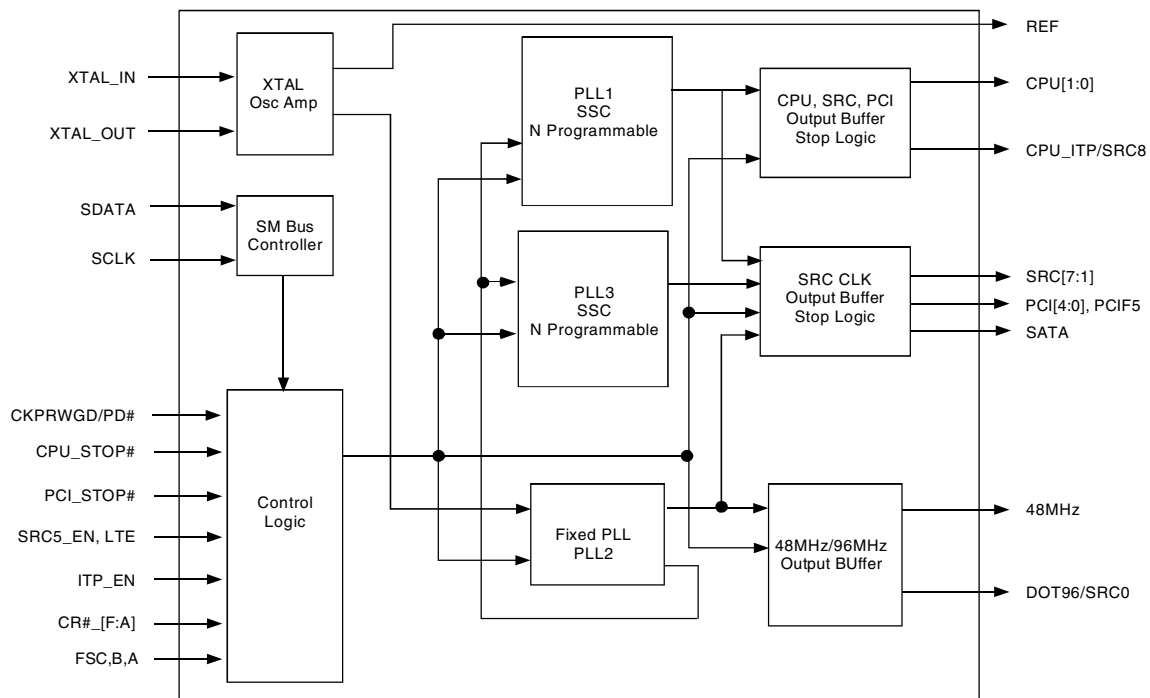
DESCRIPTION:

IDTCV174C is a 56 pin clock device, incorporating Intel CK505 requirements for the Intel advance P4 processor. The CPU output buffer is designed to support up to 400MHz reference clock for the CPU. This chip has three PLLs inside for CPU, SRC/PCI and 48MHz/DOT96 IO clocks.

OUTPUTS:

- 2*0.7V differential CPU CLK pair
- 7*0.7V differential SRC CLK pair
- One CPU_ITP/SRC differential clock pair
- One SRC0/DOT96 differential clock pair
- 6*PCI, 33.3MHz
- 1*48MHz
- 1*REF
- 1*SATA

FUNCTIONAL BLOCK DIAGRAM

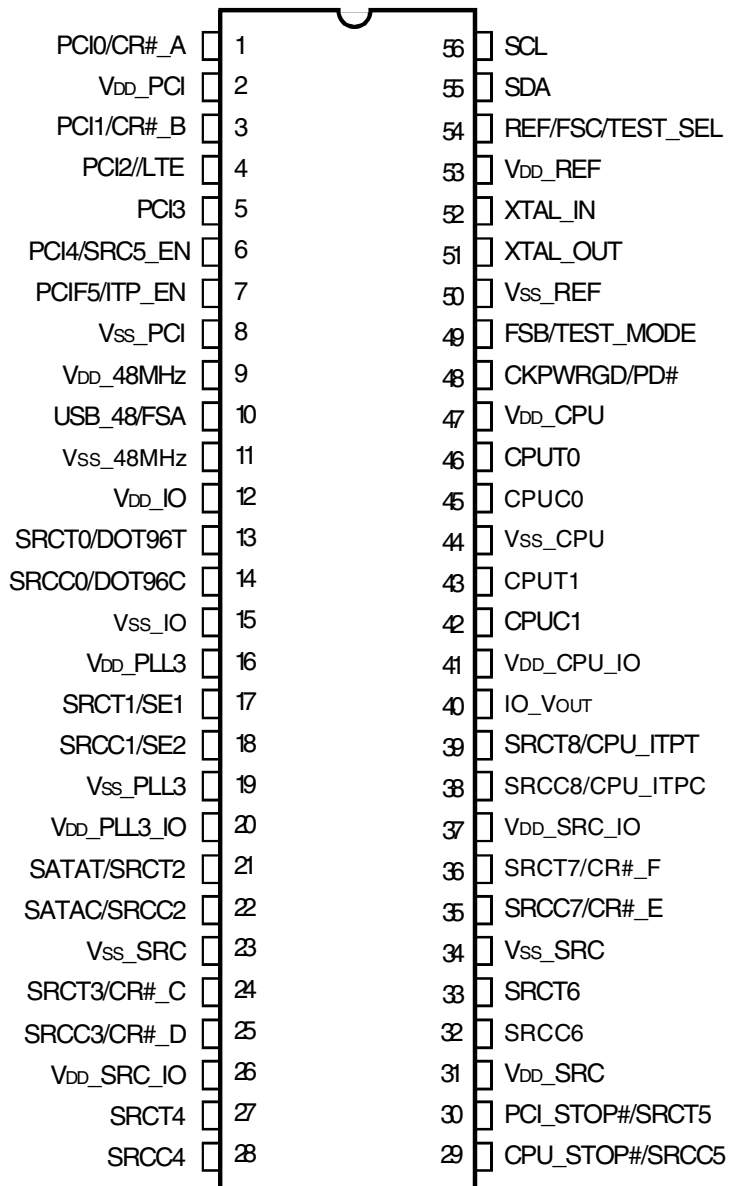


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COMMERCIAL TEMPERATURE RANGE

MAY 2006

PIN CONFIGURATION



TSSOP
TOP VIEW

PIN DESCRIPTION

| Pin # | Name | Type | Description |
|-------|-------------------------|------|---|
| 1 | PCI0/CR#_A | I/O | 33.33MHz/SRC0, 2 Differential clock output enable, control SRC0 and SRC2, 0 = enable. Mode is selected by SMBus control register. Default is PCI clock mode |
| 2 | V _{DD_PCI} | PWR | 3.3V |
| 3 | PCI1/CR#_B | I/O | 33.33MHz/SRC1, 2 Differential clock output enable, control SRC1 and SRC4, 0 = enable. Mode is selected by SMBus control register. Default is PCI clock mode |
| 4 | PCI2/LTE | I/O | 33.33MHz. High = overlocking disabled. Power-on latch. |
| 5 | PCI3 | OUT | 33.33MHz |
| 6 | PCI4/SRC5_EN | I/O | 33.33MHz. Pin 29, 30 mode selection. Power on latch, high = SRC5, low = CPU and PCI Stop# |
| 7 | PCIF5/ITP_EN | I/O | 33.33MHz. Pin 38, 39 mode selection. Power on latch, high = CPU_ITP, low = SRC8 |
| 8 | V _{SS_PCI} | GND | GND |
| 9 | V _{DD_48} | PWR | 3.3V |
| 10 | USB 48/FS_A | I/O | 48MHz/ Frequency select, power on latch |
| 11 | V _{SS_48} | GND | GND |
| 12 | V _{DD_IO} | PWR | 0.8V |
| 13 | SRCT0/DOT96T | OUT | Differential output clock. SRC or DOT96. Mode selected by SMBus control register, default is SRC0 |
| 14 | SRCC0/DOT96C | OUT | Differential output clock. SRC or DOT96. Mode selected by SMBus control register, default is SRC0 |
| 15 | V _{SS_IO} | GND | GND |
| 16 | V _{DD_PLL3} | PWR | 3.3V |
| 17 | SRCT1/SE1 | OUT | Differential or single end clock output. Mode selected by SMBus control register. Default is SRC1. |
| 18 | SRCC1/SE2 | OUT | Differential or single end clock output. Mode selected by SMBus control register. Default is SRC1 |
| 19 | V _{SS_PLL3} | GND | GND |
| 20 | V _{DD_PLL3_IO} | PWR | 0.8V |
| 21 | SRCT2/SATAT | OUT | Differential output clock |
| 22 | SRCC2/SATAC | OUT | Differential output clock |
| 23 | V _{SS_SRC} | GND | GND |
| 24 | SRCT3/CR#_C | I/O | SRC clock/ SRC differential clock output enable, control SRC0 and SRC2, 0 = enable. Mode selected by SMBus control register. Default is SRC3. |
| 25 | SRCC3/CR#_D | I/O | SRC clock/ SRC differential clock output enable, control SRC1 and SRC4, 0 = enable. Mode selected by SMBus control register. Default is SRC3.. |
| 26 | V _{DD_SRC_IO} | PWR | 0.8V |
| 27 | SRCT4 | OUT | Differential output clock |
| 28 | SRCC4 | OUT | Differential output clock |
| 29 | CPU_Stop#/SRCC5 | I/O | CPU stop, low = stop/ SRC clock. Mode selected by pin6, SRC5_EN. |
| 30 | PCI_Stop#/SRCT5 | I/O | PCI stop, low = stop/ SRC clock. Mode selected by pin6, SRC5_EN. |
| 31 | V _{DD_SRC} | PWR | 3.3V |
| 32 | SRCC6 | OUT | Differential output clock |
| 33 | SRCT6 | OUT | Differential output clock |
| 34 | V _{SS_SRC} | GND | GND |
| 35 | SRCC7/CR#_E | I/O | SRC clock/ SRC differential clock output enable, control SRC6, 0 = enable. Mode selected by SMBus control register. Default is SRC7. |
| 36 | SRCT7/CR#_F | I/O | SRC clock/ SRC differential clock output enable, control SRC8, 0 = enable. Mode selected by SMBus control register. Default is SRC7. |
| 37 | V _{DD_SRC_IO} | PWR | 0.8V |
| 38 | SRCC8/CPU_ ITPC | OUT | SRC clock/CPU clock. Mode selected by pin7. |
| 39 | SRCT8/CPU_ ITPT | OUT | SRC clock/CPU clock. Mode selected by pin7. |
| 40 | IO_V _{OUT} | OUT | V _{IO} adjustment |

PIN DESCRIPTION, CONTINUED

| Pin # | Name | Type | Description |
|-------|------------------------|------|--|
| 41 | V _{DD_CPU_IO} | PWR | 0.8V |
| 42 | CPUC1 | OUT | Differential output clock |
| 43 | CPUT1 | OUT | Differential output clock |
| 44 | V _{SS_CPU} | GND | GND |
| 45 | CPUC0 | OUT | Differential output clock |
| 46 | CPUT0 | OUT | Differential output clock |
| 47 | V _{DD_CPU} | PWR | 3.3V |
| 48 | CKPWRGD/PD# | IN | CKPWRGD power good, active LOW, used to latch FSA,B,C, ITP_EN, TME, and SRC5_EN, active HIGH. After, becomes power down, LOW active. |
| 49 | FS_B/TestMode | IN | Frequency Select at CKPWRGD assertion. Test Mode selection, see TEST_MODE selection table |
| 50 | V _{SS_REF} | GND | GND |
| 51 | XTAL_OUT | OUT | XTAL out |
| 52 | XTAL_IN | IN | XTAL in |
| 53 | V _{DD_REF} | PWR | 3.3V |
| 54 | REF/FS_C/TestSel | I/O | 14.318MHz. Frequency Select at CKPWRGD assertion. Selects test mode if pulled above 2V at CKPWRGD assertion. |
| 55 | SDA | I/O | SMBus clock |
| 56 | SCL | IN | SMBus data |

TEST MODE SELECTION⁽¹⁾

If TEST_SEL sampled above 2V at CKPWRGD active LOW

| Test_Mode | CPU | SRC | PCI/F | REF | DOT_96/DOT_SSC | USB |
|-----------|-------|-------|-------|------|----------------|-------|
| 1 | REF/N | REF/N | REF/N | REF | REF/N | REF/N |
| 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

NOTE:

1. Once test clock operation has been invoked, TEST_MODE pin will select between the Hi-Z and REF/N, with V_{IH_FS} and V_{IL_FS} thresholds.

FREQUENCY SELECTION

| FSC, B, A | CPU | SRC[7:0] | PCI | USB | DOT | REF |
|-----------|---------|----------|------|-----|-----|--------|
| 101 | 100 | 100 | 33.3 | 48 | 96 | 14.318 |
| 001 | 133 | 100 | 33.3 | 48 | 96 | 14.318 |
| 011 | 166 | 100 | 33.3 | 48 | 96 | 14.318 |
| 010 | 200 | 100 | 33.3 | 48 | 96 | 14.318 |
| 000 | 266 | 100 | 33.3 | 48 | 96 | 14.318 |
| 100 | 333 | 100 | 33.3 | 48 | 96 | 14.318 |
| 110 | 400 | 100 | 33.3 | 48 | 96 | 14.318 |
| 111 | Reserve | 100 | 33.3 | 48 | 96 | 14.318 |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Min | Max | Unit |
|----------------------|--|-----------|------|------|
| V _{DDA} | 3.3V Core Supply Voltage | | 4.6 | V |
| V _{DD} | 3.3V Logic Input Supply Voltage | GND - 0.5 | 4.6 | V |
| T _{STG} | Storage Temperature | -65 | +150 | °C |
| T _{AMBIENT} | Ambient Operating Temperature | 0 | +70 | °C |
| T _{CASE} | Case Temperature | | +115 | °C |
| ESD Prot | Input ESD Protection Human Body Model | 2000 | | V |

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RESOLUTION

| | N Resolution (MHz) | % | N = |
|--------------|--------------------|------|-----|
| CPU = 100MHz | 0.500000 | 0.5% | 200 |
| CPU = 133MHz | 0.666667 | 0.5% | 200 |
| CPU = 166MHz | 0.666667 | 0.4% | 250 |
| CPU = 200MHz | 1.000000 | 0.5% | 200 |
| CPU = 266MHz | 1.333333 | 0.5% | 200 |
| CPU = 333MHz | 1.333333 | 0.4% | 250 |
| CPU = 400MHz | 2.000000 | 0.5% | 200 |
| SRC = 100MHz | 0.500000 | 0.5% | 200 |

SM PROTOCOL

INDEX BLOCK WRITE PROTOCOL

| Bit | # of bits | From | Description |
|-------|-----------|--------|--------------------------------------|
| 1 | 1 | Master | Start |
| 2-9 | 8 | Master | D2h |
| 10 | 1 | Slave | Ack (Acknowledge) |
| 11-18 | 8 | Master | Register offset byte (starting byte) |
| 19 | 1 | Slave | Ack (Acknowledge) |
| 20-27 | 8 | Master | Byte count, N (0 is not valid) |
| 28 | 1 | Slave | Ack (Acknowledge) |
| 29-36 | 8 | Master | first data byte (Offset data byte) |
| 37 | 1 | Slave | Ack (Acknowledge) |
| 38-45 | 8 | Master | 2nd data byte |
| 46 | 1 | Slave | Ack (Acknowledge) |
| | | | : |
| | | Master | Nth data byte |
| | | Slave | Acknowledge |
| | | Master | Stop |

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit 30-37).

| Bit | # of bits | From | Description |
|-------|-----------|--------|--|
| 1 | 1 | Master | Start |
| 2-9 | 8 | Master | D2h |
| 10 | 1 | Slave | Ack (Acknowledge) |
| 11-18 | 8 | Master | Register offset byte (starting byte) |
| 19 | 1 | Slave | Ack (Acknowledge) |
| 20 | 1 | Master | Repeated Start |
| 21-28 | 8 | Master | D3h |
| 29 | 1 | Slave | Ack (Acknowledge) |
| 30-37 | 8 | Slave | Byte count, N (block read back of N bytes) |
| 38 | 1 | Master | Ack (Acknowledge) |
| 39-46 | 8 | Slave | first data byte (Offset data byte) |
| 47 | 1 | Master | Ack (Acknowledge) |
| 48-55 | 8 | Slave | 2nd data byte |
| | | | Ack (Acknowledge) |
| | | | : |
| | | Master | Ack (Acknowledge) |
| | | Slave | Nth data byte |
| | | | Not acknowledge |
| | | Master | Stop |

PLL3 CONFIG TABLE⁽¹⁾

| PLL#_CFB[3,2,1,0] | | Comments |
|-------------------|----------------------|---------------------------------|
| 0000 | PLL3 Disabled | PLL3 off, SRC1 = SRC_Main |
| 0001 | 100MHz 0.5% SSC Stby | PLL3 on, SRC1 = SRC_Main |
| 0010 | 100MHz 0.5% SSC | only SRC1 sourced from PLL3 |
| 0011 | 100MHz 1.0% SSC | only SRC1 sourced from PLL3 |
| 0100 | 100MHz 1.5% SSC | only SRC1 sourced from PLL3 |
| 0101 | 100MHz 2.0% SSC | only SRC1 sourced from PLL3 |
| 0110 | 100MHz 2.5% SSC | only SRC1 sourced from PLL3 |
| 0111 | Reserved | Reserved |
| 1000 | 1394A 3.3V | only 1394A on SE1 and SE2 |
| 1001 | 1394A&B 3.3V | only 1394A on SE1, 1394B on SE2 |
| 1010 | 1394B 3.3V | only 1394B on SE1 and SE2 |
| 1011 | 27MHz, 3.3V | only 27MHz on SE1 and SE2 |
| 1100 | 25MHz 3.3V | only 25MHz on SE1 and SE2 |
| 1101 | Reserved | Reserved |
| 1110 | Reserved | Reserved |
| 1111 | Reserved | Reserved |

NOTE:

1. PLL3 spread depend on byte4 bit0 and byte1 bit5, default -0.5%.

DEVICE ID TABLE

| ID3,ID2,ID1,ID0 | | Comments |
|-----------------|--------------------|---------------------------|
| 0000 | CK505 56 pin TSSOP | CK505 YC |
| 0001 | CK505 64 pin TSSOP | CK505 YC |
| 0010 | 48 pin QFN | CK505 YC |
| 0011 | 56 pin QFN | CK505 YC |
| 0100 | 64 pin QFN | CK505 YC |
| 0101 | 72 pin QFN | CK505 YC |
| 0110 | 48 pin SSOP | CK505 YC |
| 0111 | 56 pin SSOP | CK505 YC |
| 1000 | Reserved | CK505 Derivative (non YC) |
| 1001 | Reserved | |
| 1010 | Reserved | |
| 1011 | Reserved | |
| 1100 | Reserved | |
| 1101 | Reserved | |
| 1110 | Reserved | |
| 1111 | Reserved | |

IO_VOUT [2:0] TABLE

| | |
|-----|------|
| 000 | 0.3V |
| 001 | 0.4V |
| 010 | 0.5V |
| 011 | 0.6V |
| 100 | 0.7V |
| 101 | 0.8V |
| 110 | 0.9V |
| 111 | 1V |

IB TABLE

| IB1, IB0 | CPU Frequency |
|----------|---------------------------|
| 01 | (N + 0.3333) * resolution |
| 10 | (N + 0.6666) * resolution |
| 00, 11 | N * resolution |

N-PROGRAMMING PROCEDURE

SRC

1. Power on SRC frequency = 100MHz.
2. To change SRC frequency from 100MHz to 50MHz, divide 50 by 0.5 (50 / 0.5 = 100 [decimal] = 64 [hex]).
3. Program Byte 18 with 64h. SRC frequency changes from 100MHz to 50MHz.

CPU

1. Power on CPU frequency = 200MHz. Resolution corresponding to 200MHz is 1.0
2. To change CPU frequency from 200MHz to 100MHz, divide 100 by 1.0- (100 / 1.0 = 100 [decimal] = 64 [hex]).
3. Program Byte 17 with 64h. CPU frequency changes from 200MHz to 100MHz.

CONTROL REGISTERS

BYTE 0

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|------------------------------|-------------------------------------|------|------------------------------|
| 7 | FSC | Latched FSC | | | R | Latched Value |
| 6 | FSB | Latched FSB | | | R | Latched Value |
| 5 | FSA | Latched FSA | | | R | Latched Value |
| 4 | iAMT_EN | iAMT Mode | Legacy Mode | Enabled | RW | HW M1 setting ⁽¹⁾ |
| 3 | Reserved | | | | | 0 |
| 2 | SRC_SEL | SRC clock source | PLL1, PLL3_CFG table applies | PLL3, PLL3_CFG table not applicable | RW | 0 |
| 1 | SATA_SEL | SATA source | SRC_main | PLL2 ⁽²⁾ | RW | 0 |
| 0 | PD_Restore | SMBUS control registers setting after the power down | Power on default | Save register contents | RW | 1 |

NOTES:

1. Sticky 1, can only be reset by power off.
2. 100MHz, no SSC.

BYTE 1

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|-------------|--------------------|------|----------|
| 7 | SRC0_sel | Pin13/14 mode select | SRC0 | DOT96 | RW | 0 |
| 6 | PLL1_SSC_DC | SSC mode selection | Down spread | Center spread | RW | 0 |
| 5 | PLL3_SSC_DC | SSC mode selection | Down spread | Center spread | RW | 0 |
| 4 | PLL3_CFB3 | | | | RW | 0 |
| 3 | PLL3_CFB2 | Only valid if Byte0 bit2 = 0 See PLL3_CFB table, configure pin17, 18 output mode | | | RW | 0 |
| 2 | PLL3_CFB1 | | | | RW | 0 |
| 1 | PLL3_CFB0 | | | | RW | 1 |
| 0 | PCI | PCI select | PLL1 | SRC, as byte0 bit2 | RW | 1 |

BYTE 2

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------|----------|--------|------|----------|
| 7 | REF | Output Enable | Tristate | Enable | RW | 1 |
| 6 | USB_48 | Output Enable | Tristate | Enable | RW | 1 |
| 5 | PCIF5 | Output Enable | Tristate | Enable | RW | 1 |
| 4 | PCI4 | Output Enable | Tristate | Enable | RW | 1 |
| 3 | PCI3 | Output Enable | Tristate | Enable | RW | 1 |
| 2 | PCI2 | Output Enable | Tristate | Enable | RW | 1 |
| 1 | PCI1 | Output Enable | Tristate | Enable | RW | 1 |
| 0 | PCI0 | Output Enable | Tristate | Enable | RW | 1 |

BYTE 3

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------|----------|---------|------|----------|
| 7 | Reserved | | | | RW | 1 |
| 6 | Reserved | | | | RW | 1 |
| 5 | Reserved | | | | RW | 1 |
| 4 | SRC8/ITP | Output Enable | Tristate | Enabled | RW | 1 |
| 3 | SRC7 | Output Enable | Tristate | Enabled | RW | 1 |
| 2 | SRC6 | Output Enable | Tristate | Enabled | RW | 1 |
| 1 | SRC5 | Output Enable | Tristate | Enabled | RW | 1 |
| 0 | SRC4 | Output Enable | Tristate | Enabled | RW | 1 |

BYTE 4

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|----------------------|----------|---------|------|----------|
| 7 | SRC3 | Output Enable | Disabled | Enabled | RW | 1 |
| 6 | SATA/SRC2 | Output Enable | Disabled | Enabled | RW | 1 |
| 5 | SRC1 | Output Enable | Disabled | Enabled | RW | 1 |
| 4 | SRC0/DOT96 | Output Enable | Disabled | Enabled | RW | 1 |
| 3 | CPU1 | Output Enable | Disabled | Enabled | RW | 1 |
| 2 | CPU0 | Output Enable | Disabled | Enabled | RW | 1 |
| 1 | PLL1_SSC_ON | SSC Enable | Disabled | Enabled | RW | 1 |
| 0 | PLL3_SSC_ON | SSC Enable | Disabled | Enabled | RW | 1 |

BYTE 5

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|-------------------------|---------------------|------------|------|----------|
| 7 | CR#_A | Pin1 mode selection | PCI0 mode | CR#_A mode | RW | 0 |
| 6 | CR#_A control | CR#_A control selection | SRC0 | SRC2 | RW | 0 |
| 5 | CR#_B | Pin3 mode selection | PCI1 mode | CR#_B mode | RW | 0 |
| 4 | CR#_B control | CR#_B control selection | SRC1 ⁽¹⁾ | SRC4 | RW | 0 |
| 3 | CR#_C | Pin24 mode selection | SRCT3 mode | CR#_C mode | RW | 0 |
| 2 | CR#_C control | CR#_C control selection | SRC0 | SRC2 | RW | 0 |
| 1 | CR#_D | Pin25 mode selection | SRCC3 mode | CR#_D mode | RW | 0 |
| 0 | CR#_D control | CR#_D control selection | SRC1 | SRC4 | RW | 0 |

NOTE:

1. Only when SRC1 is SRC Clock.

BYTE 6⁽¹⁾

| Bit | Output(s) Affected | Description/Function | 0 | 1 | Type | Power On |
|-----|--------------------|-------------------------------------|-------------|------------|------|----------|
| 7 | CR#_E | Pin 35 mode selection, control SRC6 | SRCC7 mode | CR#_E mode | RW | 0 |
| 6 | CR#_F | Pin 36 mode selection, control SRC8 | SRCT7 mode | CR#_F mode | RW | 0 |
| 5 | Reserved | | | | RW | 0 |
| 4 | Reserved | | | | RW | 0 |
| 3 | Reserved | | | | RW | 0 |
| 2 | Reserved | | | | RW | 0 |
| 1 | SSCD_STP_CRTL | If set, SSCD stop with PCI_STOP# | Freerunning | Stoppable | RW | 0 |
| 0 | SRC_STP_CRTL | If set, SRCs stop with PCI_STOP# | Freerunning | Stoppable | RW | 0 |

NOTE:

1. STOP - CPUT and SRCT stay high, CPUC and SRCC stay low.

BYTE 7

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|---|------|----------|
| 7 | | Revision ID | | | | 0 |
| 6 | | Revision ID | | | | 0 |
| 5 | | Revision ID | | | | 0 |
| 4 | | Revision ID | | | | 0 |
| 3 | | Vendor ID | | | | 0 |
| 2 | | Vendor ID | | | | 1 |
| 1 | | Vendor ID | | | | 0 |
| 0 | | Vendor ID | | | | 1 |

BYTE 8

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|----------|---------|------|----------|
| 7 | Device_ID3 | See device ID table | | | R | |
| 6 | Device_ID2 | | | | R | |
| 5 | Device_ID1 | | | | R | |
| 4 | Device_ID0 | | | | R | |
| 3 | | | | | RW | 0 |
| 2 | | | | | RW | 0 |
| 1 | SE1_OE | Output Enable | Disabled | Enabled | RW | 0 |
| 0 | SE2_OE | Output Enable | Disabled | Enabled | RW | 0 |

BYTE 9

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|----------------------|--------------------------------------|------------------|--------------------------------------|------|----------|
| 7 | PCIF5 with PCI_STOP# | Freerunning | Free running | stoppable | RW | 0 |
| 6 | LTE_STRAP | Over-clocking Enable (N programming) | normal | No overclocking | R | 0 |
| 5 | REF Drive Strength | Strength control | 1x | 2x | RW | 1 |
| 4 | | Only valid when Byte9 bit3 is 1 | Hi-Z | REF/N mode | RW | 0 |
| 3 | | Test Mode entry control | Normal operation | Test mode, controlled by byte9 bit 4 | RW | 0 |
| 2 | IO_VOUT2 | | | | RW | 1 |
| 1 | IO_VOUT1 | Programmable IO_Vout voltage | | | RW | 0 |
| 0 | IO_VOUT0 | | | | RW | 1 |

BYTES 10 + 11 - RESERVED

BYTE 12 - BYTE COUNT - DEFAULT 0x0D

BYTE 13

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|------------------------|---|-----|------|----------|
| 7 | 48M | Strength control | 1 | 1.2 | RW | 0 |
| 6 | REF | Strength control | 1 | 1.2 | RW | 0 |
| 5 | PCIF5 | Strength control | 1 | 1.2 | RW | 0 |
| 4 | PCI4 | Strength control | 1 | 1.2 | RW | 0 |
| 3 | PCI3 | Strength control | 1 | 1.2 | RW | 0 |
| 2 | PCI2 | Strength control | 1 | 1.2 | RW | 0 |
| 1 | PCI1 | Strength control | 1 | 1.2 | RW | 0 |
| 0 | PCI0 | Strength control | 1 | 1.2 | RW | 0 |

BYTE 14

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|------------------------|----------------------------|-------|-------|------|----------|
| 7 | SRC skew selection | | 250ps | 400ps | RW | 0 |
| 6 | Reserved | | | | RW | 0 |
| 5 | Reserved | | | | RW | 0 |
| 4 | SRC3, 4, 5, 6 | Strength(output impedance) | 17Ω | 25Ω | RW | 0 |
| 3 | SRC2, 7, 8 | Strength | 17Ω | 25Ω | RW | 0 |
| 2 | CPU strength | Strength | 17Ω | 25Ω | RW | 0 |
| 1 | SRC0/ DOT strength | Strength | 17Ω | 25Ω | RW | 0 |
| 0 | SRC1/ PLL3CLK Strength | Strength | 17Ω | 25Ω | RW | 0 |

BYTE 15, WATCH DOG⁽¹⁾

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|-----------------------------|--|-----------------|---------------------|------|----------|
| 7 | Watch Dog Enable | Watch Dog Alarm Enable | Disabled | Enabled | RW | 0 |
| 6 | Watch Dog Select | Watch Dog Hard/Soft Alarm Select | Hard Alarm Only | Hard and Soft Alarm | RW | 0 |
| 5 | Watch Dog Hard Alarm Status | Watch Dog Hard Alarm Status | Normal | Alarm | R | |
| 4 | Watch Dog Soft Alarm Status | Watch Dog Soft Alarm Status | Normal | Alarm | R | |
| 3 | Watch Dog control | Watch Dog Time Base Control | 290ms base | 1160ms base | RW | 0 |
| 2 | WD_1_Timer2 | WatchDog_1_Alarm Timer Default is 7*290ms | | | RW | 1 |
| 1 | WD_1_Timer1 | | | | RW | 1 |
| 0 | WD_1_Timer0 | | | | RW | 1 |

NOTE:

1. Hard Alarm switch to HW FS frequency.

BYTE 16

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|---|--------------|---------|------|----------|
| 7 | WDEAPD | Set Byte15 bit7 = 1 after Power Down to enable the watch dog after the power down | Disabled | Enabled | RW | 0 |
| 6 | Reserved | | | | RW | 0 |
| 5 | Reserved | | | | RW | 0 |
| 4 | Reserved | | | | RW | 0 |
| 3 | Reserved | | | | RW | 0 |
| 2 | IB1 | Increment bit1, fine tune CPU frequency | See IB table | | RW | 0 |
| 1 | IB0 | Increment bit0 | See IB table | | RW | 0 |
| 0 | CPUN8 | | | | RW | FS latch |

BYTE 17 (PLL1)

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|---|---|------|----------|
| 7 | CPUN7 | CPU frequency = N*Resolution (see Resolution table, N-Programming Procedure) | | | RW | FS latch |
| 6 | CPUN6 | | | | RW | |
| 5 | CPUN5 | | | | RW | |
| 4 | CPUN4 | | | | RW | |
| 3 | CPUN3 | | | | RW | |
| 2 | CPUN2 | | | | RW | |
| 1 | CPUN1 | | | | RW | |
| 0 | CPUN0 | | | | RW | |

BYTE 18 (PLL3)

| Bit | Output(s) Affected | Description / Function | 0 | 1 | Type | Power On |
|-----|--------------------|--|---|---|------|----------|
| 7 | PN 7 | SRC frequency = N*Resolution (see Resolution table, N-Programming Procedure) | | | RW | 100MHz |
| 6 | PN 6 | | | | RW | |
| 5 | PN 5 | | | | RW | |
| 4 | PN 4 | | | | RW | |
| 3 | PN 3 | | | | RW | |
| 2 | PN 2 | | | | RW | |
| 1 | PN 1 | | | | RW | |
| 0 | PN 0 | | | | RW | |

BYTE 19, CLOCK SOURCE SELECTION, WRITEN AFTER STOP BIT

| Bit | Output(s) affected | Description/ Function | 0 | 1 | Type | Power On |
|-----|----------------------|--|--|--------------------------|------|--------------------|
| 7 | CPU MODE Control | Will be reset to 0 during the Hard Alarm | CPU Mode is based on Hardware SFS | CPU Mode is based on SFS | RW | 0 |
| 6 | SFSC | | | | RW | LATCH |
| 5 | SFSB | | | | RW | Latch |
| 4 | SFSA | | | | RW | Latch |
| 3 | N programming enable | | enable | disable | RW | Power on LTE latch |
| 2 | SRC1 source | | controlled by PLL3_CFB[3:0] and byte0 bit2 | PLL2 | RW | 0 |
| 1 | PCI source | | Follow byte1 bit0 | PLL2 | RW | 0 |
| 0 | Reserved | - | - | - | - | 0 |

DC OPERATING CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------------------|---|---------------------------------------|-----------------------|-----------------------|------|
| V _{DD_3.3} | Supply Voltage | 5 % | 3.125 | 3.465 | V |
| V _{IH} | Input HIGH Voltage (SE) ⁽¹⁾ | | 2 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage (SE) ⁽¹⁾ | | V _{SS} - 0.3 | 0.8 | V |
| V _{IH_FS_Test} | Input HIGH Voltage (SE) ⁽²⁾ | | 2 | V _{DD} + 0.3 | V |
| V _{IH_FS_Normal} | Input HIGH Voltage (FS) ⁽²⁾ | | 0.7 | 1.5 | V |
| V _{IL_FS_Normal} | Input LOW Voltage (FS) ⁽²⁾ | | V _{SS} - 0.3 | 0.35 | V |
| I _{IL} | Input Leakage Current ⁽³⁾ | 0 < V _{IN} < V _{DD} | -5 | +5 | μA |
| V _{OH} | Output HIGH Voltage (SE) ⁽⁴⁾ | I _{OH} = -1 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage (SE) ⁽⁴⁾ | I _{OL} = 1 mA | — | .4 | V |
| V _{DD_IO} | LOW Voltage Differential | | 0.72 | 0.88 | V |
| C _{IN} | Input Pin Capacitance | | 1.5 | 5 | pF |
| C _{OUT} | Output Pin Capacitance | | — | 6 | pF |
| I _{DD_CFG1_3.3V} | Operating Supply Current, default configuration | | — | 250 | mA |
| I _{DD_CFG2_3.3V} | Operating Supply Current, PLL3 differential out | | — | 250 | mA |
| I _{DD_CFG3_3.3V} | Operating Supply Current, PLL3 single-ended out | | — | 250 | mA |
| I _{DD_IO_0.8V} | Differential IO Current, all outputs enabled | | 25 | 80 | mA |
| I _{DD_PWRDWN_3.3V} | Power Down Supply Current | | — | 1 | mA |
| I _{DD_PWRDWN_0.8V} | Power Down Supply Current | | — | 0.1 | mA |
| I _{DD_M1_3.3V} | MT Mode Supply Current | | — | 25 | mA |
| I _{DD_M1_0/8V} | MT Mode Supply Current | | — | 0.8 | mA |

NOTES:

1. All inputs referenced to 3.3V power supply.
2. Frequency select inputs which have tri-level input.
3. Input leakage current does not include inputs with pull-up or pull-down resistors.
4. Signal edge is required to be monotonic when transitioning through this region.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 DIFFERENTIAL PAIR⁽¹⁾

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = 0°C to +70°C, Supply Voltage: VDD = 3.3V ± 5%; CL = 2pF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------|---------------------------------------|---|---------|------|---------|------|
| VHIGH | Voltage HIGH ⁽²⁾ | Statistical measurement on single-ended signal using oscilloscope math function | 660 | — | 850 | mV |
| VLOW | Voltage LOW ⁽²⁾ | | -150 | — | +150 | |
| VOVS | Max Voltage ⁽²⁾ | Measurement on single-ended signal using absolute value | — | — | 1150 | mV |
| VUDS | Min Voltage ⁽²⁾ | | -300 | — | — | |
| VCROSS(ABS) | Crossing Voltage (abs) ⁽²⁾ | | 250 | — | 550 | mV |
| d - VCROSS | Crossing Voltage (var) ⁽²⁾ | Variation of crossing over all edges | — | — | 140 | mV |
| ppm | Static Error ^(2,3) | See TPERIOD Min. - Max. values | — | — | 0 | ppm |
| TPERIOD | Average Period ⁽³⁾ | 400MHz nominal / -0.5% spread | 2.4993 | — | 2.5133 | ns |
| | | 333.33MHz nominal / -0.5% spread | 2.9991 | — | 3.016 | |
| | | 266.66MHz nominal / -0.5% spread | 3.7489 | — | 3.77 | |
| | | 200MHz nominal / -0.5% spread | 4.9985 | — | 5.0266 | |
| | | 166.66MHz nominal / -0.5% spread | 5.9982 | — | 6.032 | |
| | | 133.33MHz nominal / -0.5% spread | 7.4978 | — | 7.54 | |
| | | 100MHz nominal / -0.5% spread | 9.997 | — | 10.0533 | |
| | | 96MHz nominal | 10.4135 | — | 10.4198 | |
| TABSMIN | Absolute Min Period ^(2,3) | 400MHz nominal / -0.5% spread | 2.4143 | — | — | ns |
| | | 333.33MHz nominal / -0.5% spread | 2.9141 | — | — | |
| | | 266.66MHz nominal / -0.5% spread | 3.6639 | — | — | |
| | | 200MHz nominal / -0.5% spread | 4.9135 | — | — | |
| | | 166.66MHz nominal / -0.5% spread | 5.9132 | — | — | |
| | | 133.33MHz nominal / -0.5% spread | 7.4128 | — | — | |
| | | 100MHz nominal / -0.5% spread | 9.912 | — | — | |
| | | 96MHz nominal | 10.1635 | — | — | |
| tr | Rise Time ⁽²⁾ | VOL = 0.175V, VOH = 0.525V | 175 | — | 700 | ps |
| tf | Fall Time ⁽²⁾ | VOL = 0.175V, VOH = 0.525V | 175 | — | 700 | ps |
| d-tr | Rise Time Variation ⁽²⁾ | | — | — | 125 | ps |
| d-tf | Fall Time Variation ⁽²⁾ | | — | — | 125 | ps |
| dt3 | Duty Cycle ⁽²⁾ | Measurement from differential waveform | 45 | — | 55 | % |

NOTES:

- SRC clock outputs run only at 100MHz.
- This parameter is guaranteed by design, but not 100% production tested.
- All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR, CONTINUED⁽¹⁾

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 2\text{pF}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|---|--|------|------|------|------|
| tsk3 | Skew, CPU[1:0] ⁽²⁾ | $V_T = 50\%$ | — | — | 100 | ps |
| | Skew, CPU2 ⁽²⁾ | | — | — | 250 | |
| | Skew, SRC ⁽²⁾ | | — | — | 250 | |
| t _{cy-cyc} | Jitter, Cycle to Cycle, CPU[1:0] ⁽²⁾ | Measurement from differential waveform | — | — | 85 | ps |
| | Jitter, Cycle to Cycle, CPU2 ⁽²⁾ | | — | — | 100 | |
| | Jitter, Cycle to Cycle, SRC ⁽²⁾ | | — | — | 125 | |
| | Jitter, Cycle to Cycle, DOT96 ⁽²⁾ | | — | — | 250 | |

NOTES:

- SRC clock outputs run only at 100MHz.
- This parameter is guaranteed by design, but not 100% production tested.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10 - 30\text{pF}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|---------------------------------------|--|--------|------|---------|------|
| ppm | Static Error ^(1,2) | See Tperiod Min. - Max. values | — | — | 0 | ppm |
| T _{PERIOD} | Clock Period ⁽²⁾ | 33.33MHz output nominal | 29.991 | — | 30.009 | ns |
| | | 33.33MHz output spread | 29.991 | — | 30.1598 | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -1mA | 2.4 | — | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 1mA | — | — | 0.55 | V |
| I _{OH} | Output HIGH Current | V _{OH} at Min. = 1V | -33 | — | — | mA |
| | | V _{OH} at Max. = 3.135V | — | — | -33 | |
| I _{OL} | Output LOW Current | V _{OL} at Min. = 1.95V | 30 | — | — | mA |
| | | V _{OL} at Max. = 0.4V | — | — | 38 | |
| | Edge Rate ⁽¹⁾ | Rising edge rate | 1 | — | 4 | V/ns |
| | Edge Rate ⁽¹⁾ | Falling edge rate | 1 | — | 4 | V/ns |
| t _{R1} | Rise Time ⁽¹⁾ | V _{OL} = 0.8V, V _{OH} = 2V | 0.3 | — | 1.2 | ns |
| t _{F1} | Fall Time ⁽¹⁾ | V _{OL} = 0.8V, V _{OH} = 2V | 0.3 | — | 1.2 | ns |
| d _{T1} | Duty Cycle ⁽¹⁾ | V _T = 1.5V | 45 | — | 55 | % |
| tsk1 | Skew ⁽¹⁾ | V _T = 1.5V | — | — | 250 | ps |
| t _{cy-cyc} | Jitter, Cycle to Cycle ⁽¹⁾ | V _T = 1.5V | — | — | 500 | ps |

NOTES:

- This parameter is guaranteed by design, but not 100% production tested.
- All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10 - 20\text{pF}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------|-------------------------------|--------------------------------|---------|------|--------|------|
| ppm | Static Error ^(1,2) | See Tperiod Min. - Max. values | — | — | 0 | ppm |
| TPERIOD | Clock Period ⁽²⁾ | 48MHz output nominal | 20.8257 | — | 20.834 | ns |
| VOH | Output HIGH Voltage | IOH = -1mA | 2.4 | — | — | V |
| VOL | Output LOW Voltage | IOL = 1mA | — | — | 0.55 | V |
| IOH | Output HIGH Current | VOH at Min. = 1V | -29 | — | — | mA |
| | | VOH at Max. = 3.135V | — | — | -23 | |
| IOL | Output LOW Current | VOL at Min. = 1.95V | 29 | — | — | mA |
| | | VOL at Max. = 0.4V | — | — | 27 | |
| | Edge Rate ⁽¹⁾ | Rising edge rate | 1 | — | 2 | V/ns |
| | Edge Rate ⁽¹⁾ | Falling edge rate | 1 | — | 2 | V/ns |
| tr1 | Rise Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.5 | — | 1.2 | ns |
| tf1 | Fall Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.5 | — | 1.2 | ns |
| dT1 | Duty Cycle ⁽¹⁾ | VT = 1.5V | 45 | — | 55 | % |
| tCYC-CYC | Jitter, Cycle to Cycle | | — | — | 350 | ps |

NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Supply Voltage: $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10 - 20\text{pF}$

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------|---------------------------------------|--------------------------------|--------|------|--------|------|
| ppm | Long Accuracy ⁽¹⁾ | See Tperiod Min. - Max. values | — | — | 0 | ppm |
| TPERIOD | Clock Period | 14.318MHz output nominal | 69.827 | — | 69.855 | ns |
| VOH | Output HIGH Voltage ⁽¹⁾ | IOH = -1mA | 2.4 | — | — | V |
| VOL | Output LOW Voltage ⁽¹⁾ | IOL = 1mA | — | — | 0.4 | V |
| IOH | Output HIGH Current | VOH at Min. = 1V | -33 | — | — | mA |
| | | VOH at Max. = 3.135V | — | — | -33 | |
| IOL | Output LOW Current | VOL at Min. = 1.95V | 30 | — | — | mA |
| | | VOL at Max. = 0.4V | — | — | 38 | |
| | Edge Rate ⁽¹⁾ | Rising edge rate | 1 | — | 4 | V/ns |
| | Edge Rate ⁽¹⁾ | Falling edge rate | 1 | — | 4 | V/ns |
| tr1 | Rise Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.3 | — | 1.2 | ns |
| tf1 | Fall Time ⁽¹⁾ | VOL = 0.8V, VOH = 2V | 0.3 | — | 1.2 | ns |
| dT1 | Duty Cycle ⁽¹⁾ | VT = 1.5V | 45 | — | 55 | % |
| tCYC-CYC | Jitter, Cycle to Cycle ⁽¹⁾ | VT = 1.5V | — | — | 1000 | ps |

NOTE:

1. This parameter is guaranteed by design, but not 100% production tested.

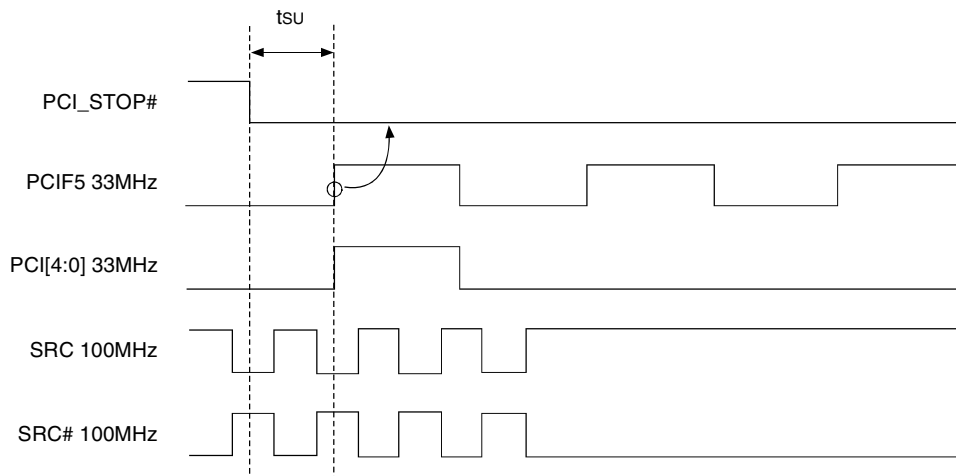
MISC. AC TIMING REQUIREMENTS

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------------------|--|------|------|------|
| T _{STABLE} | All Clock Stabilization from Power-Up | — | <1.8 | ns |
| T _{DRIVE_SRC} | SRC Output Driven After PCI_STOP# De-assertion | — | 15 | ns |
| T _{DRIVE_PCI} | PCI Output Driven After PCI_STOP# De-assertion | — | 15 | us |
| T _{DRIVE_CR#} | SRC Output Driven After CR# De-assertion | — | 15 | ns |
| T _{DRIVE_PWRDWN} | Differential Output Enable after PWRDWN De-assertion | — | 300 | ns |
| T _{RISE_Control_Sig} | Rise Time for All Control Inputs (LVTTTL 20-80%) | — | 10 | us |
| T _{FALL_Control_Sig} | Fall time for All Control Inputs (LVTTTL 20-80%) | — | 10 | ns |

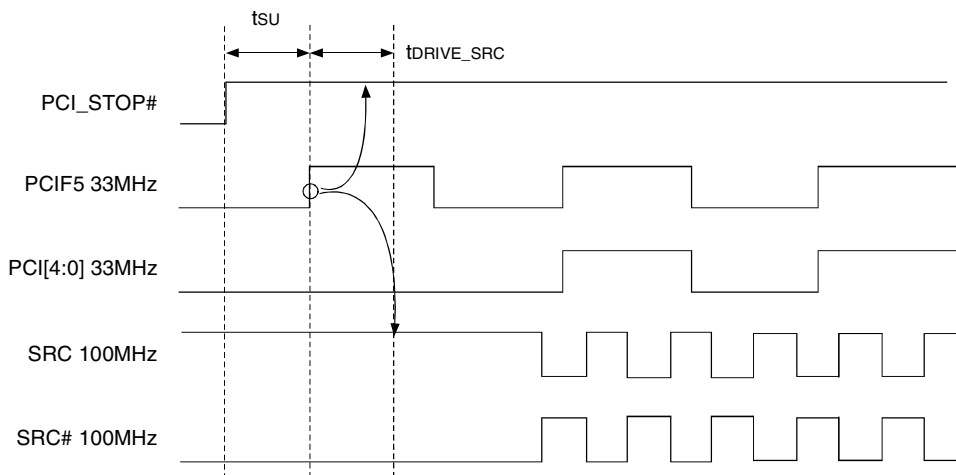
PCI STOP FUNCTIONALITY

| PCI_STOP# | SRC | SRC# | PCI |
|-----------|--------|--------|-------|
| 1 | Normal | Normal | 33MHz |
| 0 | High | Low | Low |

PCI_STOP# ASSERTION (TRANSITION FROM '1' TO '0')



PCI_STOP# - DE-ASSERTION (TRANSITION FROM '0' TO '1')



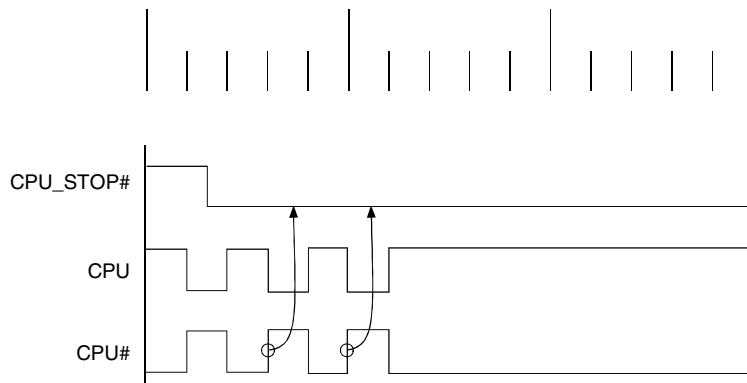
CPU STOP FUNCTIONALITY

The CPU_STOP# signal is an active low input controlling the CPU outputs. This signal can be asserted asynchronously.

| CPU_STOP# | CPU | CPU# |
|-----------|--------|--------|
| 1 | Normal | Normal |
| 0 | High | Low |

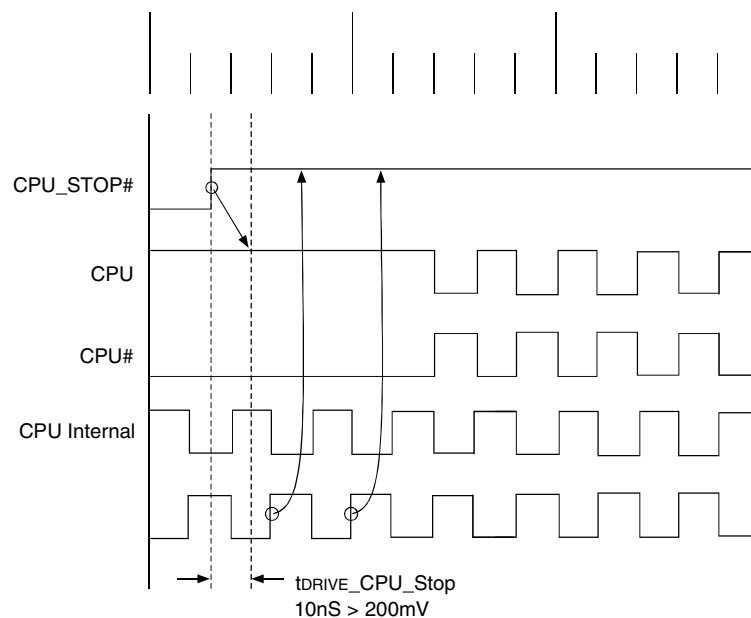
CPU_STOP# ASSERTION (TRANSITION FROM '1' TO '0')

Asserting CPU_STOP# pin stops all CPU outputs that are set to be stoppable after their next transition. When the SMBus CPU_STOP tri-state bit corresponding to the CPU output of interest is programmed to a '0', CPU output will stop CPU_True = High and CPU_Complement = Low. When the SMBus CPU_STOP tri-state bit corresponding to the CPU output of interest is programmed to a '1', CPU outputs will be tri-stated.

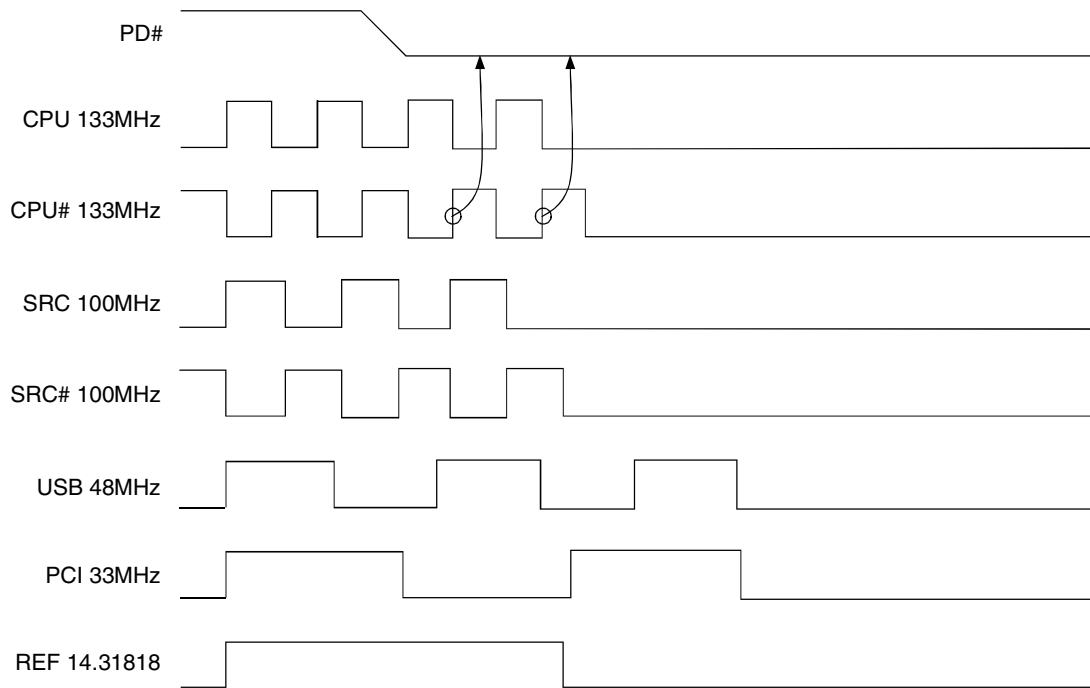


CPU_STOP# - DE-ASSERTION (TRANSITION FROM '0' TO '1')

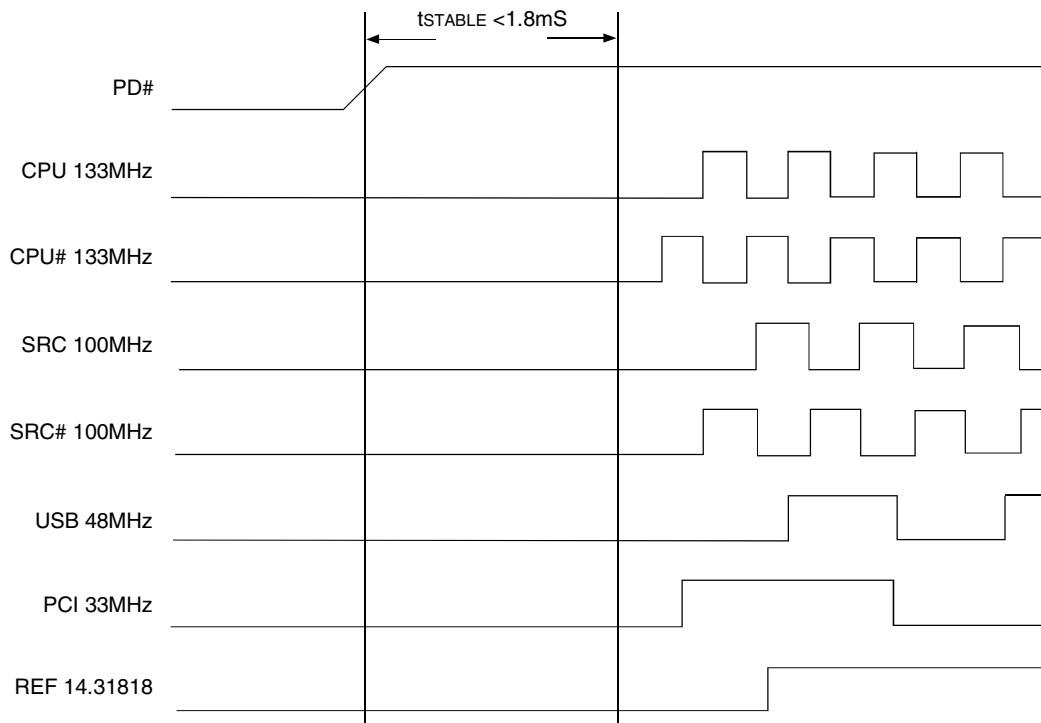
With the de-assertion of CPU_STOP# all stopped CPU outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is two to six CPU clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped CPU outputs will be driven High within 10nS of CPU_STOP# de-assertion to a voltage greater than 200mV.



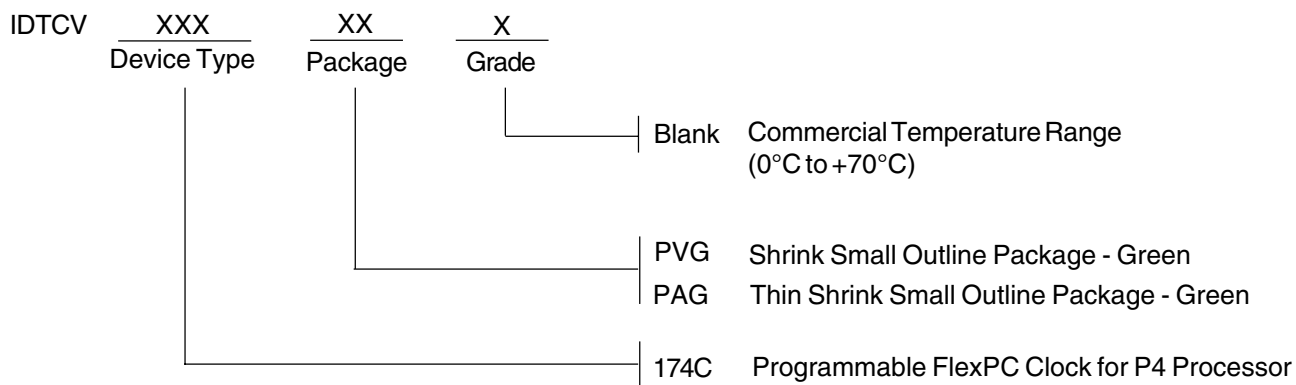
PD# ASSERTION



PD# DE-ASSERTION



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