



**THE DATASHEET OF
HEF4028BP,652**



HEF4028B

BCD to decimal decoder

Rev. 11 — 8 August 2024

Product data sheet

1. General description

The HEF4028B is a 4-bit BCD to 1-of-10 decoder. A 1-2-4-8 BCD code applied to inputs A0 to A3 causes the selected output to be HIGH, the other nine will be LOW. To use as a 1-of-8 decoder with enable, 3-bit octal inputs are applied to inputs A0, A1 and A2 selecting an output Y0 to Y7. Input A3 then becomes an active LOW enable, forcing the selected output LOW when A3 is HIGH. The device may also be used as an 8-output (Y0 to Y7) demultiplexer with A0 to A2 as address inputs and A3 as an active LOW data input. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4028BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

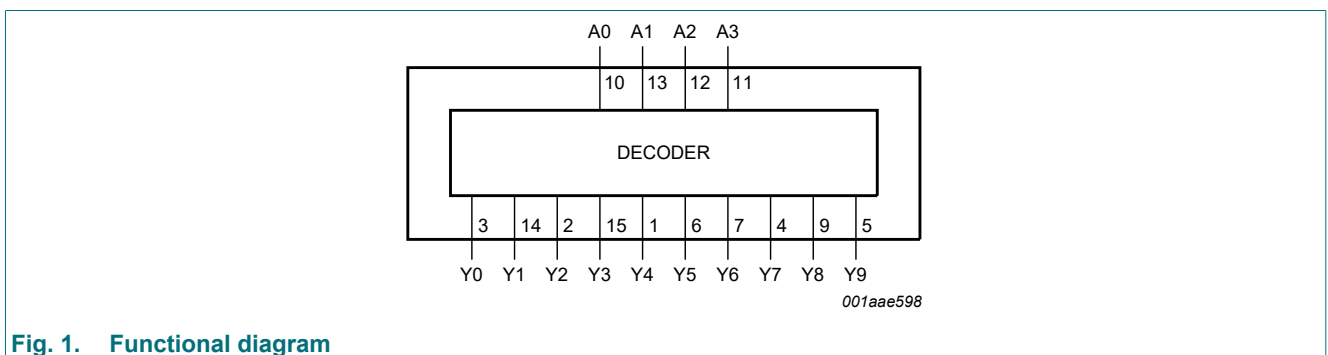


Fig. 1. Functional diagram

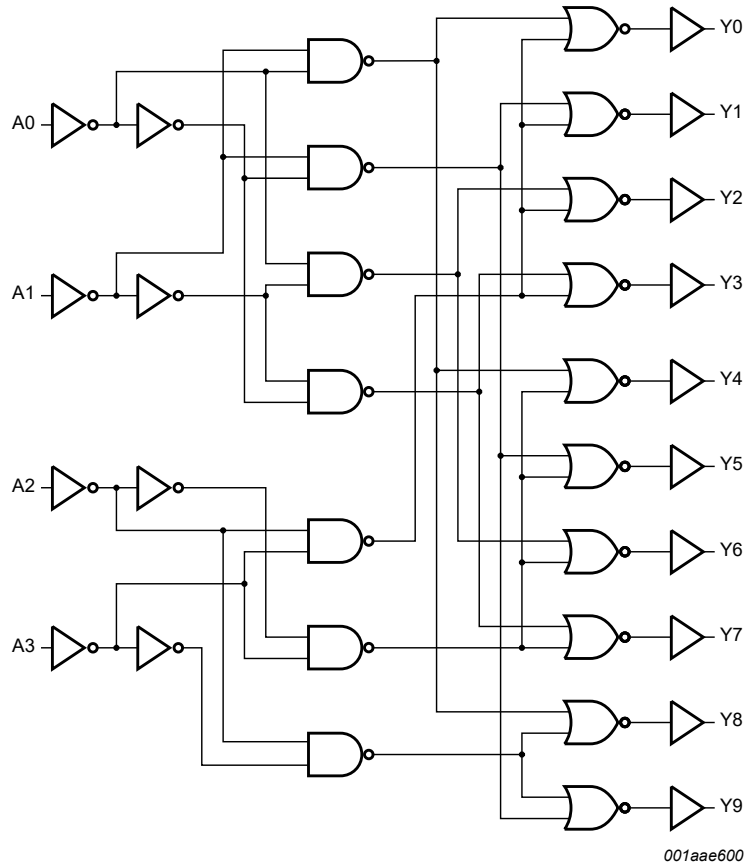
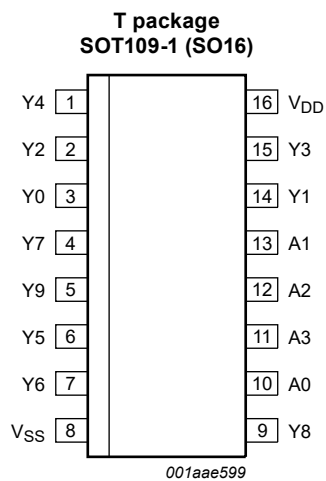


Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9	3, 14, 2, 15, 1, 6, 7, 4, 9, 5	output (active HIGH)
V _{SS}	8	ground supply voltage
A0, A1, A2, A3	10, 13, 12, 11	address input
V _{DD}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs				Outputs									
A3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	X	L	L	L	L	L	L	L	L	L	L
H	H	X	X	L	L	L	L	L	L	L	L	L	L

[1] Extraordinary states.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA
V _I	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	6.25	ms/V
		$V_{DD} = 10\text{ V}$	-	-	0.5	ms/V
		$V_{DD} = 15\text{ V}$	-	-	0.08	ms/V

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} .

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.3	-	± 0.3	-	± 1.0	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for the test circuit, see Fig. 4.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	An to Yn; see Fig. 3	5 V	$73\text{ ns} + (0.55\text{ ns/pF})C_L$	-	100	200	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	An to Yn; see Fig. 3	5 V	$63\text{ ns} + (0.55\text{ ns/pF})C_L$	-	90	180	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t_t	transition time	see Fig. 3	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 350 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 2200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 7350 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

10.1. Waveforms and test circuit

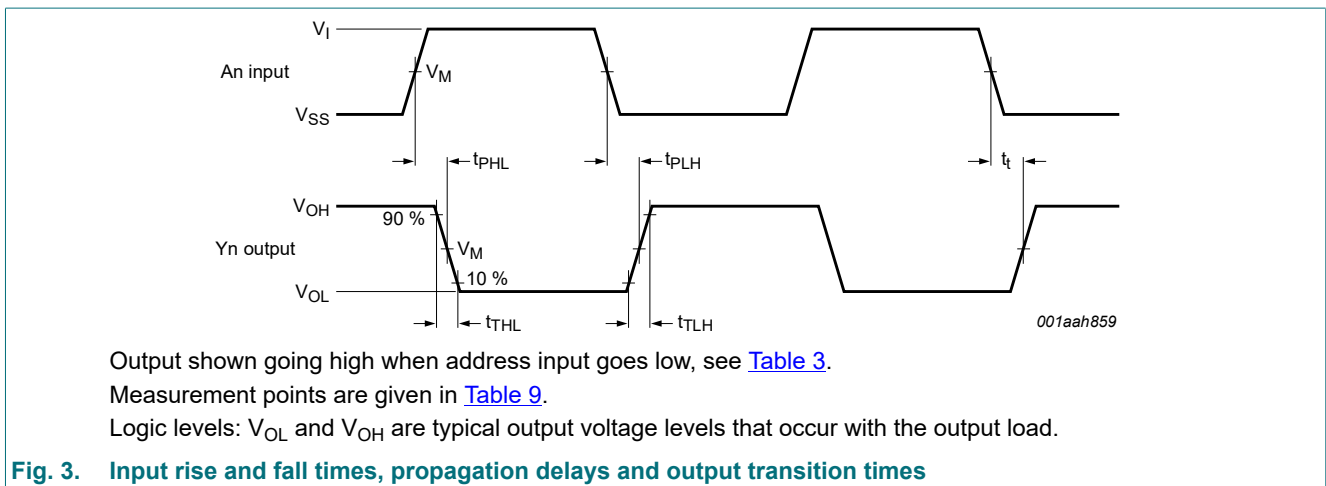
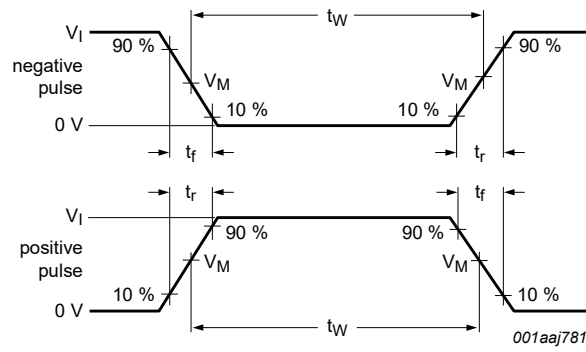


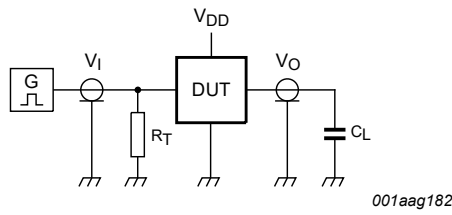
Fig. 3. Input rise and fall times, propagation delays and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



a. Input waveforms



b. Test circuit

Test data is given in [Table 10](#).

Definitions test circuit:

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 4. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

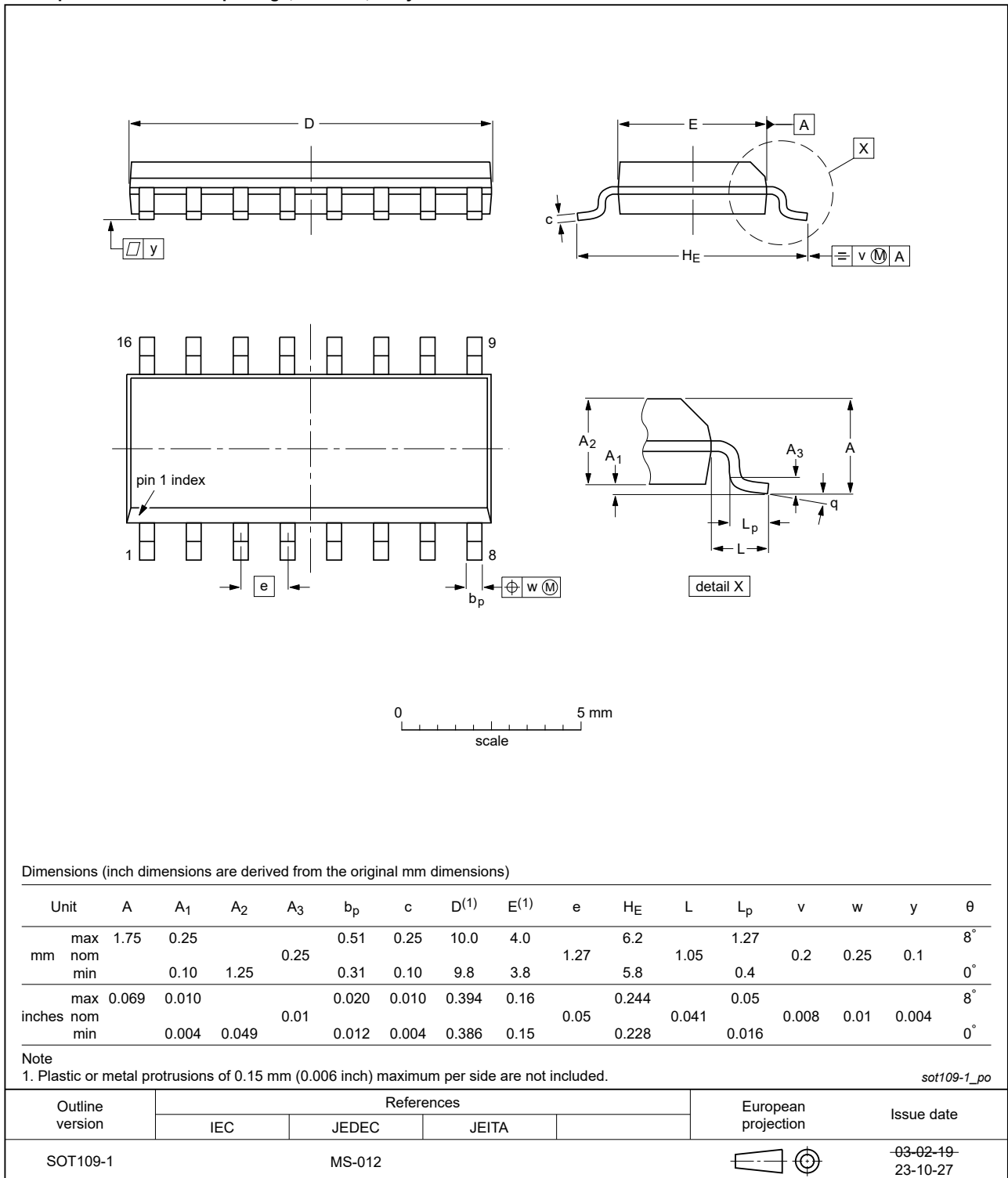


Fig. 5. Package outline SOT109-1 (SO16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BCD	Binary Coded Decimal
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4028B v.11	20240808	Product data sheet	-	HEF4028B v.10
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 5: Aligned SO package outline drawing to JEDEC MS-012 			
HEF4028B v.10	20211207	Product data sheet	-	HEF4028B v.9
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. 			
HEF4028B v.9	20160323	Product data sheet	-	HEF4028B v.8
Modifications:	<ul style="list-style-type: none"> • Type number HEF4028BP (SOT38-4) removed. 			
HEF4028B v.8	20111117	Product data sheet	-	HEF4028B v.7
Modifications:	<ul style="list-style-type: none"> • Legal pages updated. • Changes in Section 1 and Section 2. • Section "Applications" removed. 			
HEF4028B v.7	20111010	Product data sheet	-	HEF4028B v.6
HEF4028B v.6	20091125	Product data sheet	-	HEF4028B v.5
HEF4028B v.5	20090707	Product data sheet	-	HEF4028B v.4
HEF4028B v.4	20090304	Product data sheet	-	HEF4028B_CNV v.3
HEF4028B_CNV v.3	19950101	Product specification	-	HEF4028B_CNV v.2
HEF4028B_CNV v.2	19950101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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