OSD335x-SM Family

Rev. 12 12/1/2024

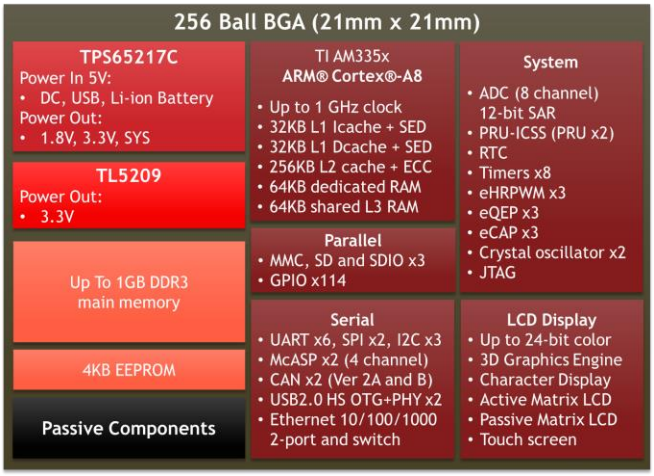
Introduction

The OSD335x-SM Family of System-In-Package (SiP) products are building blocks designed to allow easy and cost-effective implementation of systems based on Texas Instruments' powerful Sitara™ AM335x line of processors. The OSD335x-SM integrates the AM335x along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 Gigabyte (GB) of DDR3 Memory, a 4 Kilobyte (KB) EEPROM for non-volatile configuration storage and resistors, capacitors, and inductors into a single 21mm x 21mm design-in-ready package.

With this level of integration, the OSD335x-SM Family of SiPs allows designers to focus on the key aspects of their system without spending time on the complicated high-speed design of the processor/DDR3 interface or the PMIC power distribution. It also reduces the overall size and complexity of the design and the supply chain. The OSD335x-SM can significantly decrease the time to market for AM335x-based products.

Features

- TI AM335x, TPS65217C, TL5209, DDR3, EEPROM and passive components integrated into a single package
- TI AM335x Features:
  - ARM® Cortex®-A8 up to 1GHz
  - 8 channel 12-bit SAR ADC
  - Ethernet 10/100/1000 x 2
  - USB 2.0 HS OTG + PHY x2
  - MMC, SD and SDIO x3
  - LCD Controller
  - SGX 3D Graphics Engine
  - PRU Subsystem
- Access to all AM335x Peripherals: CAN, SPI, UART, I2C, GPIO, etc.
- Up to 1GB DDR3



OSD335x-SM Block Diagram

- PWR In: AC Adapter, USB or Single cell (1S) Li-Ion / Li-Po Battery
- PWR Out: 1.8V, 3.3V and SYS
- Selectable AM335x I/O Voltage: 1.8V or 3.3V

Benefits

- Integrates over 100 components into one package
- Compatible with AM335x development tools and software
- Wide BGA ball pitch allows for low-cost assembly.
- Significantly reduces design time
- Decreases layout complexity
- 60% reduction in board space vs discrete implementation
- Increased reliability through reduced number of components

Package

- 256 Ball BGA (21mm X 21mm)
- 16 X 16 grid, 1.27mm pitch
- Temp Range: 0 to 85°C, -40 to 85°C

Table of Contents

1 Revision History

Revision Number	Revision Date	Changes	Author
1.0	19 Sept 2017	Initial Release	Greg Sheridan, Erik Welsh
2.0	16 Oct 2017	Added notes for power rails and updated minimum interface connections	Neeraj Dantu
3.0	21 Nov 2017	Updated SYS_VDD2_3P3V max current	Greg Sheridan
4.0	28 December 2017	Updated Mechanical Drawing for Clarity. Fixed table 2.1	Greg Sheridan
5.0	27 January 2018	Adjusted page numbering so they match with PDF page number	Greg Sheridan
6.0	16 February 2018	Updated voltage measurements and notes on EEPROM	Neeraj Dantu
7.0	24 May 2018	Added section on minimum required VDDSHV connections	Neeraj Dantu
8.0	19 March 2018	Updated VIN_BAT information; Passives Table	Erik Welsh
9.0	1 January 2021	Added more Reference Documents, Updated Table 5.6 USB descriptions, added information on Landing Pad Sizes	Gene Frantz
10	1 April 2022	Updated Storage Requirements, Added In-rush current and Rise time Requirements, updated SYS_VDD3_3P3V and SYS_VDD_1P8V	Greg Sheridan
11	22 August 2022	Added PMIC I2C address, Updated Mechanical Specs	Eshtaartha Basu
12	1 December 2024	Updated Storage Requirements	Greg Sheridan

NOTICE: These devices are susceptible to moisture and are classified as **MSL 4**. Ensure you are following the guidelines in the **Storage Requirements** section in this document.

2 Block Diagram

The OSD335x-SM family of devices consist of 5 main components serving 4 distinct functions. The main processor is a Texas Instruments Sitara™ AM335x ARM® Cortex®-A8. The power system has 2 devices from Texas Instruments, the TPS65217C Power Management IC (PMIC) and the TL5209 LDO. The system memory uses up to 1GB DDR3 memory. The last main component is the 4KB EEPROM for configuration data. Figure 2.1 shows a detailed block diagram of the OSD335x and breaks out the key functions of the AM335x processor.

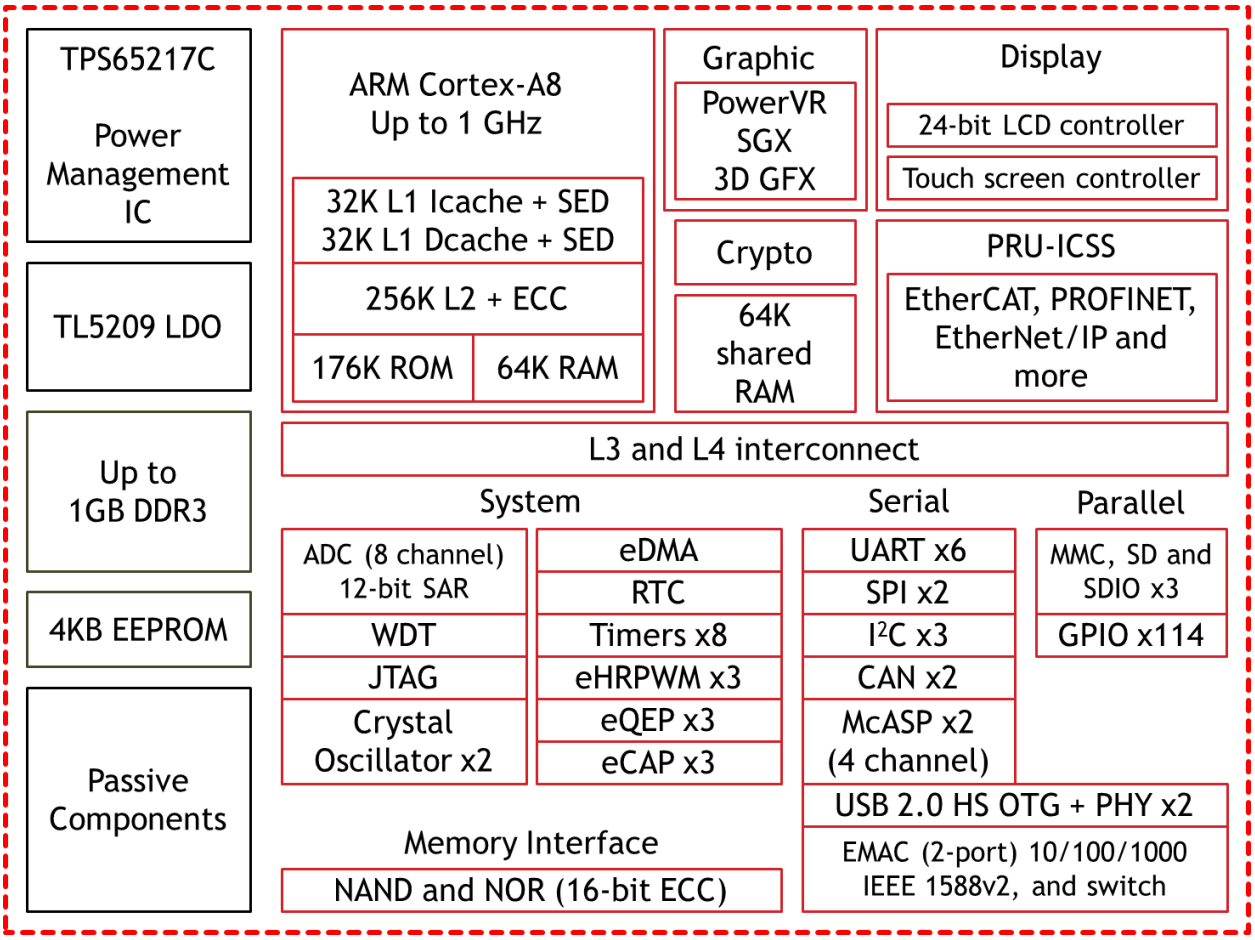


Figure 2.1. OSD335x-SM Detailed Block Diagram

2.1 Passives

Besides the five major components, the OSD335x-SM also integrates capacitors, resistors, inductors, and ferrite beads (Passives). Table 2-2 and Table 2-3 list the information to design around the OSD335x-SM. This includes the approximate bulk capacitance on input and output power rails as well as all pull-up resistor locations and values. The OSD335x-SM does not require any external decoupling / bypass capacitors in most applications. However, it does require additional bulk capacitance on one of the output power rails.

2.1.1 Additional Required Bulk Capacitance

The following output power rails require additional bulk capacitance to avoid in-rush / power up issues.

Table 2-1 - OSD335x-SM Required Additional Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
SYS_VOUT	DGND	TPS65217C	SYS_VOUT output capacitance	C	~50uF

2.1.2 Integrated Bulk Capacitance

The following input and output power have bulk capacitance integrated within the SiP. This table is for informative purposes only.

Table 2-2 - OSD335x-SM Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
VIN_AC	DGND	TPS65217C	VIN_AC input capacitance	C	10uF
VIN_USB	DGND	TPS65217C	VIN_USB input capacitance	C	10uF
VIN_BAT	DGND	TPS65217C	VIN_BAT input capacitance	C	10uF
SYS_VOUT	DGND	TPS65217C	SYS_VOUT output capacitance	C	30uF
SYS_VDD1_3P3V	DGND	TL5209	SYS_VDD1_3P3V output capacitance	C	2.2uF
SYS_VDD2_3P3V	DGND	TPS65217C	SYS_VDD2_3P3V output capacitance	C	2.2uF
SYS_VDD3_3P3V	DGND	TPS65217C	SYS_VDD3_3P3V output capacitance	C	10uF
SYS_VDD_1P8V	DGND	TPS65217C	SYS_VDD_1P8V output capacitance	C	10uF
SYS_RTC_1P8V	DGND	TPS65217C	SYS_RTC_1P8V output capacitance	C	10uF
CAP_VDD_RTC	DGND	AM335x	CAP_VDD_RTC capacitance	C	1uF

2.1.3 Integrated Resistors

The following pins have pull-up or pull-down resistors integrated within the SiP. This table is for informative purposes only.

Table 2-3 - OSD335x-SM Resistors (Pull-ups / Pull-downs)

From	To	Device	Description	Type	Value
PMIC_PWR_EN	SYS_RTC_1P8V	TPS65217C	PWR_EN pull-up	R	4.7K Ohm
EXT_WAKEUP	SYS_RTC_1P8V	AM335x	EXT_WAKEUP input pull-up	R	4.7K Ohm
EXTINTIN	VDDSHV6	AM335x	nNMI pull-up	R	4.7K Ohm
I2C0_SCL	VDDSHV6	AM335x	I2C0 SCL pull-up	R	4.7K Ohm
I2C0_SDA	VDDSHV6	AM335x	I2C0 SDA pull-up	R	4.7K Ohm
EEPROM_WP	VDDSHV6	EEPROM	EEPROM WP pull-up	R	4.7K Ohm

3 Product Number Information

Figure 3.1 shows an example of an orderable product number for the OSD335x-SM family. This section explains the different sections of the product number. It will also list the valid entries and their meaning for each designator.

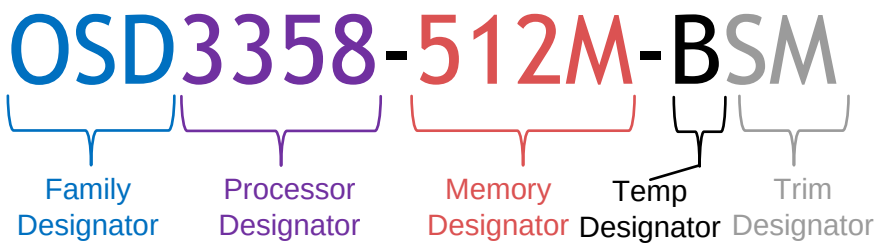


Figure 3.1. Example Product Number

Family Designator – Three letters that designate the family of device.

Family Designator	Family
OSD	OSD Family of devices.

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 3-1 shows the valid values for the Processor Designator.

Table 3-1. Processor Designators

Processor Designator	Processor
3358	Texas Instruments AM3358

Memory Designator – A set of letters and numbers that designate the DDR3 memory size in the device. Table 3-2 shows the valid values for the Memory Designator.

Table 3-2. Memory Designator

Memory Designator	DDR Memory Size
1G	1GB DDR3
512M	512 MB DDR3

Temp Designator – A letter or number that designates the temperature range of the device. Table 3-3 shows the valid values for the Temp Designator.

Table 3-3. Temp Designator

Temp Designator	Temperature Range
B	Commercial: 0 to 85°C
I	Industrial: -40 to 85°C

Trim Designator – A set of letters and numbers that designate the set of features in the device. Table 3-4 shows the valid values for the Trim Designator.

Table 3-4. Trim Designator

Trim Designator	Device Options
SM	Base Model containing the Processer, DDR Memory, PMIC, LDO and 4KB EEPROM in 21mm x 21mm 256 Ball BGA

4 Reference Documents

4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD335x-SM. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD335x-SM system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD335x-SM.

- Processor AM335X http://www.ti.com/product/am3358/datasheet
- PMIC TPS62517C http://www.ti.com/product/TPS65217/datasheet
- LDO TL509 http://www.ti.com/product/TL5209/datasheet
- EEPROM 24LC32A http://www.microchip.com/wwwproducts/en/24LC32A

4.2 Other References

This section contains links to other reference documents that could be helpful when using the OSD335x-SM device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations
  http://www.ti.com/lit/snoa550
- OSD335x-SM Pin Assignments and Application Differences from TI AM3358
  https://octavosystems.com/app_notes/osd335x-family-pin-assignments/
- OSD335x-SM Layout Guide
  https://octavosystems.com/app_notes/osd335x-sm-layout-guide/
- AM335x DR PHY register configuration for DDR3 using Software Leveling
  http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling
- AM335x Power Estimation Tool
  http://processors.wiki.ti.com/index.php/AM335x_Power_Estimation_Tool
- Powering the AM335x with the TPS65217x
  http://www.ti.com/lit/slvu551
- OSD3358-SM Reference, Evaluation and Development Platform
  https://octavosystems.com/octavo_products/osd3358-sm-red/
- Powering the AM335x, AM335x, with LiPo and Li-Ion Batteries
  https://octavosystems.com/app_notes/am335x-battery-applications-with-osd335x-sip/
- OSD335x RTC Use Cases
  https://octavosystems.com/app_notes/osd335x-rtc-use-cases/

5 Ball Map

The pins on the OSD335x-SM belong to 4 distinct categories, AM335x Signals, TPS65217C signals, Oscillators and Power Domains. The signal names for the AM335x and the TPS65217C have been named so they can be easily cross-referenced to the corresponding pin in the TI Datasheet.

All AM335x signals on the OSD335x-SM Ball Map match the signal names of the default functions in the AM335x datasheet.

All the TPS65217C signals have the prefix PMIC_ then the TPS65217C signal name from the TI Datasheet.

NOTE: This is true except for the signal PMIC_POWER_EN which is an AM335x signal.

The arrangement of the signals has been optimized for easy escape of the BGA. Table 5-1 through Table 5-4 show the ball map for the OSD335x-SM.

Table 5-1. OSD335x-SM Ball Map Top View (Columns A-D)

	A	B	C	D
16	MMC0_DAT0	MMC0_CMD	MMC0_DAT2	MII1_RXD1
15	MMC0_DAT1	MMC0_CLK	MMC0_DAT3	MII1_RXD2
14	SPI0_CS0	SPI0_D1	SPI0_CS1	MII1_RXD3
13	SPI0_SCLK	SPI0_D0	UART0_RTSN	MDC
12	UART0_RXD	UART0_TXD	UART0_CTSN	NC
11	UART1_RXD	UART1_TXD	I2C0_SDA	PMIC_SDA
10	UART1_RTSN	UART1_CTSN	I2C0_SCL	PMIC_SCL
9	AGND_ADC	VREFN	AIN6	DGND
8	AIN0	AIN1	AIN5	DGND
7	SYS_ADC_1P8V	VREFP	AIN4	AIN7
6	OSC1_IN	AIN2	AIN3	PMIC_MUX_OUT
5	OSC1_OUT	OSC1_GND	ECAP0_IN_PWM0_OUT	CAP_VDD_RTC
4	XDMA_EVENT_INTR0	XDMA_EVENT_INTR1	MCASP0_AHCLKX	EXTINTN
3	MCASP0_ACLKR	MCASP0_FSR	MCASP0_AXR1	TRSTN
2	MCASP0_FSX	MCASP0_AXR0	TDO	TMS
1	MCASP0_ACLKX	MCASP0_AHCLKR	TDI	TCK

Table 5-2. OSD335x-SM Ball Map Top View (Columns E-H)

	E	F	G	H
16	MII1_RX_CLK	MII1_RX_DV	MII1_TXD2	MII1_TX_CLK
15	MII1_RX_ER	MII1_COL	MII1_TXD3	MII1_TXD0
14	MII1_RXD0	MII1_CRS	MII1_TX_EN	MII1_TXD1
13	MDIO	VDD_MPU	VDDS_PLL	DGND
12	DGND	DGND	DGND	DGND
11	DGND	SYS_VDD2_3P3V	SYS_VDD2_3P3V	SYS_VDD_1P8V
10	DGND	SYS_VDD_1P8V	SYS_VDD_1P8V	SYS_VDD_1P8V
9	DGND	VDDSHV4	VDDSHV5	VDDSHV6
8	DGND	SYS_VDD3_3P3V	SYS_VDD3_3P3V	SYS_VDD3_3P3V
7	DGND	SYS_VDD1_3P3V	SYS_VDD1_3P3V	SYS_VDD3_3P3V
6	DGND	SYS_VDD1_3P3V	SYS_VDD1_3P3V	VPP
5	DGND	DGND	DGND	DGND
4	PMIC_NINT	VDDS_DDR	VDD_CORE	DGND
3	EMU1	LCD_VSYNC	LCD_DATA0	LCD_DATA3
2	EMU0	LCD_HSYNC	LCD_DATA1	LCD_DATA4
1	LCD_AC_BIAS_EN	LCD_PCLK	LCD_DATA2	LCD_DATA5

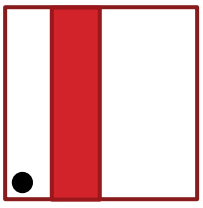


Table 5-3. OSD335x-SM Ball Map Top View (Columns J-M)

	J	K	L	M
16	USB0_VBUS	USB0_DM	USB1_DM	RTC_KALDO_ENN
15	USB0_DRVVBUS	USB0_DP	USB1_DP	USB1_VBUS
14	RMII1_REF_CLK	USB0_ID	USB1_ID	USB1_DRVVBUS
13	DGND	USB0_CE	USB1_CE	PMIC_NRESET
12	DGND	DGND	DGND	DGND
11	SYS_VDD_1P8V	SYS_RTC_1P8V	SYS_RTC_1P8V	DGND
10	SYS_VDD_1P8V	SYS_VDD_1P8V	SYS_VDD_1P8V	DGND
9	VDDSHV1	VDDSHV2	VDDSHV3	DGND
8	SYS_VDD3_3P3V	SYS_VDD3_3P3V	SYS_VDD3_3P3V	DGND
7	SYS_VDD3_3P3V	SYS_VOUT	SYS_VOUT	DGND
6	NC	SYS_VOUT	SYS_VOUT	DGND
5	DGND	DGND	DGND	DGND
4	DGND	NC	PMIC_NWAKEUP	EXT_WAKEUP
3	LCD_DATA6	LCD_DATA9	LCD_DATA12	LCD_DATA15
2	LCD_DATA7	LCD_DATA10	LCD_DATA13	EEPROM_WP
1	LCD_DATA8	LCD_DATA11	LCD_DATA14	GPMC_ADVN_ALE

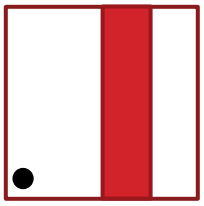
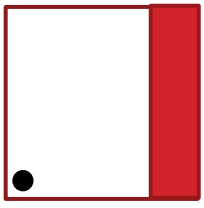


Table 5-4. OSD335x-SM Ball Map Top View (Columns N-T)

	N	P	R	T
16	OSC0_OUT	OSC0_IN	GPMC_WPN	GPMC_A11
15	OSC0_GND	GPMC_WAIT0	GPMC_A10	GPMC_A9
14	GPMC_BEN1	GPMC_A8	GPMC_A7	GPMC_A6
13	PMIC_MUX_IN	GPMC_A5	GPMC_A4	GPMC_A3
12	PMIC_PGOOD	GPMC_A2	GPMC_A1	GPMC_A0
11	PMIC_PWR_EN	PWRONRSTN	WARMRSTN	PMIC_PB_IN
10	PMIC_POWER_EN	VIN_AC	VIN_AC	VIN_AC
9	DGND	VIN_USB	VIN_USB	VIN_USB
8	DGND	VIN_BAT	VIN_BAT	VIN_BAT
7	PMIC_BAT_SENSE	GPMC_AD15	GPMC_CSN3	GPMC_CLK
6	PMIC_TS	GPMC_AD12	GPMC_AD13	GPMC_AD14
5	RTC_PWRONRSTN	GPMC_AD9	GPMC_AD10	GPMC_AD11
4	PMIC_LDO_PGOOD	GPMC_AD6	GPMC_AD7	GPMC_AD8
3	GPMC_BEN0_CLE	GPMC_CSN0	GPMC_AD0	GPMC_AD3
2	GPMC_WEN	GPMC_CSN1	GPMC_AD1	GPMC_AD4
1	GPMC_OEN_REN	GPMC_CSN2	GPMC_AD2	GPMC_AD5



5.1 Ball Description

Table 5-5 lists all the unique balls of the OSD335x-SM and gives a brief explanation of their function. The table also lists the equivalent pin number for the signal on the OSD335x package and the AM335x ZCZ package. For more detail please refer to the datasheet in section 4.1 for the individual device that ball is associated with.

Table 5-5 OSD335x-SM Ball Descriptions

Pin Name	Description	Pin Number	
		OSD335x-SM	AM335x (ZCZ)
AGND_ADC	Analog Ground (VSSA_ADC in AM335x)	A9	E8
AIN0	Analog Input / Output	A8	B6
AIN1	Analog Input / Output	B8	C7
AIN2	Analog Input / Output	B6	B7
AIN3	Analog Input / Output	C6	A7
AIN4	Analog Input / Output	C7	C8
AIN5	Analog Input	C8	B8
AIN6	Analog Input	C9	A8
AIN7	Analog Input	D7	C9
CAP_VDD_RTC	RTC Supply Voltage Input	D5	D6
DGND	Digital Ground (VSS in AM335x)	D8, D9, E5, E6, E7, E8, E9, E10, E11, E12, F5, F12, G5, G12, H4, H5, H12, H13, J4, J5, J12, J13, K5, K12, L5, L12, M5, M6, M7, M8, M9, M10, M11, M12, N8, N9	See VSS pin in AM335x datasheet.
ECAP0_IN_PWM0_OUT	Enhanced Capture 0 Input or PWM0 Output	C5	C18
EEPROM_WP	EEPROM Write Protect Pin	M2	N/A
EMU0	Miscellaneous Emulation Pin	E2	C14
EMU1	Miscellaneous Emulation Pin	E3	B14
EXTINTN	AM335x External Interrupt to ARM Cortex-A8	D4	B18
EXT_WAKEUP	AM335x EXT_WAKEUP Input	M4	C5
GPMC_A0	GPMC Address	T12	R13
GPMC_A1	GPMC Address	R12	V14
GPMC_A2	GPMC Address	P12	U14
GPMC_A3	GPMC Address	T13	T14
GPMC_A4	GPMC Address	R13	R14
GPMC_A5	GPMC Address	P13	V15
GPMC_A6	GPMC Address	T14	U15
GPMC_A7	GPMC Address	R14	T15
GPMC_A8	GPMC Address	P14	V16
GPMC_A9	GPMC Address	T15	U16
GPMC_A10	GPMC Address	R15	T16
GPMC_A11	GPMC Address	T16	V17
GPMC_AD0	GPMC Address and Data	R3	U7
GPMC_AD1	GPMC Address and Data	R2	V7
GPMC_AD2	GPMC Address and Data	R1	R8
GPMC_AD3	GPMC Address and Data	T3	T8
GPMC_AD4	GPMC Address and Data	T2	U8
GPMC_AD5	GPMC Address and Data	T1	V8
GPMC_AD6	GPMC Address and Data	P4	R9
GPMC_AD7	GPMC Address and Data	R4	T9
GPMC_AD8	GPMC Address and Data	T4	U10
GPMC_AD9	GPMC Address and Data	P5	T10
GPMC_AD10	GPMC Address and Data	R5	T11
GPMC_AD11	GPMC Address and Data	T5	U12
GPMC_AD12	GPMC Address and Data	P6	T12
GPMC_AD13	GPMC Address and Data	R6	R12
GPMC_AD14	GPMC Address and Data	T6	V13

GPMC_AD15	GPMC Address and Data	P7	U13
GPMC_ADVN_ALE	GPMC Address Valid / Address Latch Enable	M1	R7
GPMC_BEN0_CLE	GPMC Byte Enable 0 / Command Latch Enable	N3	T6
GPMC_BEN1	GPMC Byte Enable 1	N14	U18
GPMC_CLK	GPMC Clock	T7	V12
GPMC_CSN0	GPMC Chip Select	P3	V6
GPMC_CSN1	GPMC Chip Select	P2	U9
GPMC_CSN2	GPMC Chip Select	P1	V9
GPMC_CSN3	GPMC Chip Select	R7	T13
GPMC_OEN_REN	GPMC Output Enable / Read Enable	N1	T7
GPMC_WAIT0	GPMC Wait 0	P15	T17
GPMC_WEN	GPMC Write Enable	N2	U6
GPMC_WPN	GPMC Write Protect	R16	U17
I2C0_SCL	I2C Clock	C10	C16
I2C0_SDA	I2C Data	C11	C17
LCD_AC_BIAS_EN	LCD AC Bias Enable Chip Select	E1	R6
LCD_DATA0	LCD Data Bus	G3	R1
LCD_DATA1	LCD Data Bus	G2	R2
LCD_DATA2	LCD Data Bus	G1	R3
LCD_DATA3	LCD Data Bus	H3	R4
LCD_DATA4	LCD Data Bus	H2	T1
LCD_DATA5	LCD Data Bus	H1	T2
LCD_DATA6	LCD Data Bus	J3	T3
LCD_DATA7	LCD Data Bus	J2	T4
LCD_DATA8	LCD Data Bus	J1	U1
LCD_DATA9	LCD Data Bus	K3	U2
LCD_DATA10	LCD Data Bus	K2	U3
LCD_DATA11	LCD Data Bus	K1	U4
LCD_DATA12	LCD Data Bus	L3	V2
LCD_DATA13	LCD Data Bus	L2	V3
LCD_DATA14	LCD Data Bus	L1	V4
LCD_DATA15	LCD Data Bus	M3	T5
LCD_HSYNC	LCD Horizontal Sync	F2	R5
LCD_PCLK	LCD Pixel Clock	F1	V5
LCD_VSYNC	LCD Vertical Sync	F3	U5
MCASP0_ACLKR	McASP0 Receive Bit Clock	A3	B12
MCASP0_ACLKX	McASP0 Transmit Bit Clock	A1	A13
MCASP0_AHCLKR	McASP0 Receive Master Clock	B1	C12
MCASP0_AHCLKX	McASP0 Transmit Master Clock	C4	A14
MCASP0_AXR0	McASP0 Serial Data	B2	D12
MCASP0_AXR1	McASP0 Serial Data	C3	D13
MCASP0_FSR	McASP0 Receive Frame Sync	B3	C13
MCASP0_FSX	McASP0 Transmit Frame Sync	A2	B13
MDC	MDIO Clock	D13	M18
MDIO	MDIO Data	E13	M17
MII1_COL	MII Collision	F15	H16
MII1_CRS	MII Carrier Sense	F14	H17
MII1_RX_CLK	MII Receive Clock	E16	L18
MII1_RX_DV	MII Receive Data Valid	F16	J17
MII1_RX_ER	MII Receive Data Error	E15	J15
MII1_RXD0	MII Receive Data	E14	M16
MII1_RXD1	MII Receive Data	D16	L15
MII1_RXD2	MII Receive Data	D15	L16
MII1_RXD3	MII Receive Data	D14	L17
MII1_TX_CLK	MII Transmit Clock	H16	K18
MII1_TX_EN	MII Transmit Enable	G14	J16
MII1_TXD0	MII Transmit Data	H15	K17
MII1_TXD1	MII Transmit Data	H14	K16
MII1_TXD2	MII Transmit Data	G16	K15
MII1_TXD3	MII Transmit Data	G15	J18
MMC0_CLK	MMC/SD/SDIO Clock	B15	G17
MMC0_CMD	MMC/SD/SDIO Command	B16	G18
MMC0_DAT0	MMC/SD/SDIO Data	A16	G16

MMC0_DAT1	MMC/SD/SDIO Data	A15	G15
MMC0_DAT2	MMC/SD/SDIO Data	C16	F18
MMC0_DAT3	MMC/SD/SDIO Data	C15	F17
NC	No Connect	D12, J6, K4	N/A
OSC0_GND	High Frequency Oscillator Ground (VSS_OSC)	N15	V11
OSC0_IN	High Frequency Oscillator Input (XTALIN)	P16	V10
OSC0_OUT	High Frequency Oscillator Output (XTALOUT)	N16	U11
OSC1_GND	Real Time Clock Oscillator Ground (VSS_RTC)	B5	A5
OSC1_IN	Real Time Clock Oscillator Input (RTC_XTALIN)	A6	A6
OSC1_OUT	Real Time Clock Oscillator Output (RTC_XTALOUT)	A5	A4
PMIC_BAT_SENSE	TPS65217C BAT_SENSE Input	N7	N/A
PMIC_LDO_PGOOD	TPS65217C LDO_PGOOD Output	N4	N/A
PMIC_MUX_IN	TPS65217C MUX_IN Input	N13	N/A
PMIC_MUX_OUT	TPS65217C MUX_OUT Output	D6	N/A
PMIC_NINT	TPS65217C NINT Output	E4	N/A
PMIC_NRESET	TPS65217C NRESET Input	M13	N/A
PMIC_NWAKEUP	TPS65217C NWAKEUP Output	L4	N/A
PMIC_PB_IN	TPS65217C PB_IN Input	T11	N/A
PMIC_PGOOD	TPS65217C PGOOD Output	N12	N/A
PMIC_POWER_EN	AM335x PMIC_POWER_EN Output	N10	C6
PMIC_PWR_EN	TPS65217C PWR_EN Input	N11	N/A
PMIC_SCL	TPS65217C SCL Input	D10	N/A
PMIC_SDA	TPS65217C SDA Input / Output	D11	N/A
PMIC_TS	TPS65217C TS Input	N6	N/A
PWRONRSTN	Power On Reset Input (Active Low)	P11	B15
RMII1_REF_CLK	RMII Reference Clock	J14	H18
RTC_KALDO_ENN	Enable input for internal CAP_VDD_RTC voltage regulator (Active Low)	M16	B4
RTC_PWRONRSTN	RTC Reset Input (Active Low)	N5	B5
SPI0_CS0	SPI Chip Select	A14	A16
SPI0_CS1	SPI Chip Select	C14	C15
SPI0_D0	SPI Data	B13	B17
SPI0_D1	SPI Data	B14	B16
SPI0_SCLK	SPI Clock	A13	A17
SYS_ADC_1P8V	Output Power Supply, Analog, 1.8VDC	A7	N/A
SYS_RTC_1P8V	Output Power Supply, RTC, 1.8VDC	K11, L11	N/A
SYS_VDD_1P8V	Output Power Supply, Digital, 1.8VDC	F10, G10, H10, H11, J10, J11, K10, L10	N/A
SYS_VDD1_3P3V	Output Power Supply, Primary, 3.3VDC	F6, F7, G6, G7	N/A
SYS_VDD2_3P3V	Output Power Supply, Secondary, 3.3VDC	F11, G11	N/A
SYS_VDD3_3P3V	Output Power Supply, I/O, 3.3VDC	F8, G8, H7, H8, J7, J8, K8, L8	N/A
SYS_VOUT	TPS65217C SYS Output	K6, K7, L6, L7	N/A
TCK	JTAG Test Clock	D1	A12
TDI	JTAG Test Data Input	C1	B11
TDO	JTAG Test Data Output	C2	A11
TMS	JTAG Test Mode Select	D2	C11
TRSTN	JTAG Test Reset	D3	B10
UART0_CTSN	UART Clear to Send	C12	E18
UART0_RTSN	UART Request to Send	C13	E17
UART0_RXD	UART Receive Data	A12	E15
UART0_TXD	UART Transmit Data	B12	E16
UART1_CTSN	UART Clear to Send	B10	D18
UART1_RTSN	UART Request to Send	A10	D17
UART1_RXD	UART Receive Data	A11	D16
UART1_TXD	UART Transmit Data	B11	D15
USB0_CE	USB0 Charger Enable Output	K13	M15
USB0_DM	USB0 Data (-)	K16	N18
USB0_DP	USB0 Data (+)	K15	N17

USB0_DRVVBUS	USB0 VBUS Control Output. Driven high to enable external power logic in Host mode. Requires valid input on USB0_VBUS. Checks USB0_VBUS every 100ms and generates VBUS error interrupt if USB0_VBUS is not valid.	J15	F16
USB0_ID	USB0 OTG ID	K14	P16
USB0_VBUS	USB0 VBUS	J16	P15
USB1_CE	USB1 Charger Enable Output	L13	P18
USB1_DM	USB1 Data (-)	L16	R18
USB1_DP	USB1 Data (+)	L15	R17
USB1_DRVVBUS	USB1 VBUS Control Output. Driven high to enable external power logic in Host mode. Requires valid input on USB1_VBUS. Checks USB1_VBUS every 100ms and generates VBUS error interrupt if USB1_VBUS is not valid.	M14	F15
USB1_ID	USB1 OTG ID	L14	P17
USB1_VBUS	USB1 VBUS	M15	T18
VDD_CORE	Internal Power Supply Test Point	G4	N/A
VDD_MPU	Internal Power Supply Test Point	F13	N/A
VDDS_DDR	Internal Power Supply Test Point	F4	N/A
VDDS_PLL	Internal Power Supply Test Point	G13	N/A
VDDSHV1	Supply voltage for the dual-voltage IO domain	J9	P7, P8
VDDSHV2	Supply voltage for the dual-voltage IO domain	K9	P10, P11
VDDSHV3	Supply voltage for the dual-voltage IO domain	L9	P12, P13
VDDSHV4	Supply voltage for the dual-voltage IO domain	F9	H14, J14
VDDSHV5	Supply voltage for the dual-voltage IO domain	G9	K14, L14
VDDSHV6	Supply voltage for the dual-voltage IO domain	H9	E10, E11, E12, E13, F14, G14, N5, P5, P6
VIN_AC	TPS65217C AC Input	P10, R10, T10	N/A
VIN_BAT	TPS65217C BAT Input / Output	P8, R8, T8	N/A
VIN_USB	TPS65217C USB Input	P9, R9, T9	N/A
VPP	RESERVED	H6	M5
VREFN	Analog Negative Reference Input	B9	A9
VREFP	Analog Positive Reference Input	B7	B9
WARMRSTN	Warm Reset (Active Low)	R11	A10
XDMA_EVENT_INTR0	External DMA Event or Interrupt 0	A4	A15
XDMA_EVENT_INTR1	External DMA Event or Interrupt 1	B4	D14

5.2 Not Connected Balls

The OSD335x-SM ball map contains balls which are marked NC (No Connect). These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of the OSD335x-SM.

5.3 Reserved Signals

There is a subset of signals that are available on the OSD335x-SM ball map but ***should not be*** used externally to the device. These signals are used internally to the OSD335x-SM and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5-6.

Table 5-6. Reserved Signals

Reserved Signals
VPP
VDD_CORE
VDD_MPU
VDDS_DDR
VDDS_PLL

6 OSD335x-SM Components

The OSD335x-SM integrates the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 GB of DDR3 Memory, a 4KB EEPROM for non-volatile configuration storage and the resistors, capacitors, and inductors into a single design-in-ready package. The following section contains any specific device information needed for the integrated components to design your system with the OSD335x-SM.

6.1 AM335x Processor

The heart of the OSD335x-SM is the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor. The processor in the OSD335x-SM is configured to perform identically to a standalone device. Please refer to the data sheet in the Reference Documents section for details on using the AM335x processor.

6.1.1 I/O Voltages

The OSD335x-SM allows the I/O voltage domains (VDDSHVx) of the AM335x to be set to either 1.8V or 3.3V. The VDDSHVx pins of the OSD335x-SM (ie VDDSHV1 thru VDDSHV6), which can be found in Table 5-5, must be connected to either a 1.8V or 3.3V power source in order to provide power to the I/Os. Recommendations on how to connect the I/O voltage domain pins is in the OSD335x-SM Layout Guide in the Reference Documents section.

See the AM335x datasheet in the Reference Documents section for more information on the pins associated with each I/O voltage domain.

6.2 DDR3 Memory

The OSD335x-SM integrates a DDR3 memory into the device and handles all the connections needed between the AM335x and the DDR3. You will still have to set the proper registers to configure the AM335x DDR PHY to work correctly with the memory included in the OSD335x-SM. Typically, this would require you to run through the procedure outlined in the AM335x DDR PHY register configuration for DDR3 using Software Leveling referred to in the Reference Documents section of this document. This procedure has been run for the OSD335x-SM and a list of the recommended values for the registers is provided in Table 6-1. It is recommended that you use this set of values for optimal performance.

Table 6-1 AM335x DDR EMIF, PHY and Control Module Register Settings

Register Name	Peripheral	Recommended Value
DDR_CMDx_IOCTRL(1)	Control Module	0x0000018B
DDR_DATAx_IOCTRL(2)	Control Module	0x0000018B
SDRAM_CONFIG	EMIF	0x61C05332
SDRAM_CONFIG_2	EMIF	0x00000000
SDRAM_REF_CTRL	EMIF	0x00000C30
SDRAM_TIM_1	EMIF	0x0AAAD4DB
SDRAM_TIM_2	EMIF	0x266B7FDA
SDRAM_TIM_3	EMIF	0x501F867F
ZQ_CONFIG	EMIF	0x50074BE4
DDR_PHY_CTRL_1	EMIF	0x00100007
CMDx_REG_PHY_CTRL_SLAVE_RATIO_0(1)	DDR PHY	0x00000080
CMDx_REG_PHY_INVERT_CLKOUT_0(1)	DDR PHY	0x00000000
DATAx_REG_PHY_RD_DQS_SLAVE_RATIO_0(2)	DDR PHY	0x0000003A
DATAx_REG_PHY_WR_DQS_SLAVE_RATIO_0(2)	DDR PHY	0x00000045
DATAx_REG_PHY_FIFO_WE_SLAVE_RATIO_0(2)	DDR PHY	0x00000095
DATAx_REG_PHY_WR_DATA_SLAVE_RATIO_0(2)	DDR PHY	0x0000007F

(1) "CMDx" refers to registers where x is in [0, 1, 2]
(2) "DATAx" refers to registers where x is in [0, 1]

Settings in Table 6-1 are recommended and supported. Other values may work but are not guaranteed. If you want to rerun the calibration yourself the seed values provided in Table 6-2 should be used.

Table 6-2 AM335x DDR PHY Calibration Seed Values

DATAx_PHY_RD_DQS_SLAVE_RATIO	40
DATAx_PHY_FIFO_WE_SLAVE_RATIO	64
DATAx_PHY_WR_DQS_SLAVE_RATIO	0

6.3 EEPROM

The OSD335x-SM contains a 4KB EEPROM for non-volatile storage of configuration information. The EEPROM is connected to I2C0 at the 7-bit I2C address 0x50 (0b1010000). Please refer to the data sheet in the Reference Documents section for details on using the EEPROM.

6.3.1 EEPROM Contents

EEPROM address space 0x000 to 0xEFF is empty and can be used for board specific information during system boot. The final 256 bytes of the EEPROM (0xF00 to 0xFFF) are reserved for device specific information. The reserved space contents of the EEPROM can be found in Table 6-3

Table 6-3 EEPROM Contents Programmed by Octavo Systems

Name	Description	Size (bytes)	Start address	End address	Contents
RSVD	Reserved for Future Use	256	0xF00	0xFFF	All 0xFF

6.3.2 EEPROM Write Protection

By default, the EEPROM is write protected (ie. the EEPROM_WP pin is pulled high as seen in Table 2-3). To program values into the EEPROM, it is required to drive the EEPROM_WP pin to a logic low. See the OSD335x-SM Layout Guide in the Reference Documents section for layout / manufacturing recommendations for the EEPROM_WP pin.

7 Power Management

The power management portion of the OSD335x-SM consists of two devices, the TPS65217C (PMIC) and the TL5209 (LDO). The PMIC provides the necessary power rails to the AM335x and the DDR3 while the LDO is not used inside the SiP. Both devices provide power supply outputs that may be used to power circuitry external to the OSD335x-SM. The PMIC is connected to I2C0 at the 7-bit I2C address 0x24 (0b100100). This section describes how to power the OSD335x-SM in a system and the outputs that can be used.

7.1 Input Power

The OSD335x-SM may be powered by any combination of the following input power supplies. Please refer to the TPS65217C datasheet for details.

The maximum risetime for input rails VIN_AC and VIN_USB (defined as time for the input voltage to rise from 100 mV to 4.5 V) is 50 ms. The device may fail to power up properly if this requirement is not met.

7.1.1 VIN_AC

The OSD335x-SM may be powered by an external AC Adaptor at 5.0 VDC. If input is unused, it should be connected to DGND.

7.1.2 VIN_USB

The OSD335x-SM may be powered by a USB port at 5.0 VDC. If input is unused, it should be connected to DGND.

7.1.3 VIN_BAT

The OSD335x-SM may be powered by a single cell (1S) Li-Ion or Li-Polymer Battery nominally at 3.7 VDC.

Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS_VDD1_3P3V cannot be used once VIN_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.

When VIN_BAT is not used, it must be connected to PMIC_BAT_SENSE.

7.2 Output Power

The OSD335x-SM produces the following output power supplies.

7.2.1 SYS_VOUT: Switched VIN_AC, VIN_USB, or VIN_BAT

The OSD335x-SM contains a shared supply to power the AM335x, DDR3, and TL5209 which is also used to power external circuitry. This is supplied by the TPS65217C SYS output. The SYS output is a switched connection to one of the input power supplies selected by the TPS65217C as described in the datasheet for that device.

7.2.2 SYS_VDD1_3P3V

The OSD335x-SM contains a dedicated 3.4 VDC supply[1] to power external circuitry. This is supplied by the TL5209, powered by the TPS65217C SYS output, and enabled by the TPS65217C LDO4.

Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS_VDD1_3P3V cannot be used once VIN_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.

7.2.3 SYS_VDD2_3P3V

The OSD335x-SM contains a dedicated 3.3 VDC supply to power external circuitry. This is supplied by the TPS65217C LDO2.

7.2.4 SYS_VDD3_3P3V

The OSD335x-SM contains a shared 3.3 VDC supply. It internally provides power to VDDA3P3V_USB0 and VDDA3P3V_USB1. It can also be used to power the AM335x I/O domains (VDDSHVx). This is supplied by the TPS65217C LDO4.

7.2.5 SYS_RTC_1P8V

The OSD335x-SM contains a shared 1.8 VDC supply to power the AM335x RTC, VDDA3P3V_USB0, and VDDA3P3V_USB1. It may also be used to power external circuitry. This is supplied by the TPS65217C LDO1.

Please note that the AM335x in the OSD335x is powered by TPS65217 PMIC **version C** which does not support RTC only mode.

7.2.6 SYS_VDD_1P8V

The OSD335x-SM contains a shared 1.8 VDC supply that may be used to power the AM335x I/O domains (VDDSHVx) and external circuitry. It also supplies power to the AM335x SRAM, PLLs and USB. This is supplied by the TPS65217C LDO3.

7.2.7 SYS_ADC_1P8V

The OSD335x-SM contains a shared 1.8 VDC supply to power the AM335x ADC which may also be used to power external analog circuitry. This is supplied by the TPS65217C LDO3 and filtered for analog applications.

7.3 Internal Power

The OSD335x-SM has internal power supplies that are not available to power external circuitry. To do so will prevent the OSD335x from functioning properly. The power supplies are accessible externally for monitoring purposes only.

[1] The LDO has an accuracy of 1 – 2% depending on the ambient temperature which will also affect the nominal voltage. See the TL5209 datasheet for more information.

7.3.1 VDDS_DDR

The OSD335x-SM contains a dedicated 1.5 VDC supply to power the AM335x DDR3 interface and the DDR3 device. This is supplied by the TPS65217C DCDC1.

7.3.2 VDD_MPU

The OSD335x-SM contains a dedicated 1.1 VDC supply to power the AM335x MPU domain. This is supplied by the TPS65217C DCDC2.

7.3.3 VDD_CORE

The OSD335x-SM contains a dedicated 1.1 VDC supply to power the AM335x CORE domain. This is supplied by the TPS65217C DCDC3.

7.3.4 VDDS_PLL

The OSD335x-SM contains a filtered 1.8 VDC supply to power the AM335x PLLs and oscillators. This is supplied by the TPS65217C LDO3.

7.4 Total Current Consideration

The total current consumption of all power rails must not exceed the recommended input currents described in Table 8-2. This includes power consumption within the SiP from the AM335x and the DDR3, as well as all external loads on the output power rails from Section 7.2.

The power consumed by the AM335x can be estimated using the *AM335x Power Estimation Tool* found in the Reference Documents section of this document. When estimating power consumption, the efficiencies and types of the OSD335x-SM internal power supplies must be considered. Refer to the "*Connections Diagram for TPS65217C and AM335x*" section of *Powering the AM335x with the TPS65217x* found in the Reference Documents section of this document for more information on the power supplies providing power to the AM335x.

7.5 Control and Status

The control and status connections for Processor-PMIC interface and RTC subsystem required to power the device are described in this section.

7.5.1 Minimum IO voltage domain connections

The IO pins of AM335x are divided into 6 pin groups. The IO voltage levels of a pin group can be configured by connecting the voltage domain pins to the required voltage level. Table 7-1 lists recommended connections for each VDDSHV pin according to the voltage level required. These connections are required for IO pins of OSD335x-SM to function properly.

Table 7-1: VDDSHVx connections for OSD335x-SM

Voltage Domain	Pin	Voltage Level	Recommended pin connection
VDDSHV1	J9	3.3V	J8
		1.8V	J10
VDDSHV2	K9	3.3V	K8
		1.8V	K10
VDDSHV3	L9	3.3V	L8
		1.8V	L10
VDDSHV4	F9	3.3V	F8
		1.8V	F10
VDDSHV5	G9	3.3V	G8
		1.8V	G10
VDDSHV6	H9	3.3V	H8
		1.8V	H10

7.5.2 Minimum Processor-PMIC interface Connections

Table 7-2 lists the signals required to coordinate the operation of the AM335x and TPS65217C. Figure 7.1 and Figure 7.2 illustrate the required connections between the AM335x and the TPS65217C with RTC subsystem enabled and disabled respectively. These connections are the minimum required to operate the device in corresponding mode. The accessibility of these signals enables other uses of reset, power control, power status, interrupt, wakeup, and serial communication signals.

The figures 7.1 and 7.2 only illustrate the interface between the AM335x and TPS65217C.

Table 7-2. AM335x and TPS65217C Signal Descriptions

Signal	Description	Notes
PMIC_POWER_EN	PMIC Power Enable from AM335x	
PMIC_PWR_EN	PMIC Power Enable to TPS65217C	1
I2C0_SCL	I2C0 SCL from AM335x	1
PMIC_SCL	I2C SCL to TPS65217C	
I2C0_SDA	I2C0 SDA from AM335x	1
PMIC_SDA	I2C SDA to TPS65217C	
PMIC_PGOOD	PGOOD from TPS65217C	
PWRONRSTN	PWRONRSTN to AM335x	
PMIC_LDO_PGOOD	LDO_PGOOD from TPS65217C	
RTC_PWRONRSTN	RTC_PWRONRSTN to AM335x	
PMIC_NINT	NINT from TPS65217C	
EXTINTN	EXTINTN to AM335x	1
PMIC_NWAKEUP	NWAKEUP from TPS65217C	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2-3 for pull up on this signal

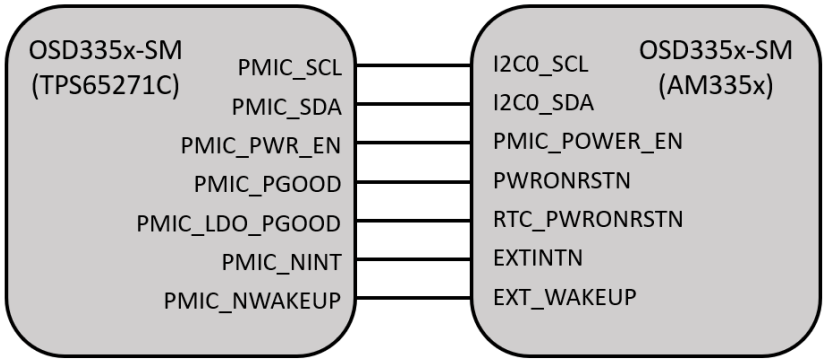


Figure 7.1. OSD335x-SM Minimum Signal Connections with RTC enabled

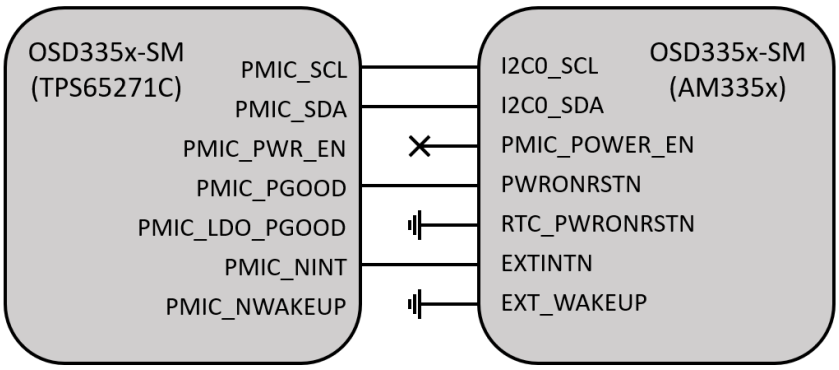


Figure 7.2. OSD335x-SM Minimum Signal Connections with RTC disabled

7.5.3 Minimum RTC Power Connections

Table 7-3 lists RTC domain signals required to operate the OSD335x-SM. In addition to the required connections described in Section 7.5.2, Figure 7.3 and Figure 7.4 illustrate additional connections with RTC subsystem enabled and disabled respectively. These connections are also included in the minimum required circuitry to operate the device.

Table 7-3. OSD335x-SM RTC Signal Descriptions

Signal	Description	Notes
CAP_VDD_RTC	Supply voltage for the RTC core domain	
RTC_KALDO_ENN	Active low enable input for internal CAP_VDD_RTC voltage regulator	
RTC_PWRONRSTN	RTC_PWRONRSTN to AM335x	
PMIC_POWER_EN	PMIC Power Enable from AM335x	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2-3 for pull up on this signal

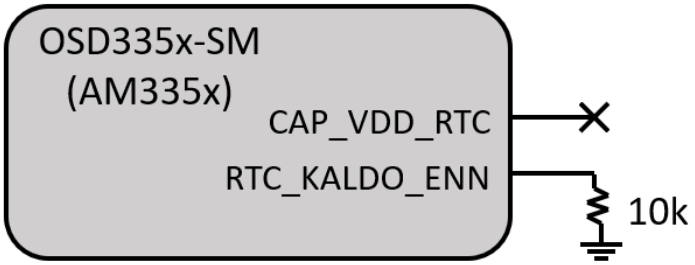


Figure 7.3. Additional connections for OSD335x-SM with RTC enabled

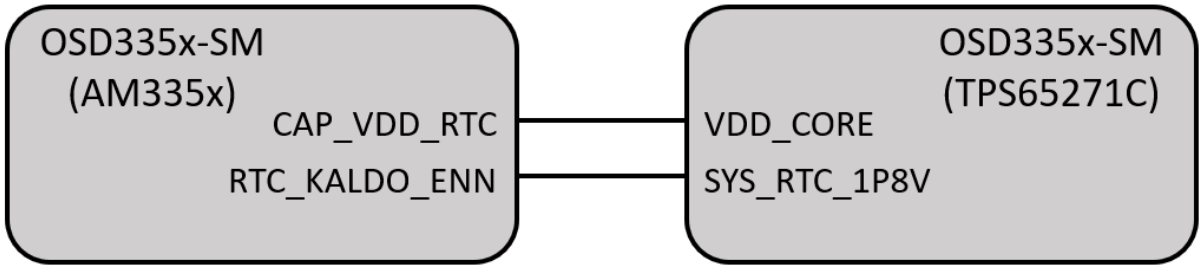


Figure 7.4. Additional connections for OSD335x-SM with RTC disabled

8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of OSD335x-SM.

Table 8-1. OSD335x-SM Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1) (2)

		Value	Unit
Supply voltage range (with respect to VSS)	VIN_BAT	-0.3 to 7	V
	VIN_USB, VIN_AC	-0.3 to 7	
Input/Output voltage range (with respect to VSS)	All pins unless specified separately	-0.3 to 3.6	V
Terminal current	SYS_VOUT, VIN_USB, VIN_BAT	3000	mA
T_C Operating case temperature	Commercial (B)	0 to 85	°C
	Industrial (I)	-40 to 85	°C
T_{stg} Storage temperature		-55 to 125	°C
ESD rating	(HBM) Human body model	±2000	V
	(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

Table 8-2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
Supply voltage, VIN_USB, VIN_AC	4.3		5.8	V
In-rush current, VIN_AC			2.1	A
In-rush current, VIN_USB			500	mA
Supply voltage Rise Time, VIN_USB, VIN_AC (100mV to 4.5V)			50	ms
Supply voltage, VIN_BAT	2.75		5.5	V
Input current from VIN_AC			2.0	A
Input current from VIN_USB			1.3	A
VIN_BAT current			2.0	A
Output voltage range for SYS_VDD1_3P3V		3.4		V
Output voltage range for SYS_VDD2_3P3V		3.3		V
Output voltage range for SYS_VDD3_3P3V		3.3		V
Output voltage range for SYS_RTC_1P8V		1.8		V
Output voltage range for SYS_VDD_1P8V		1.8		V
Output voltage range for SYS_ADC_1P8V		1.8		V
Output voltage range for VDDS_DDR[1]		1.5		V
Output voltage range for VDD_MPU[1]		1.1		V
Output voltage range for VDD_CORE[1]		1.1		V
Output voltage range for VDDS_PLL[1]		1.8		V
Output current for SYS_VOUT[2]	0		500	mA
Output current for SYS_VDD1_3P3V[2]	0		500	mA
Output current for SYS_VDD2_3P3V[2]	0		100	mA
Output current for SYS_VDD3_3P3V[2]	0		50	mA
Output current for SYS_RTC_1P8V[2]	0		100	mA
Output current for SYS_VDD_1P8V[2]	0		250	mA
Output current for SYS_ADC_1P8V[2]	0		25	mA

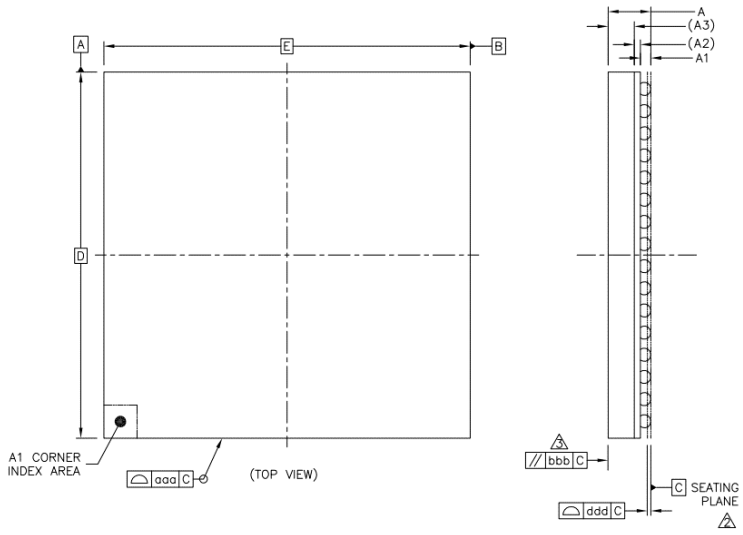
(1) *These voltage rails are for reference only and should not be used to power anything on the PCB.*
(2) *Please note that the total input current on VIN_AC, VIN_USB or VIN_BAT must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.4 for more details.*

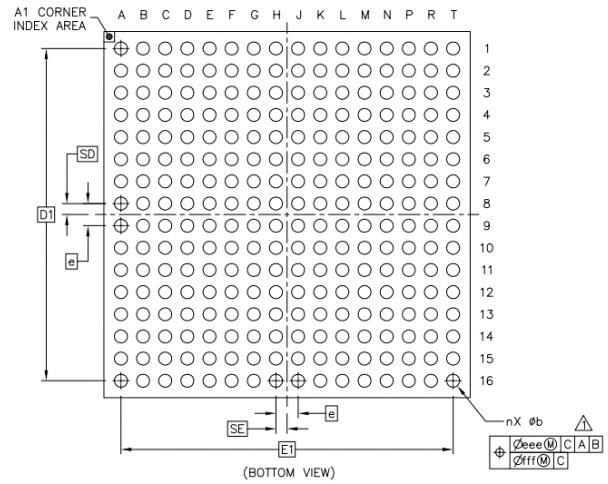
9 Packaging Information

The OSD335x-SM is packaged in a 256 ball, Ball Grid Array (BGA). The package size is 21 X 21 millimeters with a ball pitch of 1.27 millimeters. This section will give you the specifics on the package.

9.1 Mechanical Dimensions

The mechanical drawings of the OSD335x-SM show pin A1 in the lower left-hand corner when looking at the top view of the device. Pin A1 is in the upper left-hand corner if looking at the balls from the bottom view of the package.





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.58
STAND OFF	A1	0.5	---	0.7
SUBSTRATE THICKNESS	A2		0.35	REF
MOLD THICKNESS	A3		1.5	REF
BODY SIZE	D		21	BSC
	E		21	BSC
BALL DIAMETER			0.75	
BALL OPENING			0.6	
BALL WIDTH	b	0.6	---	0.9
BALL PITCH	e		1.27	BSC
BALL COUNT	n		256	
EDGE BALL CENTER TO CENTER	D1		19.05	BSC
	E1		19.05	BSC
BODY CENTER TO CONTACT BALL	SD		0.635	BSC
	SE		0.635	BSC
PACKAGE EDGE TOLERANCE	aaa		0.2	
MOLD FLATNESS	bbb		0.35	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.3	
BALL OFFSET (BALL)	fff		0.15	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

9.1.1 Landing Pad Sizing

For the nominal ball diameter of 0.75mm, specification IPC-7351A states that for NSMD pads, the nominal land diameter is 0.55mm with a land variation of 0.60mm to 0.50mm. Footprints provided by Octavo Systems generally use the minimum land pad size to enable lower cost routing (see Layout Guide in the Reference Documents section for more information). However, some applications may require a larger land pad size to enable a more robust structural connection to the circuit board or for other manufacturing constraints. Check the requirements of the application and manufacturer to determine the appropriate land pad size.

9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

9.3 Storage Requirements

The OSD335x-SM Family of devices are sensitive to moisture and need to be handled in specific ways to make sure they function properly during and after the manufacturing process. The OSD335x-SM Family of devices are rated with a **Moisture Sensitivity Level (MSL) of 4**. This means that they are stored in a sealed Dry Pack with desiccant bag and a Humidity Indicator Card (HIC). **If the HIC reads > 10% when read at 23 ± 5 C or the HIC is not present; the devices must be baked in per the directions in 9.3.3 before use.**

9.3.1 Floor Life

Once the sealed Dry Pack is opened the OSD335x-SM can be stored **for up to 72 hours in a room ≤ 30°C and ≤60% Relative Humidity (RH). If any of these conditions are not met the devices must be baked as outlined in section 9.3.3 before use.**

9.3.2 Shelf Life

Octavo System devices are shipped in Moisture Barrier Bags (MBB) that have been partially vacuumed sealed with a desiccant bag. This combination supports a shelf life of the devices in an unopened factory bag for **24 Months from the seal date.** If this is exceeded, then the devices must be **baked per the directions in section 9.3.3 before use**.

9.3.3 Baking

The devices need to be baked if they have been exposed to environments outside of the guide lines outlined in sections 9.3.1 and 9.3.2, or if there is concern about the moisture content of the devices. The devices must be baked for **34hrs at 125°C with a RH of <5%.**

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