



# THE DATASHEET OF SN65HVD1792TDEP



## Fault-Protected RS-485 Transceivers With Extended Common-Mode Range

 Check for Samples: [SN65HVD1792-EP](#)

### FEATURES

- Bus-Pin Fault Protection to  $> \pm 70$  V
- Common-Mode Voltage Range ( $-20$  V to 25 V) More Than Doubles TIA/EIA 485 Requirement
- Bus I/O Protection
  - $\pm 16$  kV JEDEC HBM Protection
- Reduced Unit Load for Up to 256 Nodes
- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions
- Low Power Consumption
  - Low Standby Supply Current, 1  $\mu$ A Typ
  - $I_{CC}$  5 mA Quiescent During Operation
- Power-Up, Power-Down Glitch-Free Operation

### APPLICATIONS

- Designed for RS-485 and RS-422 Networks

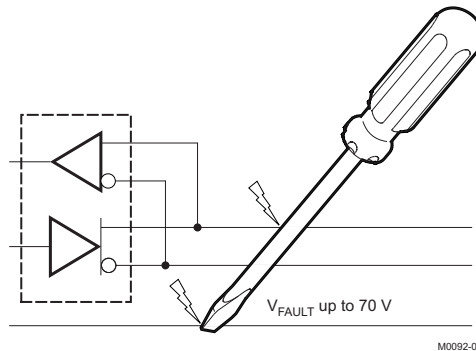
### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

### DESCRIPTION

The SN65HVD1792 is designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. It is also robust to ESD events, with high levels of protection to human-body model specifications.

The SN65HVD1792 combines a differential driver and a differential receiver, which operate from a single power supply. The SN65HVD1792 is characterized from  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ .



### ORDERING INFORMATION<sup>(1)</sup>

| $T_A$  | PACKAGE <sup>(2)</sup> | ORDERABLE PART NUMBER | TOP-SIDE MARKING | VID NUMBER       |
|--|------------------------|-----------------------|------------------|------------------|
| $-40^{\circ}\text{C}$ to $105^{\circ}\text{C}$ | SOIC - D               | SN65HVD1792TDREP      | 1792EP           | V62/13620-01XE   |
|  |                        | SN65HVD1792TDEP       |                  | V62/13620-01XE-T |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### DEVICE INFORMATION

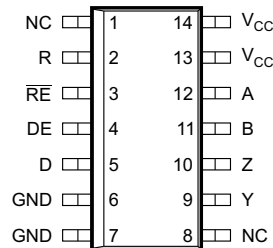
#### DRIVER FUNCTION TABLE

| Input<br>D | Enable<br>DE | Outputs |   |                                    |
|------------|--------------|---------|---|------------------------------------|
|            |              | A       | B |                                    |
| H          | H            | H       | L | Actively drive bus high            |
| L          | H            | L       | H | Actively drive bus low             |
| X          | L            | Z       | Z | Driver disabled                    |
| X          | OPEN         | Z       | Z | Driver disabled by default         |
| OPEN       | H            | H       | L | Actively drive bus high by default |

#### RECEIVER FUNCTION TABLE

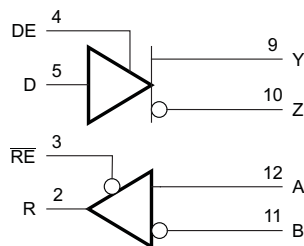
| Differential Input<br>$V_{ID} = V_A - V_B$ | Enable<br>RE | Output<br>R |                              |
|--|--------------|-------------|------------------------------|
| $V_{IT+} < V_{ID}$                         | L            | H           | Receive valid bus high       |
| $V_{IT-} < V_{ID} < V_{IT+}$               | L            | ?           | Indeterminate bus state      |
| $V_{ID} < V_{IT-}$                         | L            | L           | Receive valid bus low        |
| X  | H            | Z           | Receiver disabled            |
| X  | OPEN         | Z           | Receiver disabled by default |
| Open-circuit bus                           | L            | H           | Fail-safe high output        |
| Short-circuit bus                          | L            | H           | Fail-safe high output        |
| Idle (terminated) bus                      | L            | H           | Fail-safe high output        |

D Package  
(Top View)



NC - No internal connection  
Pins 6 and 7 are connected together internally.  
Pins 13 and 14 are connected together internally.

Logic Diagram (Positive Logic)



S0300-01

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

|          |   | VALUE                  | UNIT |
|----------|---|------------------------|------|
| $V_{CC}$ | Supply voltage  | –0.5 to 7              | V    |
|          | Voltage range at bus pins   | A, B pins<br>–70 to 70 | V    |
|          | Input voltage range at any logic pin  | –0.3 to $V_{CC} + 0.3$ | V    |
|          | Transient overvoltage pulse through 100 $\Omega$ per TIA-485                  | –100 to 100            | V    |
|          | Receiver output current   | –24 to 24              | mA   |
| $T_J$    | Junction temperature  | 170                    | °C   |
|          | IEC 60749-26 ESD (human-body model), bus terminals and GND                    | $\pm 16$               | kV   |
|          | JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND | $\pm 16$               | kV   |
|          | JEDEC Standard 22, Test Method A114 (human-body model), all pins              | $\pm 4$                | kV   |
|          | JEDEC Standard 22, Test Method C101 (charged-device model), all pins          | $\pm 2$                | kV   |
|          | JEDEC Standard 22, Test Method A115 (machine model), all pins                 | $\pm 400$              | V    |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**THERMAL INFORMATION**

| THERMAL METRIC <sup>(1)</sup> |   | SN65HVD1792-EP | UNITS |
|-------------------------------|---|----------------|-------|
|                               |   | D              |       |
|                               |   | 14 PINS        |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance <sup>(2)</sup>       | 70.8           | °C/W  |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance <sup>(3)</sup>    | 29.4           |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance <sup>(4)</sup>         | 25.3           |       |
| $\psi_{JT}$                   | Junction-to-top characterization parameter <sup>(5)</sup>   | 8.2            |       |
| $\psi_{JB}$                   | Junction-to-board characterization parameter <sup>(6)</sup> | 25             |       |
| $\theta_{JCbott}$             | Junction-to-case (bottom) thermal resistance <sup>(7)</sup> | N/A            |       |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

|            |  | MIN | NOM | MAX      | UNIT               |
|------------|--|-----|-----|----------|--------------------|
| $V_{CC}$   | Supply voltage   | 4.5 | 5   | 5.5      | V                  |
| $V_I$      | Input voltage at any bus terminal (separately or common mode) <sup>(1)</sup>     | -20 |     | 25       | V                  |
| $V_{IH}$   | High-level input voltage (driver, driver enable, and receiver enable inputs)     | 2   |     | $V_{CC}$ | V                  |
| $V_{IL}$   | Low-level input voltage (driver, driver enable, and receiver enable inputs)      | 0   |     | 0.8      | V                  |
| $V_{ID}$   | Differential input voltage   | -25 |     | 25       | V                  |
| $I_O$      | Output current, driver   | -60 |     | 60       | mA                 |
|            | Output current, receiver   | -8  |     | 8        | mA                 |
| $R_L$      | Differential load resistance   | 54  | 60  |          | $\Omega$           |
| $C_L$      | Differential load capacitance  |     | 50  |          | pF                 |
| $1/t_{UI}$ | Signaling rate   |     |     | 1        | Mbps               |
| $T_A$      | Operating free-air temperature (see application section for thermal information) | -40 |     | 105      | $^{\circ}\text{C}$ |
| $T_J$      | Junction temperature   | -40 |     | 150      | $^{\circ}\text{C}$ |

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER         |  | TEST CONDITIONS   |  | MIN                 | TYP        | MAX  | UNIT          |
|-------------------|--|---|--|---------------------|------------|------|---------------|
| $ V_{Odl} $       | Driver differential output voltage magnitude                                     | RS-485 with common-mode load, $V_{CC} > 4.75\text{ V}$ , See Figure 1             |  | 1.37                |            |      | V             |
|                   |  | $R_L = 54\ \Omega$ , $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$               |  | 1.5                 | 2          |      |               |
|                   |  | $R_L = 100\ \Omega$ , $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$              |  | 2                   | 2.5        |      |               |
| $\Delta V_{Odl} $ | Change in magnitude of driver differential output voltage                        | $R_L = 54\ \Omega$  |  | -0.2                | 0          | 0.2  | V             |
| $V_{OC(SS)}$      | Steady-state common-mode output voltage  |   |  | 1                   | $V_{CC}/2$ | 3    | V             |
| $\Delta V_{OC}$   | Change in differential driver output common-mode voltage                         |   |  | -100                | 0          | 100  | mV            |
| $V_{OC(PP)}$      | Peak-to-peak driver common-mode output voltage                                   | Center of two 27- $\Omega$ load resistors, See Figure 2                           |  |                     | 500        |      | mV            |
| $C_{OD}$          | Differential output capacitance  |   |  |                     | 23         |      | pF            |
| $V_{IT+}$         | Positive-going receiver differential input voltage threshold                     | $V_{CM} = -20\text{ V to } 25\text{ V}$   |  |                     | -100       | -10  | mV            |
| $V_{IT-}$         | Negative-going receiver differential input voltage threshold                     |   |  | -205                | -150       | mV   |               |
| $V_{HYS}$         | Receiver differential input voltage threshold hysteresis ( $V_{IT+} - V_{IT-}$ ) |   |  | 30                  | 50         | mV   |               |
| $V_{OH}$          | Receiver high-level output voltage   | $I_{OH} = -8\text{ mA}$   |  | 2.4                 | $V_{CC}$   | -0.3 | V             |
|                   |  | $I_{OH} = -400\ \mu\text{A}$  |  | 4                   |            |      |               |
| $V_{OL}$          | Receiver low-level output voltage  | $I_{OL} = 8\text{ mA}$  |  |                     | 0.2        | 0.5  | V             |
| $I_I$             | Driver input, driver enable, and receiver enable input current                   |   |  | -100                |            | 100  | $\mu\text{A}$ |
| $I_{OZ}$          | Receiver output high-impedance current   | $V_O = 0\text{ V or } V_{CC}$ , $\overline{RE}$ at $V_{CC}$                       |  | -1                  |            | 1    | $\mu\text{A}$ |
| $I_{OS}$          | Driver short-circuit output current  |   |  | -250                |            | 250  | mA            |
| $I_I$             | Bus input current (disabled driver)  | $V_{CC} = 4.5\text{ to } 5.5\text{ V or } V_{CC} = 0\text{ V, DE at } 0\text{ V}$ |  |                     | 75         | 125  | $\mu\text{A}$ |
|                   |  |   |  | $V_I = 12\text{ V}$ |            |      |               |
|                   |  |   |  | -100                | -40        |      |               |

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER                |                            | TEST CONDITIONS                     |   | MIN   | TYP | MAX | UNIT |
|--------------------------|----------------------------|-------------------------------------|---|---|-----|-----|------|
| $I_{CC}$                 | Supply current (quiescent) | Driver and receiver enabled         | DE = $V_{CC}$ ,<br>RE = GND,<br>no load             |   | 4   | 6.3 | mA   |
|                          |                            | Driver enabled, receiver disabled   | DE = $V_{CC}$ ,<br>RE = $V_{CC}$ ,<br>no load       |   | 3   | 5.2 |      |
|                          |                            | Driver disabled, receiver enabled   | DE = GND,<br>RE = GND,<br>no load                   |   | 2   | 4.3 |      |
|                          |                            | Driver and receiver disabled        | DE = GND,<br>D = open<br>RE = $V_{CC}$ ,<br>no load | $T_J = -40^{\circ}\text{C}$ to<br>$105^{\circ}\text{C}$ |     | 0.5 | 5.2  |
|                          |                            | $T_J = 150^{\circ}\text{C}$         |   | 15  | 29  |     |      |
| Supply current (dynamic) |                            | See TYPICAL CHARACTERISTICS section |   |   |     |     |      |

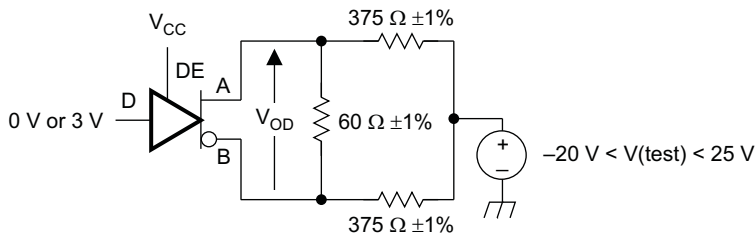
## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS   |  | MIN | TYP | MAX               | UNIT              |               |
|--|---|---|--|-----|-----|-------------------|-------------------|---------------|
| <b>DRIVER</b>  |   |   |  |     |     |                   |                   |               |
| $t_r, t_f$   | Driver differential output rise/fall time                       | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , See <a href="#">Figure 3</a> |  | 50  |     | 300               | ns                |               |
| $t_{PHL}, t_{PLH}$                                   | Driver propagation delay  |   |  |     |     | 200               | ns                |               |
| $t_{SK(P)}$  | Driver differential output pulse skew,<br>$ t_{PHL} - t_{PLH} $ |   |  |     |     | 29                | ns                |               |
| $t_{PHZ}, t_{PLZ}$                                   | Driver disable time   | Receiver enabled  | See <a href="#">Figure 4</a> and<br><a href="#">Figure 5</a> |     |     | 3                 | $\mu\text{s}$     |               |
| $t_{PZH}, t_{PZL}$                                   | Driver enable time  |   |  |     |     | Receiver disabled | 300               | ns            |
|  |   |   |  |     |     | Receiver enabled  | $V_{CM} > V_{CC}$ | 10            |
| <b>RECEIVER</b>                                      |   |   |  |     |     |                   |                   |               |
| $t_r, t_f$   | Receiver output rise/fall time                                  | $C_L = 15 \text{ pF}$ , See <a href="#">Figure 6</a>                  |  |     |     | 4                 | 15                | ns            |
| $t_{PHL}, t_{PLH}$                                   | Receiver propagation delay time                                 |   |  |     |     | 100               | 200               | ns            |
| $t_{SK(P)}$  | Receiver output pulse skew,<br>$ t_{PHL} - t_{PLH} $            |   |  |     |     | 6                 | 20                | ns            |
| $t_{PLZ}, t_{PHZ}$                                   | Receiver disable time   | Driver enabled, See <a href="#">Figure 7</a>                          |  |     |     | 15                | 100               | ns            |
| $t_{PZL(1)}, t_{PZH(1)}$<br>$t_{PZL(2)}, t_{PZH(2)}$ | Receiver enable time  | Driver enabled, See <a href="#">Figure 7</a>                          |  |     |     | 80                | 300               | ns            |
|  |   | Driver disabled, See <a href="#">Figure 8</a>                         |  |     |     | 3                 | 9                 | $\mu\text{s}$ |

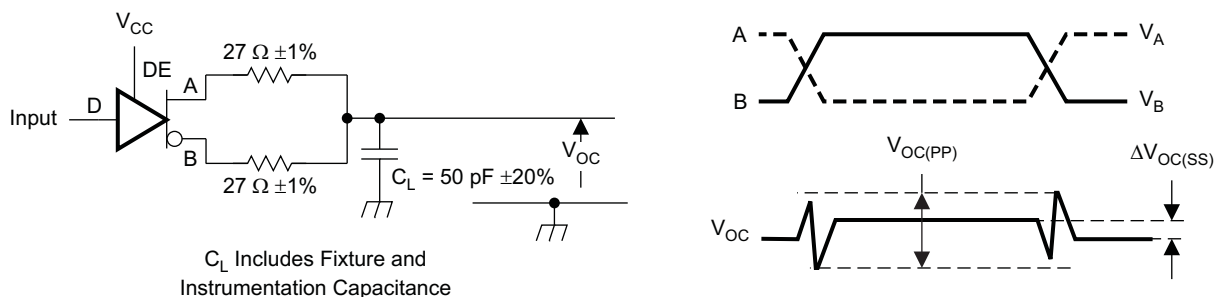
### PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.



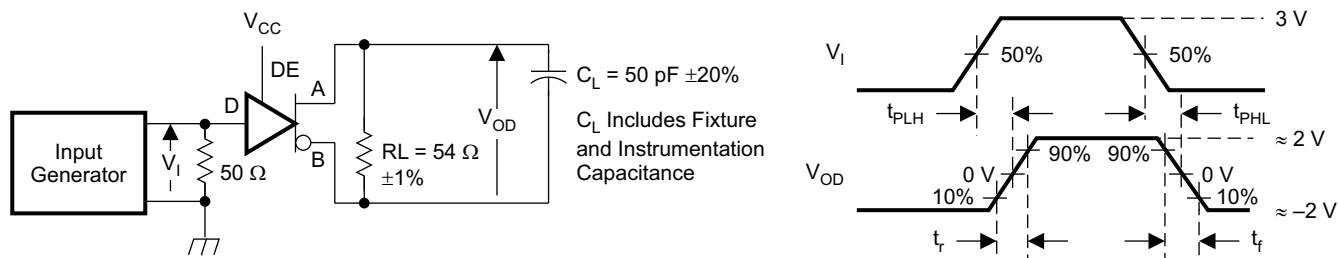
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**Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load**



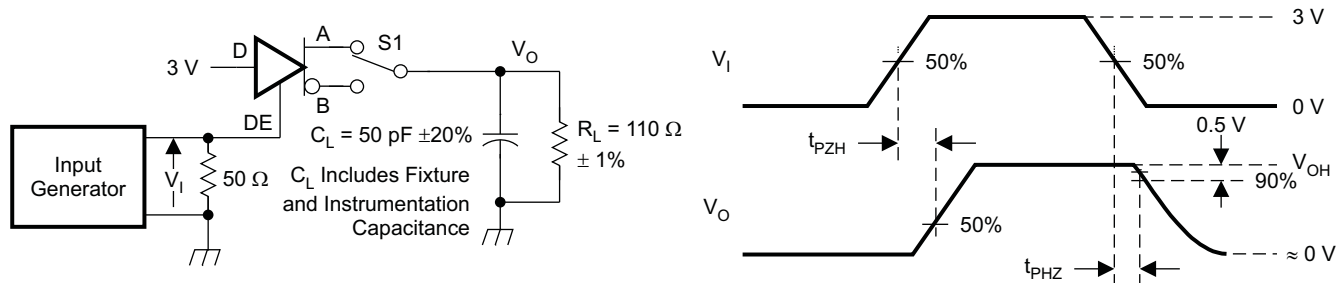
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**Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load**



S0303-01

**Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays**



S0304-01

NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

**Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load**

PARAMETER MEASUREMENT INFORMATION (continued)

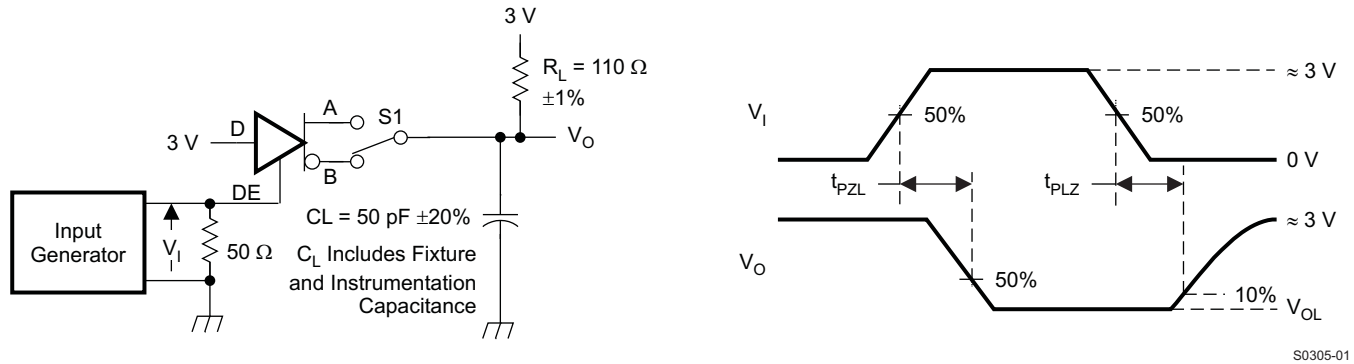


Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

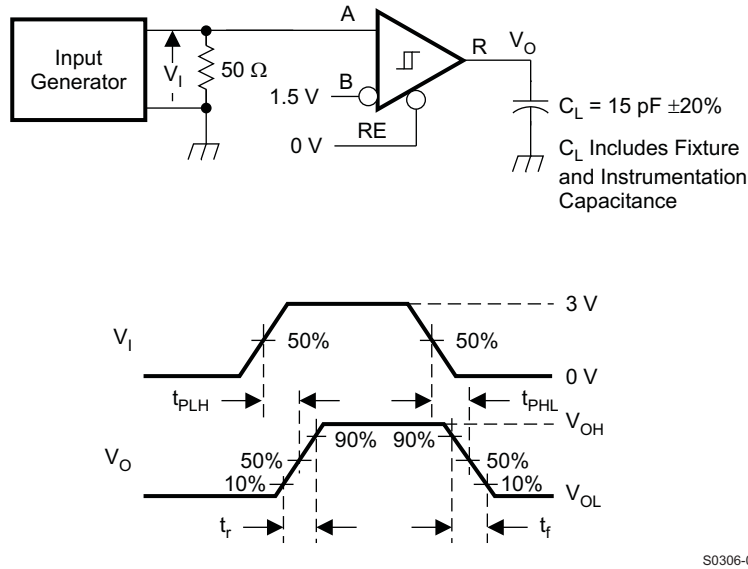
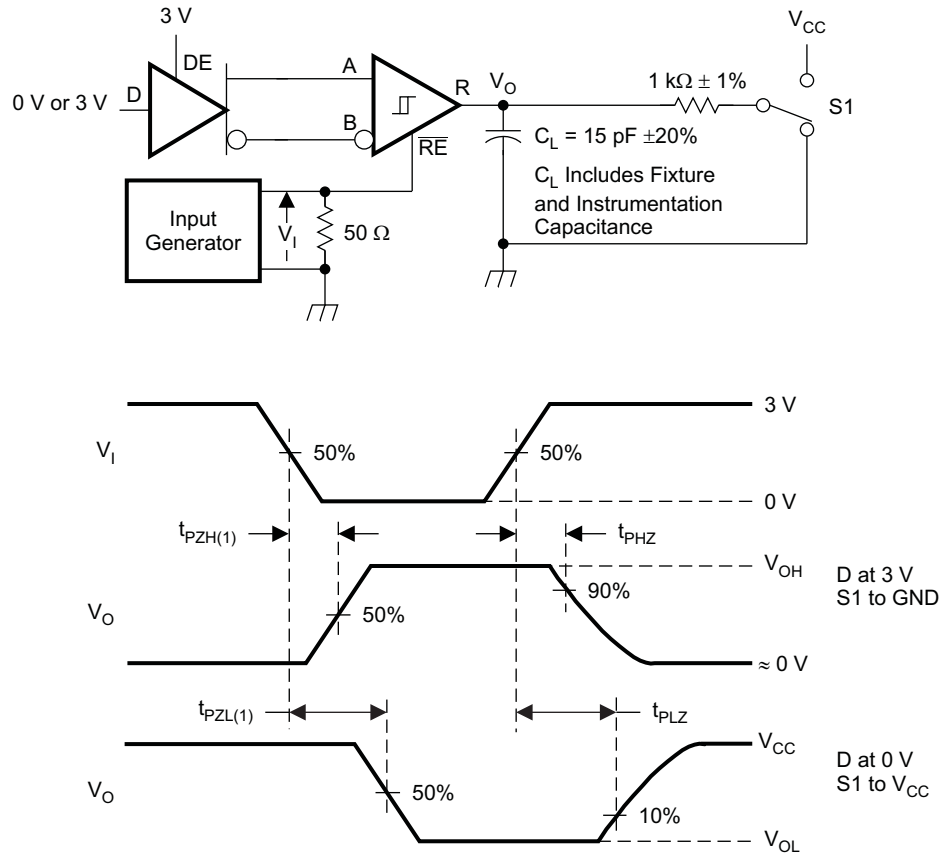


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

**PARAMETER MEASUREMENT INFORMATION (continued)**



S0307-01

**Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled**

PARAMETER MEASUREMENT INFORMATION (continued)

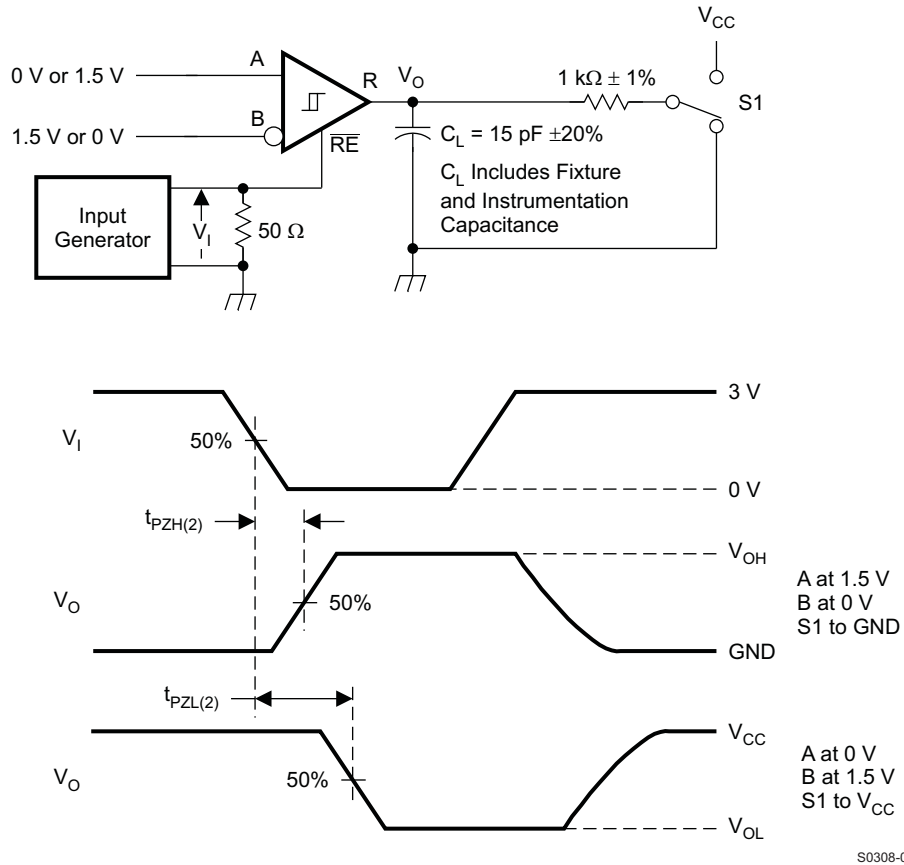
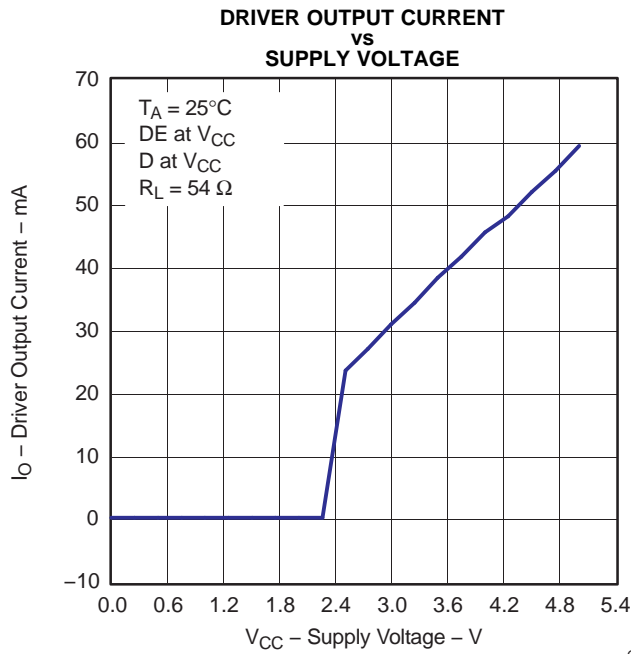
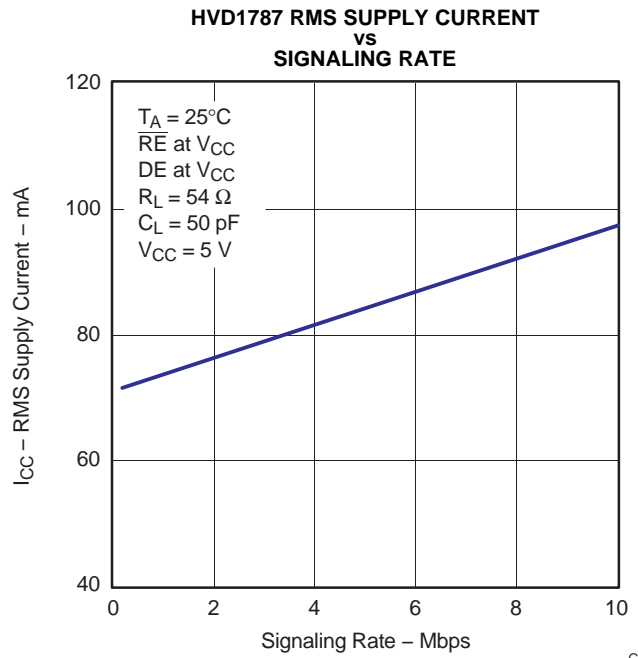


Figure 8. Measurement of Receiver Enable Times With Driver Disabled

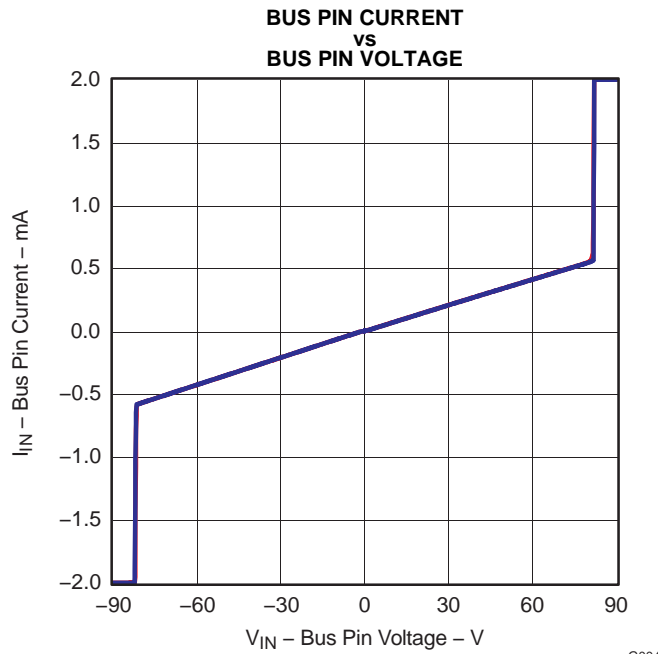
**TYPICAL CHARACTERISTICS**



**Figure 9.**



**Figure 10.**



**Figure 11.**

**TYPICAL CHARACTERISTICS (continued)**  
DIFFERENTIAL OUTPUT VOLTAGE  
vs  
DIFFERENTIAL LOAD CURRENT

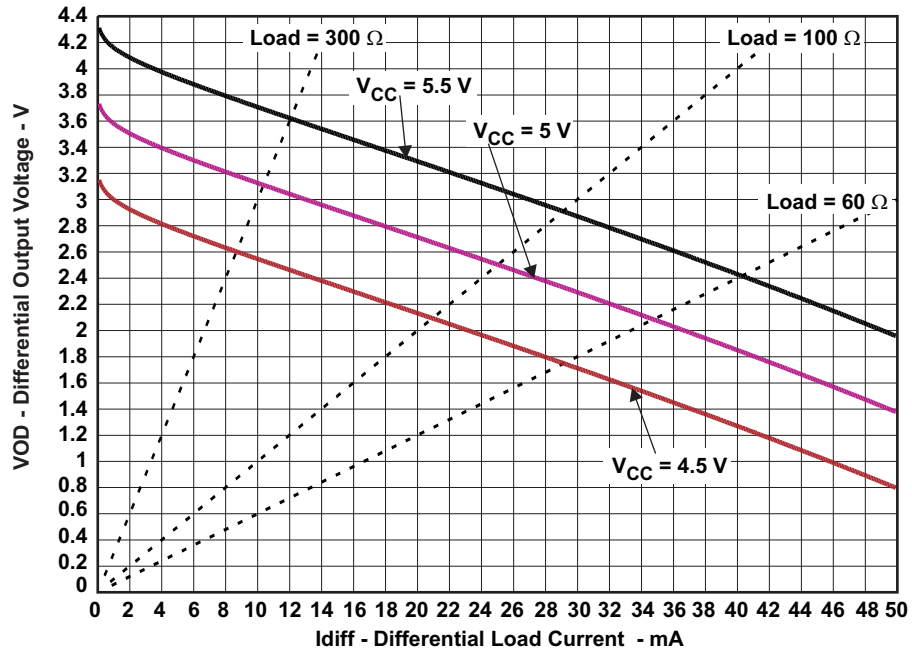


Figure 12.

### ADDITIONAL OPTIONS

The SN65HVD1792 also has options for J1708 applications, for always-enabled full-duplex versions (industry-standard SN65LBC179 footprint) and for inverting-polarity versions, which allow users to correct a reversal of the bus wires without re-wiring. Contact your local Texas Instruments representative for information on these options.

| PART NUMBER                               | SN65HVD1792 |        |      |
|---|-------------|--------|------|
|   | SLOW        | MEDIUM | FAST |
| Half-duplex (176 pinout)                  | 85          | 86     | 87   |
| Full-duplex no enables (179 pinout)       | 88          | 89     | 90   |
| Full-duplex with enables (180 pinout)     | 91          | 92     | 93   |
| Half-duplex with cable invert             | 94          | 95     | 96   |
| Full-duplex with cable invert and enables | 97          | 98     | 99   |
| J1708                                     | 08          | 09     | 10   |

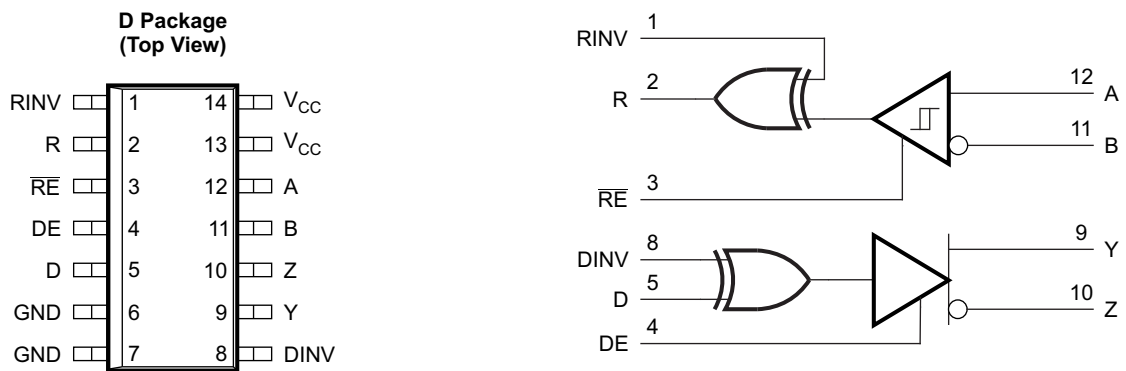


Figure 13. SN65HVD1792 With Inverting Feature to Correct for Miswired Cables

### APPLICATION INFORMATION

#### Hot-Plugging

The SN65HVD1792 is designed to operate in "hot swap" or "hot pluggable" applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. As shown in Figure 9, an internal Power-On Reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device **FUNCTION TABLE**, the *ENABLE* inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

## Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together,
- or idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

In the SN65HVD1792, receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input  $V_{ID}$  is more positive than 200 mV, and must output a Low when the  $V_{ID}$  is more negative than -200 mV. The SN65HVD1792 receiver parameters which determine the failsafe performance are  $V_{IT+}$  and  $V_{IT-}$  and  $V_{HYS}$ . In the *Electrical Characteristics* table,  $V_{IT-}$  has a typical value of -150 mV and a minimum (most negative) value of -200 mV, so differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than 200 mV will always cause a High receiver output, because the typical value of  $V_{IT+}$  is -100mV, and  $V_{IT+}$  is never more positive than -10 mV under any conditions of temperature, supply voltage, or common-mode offset.

When the differential input signal is close to zero, it will still be above the  $V_{IT+}$  threshold, and the receiver output will be High. Only when the differential input is more negative than  $V_{IT-}$  will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value  $V_{HYS}$  (the separation between  $V_{IT+}$  and  $V_{IT-}$ ) as well as the value of  $V_{IT+}$ .

For the SN65HVD1792, the typical noise immunity is typically about 150 mV, which is the negative noise level needed to exceed the  $V_{IT-}$  threshold ( $V_{IT-}$  TYP = -150 mV). In the worst case, the failsafe noise immunity is never less than 40 mV, which is set by the maximum positive threshold ( $V_{IT+}$  MAX = -10mV) plus the minimum hysteresis voltage ( $V_{HYS}$  MIN = 30 mV).

## 70-V Fault-Protection

The SN65HVD1792 is designed to survive bus pin faults up to  $\pm 70V$ . The devices designed for fast signaling rate (10 Mbps) will not survive a bus pin fault with a direct short to voltages above 30V when:

1. the device is powered on AND
  - 2a. the driver is enabled (DE=HIGH) AND D=HIGH AND the bus fault is applied to the A pin OR
  - 2b. the driver is enabled (DE=HIGH) AND D=LOW AND the bus fault is applied to the B pin

Under other conditions, the device will survive shorts to bus pin faults up to 70V. [Table 1](#) summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

**Table 1. Device Conditions**

| POWER | DE | D | A                  | B                  | RESULTS          |
|-------|----|---|--------------------|--------------------|------------------|
| OFF   | X  | X | $-70V < V_A < 70V$ | $-70V < V_B < 70V$ | Device survives  |
| ON    | LO | X | $-70V < V_A < 70V$ | $-70V < V_B < 70V$ | Device survives  |
| ON    | HI | L | $-70V < V_A < 70V$ | $-70V < V_B < 30V$ | Device survives  |
| ON    | HI | L | $-70V < V_A < 70V$ | $30V < V_B$        | Damage may occur |
| ON    | HI | H | $-70V < V_A < 30V$ | $-70V < V_B < 30V$ | Device survives  |
| ON    | HI | H | $30V < V_A$        | $-70V < V_B < 30V$ | Damage may occur |

**PACKAGING INFORMATION**

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN65HVD1792TDEP</a>  | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 1792EP              |
| SN65HVD1792TDEP.A                | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 1792EP              |
| <a href="#">SN65HVD1792TDREP</a> | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 1792EP              |
| SN65HVD1792TDREP.A               | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 1792EP              |
| <a href="#">V62/13620-01XE</a>   | Active        | Production           | SOIC (D)   14  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 1792EP              |
| <a href="#">V62/13620-01XE-T</a> | Active        | Production           | SOIC (D)   14  | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 1792EP              |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN65HVD1792-EP :**

- Catalog : [SN65HVD1792](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65HVD1792TDREP | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65HVD1792TDREP | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65HVD1792TDEP   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN65HVD1792TDEP.A | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| V62/13620-01XE-T  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |

D0014A



# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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