



IDT 128K X 36, 256K X 18
 3.3V Synchronous SRAMs
 2.5V I/O, Pipelined Outputs,
 Burst Counter, Single Cycle Deselect

IDT71V2576S
IDT71V2578S
IDT71V2576SA
IDT71V2578SA

Features

- ◆ 128K x 36, 256K x 18 memory configurations
- ◆ Supports high system speed:
Commercial and Industrial:
 - 150MHz 3.8ns clock access time
 - 133MHz 4.2ns clock access time
- ◆ **LBO** input selects interleaved or linear burst mode
- ◆ Self-timed write cycle with global write control (**GW**), byte write enable (**BWE**), and byte writes (**BW_x**)
- ◆ 3.3V core power supply
- ◆ Power down controlled by **ZZ** input
- ◆ 2.5V I/O
- ◆ Optional - Boundary Scan JTAG Interface (IEEE 1149.1 compliant)
- ◆ Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA)

Description

The IDT71V2576/78 are high-speed SRAMs organized as 128K x 36/256K x 18. The IDT71V2576/78 SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V2576/78 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected (**ADV**=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the **LBO** input pin.

The IDT71V2576/78 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA).

Pin Description Summary

| | | | |
|---|-----------------------------------|--------|--------------|
| A ₀ -A ₁₇ | Address Inputs | Input | Synchronous |
| \overline{CE} | Chip Enable | Input | Synchronous |
| CS ₀ , \overline{CS}_1 | Chip Selects | Input | Synchronous |
| \overline{OE} | Output Enable | Input | Asynchronous |
| \overline{GW} | Global Write Enable | Input | Synchronous |
| \overline{BWE} | Byte Write Enable | Input | Synchronous |
| \overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 , $\overline{BW}_4^{(1)}$ | Individual Byte Write Selects | Input | Synchronous |
| CLK | Clock | Input | N/A |
| \overline{ADV} | Burst Address Advance | Input | Synchronous |
| \overline{ADSC} | Address Status (Cache Controller) | Input | Synchronous |
| \overline{ADSP} | Address Status (Processor) | Input | Synchronous |
| \overline{LBO} | Linear / Interleaved Burst Order | Input | DC |
| TMS | Test Mode Select | Input | Synchronous |
| TDI | Test Data Input | Input | Synchronous |
| TCK | Test Clock | Input | N/A |
| TDO | Test Data Output | Output | Synchronous |
| \overline{TRST} | JTAG Reset (Optional) | Input | Asynchronous |
| ZZ | Sleep Mode | Input | Asynchronous |
| I/O ₀ -I/O ₃₁ , I/OP ₁ -I/OP ₄ | Data Input / Output | I/O | Synchronous |
| V _{DD} , V _{DDQ} | Core Power, I/O Power | Supply | N/A |
| V _{SS} | Ground | Supply | N/A |

NOTE:

1. \overline{BW}_3 and \overline{BW}_4 are not applicable for the IDT71V2578.

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JUNE 2003

Pin Definitions⁽¹⁾

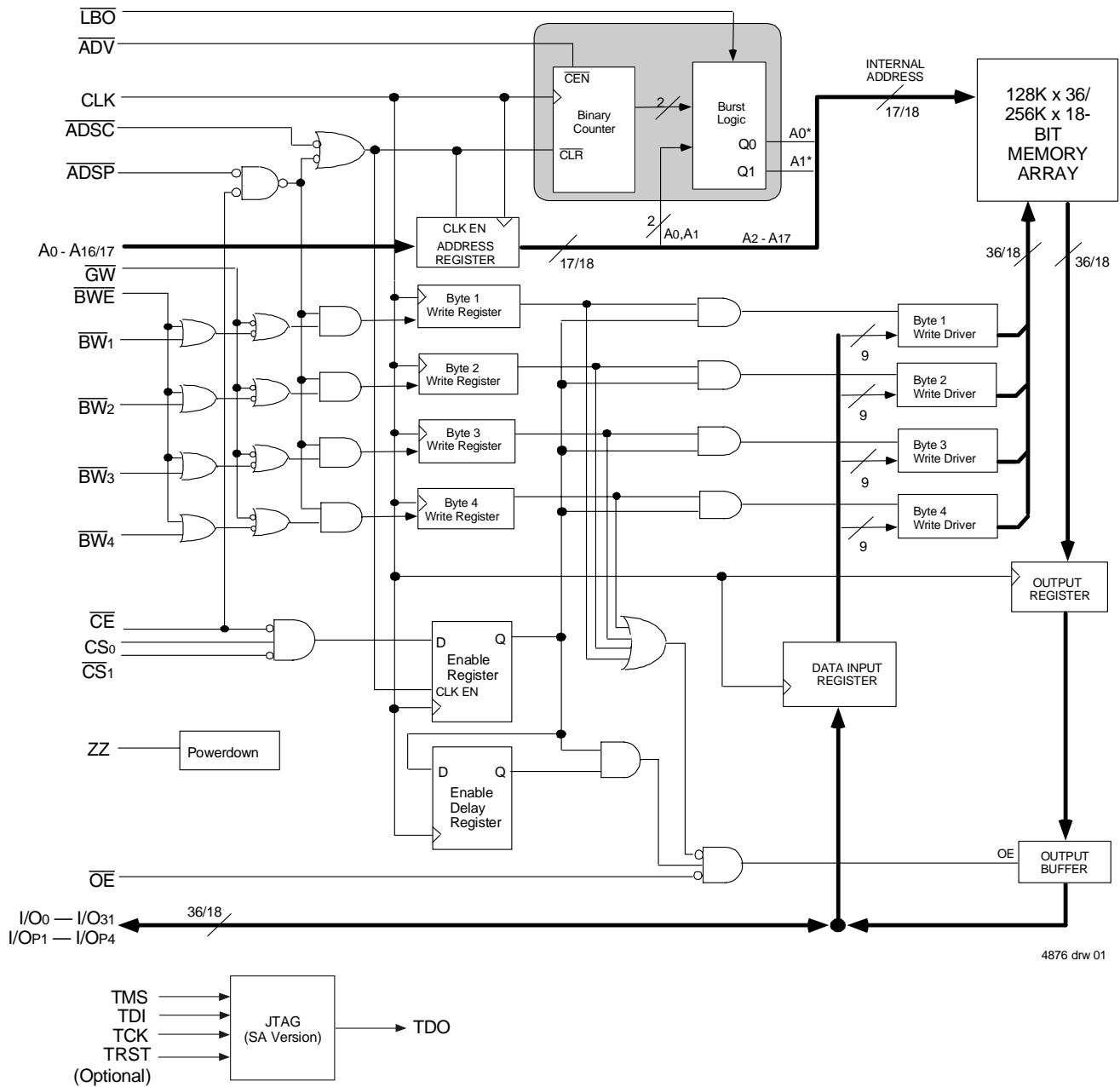
| Symbol | Pin Function | I/O | Active | Description |
|-------------------------------------|-----------------------------------|-----|--------|--|
| A0-A17 | Address Inputs | I | N/A | Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and \overline{ADSC} Low or \overline{ADSP} Low and \overline{CE} Low. |
| \overline{ADSC} | Address Status (Cache Controller) | I | LOW | Synchronous Address Status from Cache Controller. \overline{ADSC} is an active LOW input that is used to load the address registers with new addresses. |
| \overline{ADSP} | Address Status (Processor) | I | LOW | Synchronous Address Status from Processor. \overline{ADSP} is an active LOW input that is used to load the address registers with new addresses. \overline{ADSP} is gated by \overline{CE} . |
| \overline{ADV} | Burst Address Advance | I | LOW | Synchronous Address Advance. \overline{ADV} is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance. |
| \overline{BWE} | Byte Write Enable | I | LOW | Synchronous byte write enable gates the byte write inputs $\overline{BW1}$ - $\overline{BW4}$. If \overline{BWE} is LOW at the rising edge of CLK then \overline{BWx} inputs are passed to the next stage in the circuit. If \overline{BWE} is HIGH then the byte write inputs are blocked and only \overline{GW} can initiate a write cycle. |
| $\overline{BW1}$ - $\overline{BW4}$ | Individual Byte Write Enables | I | LOW | Synchronous byte write enables. $\overline{BW1}$ controls I/O0-7, I/OP1, $\overline{BW2}$ controls I/O8-15, I/OP2, etc. Any active byte write causes all outputs to be disabled. |
| \overline{CE} | Chip Enable | I | LOW | Synchronous chip enable. \overline{CE} is used with $\overline{CS0}$ and $\overline{CS1}$ to enable the IDT71V2576/78. \overline{CE} also gates \overline{ADSP} . |
| CLK | Clock | I | N/A | This is the clock input. All timing references for the device are made with respect to this input. |
| $\overline{CS0}$ | Chip Select 0 | I | HIGH | Synchronous active HIGH chip select. $\overline{CS0}$ is used with \overline{CE} and $\overline{CS1}$ to enable the chip. |
| $\overline{CS1}$ | Chip Select 1 | I | LOW | Synchronous active LOW chip select. $\overline{CS1}$ is used with \overline{CE} and $\overline{CS0}$ to enable the chip. |
| \overline{GW} | Global Write Enable | I | LOW | Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. \overline{GW} supersedes individual byte write enables. |
| I/O0-I/O31 I/OP1-I/OP4 | Data Input/Output | I/O | N/A | Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK. |
| \overline{LBO} | Linear Burst Order | I | LOW | Asynchronous burst order selection input. When \overline{LBO} is HIGH, the interleaved burst sequence is selected. When \overline{LBO} is LOW the Linear burst sequence is selected. \overline{LBO} is a static input and must not change state while the device is operating. |
| \overline{OE} | Output Enable | I | LOW | Asynchronous output enable. When \overline{OE} is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When \overline{OE} is HIGH the I/O pins are in a high-impedance state. |
| TMS | Test ModeSelect | I | N/A | Gives input command for TAP controller. Sampled on rising edge of TDK. This pin has an internal pullup. |
| TDI | Test Data Input | I | N/A | Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup. |
| TCK | Test Clock | I | N/A | Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK. This pin has an internal pullup. |
| TDO | Test DataOutput | O | N/A | Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller. |
| \overline{TRST} | JTAG Reset (Optional) | I | LOW | Optional Asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used \overline{TRST} can be left floating. This pin has an internal pullup. Only available in BGA package. |
| ZZ | Sleep Mode | I | HIGH | Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V2576/78 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pull down. |
| VDD | Power Supply | N/A | N/A | 3.3V core power supply. |
| VDDQ | Power Supply | N/A | N/A | 2.5V I/O Supply. |
| VSS | Ground | N/A | N/A | Ground. |
| NC | No Connect | N/A | N/A | NC pins are not electrically connected to the device. |

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

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Functional Block Diagram



Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial | Unit |
|------------------------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| V _{TERM} ^(3,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DD} | V |
| V _{TERM} ^(4,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DD} +0.5 | V |
| V _{TERM} ^(5,6) | Terminal Voltage with Respect to GND | -0.5 to V _{DDQ} +0.5 | V |
| T _A ⁽⁷⁾ | Commercial Operating Temperature | -0 to +70 | °C |
| | Industrial Operating Temperature | -40 to +85 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | °C |
| P _T | Power Dissipation | 2.0 | W |
| I _{OUT} | DC Output Current | 50 | mA |

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD} terminals only.
- V_{DDQ} terminals only.
- Input terminals only.
- I/O terminals only.
- This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
- T_A is the "instant on" case temperature

100 TQFP Capacitance

(T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 5 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

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165 fBGA Capacitance

(T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 7 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

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NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature ⁽¹⁾ | V _{SS} | V _{DD} | V _{DDQ} |
|------------|----------------------------|-----------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 0V | 3.3V±5% | 2.5V±5% |
| Industrial | -40°C to +85°C | 0V | 3.3V±5% | 2.5V±5% |

NOTES:

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- T_A is the "instant on" case temperature

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------|---------------------|------|--------------------------------------|------|
| V _{DD} | Core Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| V _{DDQ} | I/O Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| V _{SS} | Supply Voltage | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage - Inputs | 1.7 | — | V _{DD} +0.3 | V |
| V _{IH} | Input High Voltage - I/O | 1.7 | — | V _{DDQ} +0.3 ⁽¹⁾ | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽²⁾ | — | 0.7 | V |

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NOTES:

- V_{IH} (max) = V_{DDQ} + 1.0V for pulse width less than t_{CV}/2, once per cycle.
- V_{IL} (min) = -1.0V for pulse width less than t_{CV}/2, once per cycle.

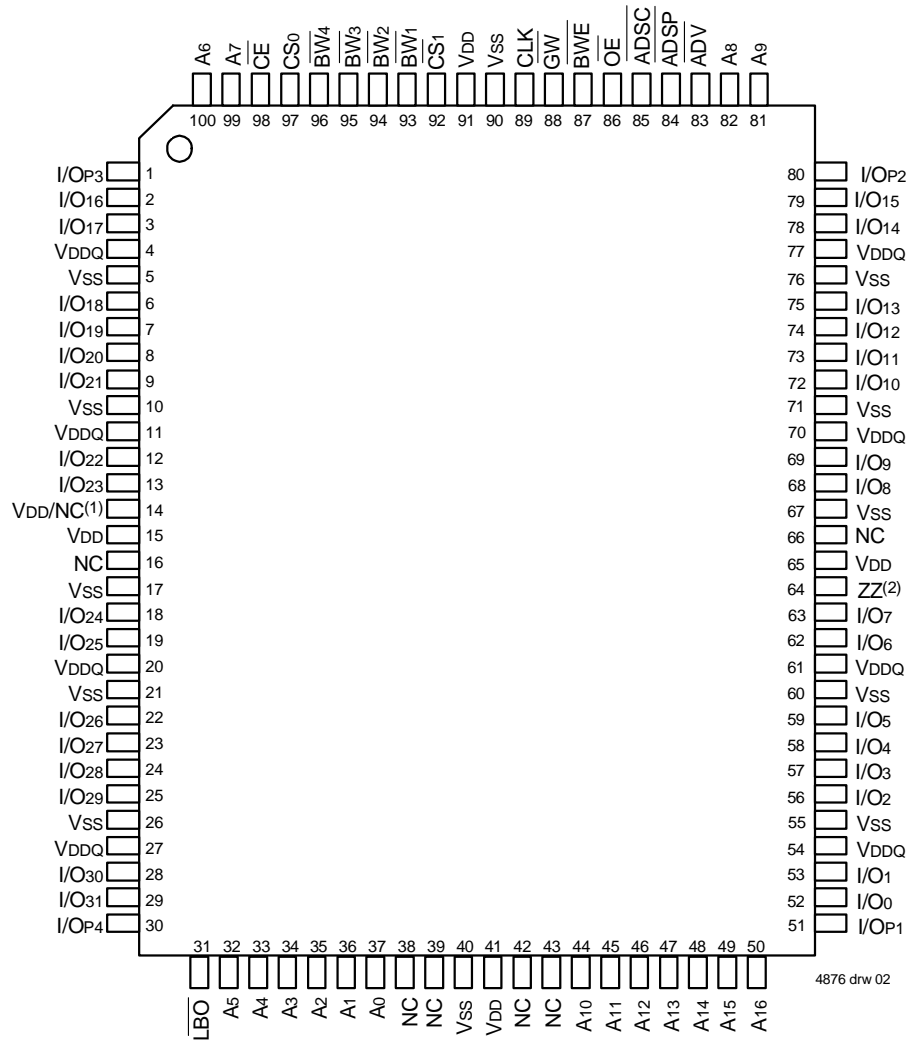
119 BGA Capacitance

(T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 7 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 3dV | 7 | pF |

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Pin Configuration – 128K x 36

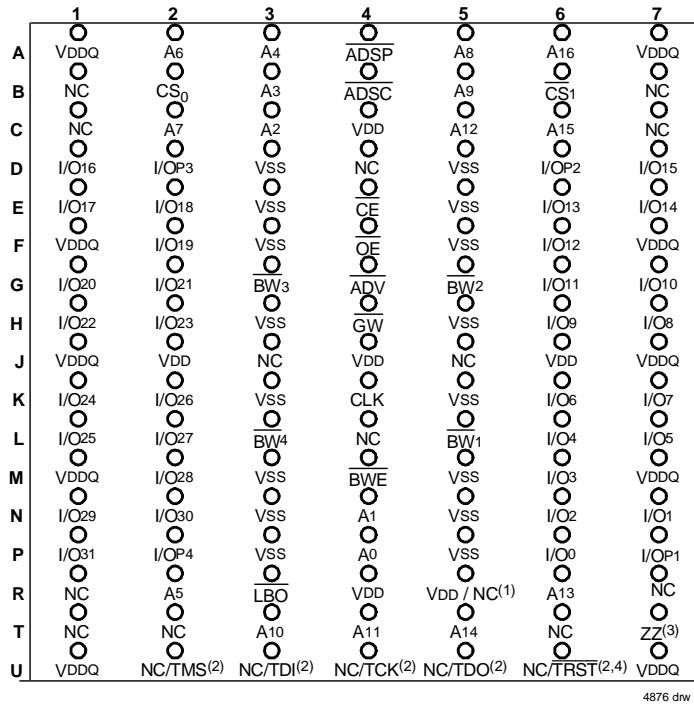


100 TQFP Top View

NOTES:

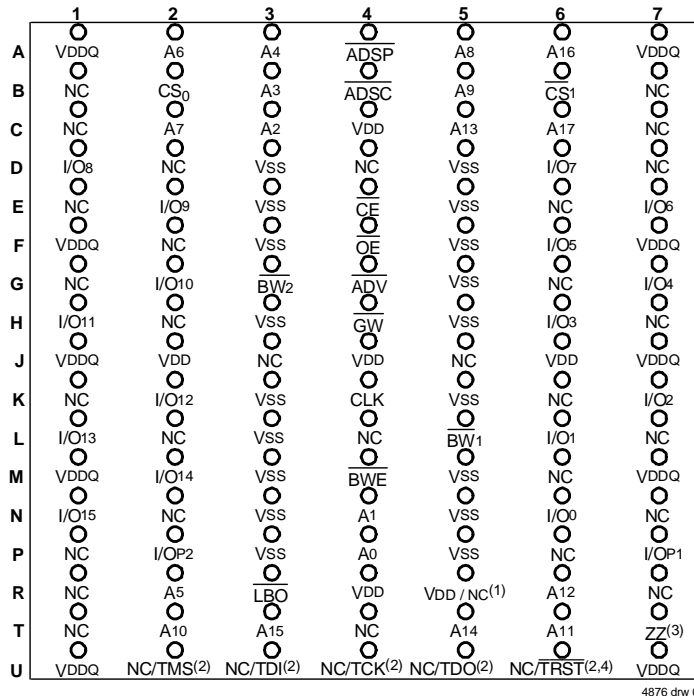
- Pin 14 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
- Pin 64 can be left unconnected and the device will always remain in active mode.

Pin Configuration – 128K x 36, 119 BGA



Top View

Pin Configuration – 256K x 18, 119 BGA



Top View

NOTES:

1. R5 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. These pins are NC for the "S" version or the JTAG signal listed for the "SA" version. Note: If NC, these pins can either be tied to VSS, VDD or left floating.
3. T7 can be left unconnected and the device will always remain in active mode.
4. TRST is offered as an optional JTAG Reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.

Pin Configuration – 128K x 36, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|-------------------|-------------------|-------------------|--------------------------|-------------------|-----------------------|-------------------|-------------------|-------------------|-------------------|
| A | NC ⁽⁴⁾ | A7 | \overline{CE}_1 | \overline{BW}_3 | \overline{BW}_2 | \overline{CS}_1 | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A8 | NC |
| B | NC | A6 | CS0 | \overline{BW}_4 | \overline{BW}_1 | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A9 | NC ⁽⁴⁾ |
| C | I/O _{P3} | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/O _{P2} |
| D | I/O ₁₇ | I/O ₁₆ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁₅ | I/O ₁₄ |
| E | I/O ₁₉ | I/O ₁₈ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁₃ | I/O ₁₂ |
| F | I/O ₂₁ | I/O ₂₀ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁₁ | I/O ₁₀ |
| G | I/O ₂₃ | I/O ₂₂ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₉ | I/O ₈ |
| H | VDD ⁽¹⁾ | NC | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ ⁽³⁾ |
| J | I/O ₂₅ | I/O ₂₄ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₇ | I/O ₆ |
| K | I/O ₂₇ | I/O ₂₆ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₅ | I/O ₄ |
| L | I/O ₂₉ | I/O ₂₈ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₃ | I/O ₂ |
| M | I/O ₃₁ | I/O ₃₀ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁ | I/O ₀ |
| N | I/O _{P4} | NC | VDDQ | VSS | NC/TRST ^(2,5) | NC ⁽⁴⁾ | NC | VSS | VDDQ | NC | I/O _{P1} |
| P | NC | NC ⁽⁴⁾ | A5 | A2 | NC/TDI ⁽²⁾ | A1 | NC/TDO ⁽²⁾ | A10 | A13 | A14 | NC ⁽⁴⁾ |
| R | \overline{LBO} | NC ⁽⁴⁾ | A4 | A3 | NC/TMS ⁽²⁾ | A0 | NC/TCK ⁽²⁾ | A11 | A12 | A15 | A16 |

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Pin Configuration – 256K x 18, 165 fBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|--------------------|-------------------|-------------------|-------------------|--------------------------|-------------------|-----------------------|-------------------|-------------------|------------------|-------------------|
| A | NC ⁽⁴⁾ | A7 | \overline{CE}_1 | \overline{BW}_2 | NC | \overline{CS}_1 | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A8 | A10 |
| B | NC | A6 | CS0 | NC | \overline{BW}_1 | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A9 | NC ⁽⁴⁾ |
| C | NC | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | I/O _{P1} |
| D | NC | I/O ₈ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₇ |
| E | NC | I/O ₉ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₆ |
| F | NC | I/O ₁₀ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₅ |
| G | NC | I/O ₁₁ | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | I/O ₄ |
| H | VDD ⁽¹⁾ | NC | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ ⁽³⁾ |
| J | I/O ₁₂ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₃ | NC |
| K | I/O ₁₃ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₂ | NC |
| L | I/O ₁₄ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₁ | NC |
| M | I/O ₁₅ | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | I/O ₀ | NC |
| N | I/O _{P2} | NC | VDDQ | VSS | NC/TRST ^(2,5) | NC ⁽⁴⁾ | NC | VSS | VDDQ | NC | NC |
| P | NC | NC ⁽⁴⁾ | A5 | A2 | NC/TDI ⁽²⁾ | A1 | NC/TDO ⁽²⁾ | A11 | A14 | A15 | NC ⁽⁴⁾ |
| R | \overline{LBO} | NC ⁽⁴⁾ | A4 | A3 | NC/TMS ⁽²⁾ | A0 | NC/TCK ⁽²⁾ | A12 | A13 | A16 | A17 |

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NOTES:

- H1 can either be directly connected to VDD, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
- These pins are NC for the "S" version or the JTAG signal listed for the "SA" version. Note: If NC, these pins can either be tied to VSS, VDD or left floating.
- H11 can be left unconnected and the device will always remain in active mode.
- Pins P11, N6, B11, A1, R2 and P2 are reserved for 9M, 18M, 36M, 72M, 144M and 288M respectively.
- TRST is offered as an optional JTAG Reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 5\%$)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-------------|---|--|------|------|---------|
| $ I_{LI} $ | Input Leakage Current | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 5 | μA |
| $ I_{LZZ} $ | ZZ \overline{LBO} and JTAG Input Leakage Current ⁽¹⁾ | $V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$ | — | 30 | μA |
| $ I_{LO} $ | Output Leakage Current | $V_{OUT} = 0V \text{ to } V_{DDQ}$, Device Deselected | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = +6mA, V_{DD} = \text{Min.}$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -6mA, V_{DD} = \text{Min.}$ | 2.0 | — | V |

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NOTE:

- The \overline{LBO} , TMS, TDI, TCK and TRST pins will be internally pulled to V_{DD} and the ZZ pin will be internally pulled to V_{SS} if they are not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾

| Symbol | Parameter | Test Conditions | 150MHz | | 133MHz | | Unit |
|-----------|------------------------------------|---|--------|-----|--------|-----|------|
| | | | Com'l | Ind | Com'l | Ind | |
| I_{DD} | Operating Power Supply Current | Device Selected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$ | 295 | 305 | 250 | 260 | mA |
| I_{SB1} | CMOS Standby Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2,3)}$ | 30 | 35 | 30 | 35 | mA |
| I_{SB2} | Clock Running Power Supply Current | Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{DDQ} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$ | 105 | 115 | 100 | 110 | mA |
| I_{ZZ} | Full Sleep Mode Supply Current | $ZZ \geq V_{HD}, V_{DD} = \text{Max.}$ | 30 | 35 | 30 | 35 | mA |

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NOTES:

- All values are maximum guaranteed values.
- At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$ while $\overline{ADSC} = \text{LOW}$; $f=0$ means no input lines are changing.
- For I/Os $V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V$. For other inputs $V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V$.

AC Test Conditions ($V_{DDQ} = 2.5V$)

| | |
|--------------------------------|---------------|
| Input Pulse Levels | 0 to 2.5V |
| Input Rise/Fall Times | 2ns |
| Input Timing Reference Levels | $(V_{DDQ}/2)$ |
| Output Timing Reference Levels | $(V_{DDQ}/2)$ |
| AC Test Load | See Figure 1 |

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AC Test Load

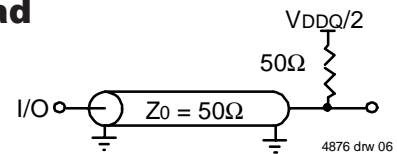


Figure 1. AC Test Load

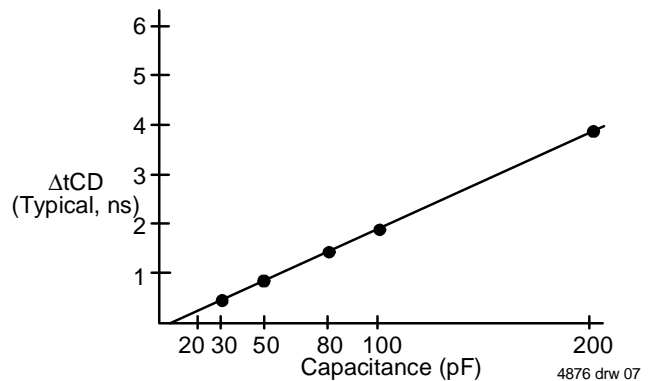


Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table^(1,3)

| Operation | Address Used | \overline{CE} | CS ₀ | \overline{CS}_1 | ADSP | ADSC | ADV | \overline{GW} | BWE | \overline{BW}_x | \overline{OE} (2) | CLK | I/O |
|------------------------------|--------------|-----------------|-----------------|-------------------|------|------|-----|-----------------|-----|-------------------|---------------------|-----|------|
| Deselected Cycle, Power Down | None | H | X | X | X | L | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | L | X | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | L | X | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | X | H | X | L | X | X | X | X | X | - | HI-Z |
| Deselected Cycle, Power Down | None | L | L | X | X | L | X | X | X | X | X | - | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | L | X | X | X | X | X | H | - | HI-Z |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | H | X | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | L | - | DOUT |
| Read Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | H | H | - | HI-Z |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | H | L | L | X | - | DI |
| Write Cycle, Begin Burst | External | L | H | L | H | L | X | L | X | X | X | - | DI |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | L | - | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | X | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | L | - | DOUT |
| Read Cycle, Continue Burst | Next | X | X | X | H | H | L | H | X | H | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | X | L | - | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | H | - | HI-Z |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | L | - | DOUT |
| Read Cycle, Continue Burst | Next | H | X | X | X | H | L | H | X | H | H | - | HI-Z |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | L | X | - | DI |
| Write Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | X | X | - | DI |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | L | X | - | DI |
| Write Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | X | X | - | DI |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | X | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | X | H | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | X | H | - | HI-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | L | - | DOUT |
| Read Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | X | H | H | - | HI-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | L | X | - | DI |
| Write Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | X | X | - | DI |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | L | X | - | DI |
| Write Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | X | X | - | DI |

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. \overline{OE} is an asynchronous input.
3. ZZ = low for this table.

4876 tbl 11

Synchronous Write Function Truth Table^(1, 2)

| Operation | \overline{GW} | \overline{BWE} | \overline{BW}_1 | \overline{BW}_2 | \overline{BW}_3 | \overline{BW}_4 |
|-----------------------------|-----------------|------------------|-------------------|-------------------|-------------------|-------------------|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write all Bytes | L | X | X | X | X | X |
| Write all Bytes | H | L | L | L | L | L |
| Write Byte 1 ⁽³⁾ | H | L | L | H | H | H |
| Write Byte 2 ⁽³⁾ | H | L | H | L | H | H |
| Write Byte 3 ⁽³⁾ | H | L | H | H | L | H |
| Write Byte 4 ⁽³⁾ | H | L | H | H | H | L |

4876 tbl 12

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. \overline{BW}_3 and \overline{BW}_4 are not applicable for the IDT71V2578.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table⁽¹⁾

| Operation ⁽²⁾ | \overline{OE} | ZZ | I/O Status | Power |
|--------------------------|-----------------|----|------------------|---------|
| Read | L | L | Data Out | Active |
| Read | H | L | High-Z | Active |
| Write | X | L | High-Z – Data In | Active |
| Deselected | X | L | High-Z | Standby |
| Sleep Mode | X | H | High-Z | Sleep |

4876 tbl 13

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}=V_{DD}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

4876 tbl 14

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}=V_{SS}$)

| | Sequence 1 | | Sequence 2 | | Sequence 3 | | Sequence 4 | |
|-------------------------------|------------|----|------------|----|------------|----|------------|----|
| | A1 | A0 | A1 | A0 | A1 | A0 | A1 | A0 |
| First Address | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Second Address | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| Third Address | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address ⁽¹⁾ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

4876 tbl 15

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC Electrical Characteristics (VDD = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

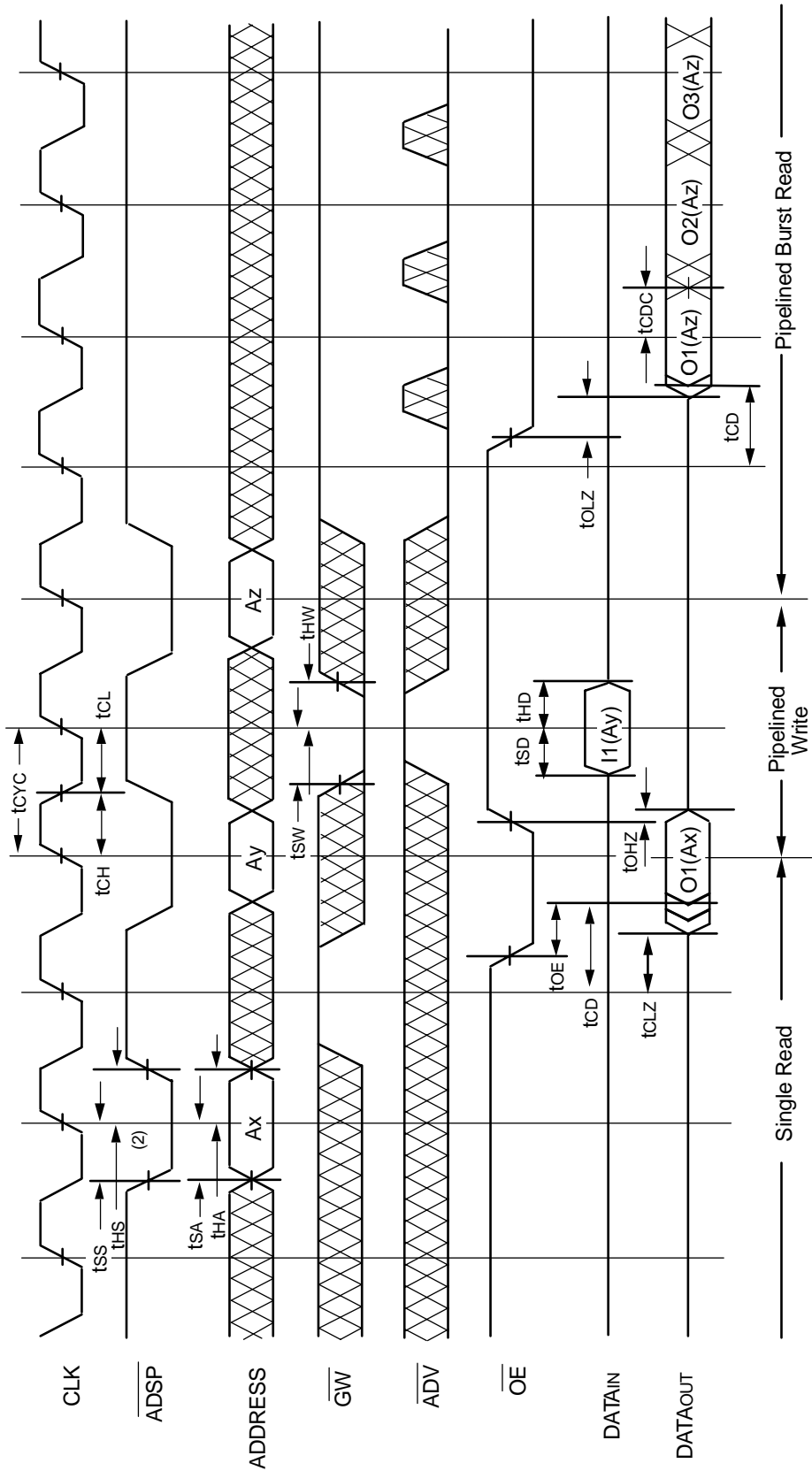
| Symbol | Parameter | 150MHz | | 133MHz | | Unit |
|--|-------------------------------------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{CYC} | Clock Cycle Time | 6.7 | — | 7.5 | — | ns |
| t _{CH} ⁽¹⁾ | Clock High Pulse Width | 2.6 | — | 3 | — | ns |
| t _{CL} ⁽¹⁾ | Clock Low Pulse Width | 2.6 | — | 3 | — | ns |
| Output Parameters | | | | | | |
| t _{CD} | Clock High to Valid Data | — | 3.8 | — | 4.2 | ns |
| t _{DC} | Clock High to Data Change | 1.5 | — | 1.5 | — | ns |
| t _{CLZ} ⁽²⁾ | Clock High to Output Active | 0 | — | 0 | — | ns |
| t _{CHZ} ⁽²⁾ | Clock High to Data High-Z | 1.5 | 3.8 | 1.5 | 4.2 | ns |
| t _{OE} | Output Enable Access Time | — | 3.8 | — | 4.2 | ns |
| t _{OLZ} ⁽²⁾ | Output Enable Low to Output Active | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽²⁾ | Output Enable High to Output High-Z | — | 3.8 | — | 4.2 | ns |
| Set Up Times | | | | | | |
| t _{SA} | Address Setup Time | 1.5 | — | 1.5 | — | ns |
| t _{SS} | Address Status Setup Time | 1.5 | — | 1.5 | — | ns |
| t _{SD} | Data In Setup Time | 1.5 | — | 1.5 | — | ns |
| t _{SW} | Write Setup Time | 1.5 | — | 1.5 | — | ns |
| t _{SAV} | Address Advance Setup Time | 1.5 | — | 1.5 | — | ns |
| t _{SC} | Chip Enable/Select Setup Time | 1.5 | — | 1.5 | — | ns |
| Hold Times | | | | | | |
| t _{HA} | Address Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{HS} | Address Status Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{HD} | Data In Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{HW} | Write Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{HAV} | Address Advance Hold Time | 0.5 | — | 0.5 | — | ns |
| t _{HC} | Chip Enable/Select Hold Time | 0.5 | — | 0.5 | — | ns |
| Sleep Mode and Configuration Parameters | | | | | | |
| t _{ZZPW} | ZZ Pulse Width | 100 | — | 100 | — | ns |
| t _{ZZR} ⁽³⁾ | ZZ Recovery Time | 100 | — | 100 | — | ns |
| t _{CFG} ⁽⁴⁾ | Configuration Set-up Time | 27 | — | 30 | — | ns |

4876 tbl 16

NOTES:

1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{\text{LB0}}$ input. $\overline{\text{LB0}}$ is a static input and must not change during normal operation.

Timing Waveform of Combined Pipelined Read and Write Cycles^(1,2,3)

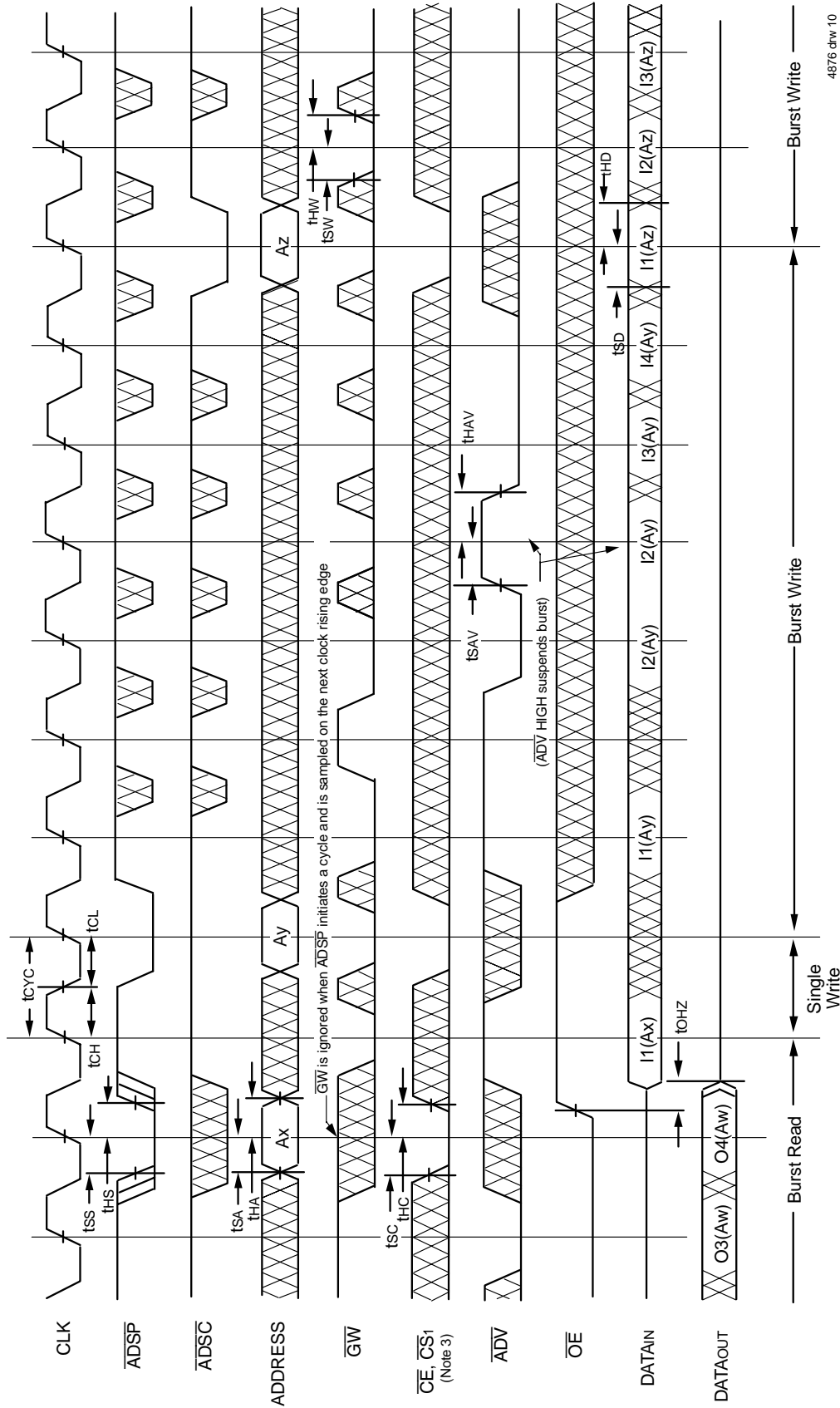


4876 drw 09

NOTES:

1. Device is selected through entire cycle: \overline{CE} and $\overline{CS1}$ are LOW, $\overline{CS0}$ is HIGH.
2. ZZ input is LOW and \overline{LBO} is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay. O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input.

Timing Waveform of Write Cycle No. 1 — \overline{GW} Controlled^(1,2,3)

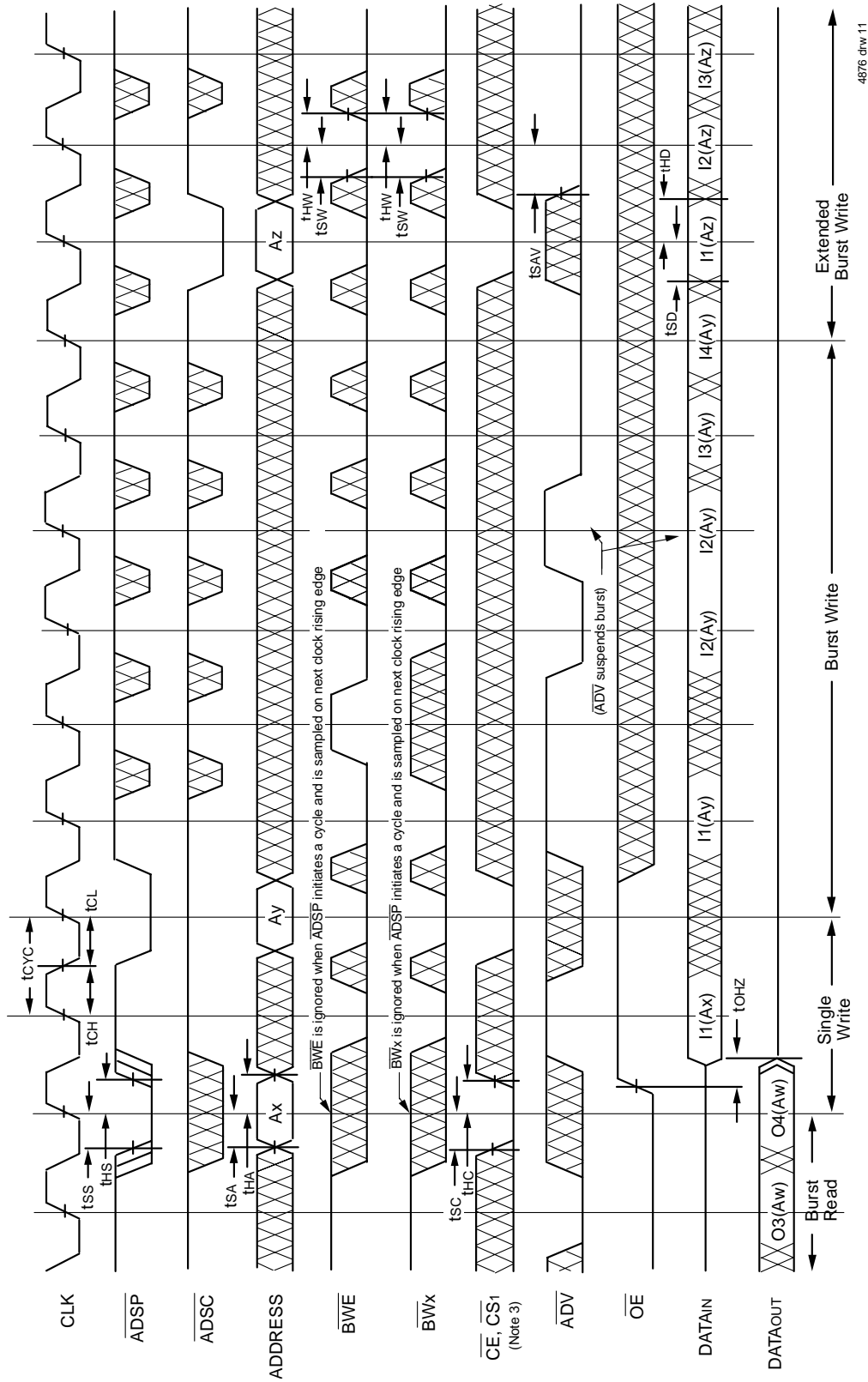


4876 drw 10

NOTES:

1. ZZ input is LOW, \overline{BWE} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay. I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input. In the case of input I2 (Ay) this data is valid for two cycles because \overline{ADV} is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Write Cycle No. 2 — Byte Controlled^(1,2,3)

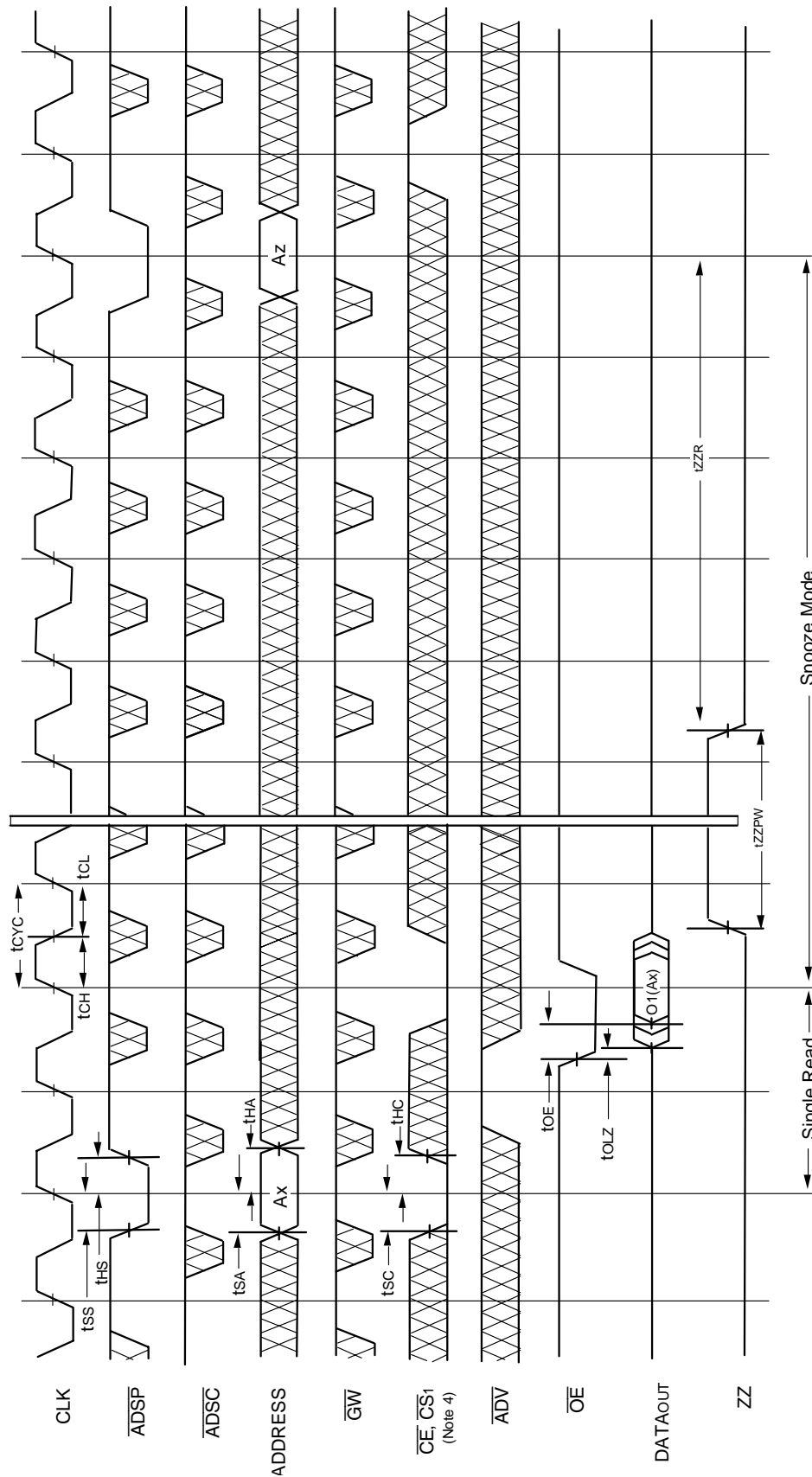


NOTES:

1. ZZ input is LOW, \overline{GW} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. O4(Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ay. I2 (Ay) represent the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input. In the case of input I2 (Ay) this data is valid for two cycles because \overline{ADV} is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the \overline{OE} and $\overline{CS1}$ signals. For example, when \overline{OE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

4876 drw 11

Timing Waveform of Sleep (ZZ) and Power-Down Modes^(1,2,3)

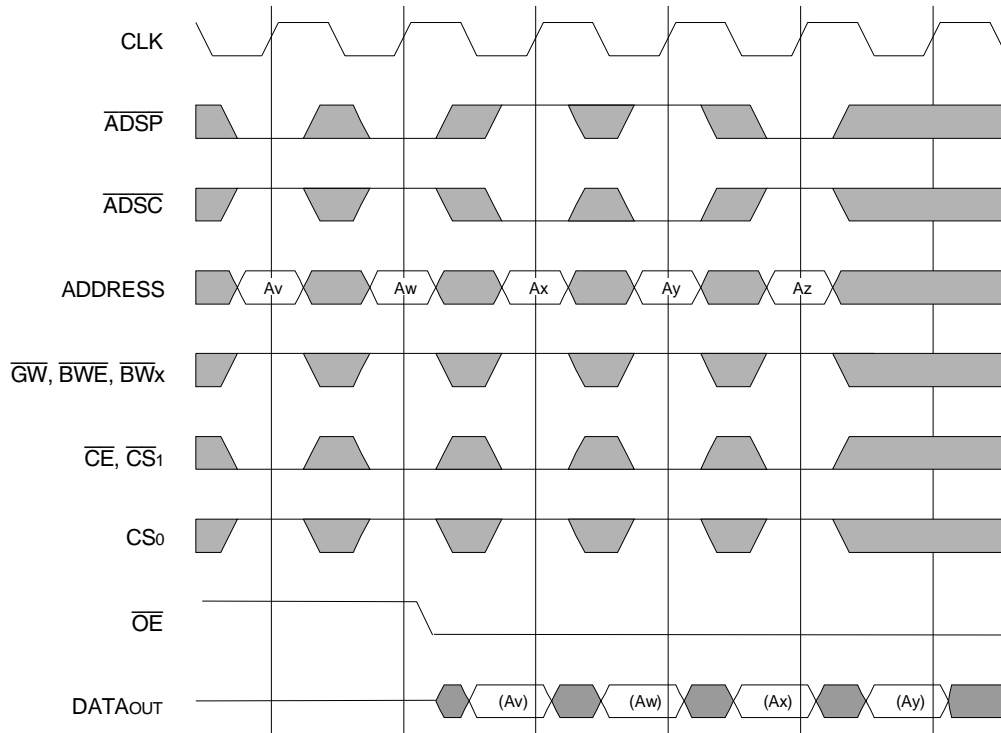


4876 drw 12

NOTES:

1. Device must power up in deselected Mode.
2. LBO is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform

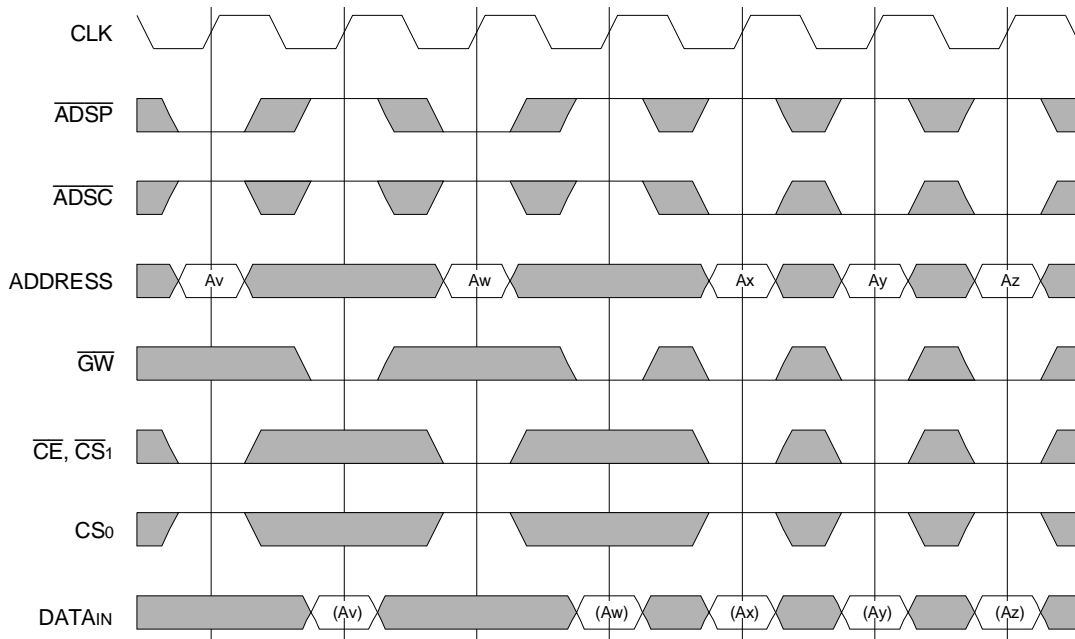


4876 drw 14

NOTES:

1. ZZ input is LOW, \overline{ADV} is HIGH and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, \overline{ADSP} and \overline{ADSC} function identically and are therefore interchangeable.

Non-Burst Write Cycle Timing Waveform

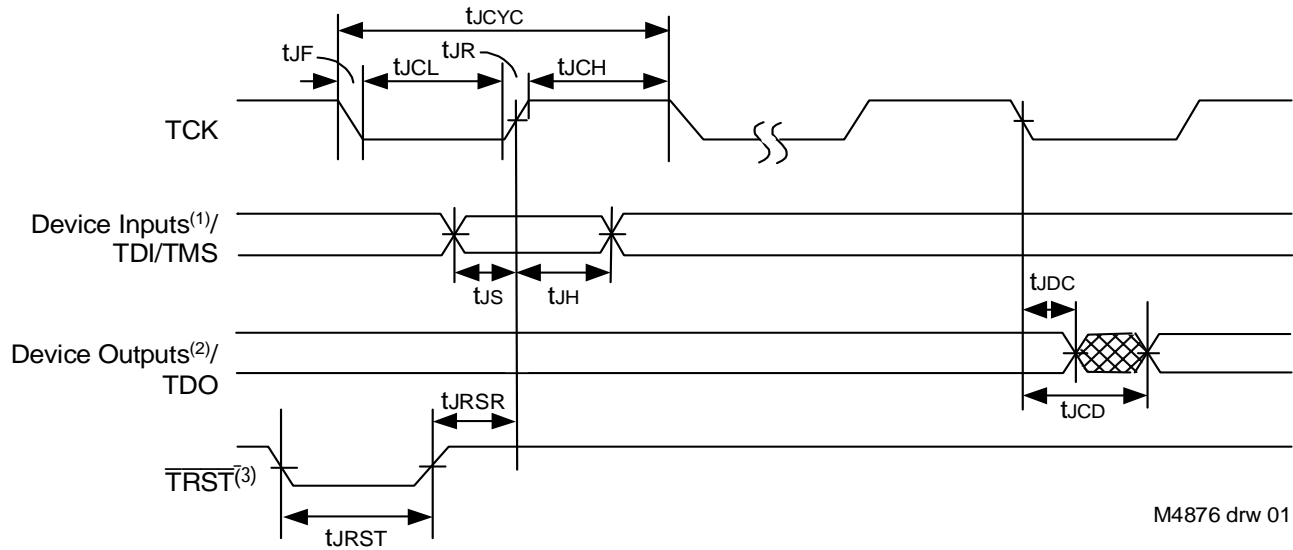


4876 drw 15

NOTES:

1. ZZ input is LOW, \overline{ADV} and \overline{OE} are HIGH, and \overline{LBO} is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only \overline{GW} writes are shown, the functionality of \overline{BWE} and \overline{BWx} together is the same as \overline{GW} .
4. For write cycles, \overline{ADSP} and \overline{ADSC} have different limitations.

JTAG Interface Specification (SA Version only)



NOTES:

1. Device inputs = All device inputs except TDI, TMS and \overline{TRST} .
2. Device outputs = All device outputs except TDO.
3. During power up, \overline{TRST} could be driven low or not be used since the JTAG circuit resets automatically. \overline{TRST} is an optional JTAG reset.

JTAG AC Electrical Characteristics^(1,2,3,4)

| Symbol | Parameter | | | |
|------------|-------------------------|------|------------------|-------|
| | | Min. | Max. | Units |
| t_{JCYC} | JTAG Clock Input Period | 100 | — | ns |
| t_{JCH} | JTAG Clock HIGH | 40 | — | ns |
| t_{JCL} | JTAG Clock Low | 40 | — | ns |
| t_{JR} | JTAG Clock Rise Time | — | 5 ⁽¹⁾ | ns |
| t_{JF} | JTAG Clock Fall Time | — | 5 ⁽¹⁾ | ns |
| t_{JRST} | JTAG Reset | 50 | — | ns |
| t_{JRSR} | JTAG Reset Recovery | 50 | — | ns |
| t_{JCD} | JTAG Data Output | — | 20 | ns |
| t_{JDC} | JTAG Data Output Hold | 0 | — | ns |
| t_{JS} | JTAG Setup | 25 | — | ns |
| t_{JH} | JTAG Hold | 25 | — | ns |

M4876 tbl 01

NOTES:

1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

| Register Name | Bit Size |
|----------------------------|----------|
| Instruction (IR) | 4 |
| Bypass (BYR) | 1 |
| JTAG Identification (JIDR) | 32 |
| Boundary Scan (BSR) | Note (1) |

M4876 tbl 03

NOTE:

1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

JTAG Identification Register Definitions (SA Version only)

| Instruction Field | Value | Description |
|-----------------------------------|--------------|--|
| Revision Number (31:28) | 0x2 | Reserved for version number. |
| IDT Device ID (27:12) | 0x239, 0x23B | Defines IDT part number 71V2576SA and 71V2578SA, respectively. |
| IDT JEDEC ID (11:1) | 0x33 | Allows unique identification of device vendor as IDT. |
| ID Register Indicator Bit (Bit 0) | 1 | Indicates the presence of an ID register. |

44876 tbl 02

Available JTAG Instructions

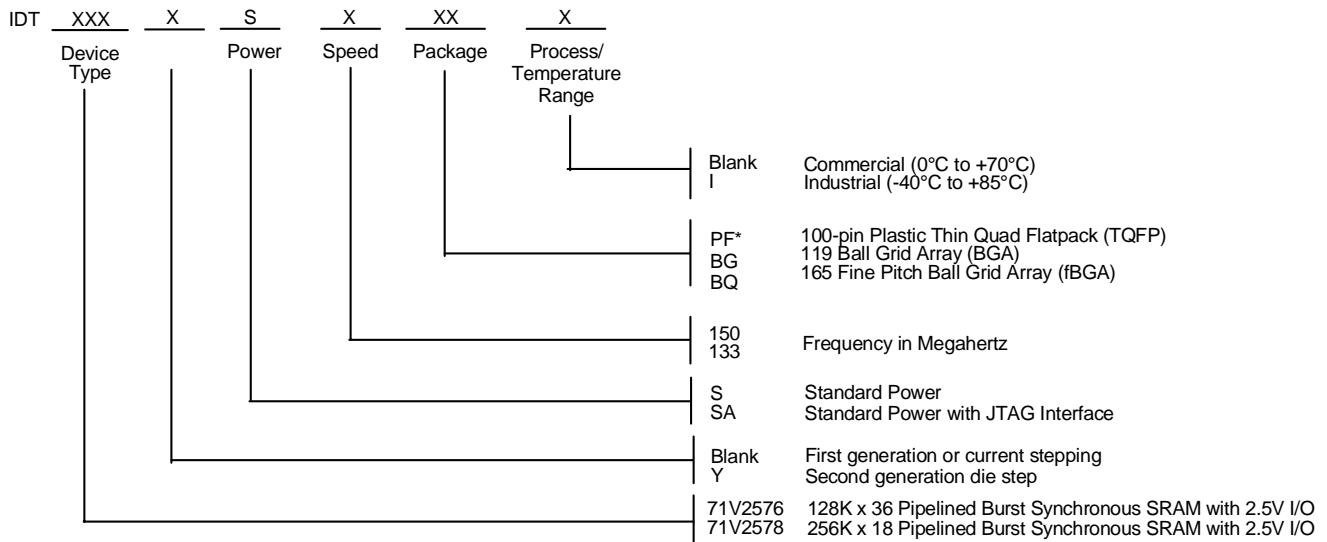
| Instruction | Description | OPCODE |
|----------------|---|--------|
| EXTEST | Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO. | 0000 |
| SAMPLE/PRELOAD | Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ and outputs ⁽¹⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI. | 0001 |
| DEVICE_ID | Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO. | 0010 |
| HIGHZ | Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state. | 0011 |
| RESERVED | Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions. | 0100 |
| RESERVED | | 0101 |
| RESERVED | | 0110 |
| RESERVED | | 0111 |
| CLAMP | Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO. | 1000 |
| RESERVED | Same as above. | 1001 |
| RESERVED | | 1010 |
| RESERVED | | 1011 |
| RESERVED | | 1100 |
| VALIDATE | Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification. | 1101 |
| RESERVED | Same as above. | 1110 |
| BYPASS | The BYPASS instruction is used to truncate the boundary scan register as a single bit in length. | 1111 |

44876 tbl 04

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.

Ordering Information



* JTAG (SA Version) is not available with 100-pin TQFP package

4876 drw 13

Package Information

100-Pin Thin Quad Plastic Flatpack (TQFP)

119 Ball Grid Array (BGA)

165 Fine Pitch Ball Grid Array (fBGA)

Information available on the IDT website

Datasheet Document History

| | | |
|----------|---------------------|---|
| 7/23/99 | | Updated to new format |
| 9/17/99 | Pg. 8 | Revised ISB1 and IZZ for speeds 100–200MHz |
| | Pg. 11 | Revised tCDC at 166MHz |
| | Pg. 18 | Added 119-Lead BGA package diagram |
| | Pg. 20 | Added Datasheet Document History |
| 12/31/99 | Pg. 1, 8, 11, 19 | Removed 166, 183, and 200MHz speed grade offerings (See IDT71V25761 and IDT71V25781) |
| | Pg. 1, 4, 8, 11, 19 | Added Industrial Temperature range offerings |
| 04/04/00 | Pg. 18 | Added 100pin TQFP Package Diagram Outline |
| | Pg. 4 | Add capacitance table for the BGA package; Add industrial temperature to table; Insert note to Absolute Max Rating and Recommended Operating Temperature tables |
| 06/01/00 | | Add new package offering 13 x 15mm 165fBGA |
| | Pg. 20 | Correct 119 BGA Package Diagram Outline |
| 07/15/00 | Pg. 7 | Add note reference to BG119 pinout |
| | Pg. 8 | Add DNU reference note to BQ165 pinout |
| | Pg. 20 | Update BG119 Package Diagram Outline Dimensions |
| 10/25/00 | | Remove Preliminary status |
| | Pg. 8 | Add reference note to pin N5 on BQ165 pinout, reserved for JTAG $\overline{\text{TRST}}$ |
| 04/22/03 | Pg. 4 | Updated 165 BGA table from information from TBA to 7 |
| 06/30/03 | Pg. 1,2,3,5-9 | Updated datasheet with JTAG information |
| | Pg. 5-8 | Removed note for NC pins (38,39(PF package); L4, U4 (BG package) H2, N7 (BQ package)) requiring NC or connection to Vss. |
| | Pg. 19,20 | Added two pages of JTAG Specification, AC Electrical, Definitions and Instructions |
| | Pg. 21-23 | Removed old package information from the datasheet |
| | Pg. 24 | Updated ordering information with JTAG and Y stepping information. Added information regarding packages available IDT website. |



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