



**THE DATASHEET OF
74HC237DB,118**





74HC237

3-to-8 line decoder, demultiplexer with address latches

Rev. 9 — 11 January 2024

Product data sheet

1. General description

The 74HC237 is a 3-to-8 line decoder, demultiplexer with latches at the three address inputs (An). The 74HC237 essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled ($\overline{LE} = \text{LOW}$), the 74HC237 acts as a 3-to-8 active LOW decoder. When the latch enable (LE) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as \overline{LE} remains HIGH. The output enable input ($\overline{E1}$ and E2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless $\overline{E1}$ is LOW and E2 is HIGH. The 74HC237 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobes (stored address) applications in bus-oriented systems.

2. Features and benefits

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active HIGH mutually exclusive outputs
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC237D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC237PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

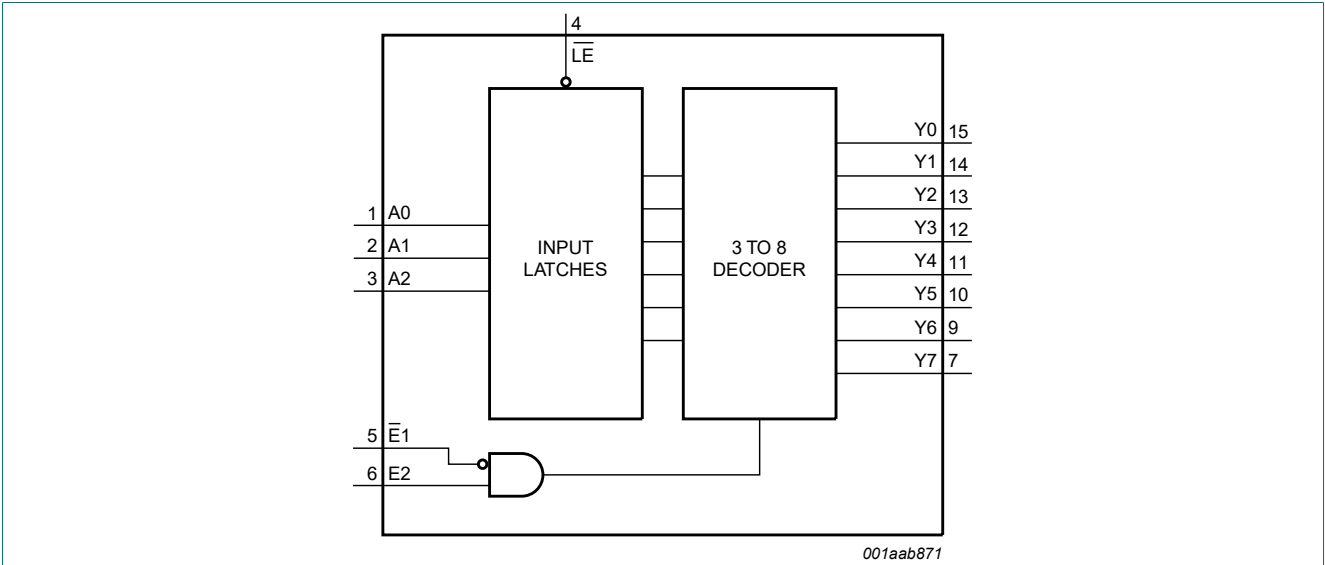


Fig. 1. Functional diagram

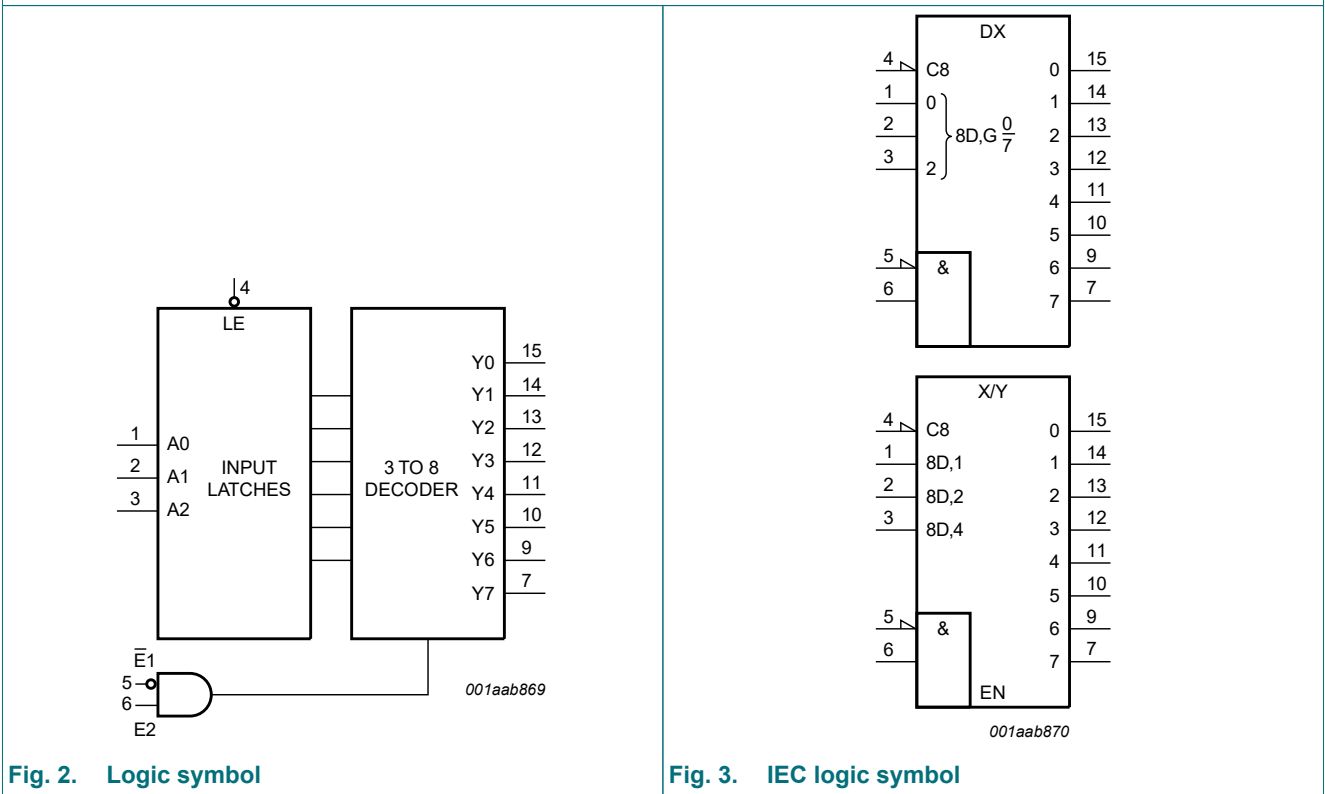


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

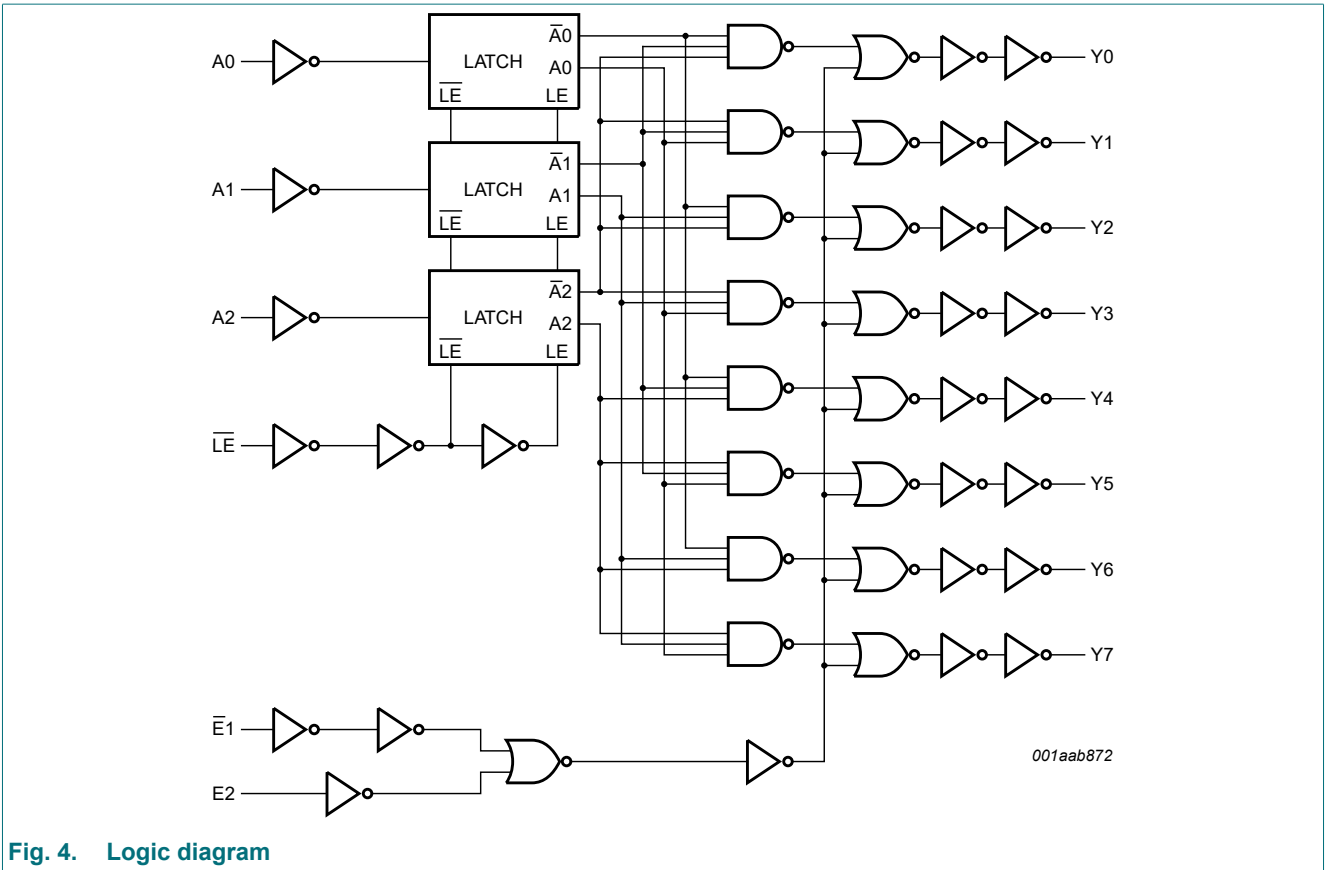
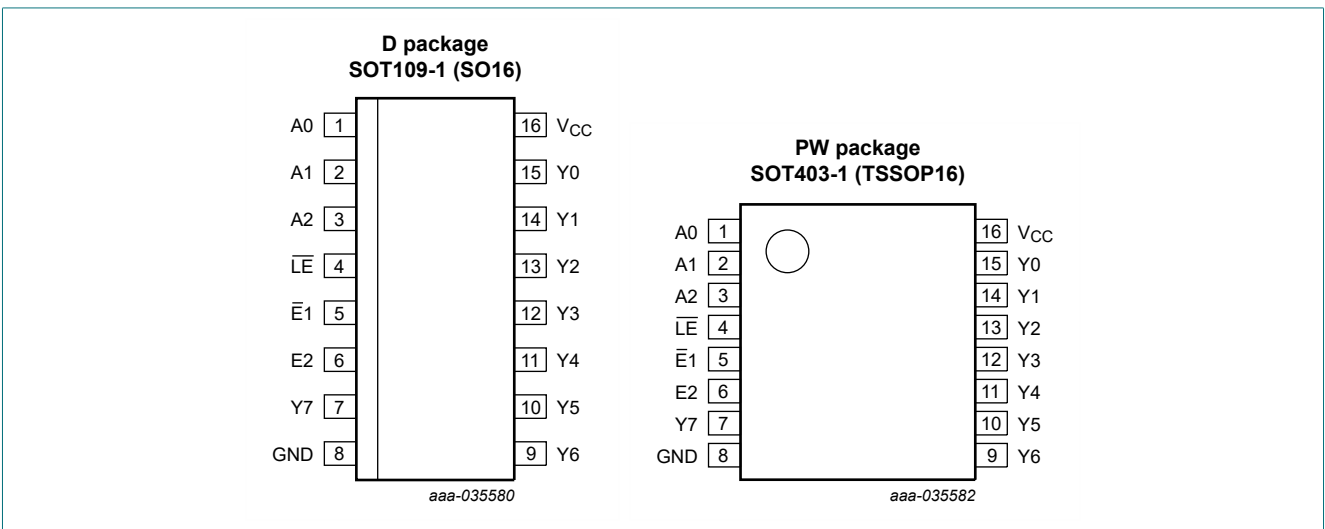


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2	1, 2, 3	data input
\overline{LE}	4	latch enable input (active LOW)
$\overline{E1}$	5	data enable input 1 (active LOW)
E2	6	data enable input 2 (active HIGH)
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	15, 14, 13, 12, 11, 10, 9, 7	output
GND	8	ground (0 V)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Enable			Input			Output							
\overline{LE}	$\overline{E1}$	E2	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	H	X	X	X	stable							
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-	-50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[1]	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20\ \mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\ \mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\ \mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
		$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see Fig. 8.

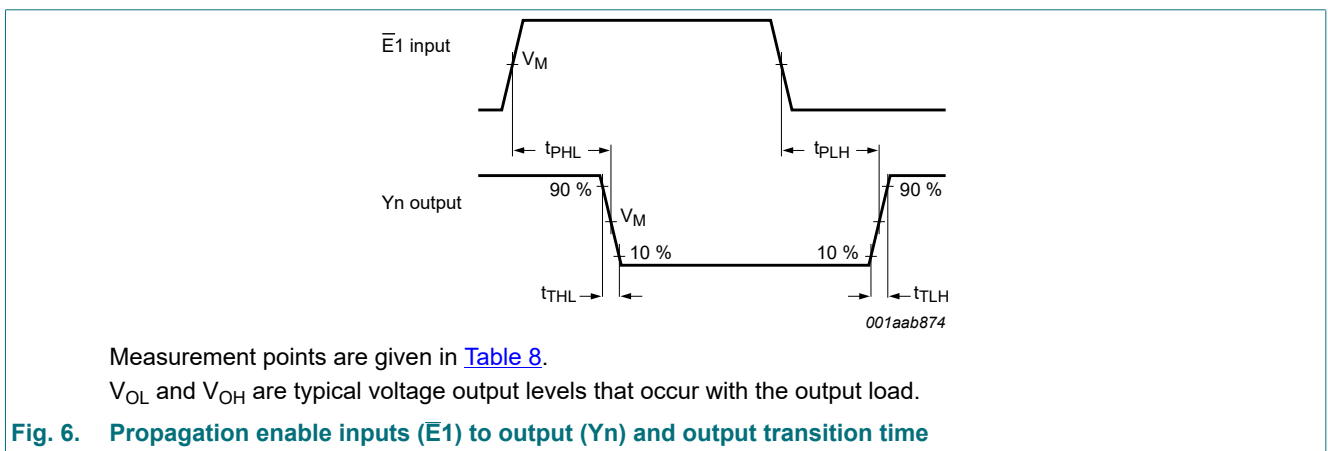
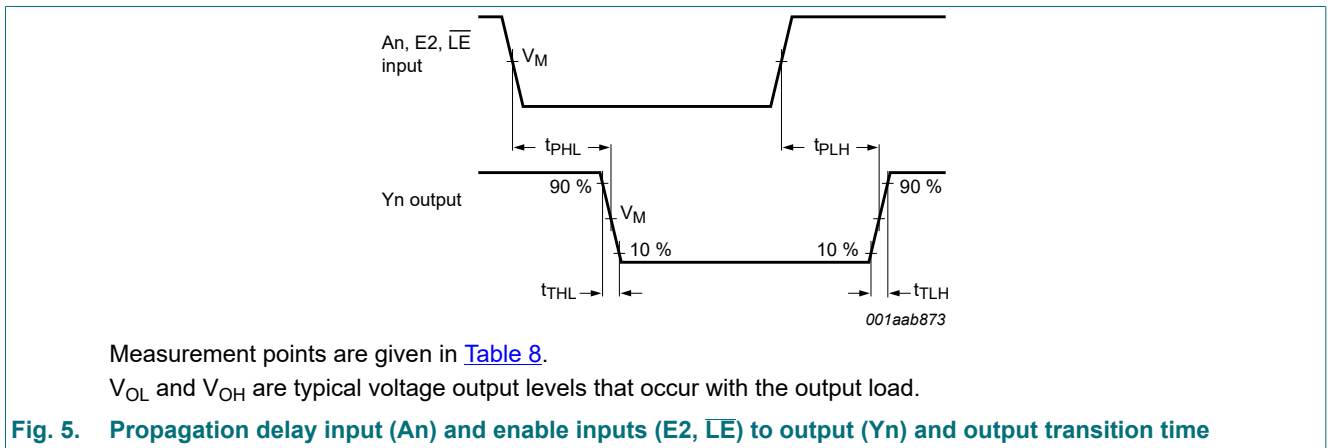
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	An to Yn; see Fig. 5 [1]								
		$V_{CC} = 2.0$ V	-	52	160	-	200	-	240	ns
		$V_{CC} = 4.5$ V	-	19	32	-	40	-	48	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	15	27	-	34	-	41	ns
		\overline{LE} to Yn; see Fig. 5 [1]								
		$V_{CC} = 2.0$ V	-	61	190	-	240	-	285	ns
		$V_{CC} = 4.5$ V	-	22	38	-	48	-	57	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	18	32	-	41	-	48	ns
		$\overline{E1}$ to Yn; see Fig. 6 [1]								
		$V_{CC} = 2.0$ V	-	47	145	-	180	-	220	ns
		$V_{CC} = 4.5$ V	-	17	29	-	36	-	44	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	14	25	-	31	-	38	ns
		t_t	transition time	Yn; see Fig. 5 and Fig. 6 [2]						
$V_{CC} = 2.0$ V	-			19	75	-	95	-	110	ns
$V_{CC} = 4.5$ V	-			7	15	-	19	-	22	ns
$V_{CC} = 6.0$ V	-			6	13	-	16	-	19	ns
t_w	pulse width	\overline{LE} HIGH; see Fig. 7								
		$V_{CC} = 2.0$ V	50	11	-	65	-	75	-	ns
		$V_{CC} = 4.5$ V	10	4	-	13	-	15	-	ns
		$V_{CC} = 6.0$ V	9	3	-	11	-	13	-	ns
t_{su}	set-up time	An to \overline{LE} ; see Fig. 7								
		$V_{CC} = 2.0$ V	50	6	-	65	-	75	-	ns
		$V_{CC} = 4.5$ V	10	2	-	13	-	15	-	ns
		$V_{CC} = 6.0$ V	9	2	-	11	-	13	-	ns

3-to-8 line decoder, demultiplexer with address latches

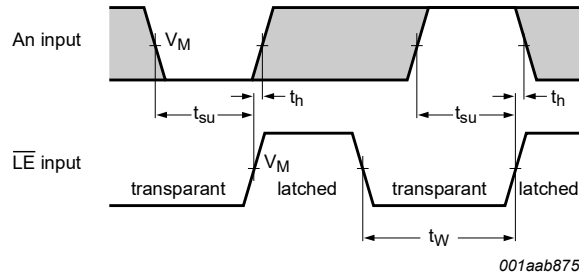
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _h	hold time	An to \overline{LE} ; see Fig. 7					-			
		V _{CC} = 2.0 V	30	3	-	40	-	45	-	ns
		V _{CC} = 4.5 V	6	1	-	8	-	9	-	ns
		V _{CC} = 6.0 V	5	1	-	7	-	8	-	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [3]	-	60	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] t_i is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



3-to-8 line decoder, demultiplexer with address latches



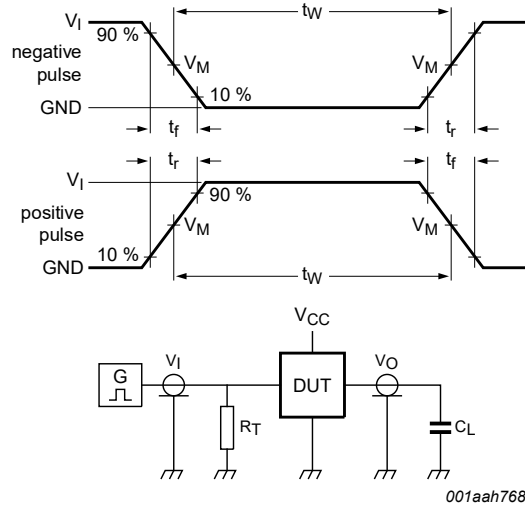
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. The data input (An) to latch enable input (\overline{LE}) set-up times, latch enable input (\overline{LE}) to data input (An) hold times and latch enable input (\overline{LE}) pulse width

Table 8. Measurement points

Input	Output
V_M	V_M
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Input		Load	Test
V_I	t_r, t_f	C_L	t_{PLH}, t_{PHL}
V_{CC}	6.0 ns	15 pF, 50 pF	

11. Application information

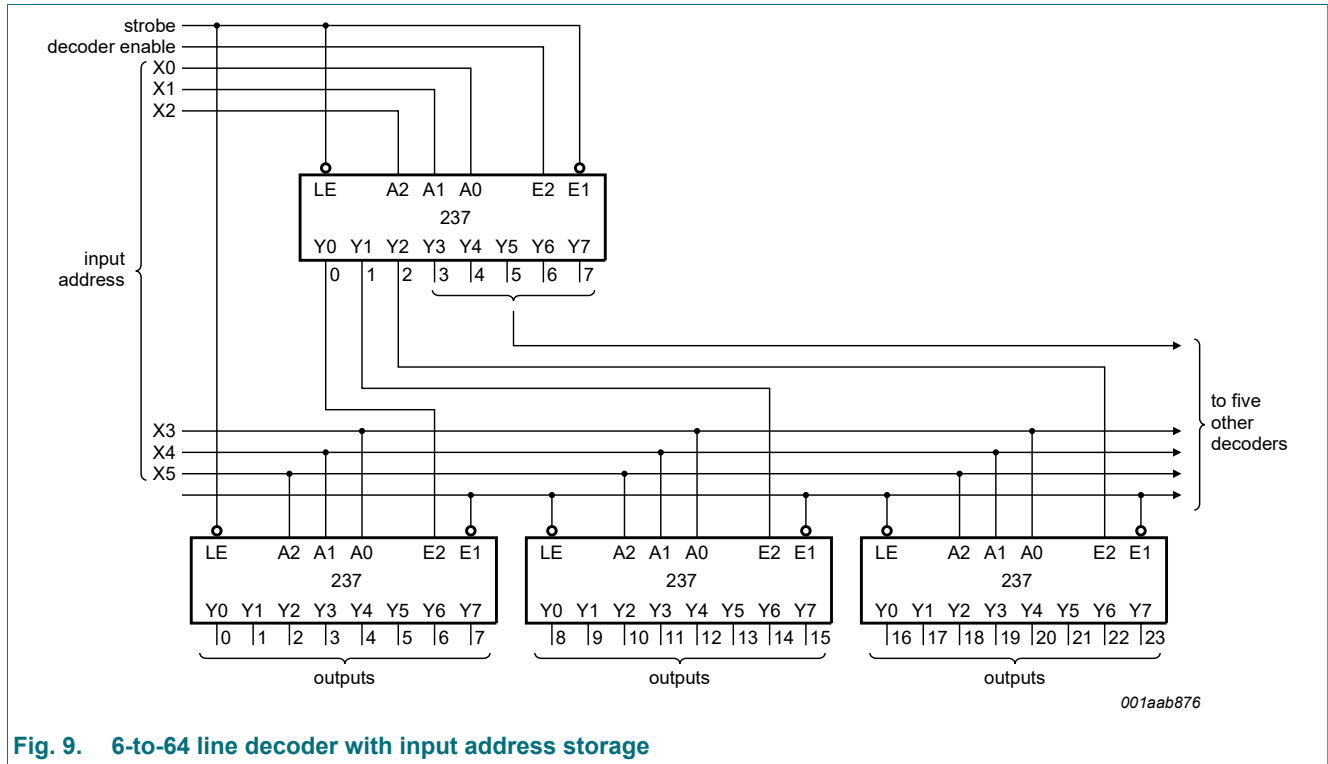


Fig. 9. 6-to-64 line decoder with input address storage

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

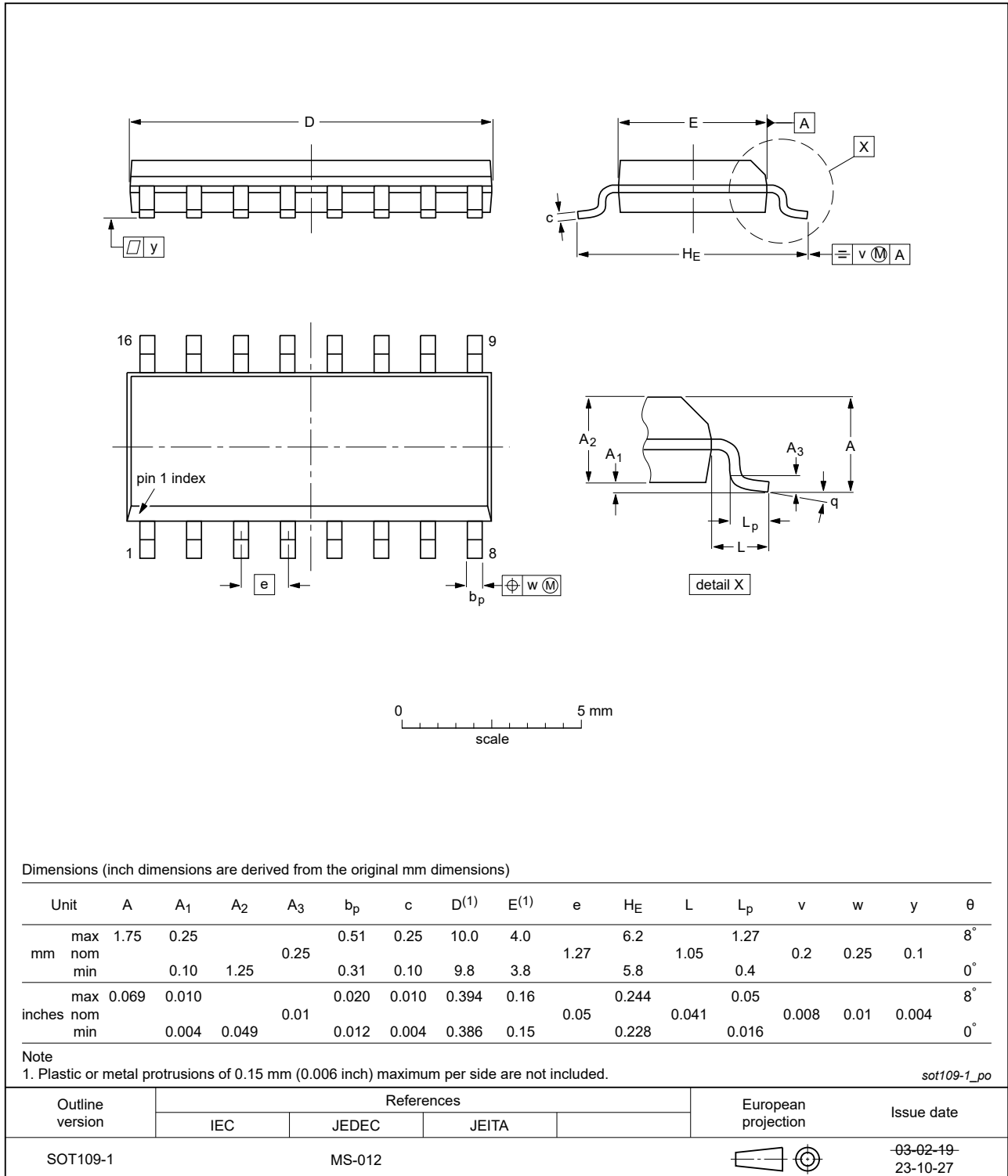


Fig. 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Fig. 11. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC237 v.9	20240111	Product data sheet	-	74HC237 v.8
Modifications:	<ul style="list-style-type: none"> Type number 74HC237DB (SOT338-1/SSOP16) removed. Section 2: ESD specification updated according to the latest JEDEC standard. Fig. 10, Fig. 11: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153 			
74HC237 v.8	20211026	Product data sheet	-	74HC237 v.7
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74HC237PW (SOT403-1/TSSOP16) added. Section 1 and Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. 			
74HC237 v.7	20160129	Product data sheet	-	74HC237 v.6
Modifications:	<ul style="list-style-type: none"> Type number 74HC237N removed. 			
74HC237 v.6	20120823	Product data sheet	-	74HC237 v.5
Modifications:	<ul style="list-style-type: none"> Measurement points added to Fig. 5 and Fig. 6 (errata). 			
74HC237 v.5	20111209	Product data sheet	-	74HC237 v.4
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74HC237 v.4	20110110	Product data sheet	-	74HC237 v.3
74HC237 v.3	20041112	Product data sheet	-	74HC_HCT237_CNV v.2
74HC_HCT237_CNV v.2	19970828	Product specification	-	74HC_HCT237 v.1
74HC_HCT237 v.1	19901201	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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