THE DATASHEET OF

CBT3244ADS,112

CBT3244A

Octal bus switch with quad output enables

Rev. 3 — 8 September 2017 Product data sheet

1 General description

The CBT3244A provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3244A device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is LOW, the switch is on and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is HIGH, the switch is open and high-impedance state exists between the two ports.

The CBT3244A is characterized for operation from -40 °C to +85 °C.

2 Features and benefits

- Standard '244-type pinout
- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
  - HBM JESD22-A114 exceeds 2000 V
  - MM JESD22-A115 exceeds 200 V
  - CDM JESD22-C101 exceeds 1000 V

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBT3244ABQ	-40 °C to + 85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
CBT3244APW	-40 °C to + 85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
CBT3244ADB	-40 °C to + 85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
CBT3244AD	-40 °C to + 85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4 Marking

Table 2. Marking codes

Type number	Marking code
CBT3244ABQ	CT3244A
CBT3244APW	CT3244A
CBT3244ADB	CT3244A
CBT3244AD	CBT3244AD

5 Functional diagram

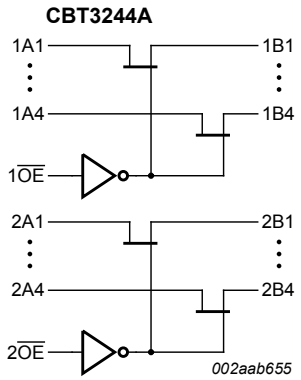


Figure 1. Logic diagram

6 Pinning information

6.1 Pinning

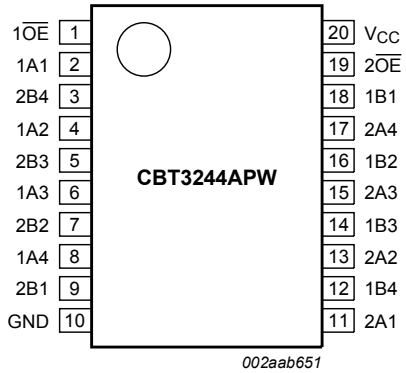


Figure 2. Pin configuration for TSSOP20

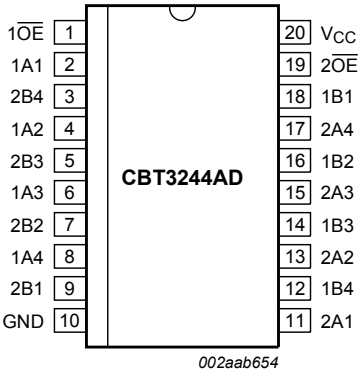


Figure 3. Pin configuration for SO20

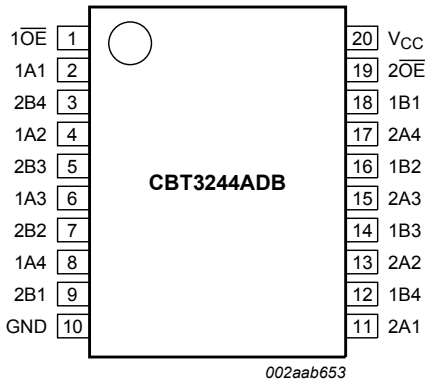
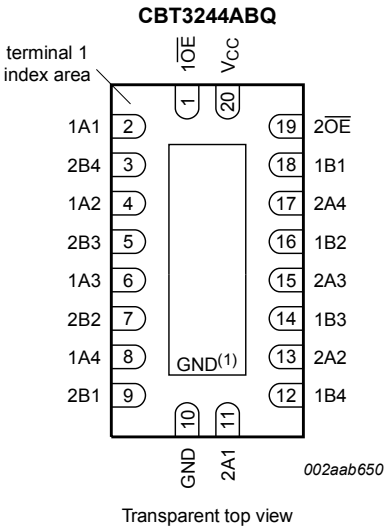


Figure 4. Pin configuration for SSOP20



Transparent top view

(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

Figure 5. Pin configuration for DHVQFN20

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 19	output enable (active LOW)
1A1, 1A2, 1A3, 1A4, 2A1, 2A2, 2A3, 2A4	2, 4, 6, 8, 11, 13, 15, 17	inputs
1B1, 1B2, 1B3, 1B4, 2B1, 2B2, 2B3, 2B4	18, 16, 14, 12, 9, 7, 5, 3	outputs
GND	10	ground (0 V)
V_{CC}	20	positive supply voltage

7 Functional description

Table 4. Function selection [1]

Inputs		Outputs	
$1\overline{OE}$	$2\overline{OE}$	1An, 1Bn	2An, 2Bn
L	L	1An = 1Bn	2An = 2Bn
L	H	1An = 1Bn	Z
H	L	Z	2An = 2Bn
H	H	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF state

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[2]	-1.2	+7.0	V
V_O	output voltage	output in OFF or HIGH state [2]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-18	mA
I_{OK}	output clamping current	$V_O < 0$ V	-	-50	mA
I_O	output current	output in LOW state	-	128	mA
T_{stg}	storage temperature		-65	+150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9 Recommended operating conditions

Table 6. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
T_{amb}	ambient temperature	operating in free-air	-40	-	+85	°C

10 Static characteristics

Table 7. Static characteristics

T_{amb} = -40 °C to +85 °C. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = -18 mA	-	-	-1.2	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	1	3	µA
ΔI_{CC}	additional supply current	per input; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND [2]	-	-	2.5	mA
C_i	input capacitance	control pins; V_I = 3 V or 0 V; $n\overline{OE}$ = V_{CC}	-	3	-	pF
$C_{I/O}$	input/output capacitance	$n\overline{OE}$ = V_{CC} = 5.0 V	-	3	-	pF
R_{on}	ON-state resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA [3]	-	4	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	-	4	7	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA	-	8	15	Ω

[1] All typical values are measured at V_{CC} = 5 V; T_{amb} = 25 °C.
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[3] Measured by the voltage level between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

11 Dynamic characteristics

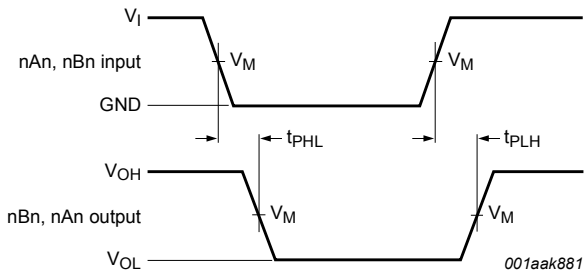
Table 8. Dynamic characteristics

T_{amb} = -40 °C to +85 °C; Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{pd}	propagation delay	nAn to nBn, or nBn to nAn; V_{CC} = 5.0 V ± 0.5 V; see Figure 6 [1] [2]	-	-	0.25	ns
t_{en}	enable time	$n\overline{OE}$ to nAn or nBn; V_{CC} = 5.0 V ± 0.5 V; see Figure 7 [3]	1.0	-	5.6	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn or nBn; V_{CC} = 5.0 V ± 0.5 V; see Figure 7 [4]	1.0	-	6.0	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{en} is the same as t_{PZH} and t_{PZL}.
[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}

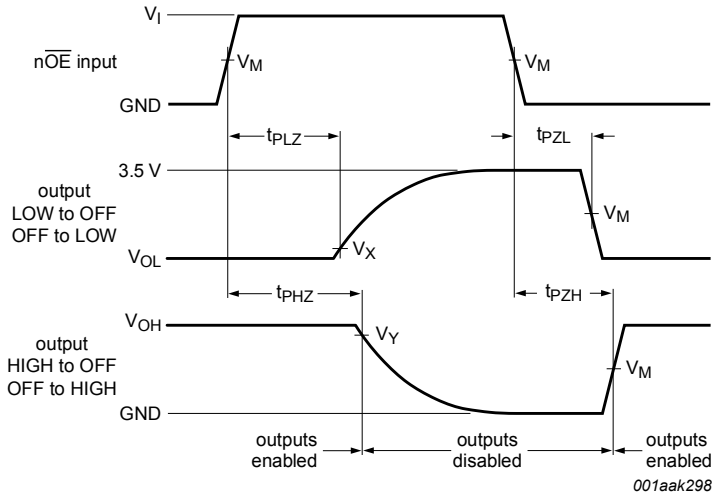
11.1 Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. The data input (A) to output (nYn) propagation delay times



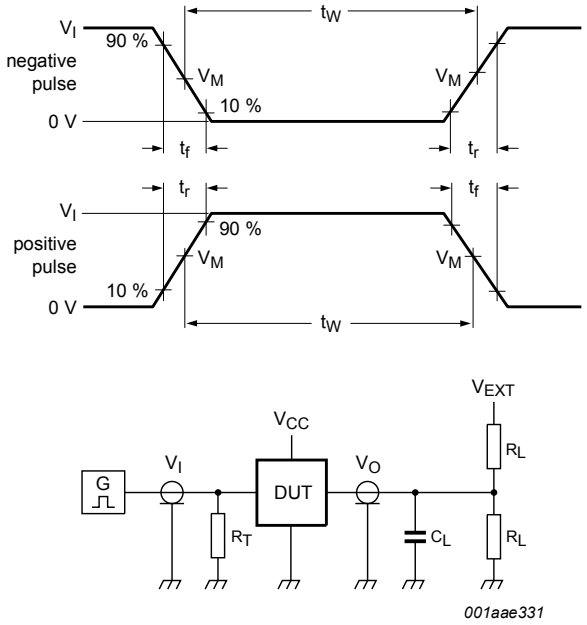
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Enable and disable times

Table 9. Measurement points

Input		Output		
V_I	V_M	V_M	V_X	V_Y
3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω

The outputs are measured one at a time with one transition per measurement.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

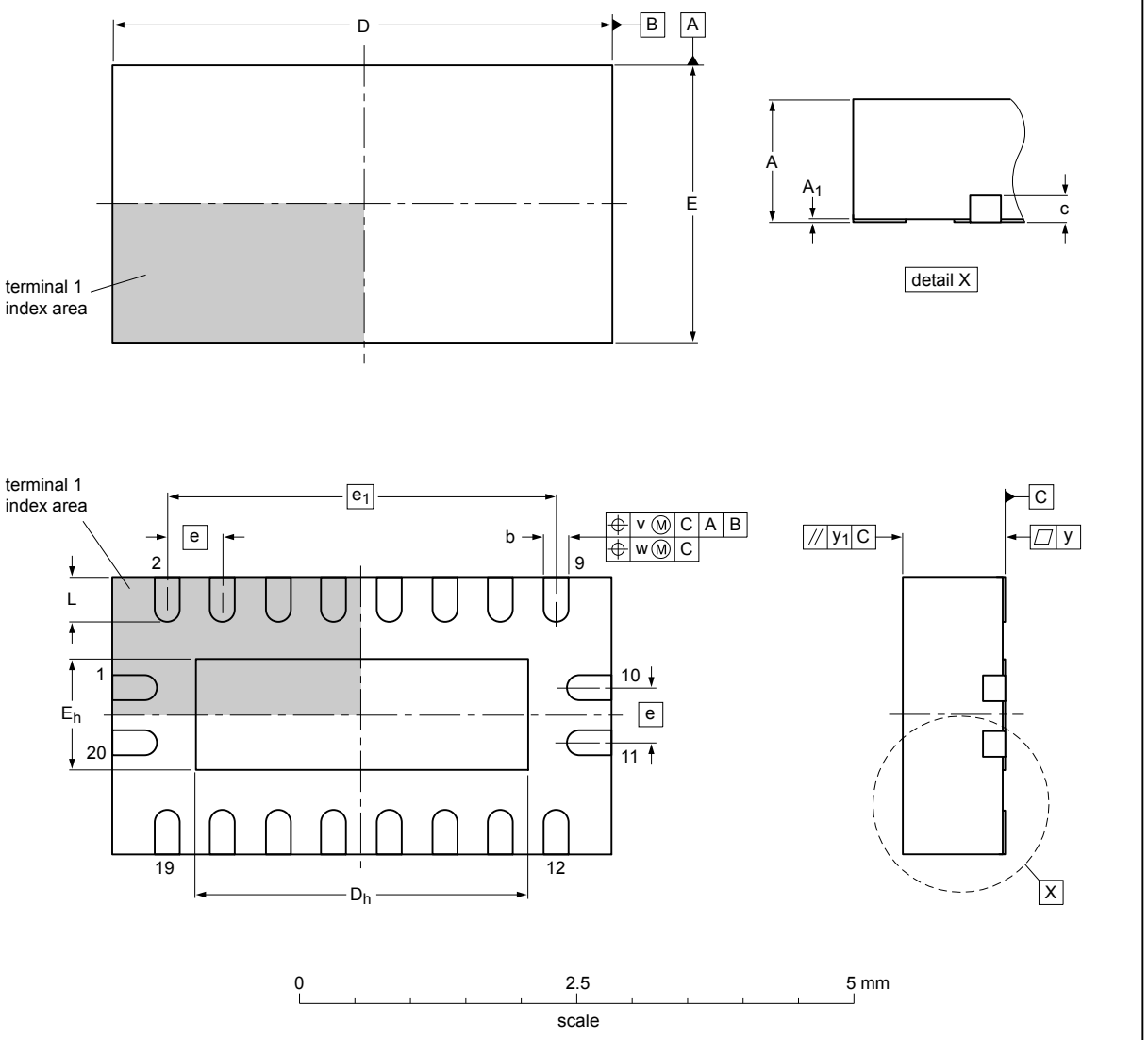
Figure 8. Test circuit for measuring switching times

Table 10. Test data

Input		Load		V_{EXT}		
V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	open	7 V

12 Package outline

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

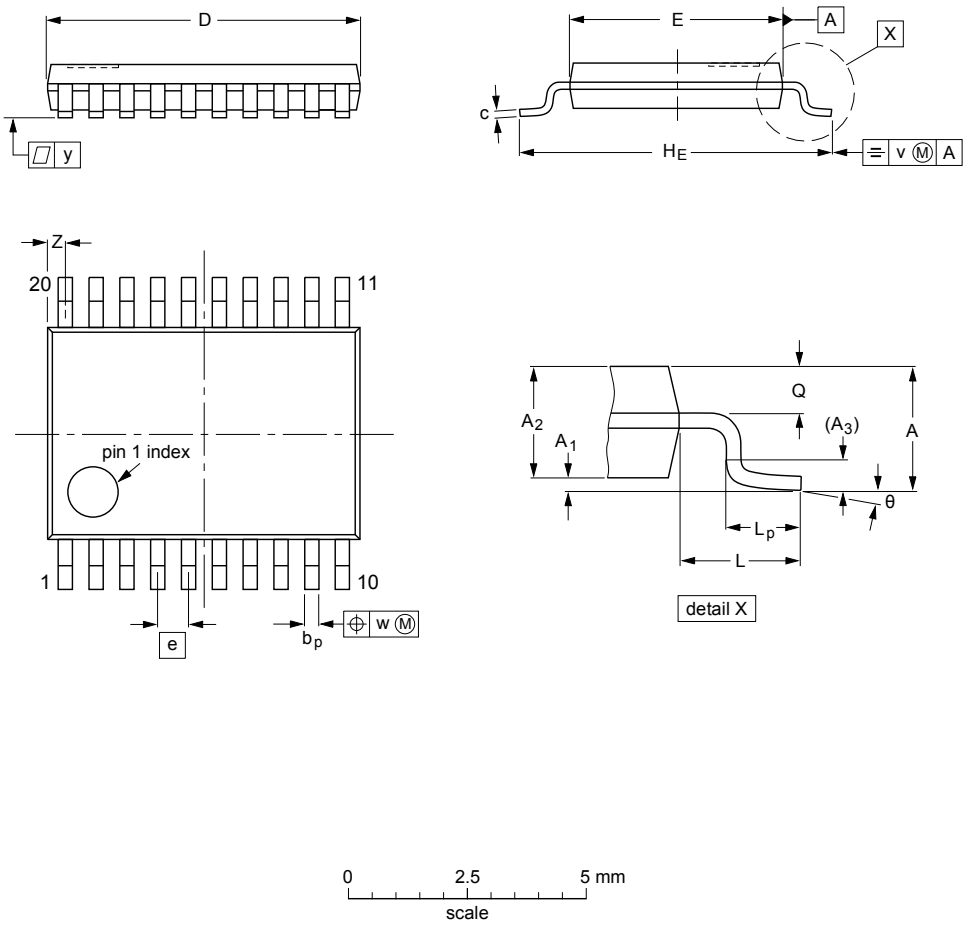
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Figure 9. Package outline SOT764-1 (DHVQFN20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

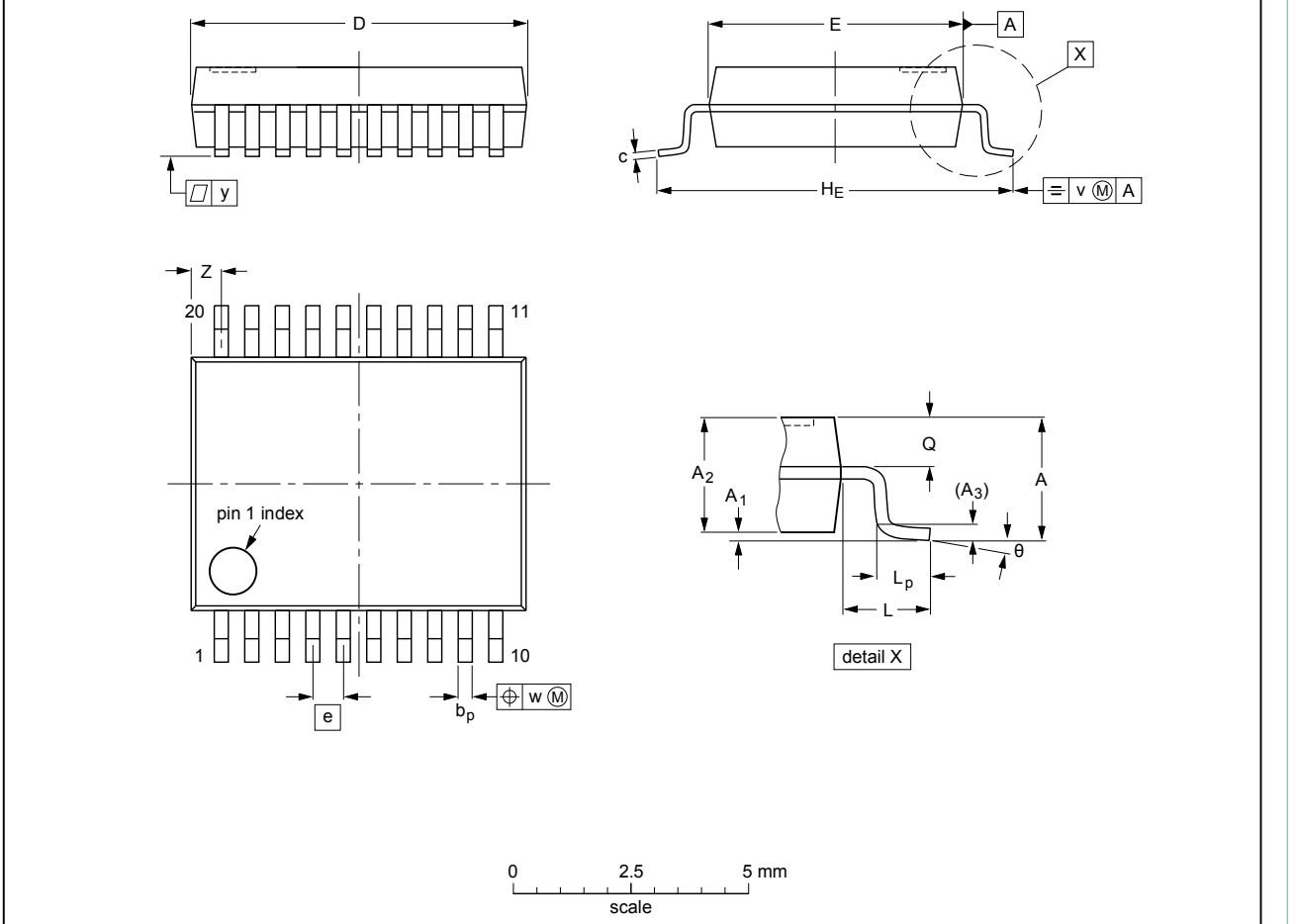
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Figure 10. Package outline SOT360-1 (TSSOP20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

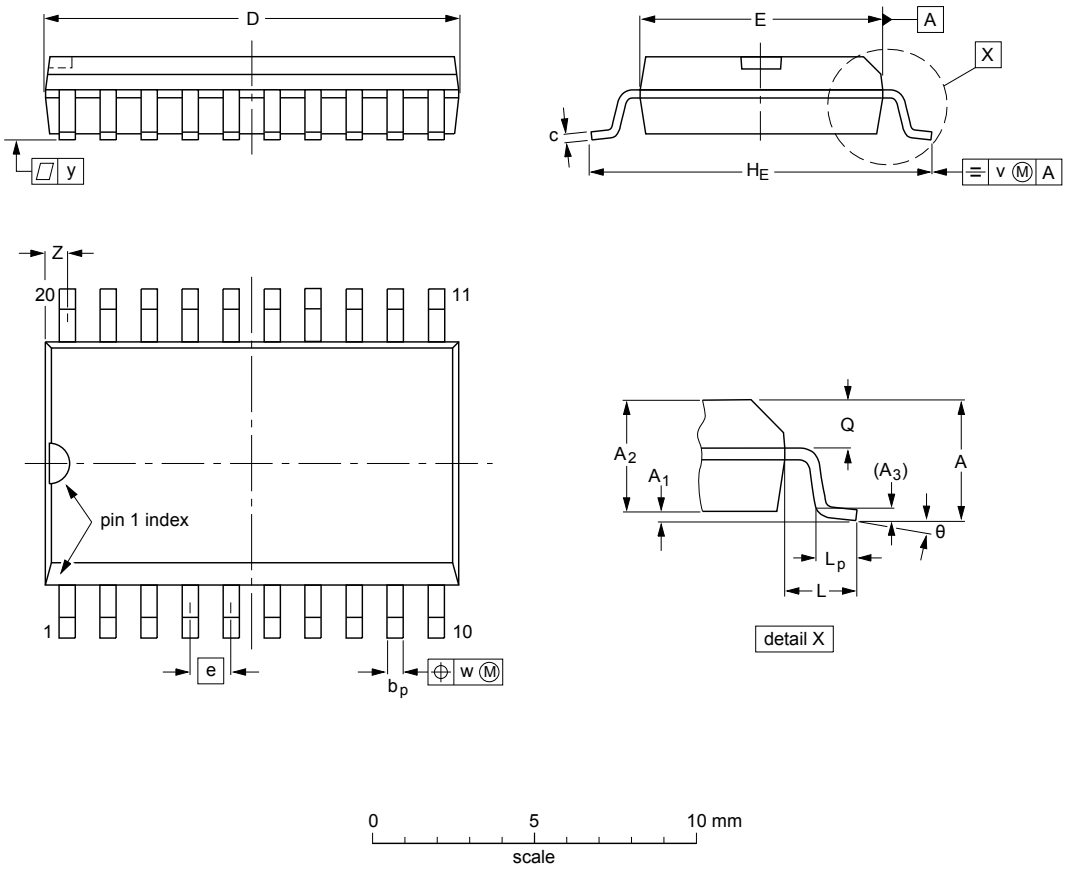
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Figure 11. Package outline SOT339-1 (SSOP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Figure 12. Package outline SOT163-1 (SO20)

13 Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3244A v.3	20170908	Product data sheet	-	CBT3244A v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number CBT3244ADS removed.			
CBT3244A v.2	20050915	Product data sheet	-	CBT3244A v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • added DHVQFN20 package option. • Section 2, 5th bullet: changed from ‘exceeds 1000 V HBM ...’ to ‘exceeds 2000 V HBM ...’ • added Section 13 Abbreviations			
CBT3244A v.1	20040526	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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