



**THE DATASHEET OF  
74HC4066DB,118**



# 74HC4066; 74HCT4066

## Quad single-pole single-throw analog switch

Rev. 12 — 1 May 2025

Product data sheet

### 1. General description

The 74HC4066; 74HCT4066 is a quad single pole, single throw analog switch. Each switch features two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### 2. Features and benefits

- Input levels nE inputs:
  - For 74HC4066: CMOS level
  - For 74HCT4066: TTL level
- Low ON resistance:
  - 50  $\Omega$  (typical) at  $V_{CC} = 4.5$  V
  - 45  $\Omega$  (typical) at  $V_{CC} = 6.0$  V
  - 35  $\Omega$  (typical) at  $V_{CC} = 9.0$  V
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74HC4066D</a>	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>
<a href="#">74HCT4066D</a>				
<a href="#">74HC4066PW</a>	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>
<a href="#">74HCT4066PW</a>				
<a href="#">74HC4066BQ</a>	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	<a href="#">SOT762-1</a>
<a href="#">74HCT4066BQ</a>				
<a href="#">74HC4066BZ</a>	-40 °C to +125 °C	DHXQFN14	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm × 2 mm × 0.48 mm	<a href="#">SOT8014-1</a>
<a href="#">74HCT4066BZ</a>				

### 4. Functional diagram

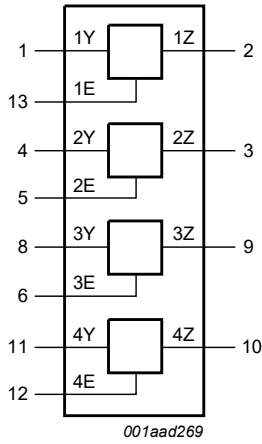


Fig. 1. Logic symbol

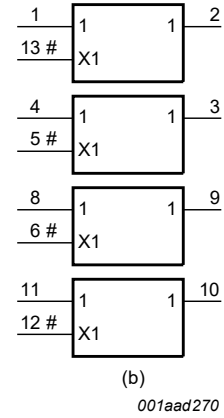
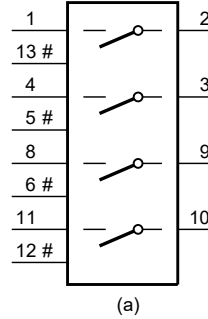


Fig. 2. IEC logic symbol

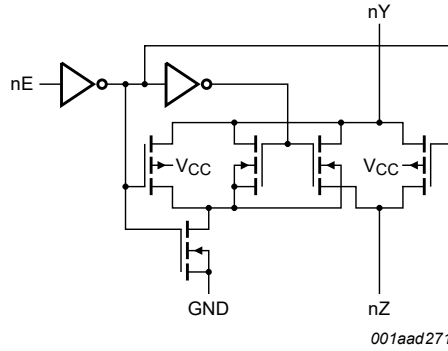


Fig. 3. Schematic diagram (one switch)

### 5. Pinning information

#### 5.1. Pinning

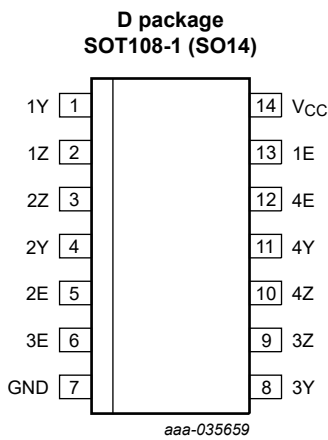


Fig. 4. Pin configuration SOT108-1 (SO14)

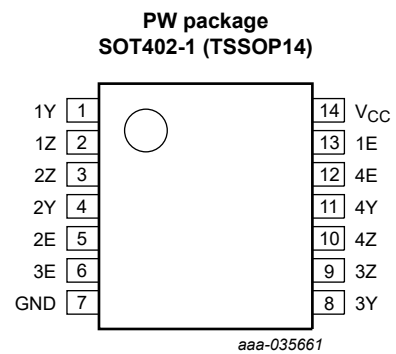
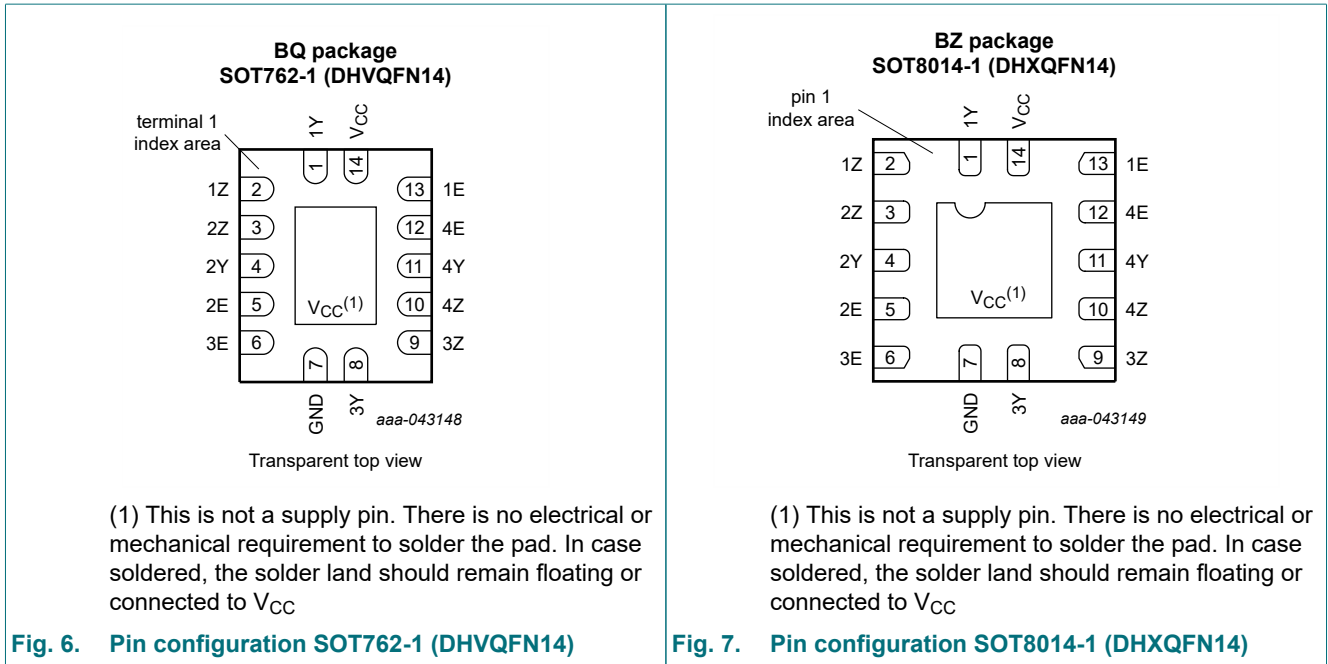


Fig. 5. Pin configuration and SOT402-1 (TSSOP14)



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Z, 2Z, 3Z, 4Z	2, 3, 9, 10	independent input or output
1Y, 2Y, 3Y, 4Y	1, 4, 8, 11	independent input or output
GND	7	ground (0 V)
1E, 2E, 3E, 4E	13, 5, 6, 12	enable input (active HIGH)
VCC	14	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nE	Switch
L	OFF
H	ON

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+11.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{SK}$	switch clamping current	$V_{SW} < -0.5\text{ V}$ or $V_{SW} > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{SW}$	switch current	$V_{SW} = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-	-50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		SOT108-1 (SO14) [2] SOT402-1 (TSSOP14) SOT762-1 (DHSVQFN14)	-	500	mW
		SOT8014-1 (DHSVQFN14) [3]	-	250	mW
$P$	power dissipation	per switch	-	100	mW

- [1] To avoid drawing  $V_{CC}$  current out of terminal Z, when switch current flows in terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{CC}$  current will flow out of terminals Yn. In this case there is no limit for the voltage drop across the switch, but the voltages at Yn and Z may not exceed  $V_{CC}$  or GND.
- [2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.  
For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.  
For SOT762-1 (DHSVQFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.
- [3] For SOT8014-1 (DHSVQFN14) package:  $P_{tot}$  derates linearly with 8.7 mW/K above 121 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	74HC4066			74HCT4066			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
$V_I$	input voltage		GND	-	$V_{CC}$	GND	-	$V_{CC}$	V
$V_{SW}$	switch voltage		GND	-	$V_{CC}$	GND	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
		$V_{CC} = 10.0\text{ V}$	-	-	35	-	-	-	ns/V

## 9. Static characteristics

**Table 6.  $R_{ON}$  resistance per switch for types 74HC4066 and 74HCT4066**

$V_I = V_{IH}$  or  $V_{IL}$ ; for test circuit see Fig. 8.

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

For 74HC4066:  $V_{CC} - GND = 2.0\text{ V}, 4.5\text{ V}, 6.0\text{ V}$  and  $9.0\text{ V}$ .

For 74HCT4066:  $V_{CC} - GND = 4.5\text{ V}$ .

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to GND						
		$V_{CC} = 2.0\text{ V}; I_{SW} = 100\ \mu\text{A}$ [2]	-	-	-	-	-	$\Omega$
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	54	-	118	142	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	42	-	105	126	$\Omega$
		$V_{CC} = 9.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	32	-	88	105	$\Omega$
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = GND$						
		$V_{CC} = 2.0\text{ V}; I_{SW} = 100\ \mu\text{A}$ [2]	-	80	-	-	-	$\Omega$
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	35	-	95	115	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	27	-	82	100	$\Omega$
		$V_{CC} = 9.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	20	-	70	85	$\Omega$
		$V_{is} = V_{CC}$						
		$V_{CC} = 2.0\text{ V}; I_{SW} = 100\ \mu\text{A}$ [2]	-	100	-	-	-	$\Omega$
		$V_{CC} = 4.5\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	42	-	106	128	$\Omega$
		$V_{CC} = 6.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	35	-	94	113	$\Omega$
		$V_{CC} = 9.0\text{ V}; I_{SW} = 1000\ \mu\text{A}$	-	20	-	78	95	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to GND						
		$V_{CC} = 2.0\text{ V}$ [2]	-	-	-	-	-	$\Omega$
		$V_{CC} = 4.5\text{ V}$	-	5	-	-	-	$\Omega$
		$V_{CC} = 6.0\text{ V}$	-	4	-	-	-	$\Omega$
		$V_{CC} = 9.0\text{ V}$	-	3	-	-	-	$\Omega$

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$ .

[2] At supply voltages ( $V_{CC} - GND$ ) approaching 2 V, the analog switch ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

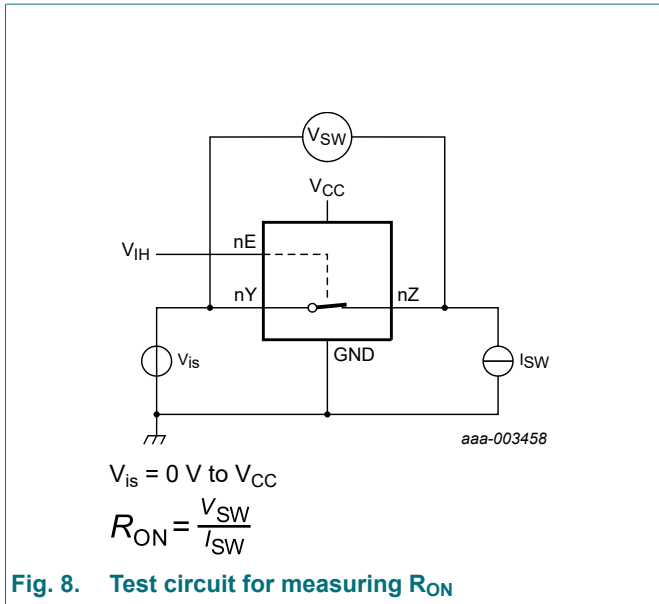


Fig. 8. Test circuit for measuring  $R_{ON}$

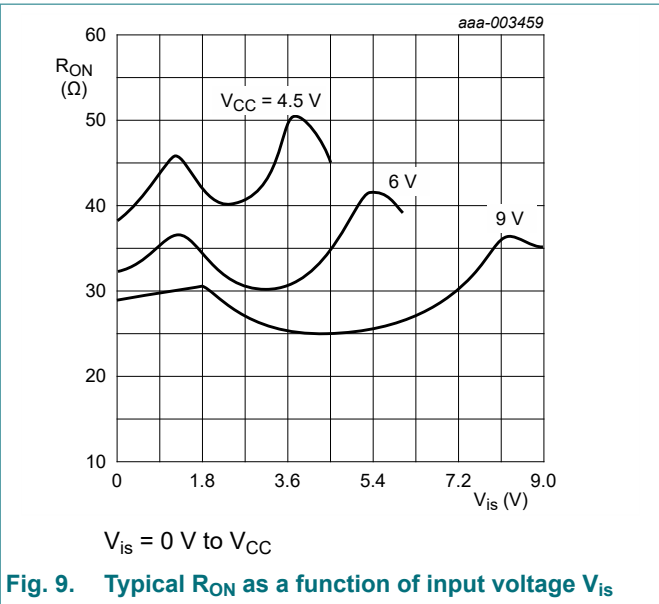


Fig. 9. Typical  $R_{ON}$  as a function of input voltage  $V_{is}$

Table 7. Static characteristics 74HC4066

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
		$V_{CC} = 9.0\text{ V}$	6.3	4.7	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.80	V
		$V_{CC} = 9.0\text{ V}$	-	4.3	2.70	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND				
		$V_{CC} = 6.0\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
		$V_{CC} = 10.0\text{ V}$	-	-	$\pm 2.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 10.0\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see Fig. 10				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 10.0\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see Fig. 11	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} = \text{GND}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or GND				
		$V_{CC} = 6.0\text{ V}$	-	-	20.0	$\mu\text{A}$
		$V_{CC} = 10.0\text{ V}$	-	-	40.0	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF
$C_{SW}$	switch capacitance		-	8	-	pF

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
		V <sub>CC</sub> = 9.0 V	6.3	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.50	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.80	V
		V <sub>CC</sub> = 9.0 V	-	-	2.70	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND				
		V <sub>CC</sub> = 6.0 V	-	-	±1.0	µA
		V <sub>CC</sub> = 10.0 V	-	-	±2.0	µA
I <sub>S(OFF)</sub>	OFF-state leakage current	V <sub>CC</sub> = 10.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;  V <sub>SW</sub>   = V <sub>CC</sub> - GND; see Fig. 10				
		per channel	-	-	±1.0	µA
I <sub>S(ON)</sub>	ON-state leakage current	V <sub>CC</sub> = 10.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;  V <sub>SW</sub>   = V <sub>CC</sub> - GND; see Fig. 11	-	-	±1.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>is</sub> = GND or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or GND				
		V <sub>CC</sub> = 6.0 V	-	-	40	µA
		V <sub>CC</sub> = 10.0 V	-	-	80	µA

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

**Table 8. Static characteristics 74HCT4066**

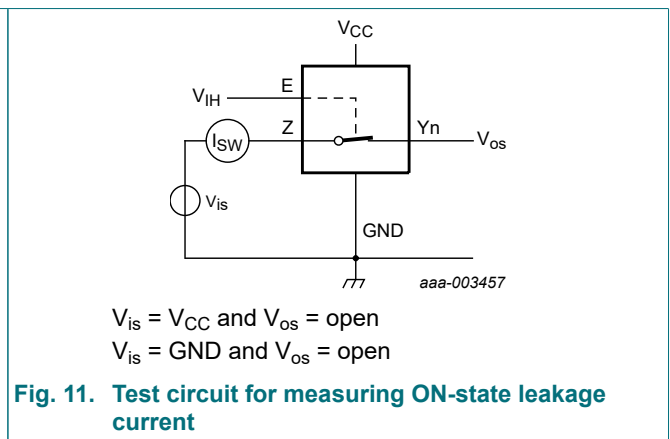
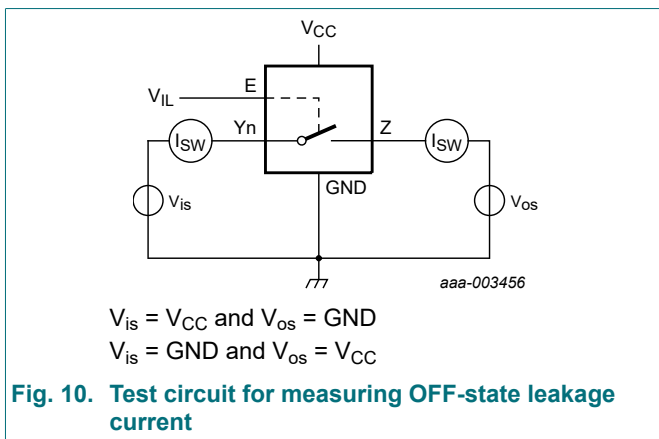
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see Fig. 10				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see Fig. 11	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} = \text{GND}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20.0	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	100	450	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF
$C_{SW}$	switch capacitance		-	8	-	pF
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see Fig. 10				
		per channel	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $ V_{SW}  = V_{CC} - \text{GND}$ ; see Fig. 11	-	-	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $V_{is} = \text{GND}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	490	$\mu\text{A}$

[1] Typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .



## 10. Dynamic characteristics

**Table 9. Dynamic characteristics 74HC4066**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$  unless specified otherwise; for test circuit see Fig. 14.

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	nY to nZ or nZ to nY; $R_L = \infty\ \Omega$ ; see Fig. 12 [2]						
		$V_{CC} = 2.0\text{ V}$	-	8	75	-	90	ns
		$V_{CC} = 4.5\text{ V}$	-	3	15	-	18	ns
		$V_{CC} = 6.0\text{ V}$	-	2	13	-	15	ns
		$V_{CC} = 9.0\text{ V}$	-	2	10	-	12	ns
$t_{off}$	turn-off time	nE to nY or nZ; see Fig. 13 [3]						
		$V_{CC} = 2.0\text{ V}$	-	44	190	-	225	ns
		$V_{CC} = 4.5\text{ V}$	-	16	38	-	45	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	13	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	13	33	-	38	ns
		$V_{CC} = 9.0\text{ V}$	-	16	26	-	30	ns
$t_{on}$	turn-on time	nE to nY or nZ; see Fig. 13 [4]						
		$V_{CC} = 2.0\text{ V}$	-	36	125	-	150	ns
		$V_{CC} = 4.5\text{ V}$	-	13	25	-	30	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	11	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	10	21	-	26	ns
		$V_{CC} = 9.0\text{ V}$	-	8	16	-	20	ns
$C_{PD}$	power dissipation capacitance	per switch; $V_I = GND$ to $V_{CC}$ [5]	-	11	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$ .

[2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[3]  $t_{off}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[4]  $t_{on}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\} \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$C_{sw}$  = switch capacitance in pF;

$V_{CC}$  = supply voltage in V.

**Table 10. Dynamic characteristics 74HCT4066**

$GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$  unless specified otherwise; for test circuit see Fig. 14.

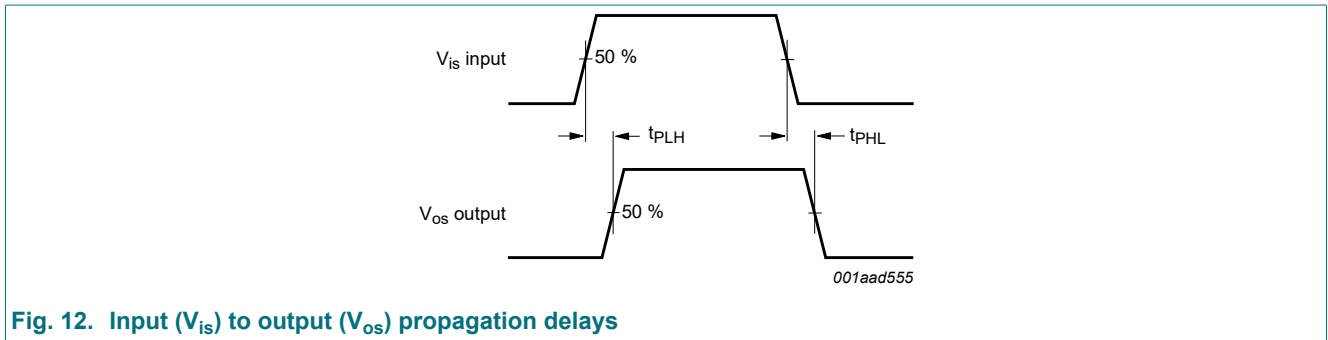
$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	nY to nZ or nZ to nY; $R_L = \infty\ \Omega$ ; see Fig. 12 [2]						
		$V_{CC} = 4.5\text{ V}$	-	3	15	-	18	ns
$t_{off}$	turn-off time	nE to nY or nZ; see Fig. 13 [3]						
		$V_{CC} = 4.5\text{ V}$	-	20	44	-	53	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	16	-	-	-	ns
$t_{on}$	turn-on time	nE to nY or nZ; see Fig. 13 [4]						
		$V_{CC} = 4.5\text{ V}$	-	12	30	-	36	ns
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	12	-	-	-	ns
$C_{PD}$	power dissipation capacitance	per switch; $V_I = GND$ to $(V_{CC} - 1.5\text{ V})$ [5]	-	12	-	-	-	pF

- [1] Typical values are measured at  $T_{amb} = 25\text{ °C}$ .
- [2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .
- [3]  $t_{off}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .
- [4]  $t_{on}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .
- [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $\sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$  = sum of outputs;  
 $C_L$  = output load capacitance in pF;  
 $C_{sw}$  = switch capacitance in pF;  
 $V_{CC}$  = supply voltage in V.

**10.1. Waveforms and test circuit**



**Fig. 12. Input ( $V_{is}$ ) to output ( $V_{os}$ ) propagation delays**

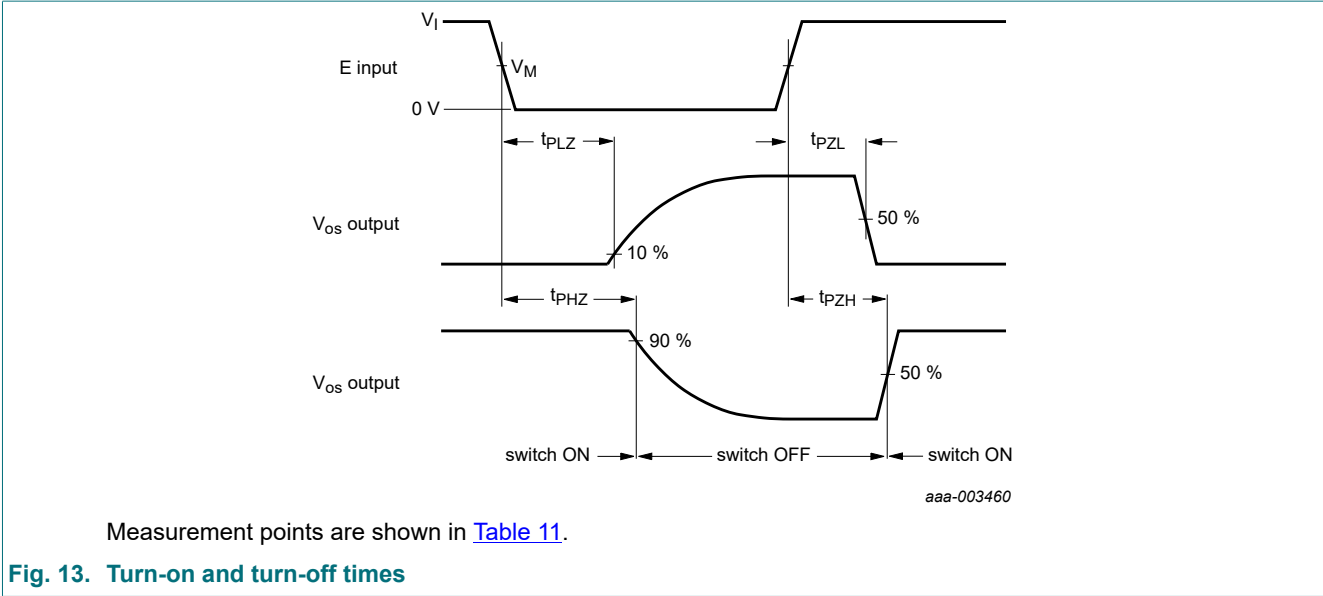


Table 11. Measurement points

Type	V <sub>I</sub>	V <sub>M</sub>
74HC4066	V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT4066	3.0 V	1.3 V

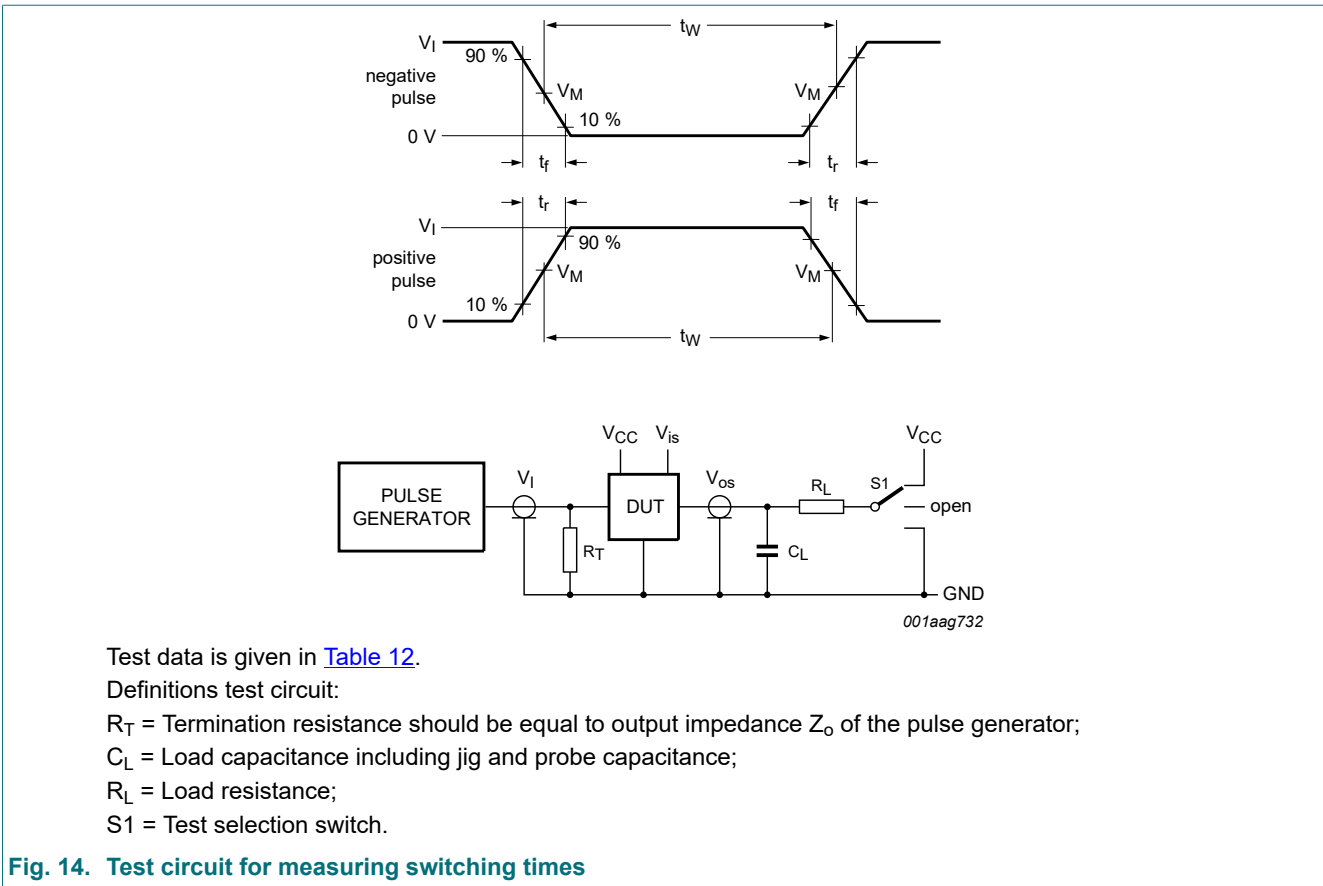


Table 12. Test data

Test	Input			Output		S1 position
	Control E	Switch Yn (Z)	$t_r, t_f$	Switch Z (Yn)		
	$V_I$ [1]	$V_{is}$		$C_L$	$R_L$	
$t_{PHL}, t_{PLH}$	GND	GND to $V_{CC}$	6 ns	50 pF	-	open
$t_{PHZ}, t_{PZH}$	GND to $V_{CC}$	$V_{CC}$	6 ns	50 pF, 15 pF	1 k $\Omega$	GND
$t_{PLZ}, t_{PZL}$	GND to $V_{CC}$	GND	6 ns	50 pF, 15 pF	1 k $\Omega$	$V_{CC}$

[1] For 74HCT4066: maximum input voltage  $V_I = 3.0$  V.

## 11. Additional dynamic characteristics

Table 13. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V;  $T_{amb} = 25$  °C.

$V_{is}$  is the input voltage at a Yn or Z terminal, whichever is assigned as an input.

$V_{os}$  is the output voltage at a Yn or Z terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1$ kHz; $R_L = 10$ k $\Omega$ ; $C_L = 50$ pF; see Fig. 15				%
		$V_{CC} = 4.5$ V; $V_I = 4.0$ V (p-p)	-	0.04	-	%
		$V_{CC} = 9.0$ V; $V_I = 8.0$ V (p-p)	-	0.02	-	%
		$f_i = 10$ kHz; $R_L = 10$ k $\Omega$ ; $C_L = 50$ pF; see Fig. 15				
		$V_{CC} = 4.5$ V; $V_I = 4.0$ V (p-p)	-	0.12	-	%
		$V_{CC} = 9.0$ V; $V_I = 8.0$ V (p-p)	-	0.06	-	%
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50$ $\Omega$ ; $C_L = 10$ pF; see Fig. 16 [1]				
		$V_{CC} = 4.5$ V	-	180	-	MHz
		$V_{CC} = 9.0$ V	-	200	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	$R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $f_i = 1$ MHz; see Fig. 17 [2]				
		$V_{CC} = 4.5$ V	-	-50	-	dB
		$V_{CC} = 9.0$ V	-	-50	-	dB
$V_{ct}$	crosstalk voltage	between digital input and switch (peak to peak value); $R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $f_i = 1$ MHz; see Fig. 18				
		$V_{CC} = 4.5$ V	-	110	-	mV
		$V_{CC} = 9.0$ V	-	220	-	mV
Xtalk	crosstalk	between switches; $R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $f_i = 1$ MHz; see Fig. 19 [2]				
		$V_{CC} = 4.5$ V	-	-60	-	dB
		$V_{CC} = 9.0$ V	-	-60	-	dB

[1] Adjust input voltage  $V_{is}$  to 0 dBm level at  $V_{os}$  for  $f_i = 1$  MHz (0 dBm = 1 mW into 50  $\Omega$ ). After set-up,  $f_i$  is increased to obtain a reading of -3 dB at  $V_{os}$ .

[2] Adjust input voltage  $V_{is}$  to 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).

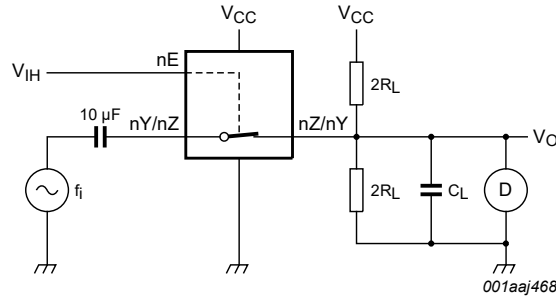
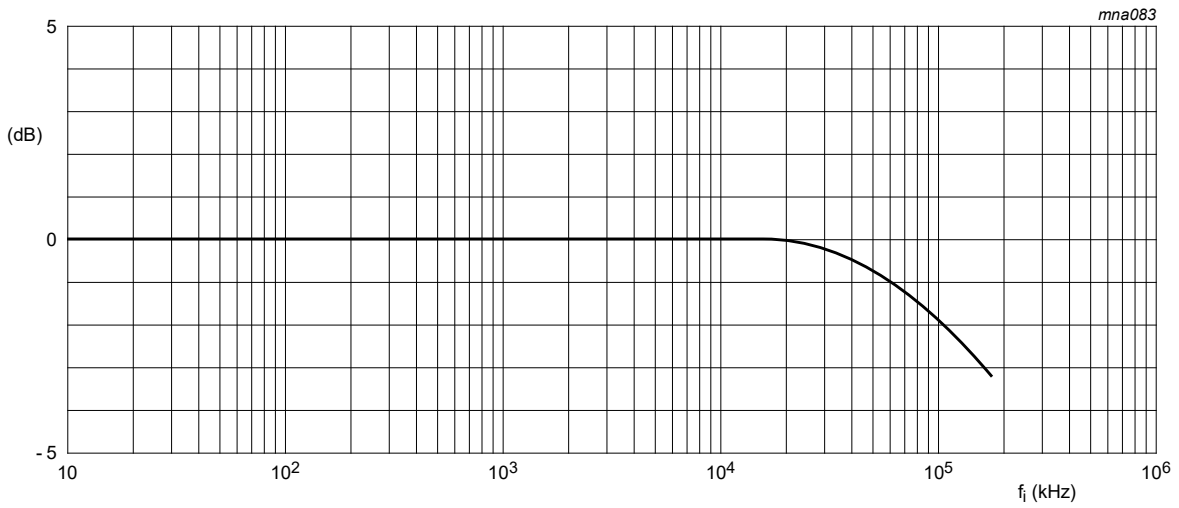
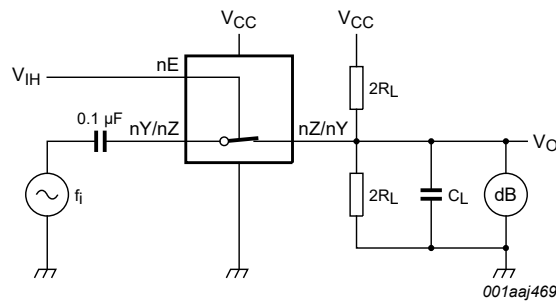


Fig. 15. Test circuit for measuring total harmonic distortion



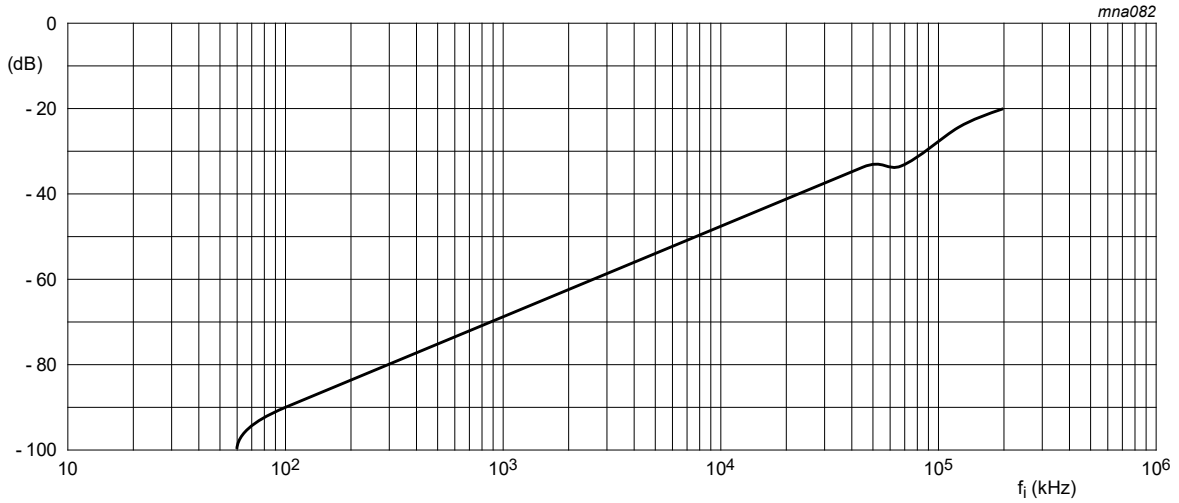
a. Typical -3 dB frequency response



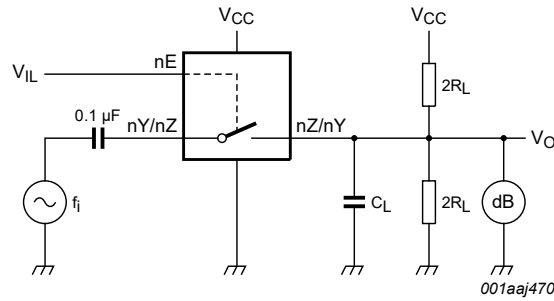
b. Test circuit

$V_{CC} = 4.5 \text{ V}$ ;  $GND = 0 \text{ V}$ ;  $R_L = 50 \text{ }\Omega$ ;  $R_{source} = 1 \text{ k}\Omega$ .

Fig. 16. -3 dB frequency response as a function of frequency



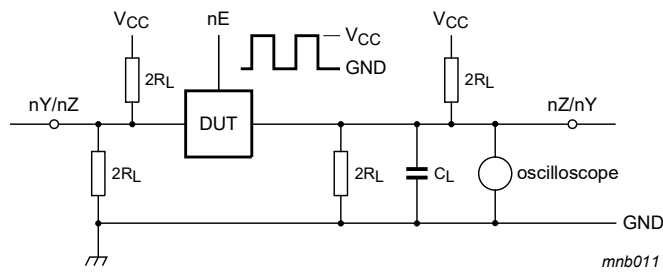
a. Isolation (OFF-state)



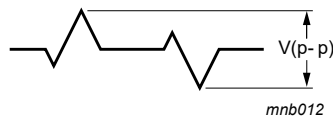
b. Test circuit

$V_{CC} = 4.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $R_L = 600\ \Omega$ ;  $R_{source} = 1\text{ k}\Omega$ .

**Fig. 17. Isolation (OFF-state) as a function of frequency**



a. Test circuit



b. Crosstalk voltage

**Fig. 18. Test circuit for measuring crosstalk voltage (between the digital input and the switch)**

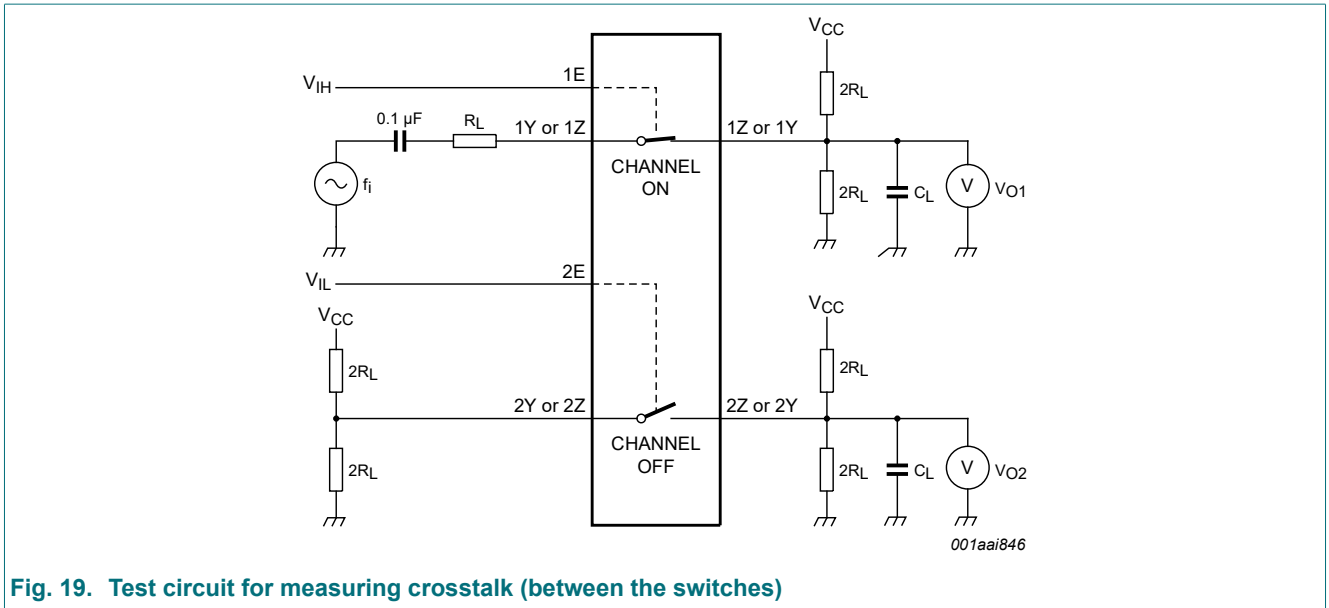


Fig. 19. Test circuit for measuring crosstalk (between the switches)

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

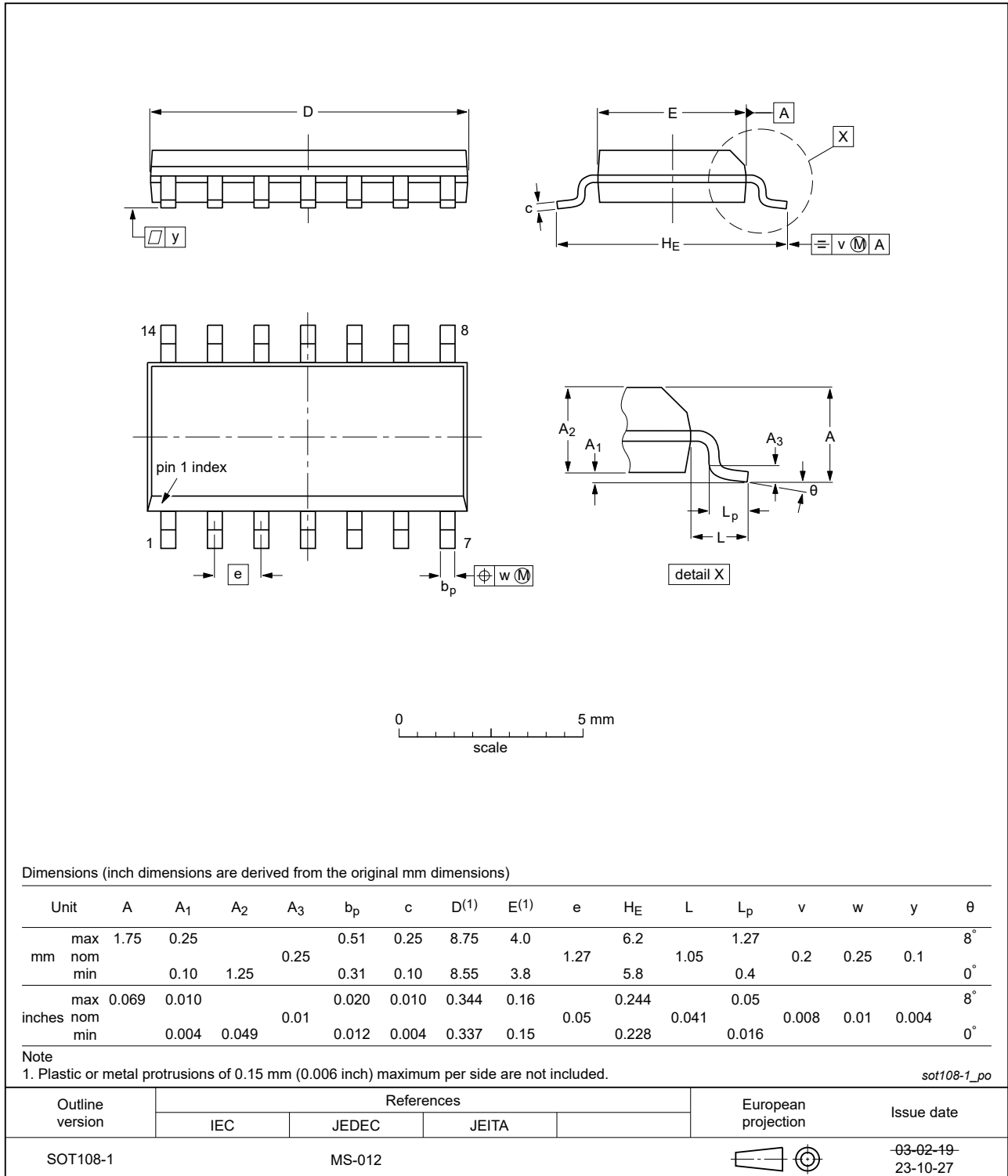


Fig. 20. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

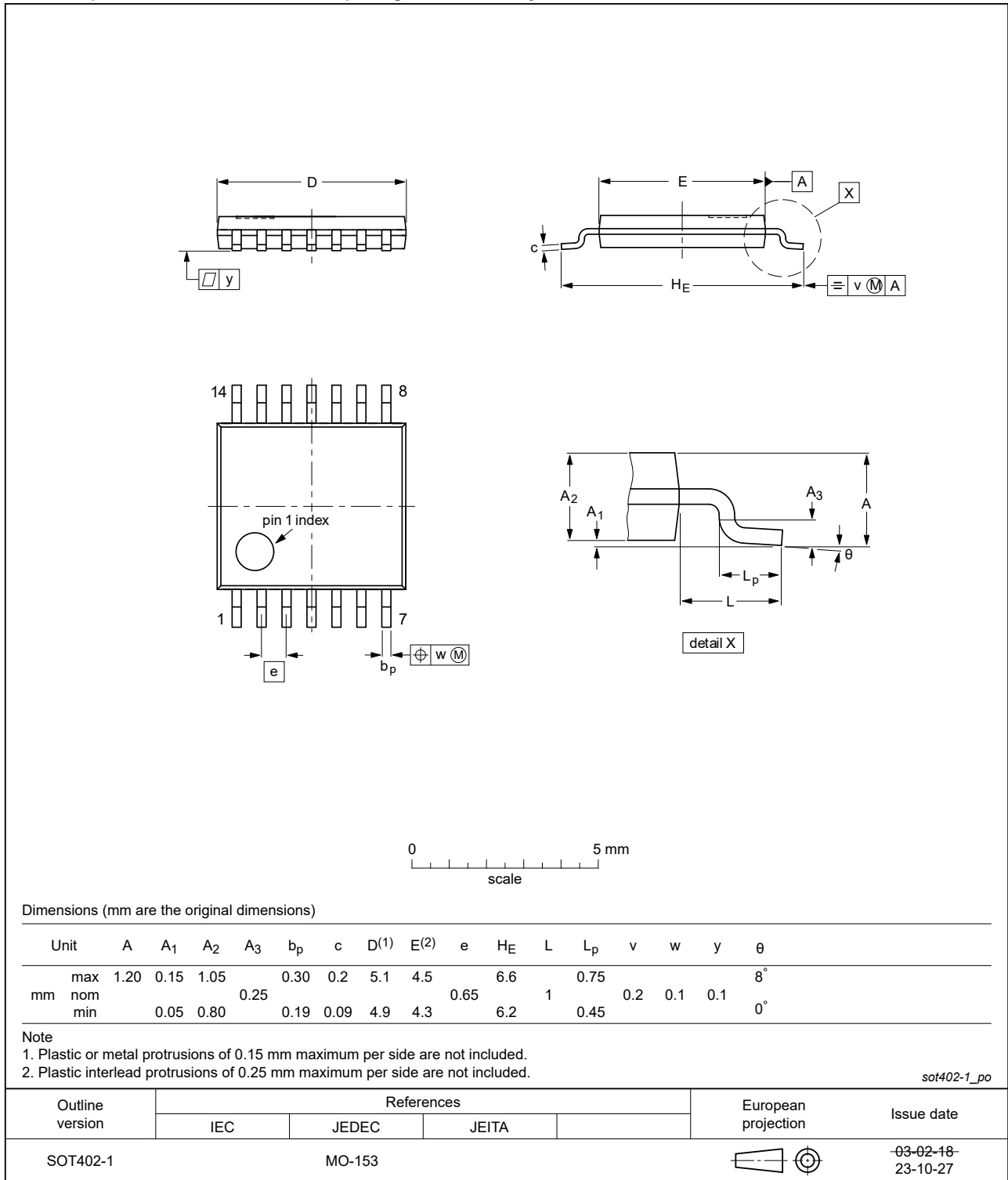


Fig. 21. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

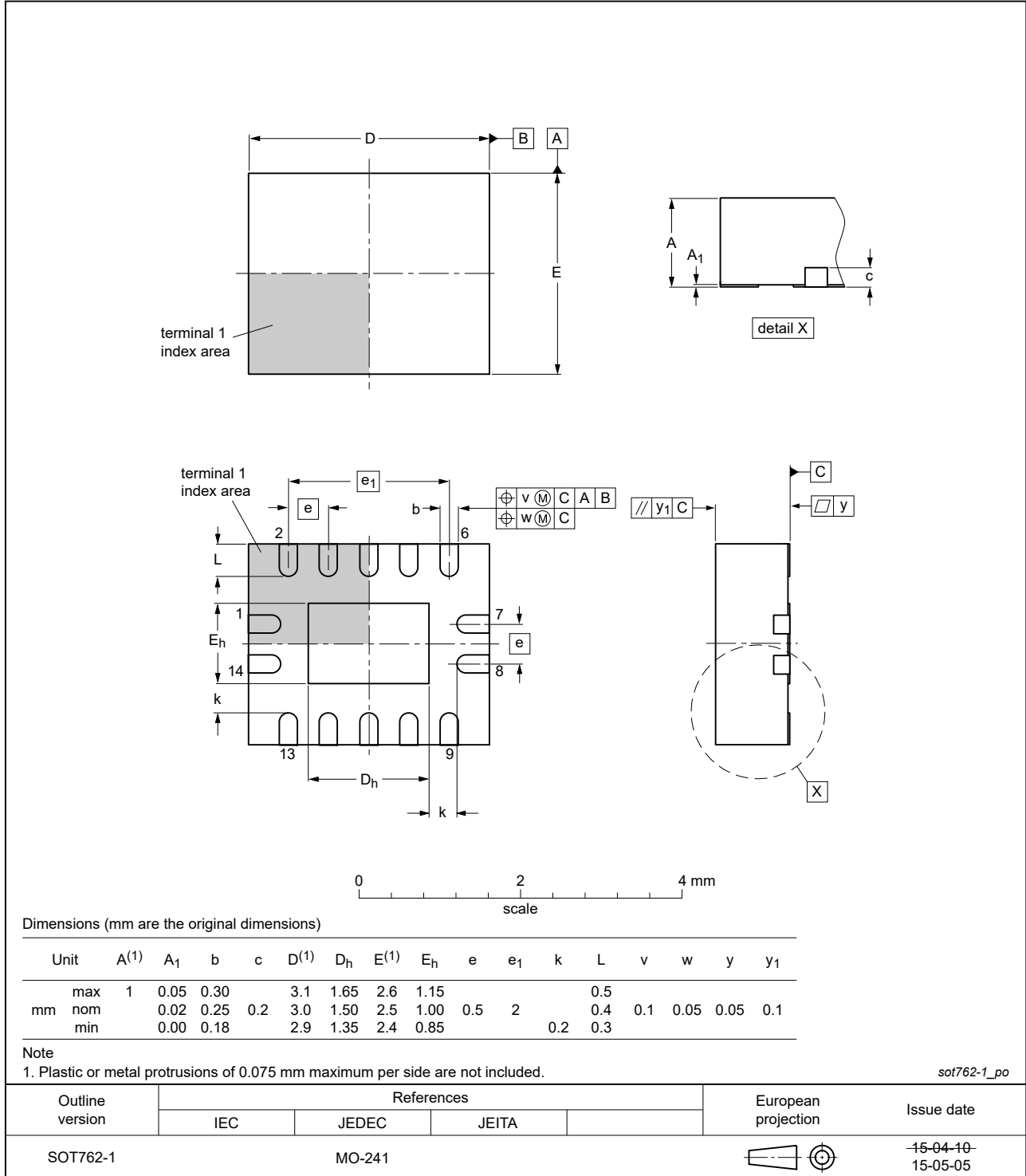


Fig. 22. Package outline SOT762-1 (DHVQFN14)

DHXQFN14: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm x 2 mm x 0.48 mm

SOT8014-1

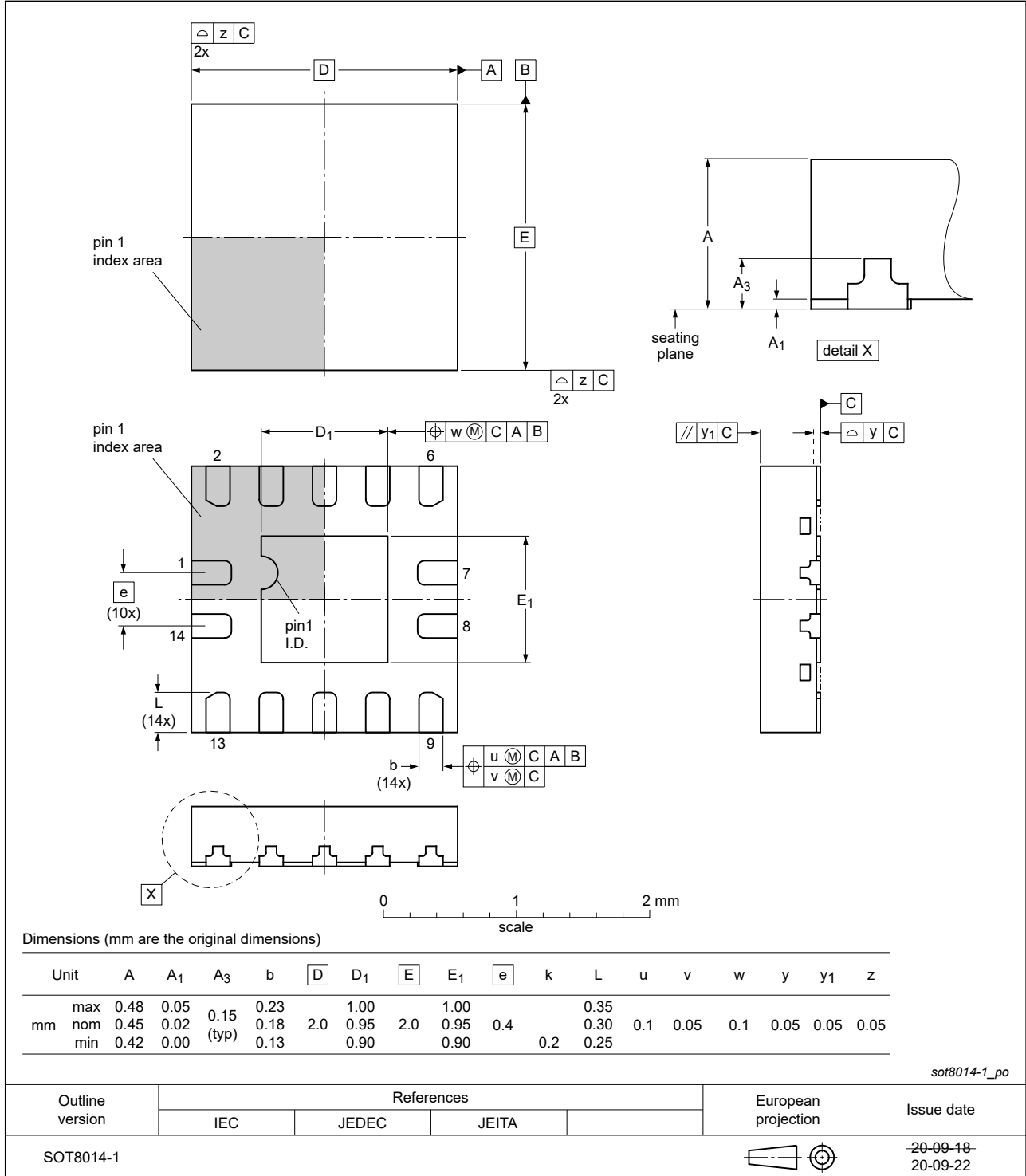


Fig. 23. Package outline SOT8014-1 (DHXQFN14)

## 13. Abbreviations

Table 14. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4066 v.12	20250501	Product data sheet	-	74HC_HCT4066 v.11
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC4066BZ and 74HCT4066BZ (SOT8014-1/DHXQFN14) added.</li> </ul>			
74HC_HCT4066 v.11	20240321	Product data sheet	-	74HC_HCT4066 v.10
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Fig. 20</a>, <a href="#">Fig. 21</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74HC_HCT4066 v.10	20210608	Product data sheet	-	74HC_HCT4066 v.9
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC4066DB and 74HCT4066DB (SOT337-1 / SSOP14) removed.</li> </ul>			
74HC_HCT4066 v.9	20200414	Product data sheet	-	74HC_HCT4066 v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 9</a>: <math>C_{PD}</math> value of 74HC4066 moved to typical column.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> </ul>			
74HC_HCT4066 v.8	20151203	Product data sheet	-	74HC_HCT4066 v.7
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC4066N and 74HCT4066N (SOT27-1) removed.</li> </ul>			
74HC_HCT4066 v.7	20130402	Product data sheet	-	74HC_HCT4066 v.6
Modifications:	<ul style="list-style-type: none"> <li>Descriptive title corrected (errata).</li> <li>New general description (errata).</li> </ul>			
74HC_HCT4066 v.6	20120718	Product data sheet	-	74HC_HCT4066 v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT4066 v.5	20041111	Product data sheet	-	74HC_HCT4066 v.4
74HC_HCT4066 v.4	20030617	Product data sheet	-	74HC_HCT4066_CNV v.3
74HC_HCT4067_CNV v.3	19981110	Product data sheet	-	74HC_HCT4066_CNV v.2
74HC_HCT4066_CNV v.2	19981002	Product specification	-	-

## 15. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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