# THE DATASHEET OF

# ICS9FG1901EKLF

www.win-source.net 0086-755-83957316

# Frequency Generator for P4™ CPU, PCI Express™ & Fully Buffered DIMM Clocks

### Recommended Application:

DB1900G: CPU Host Bus, PCI Express and Fully-Buffered DIMM clocking

### Features:

- Power up default is all outputs in 1:1 mode
- DIF_(16:0) can be “gear-shifted” from the input CPU Host Clock
- DIF_(18:17) can be “gear-shifted” from the input CPU Host Clock
- Spread spectrum compatible
- Supports output clock frequencies up to 400 MHz
- 8 Selectable SMBus addresses
- SMBus address determines PLL or Bypass mode
- VDDA controlled power down mode

### Key Specifications:

- DIF output cycle-to-cycle jitter < 50ps
- DIF (0:18) output-to-output skew < 225ps
- DIF (0:16) output-to-output skew < 100ps

### Functionality at Power Up (PLL Mode)

| FS_A_410[1] | CLK_IN (CPU FSB) MHz | DIF_(18:0) MHz |
|---|---|---|
| 1 | 100 <= CLK_IN < 200 | CLK_IN |
| 0 | 200<= CLK_IN <= 400 | CLK_IN |

1. FS_A_410 is a low-threshold input. Please see the $V_{IL_FS}$ and $V_{IH_FS}$ specifications in the Input/Supply/Common Output Parameters Table for correct values.

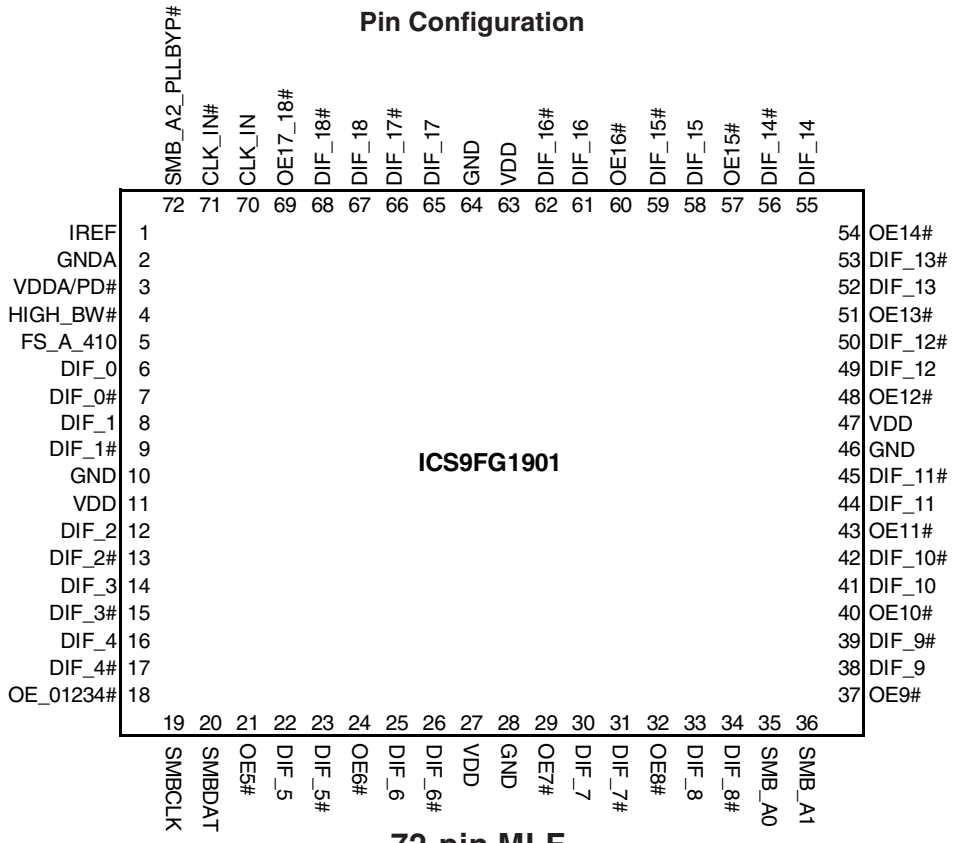
### Power Down Functionality

| INPUTS | | OUTPUTS | | PLL State |
|---|---|---|---|---|
| VDDA/PD# | CLK_IN/CLK_IN# | DIF | DIF# | |
| 3.3V (NOM) | Running | Running | | ON |
| GND | X | Hi-Z | | OFF |

**Functionality Note**

It is recommended that Byte 2, bit 6 be toggled from 1 to 0 and back to 1, the first time VDDA is applied. This ensures proper initialization of the device.

### Pin Configuration




**72-pin MLF**



Other names and brands may be claimed as the property of others.

## Pin Description

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 2 | GNDA | PWR | Ground pin for the PLL core. |
| 3 | VDDA/PD# | PWR | 3.3V power for the PLL core that also functions as Power Down. Collapsing this power supply places the device in Power Down mode. |
| 4 | HIGH_BW# | IN | 3.3V input for selecting PLL Band Width<br>0 = High, 1= Low |
| 5 | FS_A_410 | IN | 3.3V tolerant low threshold input for CPU frequency selection. This pin requires CK410 FSA. Refer to input electrical characteristics for Vil_FS and Vih_FS threshold values. |
| 6 | DIF_0 | OUT | 0.7V differential true clock output |
| 7 | DIF_0# | OUT | 0.7V differential complement clock output |
| 8 | DIF_1 | OUT | 0.7V differential true clock output |
| 9 | DIF_1# | OUT | 0.7V differential complement clock output |
| 10 | GND | PWR | Ground pin. |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | DIF_2 | OUT | 0.7V differential true clock output |
| 13 | DIF_2# | OUT | 0.7V differential complement clock output |
| 14 | DIF_3 | OUT | 0.7V differential true clock output |
| 15 | DIF_3# | OUT | 0.7V differential complement clock output |
| 16 | DIF_4 | OUT | 0.7V differential true clock output |
| 17 | DIF_4# | OUT | 0.7V differential complement clock output |
| 18 | OE_01234# | IN | Active low input for enabling DIF pairs 0, 1, 2, 3 and 4.<br>1 = tri-state outputs, 0 = enable outputs |
| 19 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 20 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 21 | OE5# | IN | Active low input for enabling DIF pair 5.<br>1 = tri-state outputs, 0 = enable outputs |
| 22 | DIF_5 | OUT | 0.7V differential true clock output |
| 23 | DIF_5# | OUT | 0.7V differential complement clock output |
| 24 | OE6# | IN | Active low input for enabling DIF pair 6.<br>1 = tri-state outputs, 0 = enable outputs |
| 25 | DIF_6 | OUT | 0.7V differential true clock output |
| 26 | DIF_6# | OUT | 0.7V differential complement clock output |
| 27 | VDD | PWR | Power supply, nominal 3.3V |
| 28 | GND | PWR | Ground pin. |
| 29 | OE7# | IN | Active low input for enabling DIF pair 7.<br>1 = tri-state outputs, 0 = enable outputs |
| 30 | DIF_7 | OUT | 0.7V differential true clock output |
| 31 | DIF_7# | OUT | 0.7V differential complement clock output |
| 32 | OE8# | IN | Active low input for enabling DIF pair 8.<br>1 = tri-state outputs, 0 = enable outputs |
| 33 | DIF_8 | OUT | 0.7V differential true clock output |
| 34 | DIF_8# | OUT | 0.7V differential complement clock output |
| 35 | SMB_A0 | IN | SMBus address bit 0 (LSB) |
| 36 | SMB_A1 | IN | SMBus address bit 1 |

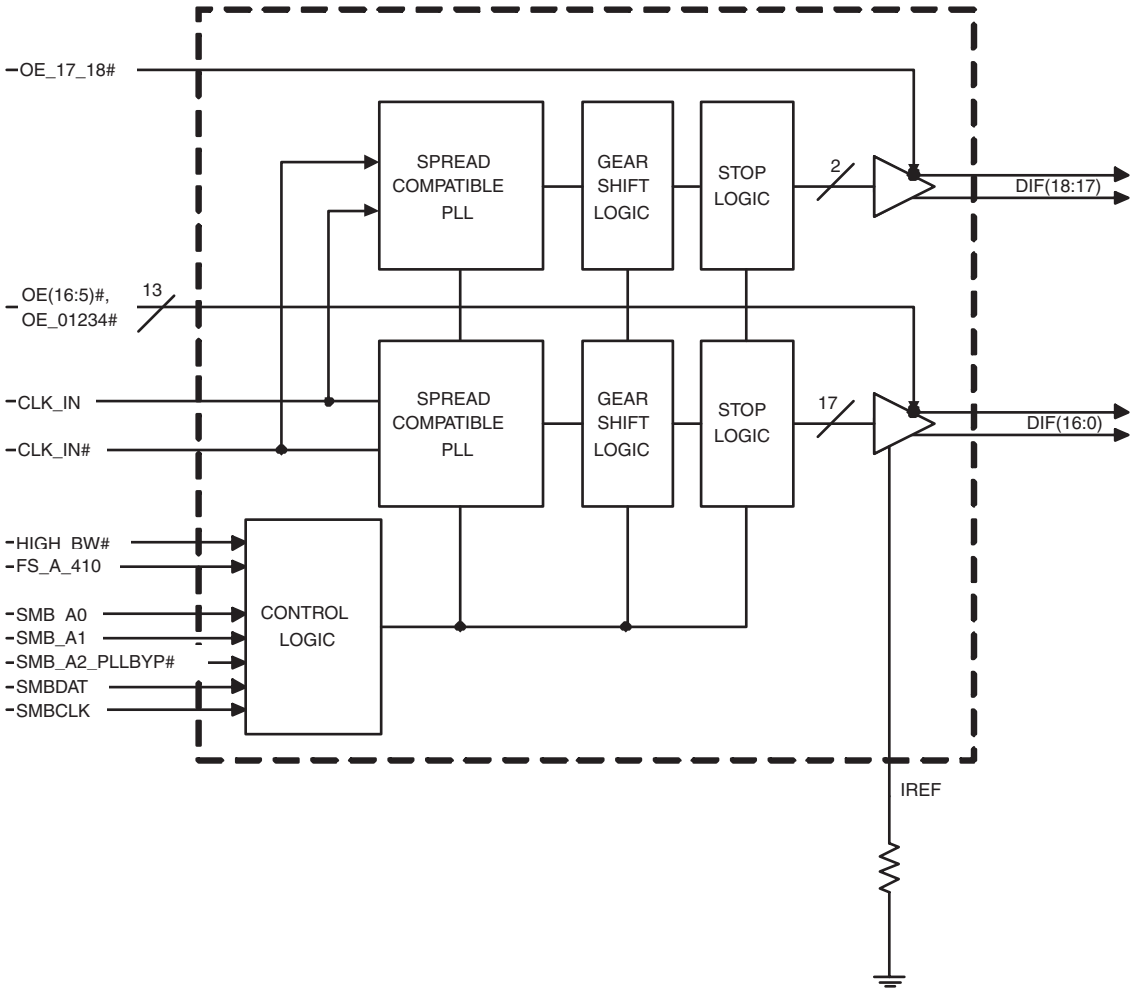
## Pin Description (Continued)

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 37 | OE9# | IN | Active low input for enabling DIF pair 9.<br>1 = tri-state outputs, 0 = enable outputs |
| 38 | DIF_9 | OUT | 0.7V differential true clock output |
| 39 | DIF_9# | OUT | 0.7V differential complement clock output |
| 40 | OE10# | IN | Active low input for enabling DIF pair 10.<br>1 = tri-state outputs, 0 = enable outputs |
| 41 | DIF_10 | OUT | 0.7V differential true clock output |
| 42 | DIF_10# | OUT | 0.7V differential complement clock output |
| 43 | OE11# | IN | Active low input for enabling DIF pair 11.<br>1 = tri-state outputs, 0 = enable outputs |
| 44 | DIF_11 | OUT | 0.7V differential true clock output |
| 45 | DIF_11# | OUT | 0.7V differential complement clock output |
| 46 | GND | PWR | Ground pin. |
| 47 | VDD | PWR | Power supply, nominal 3.3V |
| 48 | OE12# | IN | Active low input for enabling DIF pair 12.<br>1 = tri-state outputs, 0 = enable outputs |
| 49 | DIF_12 | OUT | 0.7V differential true clock output |
| 50 | DIF_12# | OUT | 0.7V differential complement clock output |
| 51 | OE13# | IN | Active low input for enabling DIF pair 13.<br>1 = tri-state outputs, 0 = enable outputs |
| 52 | DIF_13 | OUT | 0.7V differential true clock output |
| 53 | DIF_13# | OUT | 0.7V differential complement clock output |
| 54 | OE14# | IN | Active low input for enabling DIF pair 14.<br>1 = tri-state outputs, 0 = enable outputs |
| 55 | DIF_14 | OUT | 0.7V differential true clock output |
| 56 | DIF_14# | OUT | 0.7V differential complement clock output |
| 57 | OE15# | IN | Active low input for enabling DIF pair 15.<br>1 = tri-state outputs, 0 = enable outputs |
| 58 | DIF_15 | OUT | 0.7V differential true clock output |
| 59 | DIF_15# | OUT | 0.7V differential complement clock output |
| 60 | OE16# | IN | Active low input for enabling DIF pair 16.<br>1 = tri-state outputs, 0 = enable outputs |
| 61 | DIF_16 | OUT | 0.7V differential true clock output |
| 62 | DIF_16# | OUT | 0.7V differential complement clock output |
| 63 | VDD | PWR | Power supply, nominal 3.3V |
| 64 | GND | PWR | Ground pin. |
| 65 | DIF_17 | OUT | 0.7V differential true clock output |
| 66 | DIF_17# | OUT | 0.7V differential complement clock output |
| 67 | DIF_18 | OUT | 0.7V differential true clock output |
| 68 | DIF_18# | OUT | 0.7V differential complement clock output |
| 69 | OE17_18# | IN | Active low input for enabling DIF pairs 17 and 18.<br>1 = tri-state outputs, 0 = enable outputs |
| 70 | CLK_IN | IN | Input for reference clock. |
| 71 | CLK_IN# | IN | "Complementary" reference clock input. |
| 72 | SMB_A2_PLLBYP# | IN | SMBus address bit 2. When Low, the part operates as a fanout buffer with the PLL bypassed. When High, the part operates as a zero-delay buffer (ZDB) with the PLL operating.<br>0 = fanout mode (PLL bypassed), 1 = ZDB mode (PLL used) |

## General Description

The **ICS9FG1901** follows the Intel DB1900G Differential Buffer Specification. This buffer provides 19 output clocks for CPU Host Bus, PCI-Express, or Fully Buffered DIMM applications. The outputs are configured with two groups. Both groups, DIF_(16:0) and DIF_(18:17) can be equal to or have a gear ratio to the input clock. A differential CPU clock from a CK410 or CK410B main clock generator, such as the ICS954101 or ICS932S401, drives the **ICS9FG1901**. The **ICS9FG1901** can provide outputs up to 400MHz.

## Block Diagram




## Power Groups

| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 3 | 2 | Main PLL, Analog |
| 11,27,47,63 | 10,28,46,64 | DIF clocks |

## ICS9FG1901 Programmable Gear Ratios

| FS_A_410 | SMBus Byte 0 Bit 3 | Bit 2 | Bit 1 | Bit 0 | Input (m) | Output (n) | Gear Ratio (n/m) | Input (CPU FSB) and Output Frequencies (MHz) 200.0 | 266.7 | 320.0 | 333.3 | 400.0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 3 | 1 | 0.333 | 66.7 | 88.9 | 106.7 | 111.1 | 133.3 |
| 0 | 0 | 0 | 0 | 1 | 5 | 2 | 0.400 | 80.0 | 106.7 | 128.0 | 133.3 | 160.0 |
| 0 | 0 | 0 | 1 | 0 | 12 | 5 | 0.417 | 83.3 | 111.1 | 133.3 | 138.9 | 166.7 |
| 0 | 0 | 0 | 1 | 1 | 2 | 1 | 0.500 | 100.0 | 133.3 | 160.0 | 166.7 | 200.0 |
| 0 | 0 | 1 | 0 | 0 | 5 | 3 | 0.600 | 120.0 | 160.0 | 192.0 | 200.0 | 240.0 |
| 0 | 0 | 1 | 0 | 1 | 8 | 5 | 0.625 | 125.0 | 166.7 | 200.0 | 208.3 | 250.0 |
| 0 | 0 | 1 | 1 | 0 | 3 | 2 | 0.667 | 133.3 | 177.8 | 213.3 | 222.2 | 266.7 |
| 0 | 0 | 1 | 1 | 1 | 4 | 3 | 0.750 | 150.0 | 200.0 | 240.0 | 250.0 | 300.0 |
| 0 | 1 | 0 | 0 | 0 | 6 | 5 | 0.833 | 166.7 | 222.2 | 266.7 | 277.8 | 333.3 |
| **0** | **1** | **0** | **0** | **1** | **1** | **1** | **1.000** | **200.0** | **266.7** | **320.0** | **333.3** | **400.0** |
| 0 | 1 | 0 | 1 | 0 | 5 | 6 | 1.200 | 240.0 | 320.0 | 384.0 | 400.0 | NA |
| 0 | 1 | 0 | 1 | 1 | 4 | 5 | 1.250 | 250.0 | 333.3 | 400.0 | NA | NA |
| 0 | 1 | 1 | 0 | 0 | 3 | 4 | 1.333 | 266.7 | 355.6 | NA | NA | NA |
| 0 | 1 | 1 | 0 | 1 | 2 | 3 | 1.500 | 300.0 | 400.0 | NA | NA | NA |
| 0 | 1 | 1 | 1 | 0 | 3 | 5 | 1.667 | 333.3 | NA | NA | NA | NA |
| 0 | 1 | 1 | 1 | 1 | 1 | 2 | 2.000 | 400.0 | NA | NA | NA | NA |
| | | | | | | | | CLK IN (CPU FSB) Frequency (MHz) 100 | 133.33 | 160 | 166.67 | |
| 1 | 0 | 0 | 0 | 0 | 3 | 1 | 0.333 | | | | | |
| 1 | 0 | 0 | 0 | 1 | 5 | 2 | 0.400 | NA | 53.3 | 64.0 | 66.7 | |
| 1 | 0 | 0 | 1 | 0 | 12 | 5 | 0.417 | NA | 55.6 | 66.7 | 69.4 | |
| 1 | 0 | 0 | 1 | 1 | 2 | 1 | 0.500 | 50.0 | 66.7 | 80.0 | 83.3 | |
| 1 | 0 | 1 | 0 | 0 | 5 | 3 | 0.600 | 60.0 | 80.0 | 96.0 | 100.0 | |
| 1 | 0 | 1 | 0 | 1 | 8 | 5 | 0.625 | 62.5 | 83.3 | 100.0 | 104.2 | |
| 1 | 0 | 1 | 1 | 0 | 3 | 2 | 0.667 | 66.7 | 88.9 | 106.7 | 111.1 | |
| 1 | 0 | 1 | 1 | 1 | 5 | 4 | 0.800 | 80.0 | 106.7 | 128.0 | 133.3 | |
| 1 | 1 | 0 | 0 | 0 | 6 | 5 | 0.833 | NA | 111.1 | 133.3 | 138.9 | |
| **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1.000** | **100.0** | **133.3** | **160.0** | **166.7** | |
| 1 | 1 | 0 | 1 | 0 | 5 | 6 | 1.200 | 120.0 | 160.0 | 192.0 | 200.0 | |
| 1 | 1 | 0 | 1 | 1 | 4 | 5 | 1.250 | 125.0 | 166.7 | 200.0 | 208.3 | |
| 1 | 1 | 1 | 0 | 0 | 3 | 4 | 1.333 | 133.3 | 177.8 | 213.3 | 222.2 | |
| 1 | 1 | 1 | 0 | 1 | 2 | 3 | 1.500 | 150.0 | 200.0 | | | |
| 1 | 1 | 1 | 1 | 0 | 3 | 5 | 1.667 | 166.7 | 222.2 | 266.7 | 277.8 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2.000 | 200.0 | 266.7 | 320.0 | 333.3 | |

Note: Lines in **BOLD** are Power-up defaults for FS_A_410 = 0 and 1 respectively.
Shaded areas are shown for reference only and are not necessarily valid operating points

## Absolute Max

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| VDD_A | 3.3V Core Supply Voltage | | $V_{DD}$ + 0.5V | V |
| VDD_In | 3.3V Logic Input Supply Voltage | GND - 0.5 | $V_{DD}$ + 0.5V | V |
| Ts | Storage Temperature | -65 | 150 | °C |
| Tambient | Ambient Operating Temp | 0 | 70 | °C |
| Tcase | Case Temperature | | 115 | °C |
| ESD prot | Input ESD protection human body model | 2000 | | V |

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.8 | V | |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | -5 | | 5 | uA | |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA | |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA | |
| Low Threshold Input-High Voltage | $V_{IH_FS}$ | 3.3 V +/-5% | 0.7 | | $V_{DD}$ + 0.3 | V | |
| Low Threshold Input-Low Voltage | $V_{IL_FS}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.35 | V | |
| Operating Current | $I_{DD3.3OP}$ | all outputs driven | | 450 | 600 | mA | |
| Powerdown Current | $I_{DD3.3PD}$ | all differential pairs tri-stated | | 13 | 36 | mA | |
| Input Frequency | $F_i$ | $V_{DD}$ = 3.3 V | 100 | | 400 | MHz | 3 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Input Capacitance | $C_{IN}$ | Logic Inputs | | | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | 2.500 | | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up or valid input clock, whichever comes last | | 1.300 | 1.8 | ms | 1,2 |
| Modulation Frequency Tracking | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| SMBus Voltage | $V_{MAX}$ | Maximum input voltage | | | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OL}$ | @ $I_{PULLUP}$ | | | 0.4 | V | 1 |
| Current sinking at $V_{OL}$ = 0.4 V | $I_{PULLUP}$ | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | $T_{RI2C}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | $T_{FI2C}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3]Output frequency accuracy is dependent upon the accuracy of the input frequency measured at the CLK_IN pins.

## Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =2pF, $R_S$=33.2Ω, $R_P$=49.9Ω, $I_{REF}$ = 475Ω

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | $Zo^1$ | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | 750 | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | | 150 | | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 400MHz nominal | 2.4993 | | 2.5008 | ns | 2 |
| | | 400MHz spread | 2.4993 | | 2.5133 | ns | 2 |
| | | 333.33MHz nominal | 2.9991 | | 3.0009 | ns | 2 |
| | | 333.33MHz spread | 2.9991 | | 3.016 | ns | 2 |
| | | 266.66MHz nominal | 3.7489 | | 3.7511 | ns | 2 |
| | | 266.66MHz spread | 3.7489 | | 3.77 | ns | 2 |
| | | 200MHz nominal | 4.9985 | | 5.0015 | ns | 2 |
| | | 200MHz spread | 4.9985 | | 5.0266 | ns | 2 |
| | | 166.66MHz nominal | 5.9982 | | 6.0018 | ns | 2 |
| | | 166.66MHz spread | 5.9982 | | 6.0320 | ns | 2 |
| | | 133.33MHz nominal | 7.4978 | | 7.5023 | ns | 2 |
| | | 133.33MHz spread | 7.4978 | | 7.5400 | ns | 2 |
| | | 100.00MHz nominal | 9.9970 | | 10.0030 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2 |
| Absolute min period | $T_{absmin}$ | 400MHz nominal/spread | 2.4143 | | | ns | 1,2 |
| | | 333.33MHz nominal/spread | 2.9141 | | | ns | 1,2 |
| | | 266.66MHz nominal/spread | 3.6639 | | | ns | 1,2 |
| | | 200MHz nominal/spread | 4.8735 | | | ns | 1,2 |
| | | 166.66MHz nominal/spread | 5.8732 | | | ns | 1,2 |
| | | 133.33MHz nominal/spread | 7.3728 | | | ns | 1,2 |
| | | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | 175 | 400 | 700 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | 175 | 425 | 700 | ps | 1 |
| Rise Time Variation | d-$t_r$ | | | 20 | 125 | ps | 1 |
| Fall Time Variation | d-$t_f$ | | | 15 | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | 50.5 | 55 | % | 1 |
| Output-to-Output Skew - DIF(0:16) | $t_{sk3_016}$ | $V_T$ = 50%, Skew within Group of 17, 1 to 1 mode only | | 75 | 100 | ps | 1 |
| Output-to-Output Skew - DIF(0:18) | $t_{sk3_018}$ | $V_T$ = 50%, Skew across all outputs 1 to 1 mode only | | 200 | 225 | ps | 1 |
| Input-to-Output Delay | $t_{pdpll}$ | PLL Mode | -500 | | 500 | ps | 1 |
| | $t_{pdbyp}$ | Bypass Mode | 2.5 | 3.6 | 4.5 | ns | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | PLL mode, from differential wavefrom | | 40 | 50 | ps | 1 |
| | | Bypass mode as additive jitter | | 25 | 50 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that the input frequency meets CK410 accuracy requirements

[3]$I_{REF} = V_{DD}/(3xR_R)$. For $R_R$ = 475Ω (1%), $I_{REF}$ = 2.32mA. $I_{OH}$ = 6 x $I_{REF}$ and $V_{OH}$ = 0.7V @ $Z_O$=50Ω

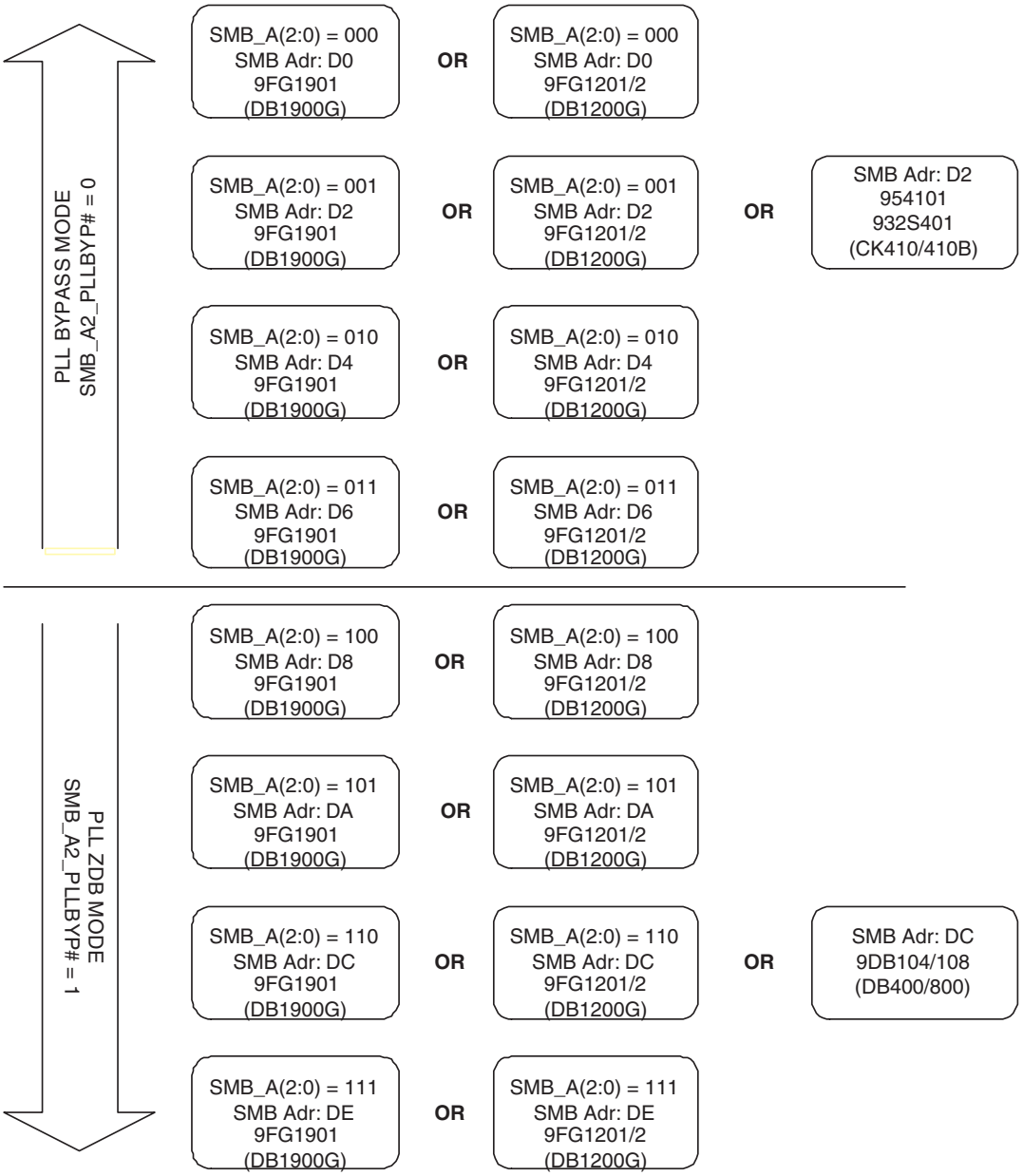
## PLL Bandwidth and Peaking

| Parameter | | Conditions | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| PLL Jitter Peaking | $j_{peak-hibw}$ | (HIGH_BW# = 0) | 0 | 1 | 2.5 | dB | 2,8 |
| PLL Jitter Peaking | $j_{peak-lobw}$ | (HIGH_BW# = 1) | 0 | 1 | 2 | dB | 2,8 |
| PLL Bandwidth | $pll_{HIBW}$ | (HIGH_BW# = 0) | 2 | 2.3 | 4 | MHz | 1,8 |
| PLL Bandwidth | $pll_{LOBW}$ | (HIGH_BW# = 1) | 0.7 | 1.28 | 1.4 | MHz | 1,8 |
| Output phase jitter impact – PCIe* Gen1 | $\theta_{PCIe1}$ | (including PLL BW 1.5-22 MHz, z = 0.54, Td=10 ns, Ftrk=1.5 MHz ) | 0 | 77 | 108 | ps | 3,6,7,8 |
| Output phase jitter impact – FBD | $\theta_{FBD}$ | (including PLL BW 11- 33 Mz, z = 0.54, Td=5 ns, Ftrk=0.2 MHz) | 0 | | 3 | ps RMS | 3,4,7,8 |

**NOTES:**

1. Measured at 3 db down or half power point.
2. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
3. Post processed evaluation through Intel supplied Matlab scripts.
4. Refer to FB-DIMM Specification: “High Speed Differential Point-to-Point Link at 1.5 V” for updates to this specification.
5. PCIe* Gen2 filter characteristics are subject to final ratification by PC ISIG. Please check the PCI* SIG for the latest specification. Tested with DBxx00G driven by low phase noise signal generator such as an Agilent 8133A.
6. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
7. $z$ = 0.54 is implying a jitter peaking of 3 dB.
8. Guaranteed by design and characterization, not 100% tested in production.

**9FG1901 SMBus Address Mapping when using CK410/CK410B, 9FG1201, and 9DB104/108**



**SMBusTable: FSB Frequency Select Register**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | DIF(16:0) | GRSEL_17 | Group of 17 gear ratio select | RW | Gear Ratio | 1:1 | 1 |
| Bit 6 | DIF(18:17) | GRSEL_2 | Group of 2 gear ratio select | RW | Gear Ratio | 1:1 | 1 |
| Bit 5 | | Reserved | | | | | X |
| Bit 4 | - | FS_A_410 Latched Input | | RW | See ICS9FG1901 Programmable Gear Ratios Table | | Latch |
| Bit 3 | - | FSBG_3 | FSB Gear Ratio FS_3 | RW | | | x |
| Bit 2 | - | FSBG_2 | FSB Gear Ratio FS_2 | RW | | | 0 |
| Bit 1 | - | FSBG_1 | FSB Gear Ratio FS_1 | RW | | | x |
| Bit 0 | - | FSBG_0 | FSB Gear Ratio FS_0 | RW | | | 1 |

**SMBusTable: Output Control Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | DIF_7 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 6 | | DIF_6 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 5 | | DIF_5 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 4 | | DIF_4 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 3 | | DIF_3 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 2 | | DIF_2 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 1 | | DIF_1 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 0 | | DIF_0 | Output Control | RW | Hi-Z | Enable | 1 |

**SMBusTable: Output and PLL BW Control Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | see note | PLL_BW# adjust | | RW | High BW | Low BW | 1 |
| Bit 6 | see note | BYPASS# test mode / PLL | | RW | Bypass | PLL | 1 |
| Bit 5 | | DIF_13 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 4 | | DIF_12 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 3 | | DIF_11 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 2 | | DIF_10 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 1 | | DIF_9 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 0 | | DIF_8 | Output Control | RW | Hi-Z | Enable | 1 |

Note: Bit 7 is wired OR to the HIGH_BW# input, any 0 selects High BW

Note: Bit 6 is wired OR to the SMB_A2_PLLBYP# input, any 0 selects Fanout Bypass mode

**SMBusTable: Output Enable Readback Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | Readback - OE9# Input | | R | Readback | | X |
| Bit 6 | | Readback - OE8# Input | | R | Readback | | X |
| Bit 5 | | Readback - OE7# Input | | R | Readback | | X |
| Bit 4 | | Readback - OE6# Input | | R | Readback | | X |
| Bit 3 | | Readback - OE5# Input | | R | Readback | | X |
| Bit 2 | | Readback - OE_01234# Input | | R | Readback | | X |
| Bit 1 | 8 | Readback - HIGH_BW# In | | R | Readback | | X |
| Bit 0 | 72 | Readback - SMB_A2_PLLBYP# In | | R | Readback | | X |

**SMBusTable: Output Enable Readback Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 69 | Readback - OE17_18# Input | | R | Readback | | X |
| Bit 6 | 60 | Readback - OE16# Input | | R | Readback | | X |
| Bit 5 | 57 | Readback - OE15# Input | | R | Readback | | X |
| Bit 4 | 54 | Readback - OE14# Input | | R | Readback | | X |
| Bit 3 | 51 | Readback - OE13# Input | | R | Readback | | X |
| Bit 2 | 48 | Readback - OE12# Input | | R | Readback | | X |
| Bit 1 | 43 | Readback - OE11# Input | | R | Readback | | X |
| Bit 0 | 40 | Readback - OE10# Input | | R | Readback | | X |

**SMBusTable: Vendor & Revision ID Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | X |
| Bit 6 | - | RID2 | | R | - | - | X |
| Bit 5 | - | RID1 | | R | - | - | X |
| Bit 4 | - | RID0 | | R | - | - | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

**SMBusTable: DEVICE ID**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Device ID 7 (MSB) | | RW | Reserved | | 1 |
| Bit 6 | - | Device ID 6 | | RW | Reserved | | 0 |
| Bit 5 | - | Device ID 5 | | RW | Reserved | | 0 |
| Bit 4 | - | Device ID 4 | | RW | Reserved | | 1 |
| Bit 3 | - | Device ID 3 | | RW | Reserved | | 0 |
| Bit 2 | - | Device ID 2 | | RW | Reserved | | 0 |
| Bit 1 | - | Device ID 1 | | RW | Reserved | | 0 |
| Bit 0 | - | Device ID 0 | | RW | Reserved | | 1 |

**SMBusTable: Byte Count Register**

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | BC7 | Writing to this register configures how many bytes will be read back. | RW | - | - | 0 |
| Bit 6 | - | BC6 | | RW | - | - | 0 |
| Bit 5 | - | BC5 | | RW | - | - | 0 |
| Bit 4 | - | BC4 | | RW | - | - | 0 |
| Bit 3 | - | BC3 | | RW | - | - | 0 |
| Bit 2 | - | BC2 | | RW | - | - | 1 |
| Bit 1 | - | BC1 | | RW | - | - | 1 |
| Bit 0 | - | BC0 | | RW | - | - | 1 |

**SMBusTable: Control Pin Readback Register**

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 5 | Readback - FS_A_410 | | R | Readback | | X |
| Bit 6 | | RESERVED | | | | | X |
| Bit 5 | | RESERVED | | | | | X |
| Bit 4 | | DIF_18 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 3 | | DIF_17 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 2 | | DIF_16 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 1 | | DIF_15 | Output Control | RW | Hi-Z | Enable | 1 |
| Bit 0 | | DIF_14 | Output Control | RW | Hi-Z | Enable | 1 |

**SMBusTable: Reserved Register**

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | RESERVED | | | | | 0 |
| Bit 2 | | RESERVED | | | | | 0 |
| Bit 1 | | RESERVED | | | | | 0 |
| Bit 0 | | RESERVED | | | | | 0 |

**SMBus Table: M/N Programming & Watchdog Safe Register**

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | M/N_EN | Gearing PLL and 1:1 PLL M/N Programming Enable | RW | Disable | Enable | 0 |
| Bit 6 | | RESERVED | | | | | X |
| Bit 5 | | RESERVED | | | | | X |
| Bit 4 | | RESERVED | | | | | X |
| Bit 3 | | RESERVED | | | | | X |
| Bit 2 | | RESERVED | | | | | X |
| Bit 1 | | RESERVED | | | | | X |
| Bit 0 | | RESERVED | | | | | X |

**SMBus Table: Gearing PLL Frequency Control Register**

| Byte 11 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Gearing PLL N Div8 | N Divider Prog bit 8 | RW | | | X |
| Bit 6 | - | Gearing PLL N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | Gearing PLL M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | - | Gearing PLL M Div4 | | RW | | | X |
| Bit 3 | - | Gearing PLL M Div3 | | RW | | | X |
| Bit 2 | - | Gearing PLL M Div2 | | RW | | | X |
| Bit 1 | - | Gearing PLL M Div1 | | RW | | | X |
| Bit 0 | - | Gearing PLL M Div0 | | RW | | | X |

**SMBus Table: Gearing PLL Frequency Control Register**

| Byte 12 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Gearing PLL N Div7 | N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6) | RW | | | X |
| Bit 6 | - | Gearing PLL N Div6 | | RW | | | X |
| Bit 5 | - | Gearing PLL N Div5 | | RW | | | X |
| Bit 4 | - | Gearing PLL N Div4 | | RW | | | X |
| Bit 3 | - | Gearing PLL N Div3 | | RW | | | X |
| Bit 2 | - | Gearing PLL N Div2 | | RW | | | X |
| Bit 1 | - | Gearing PLL N Div1 | | RW | | | X |
| Bit 0 | - | Gearing PLL N Div0 | | RW | | | X |

**SMBusTable: Gearing PLL Output Divider Register (Rev H and higher)**

| Byte 13 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | Gearing PLL OutDiv 3 | PLL 1 Output Divider | RW | See Output Divider Table | | X |
| Bit 2 | | Gearing PLL OutDiv 2 | PLL 1 Output Divider | RW | | | X |
| Bit 1 | | Gearing PLL OutDiv 1 | PLL 1 Output Divider | RW | | | X |
| Bit 0 | | Gearing PLL OutDiv 0 | PLL 1 Output Divider | RW | | | X |

**SMBusTable: Reserved Register**

| Byte 14 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | RESERVED | | | | | 0 |
| Bit 2 | | RESERVED | | | | | 0 |
| Bit 1 | | RESERVED | | | | | 0 |
| Bit 0 | | RESERVED | | | | | 0 |

**SMBusTable: Reserved Register**

| Byte 15 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | RESERVED | | | | | 0 |
| Bit 2 | | RESERVED | | | | | 0 |
| Bit 1 | | RESERVED | | | | | 0 |
| Bit 0 | | RESERVED | | | | | 0 |

**SMBusTable: Reserved Register**

| Byte 16 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | RESERVED | | | | | 0 |
| Bit 2 | | RESERVED | | | | | 0 |
| Bit 1 | | RESERVED | | | | | 0 |
| Bit 0 | | RESERVED | | | | | 0 |

**SMBus Table: 1:1 PLL Frequency Control Register**

| Byte 17 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | 1:1 PLL N Div8 | N Divider Prog bit 8 | RW | | | X |
| Bit 6 | - | 1:1 PLL N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | 1:1 PLL M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | - | 1:1 PLL M Div4 | | RW | | | X |
| Bit 3 | - | 1:1 PLL M Div3 | | RW | | | X |
| Bit 2 | - | 1:1 PLL M Div2 | | RW | | | X |
| Bit 1 | - | 1:1 PLL M Div1 | | RW | | | X |
| Bit 0 | - | 1:1 PLL M Div0 | | RW | | | X |

**SMBus Table: 1:1 PLL Frequency Control Register**

| Byte 18 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | 1:1 PLL N Div7 | N Divider Programming b(7:0) | RW | | | X |
| Bit 6 | - | 1:1 PLL N Div6 | | RW | | | X |
| Bit 5 | - | 1:1 PLL N Div5 | | RW | | | X |
| Bit 4 | - | 1:1 PLL N Div4 | | RW | | | X |
| Bit 3 | - | 1:1 PLL N Div3 | | RW | | | X |
| Bit 2 | - | 1:1 PLL N Div2 | | RW | | | X |
| Bit 1 | - | 1:1 PLL N Div1 | | RW | | | X |
| Bit 0 | - | 1:1 PLL N Div0 | | RW | | | X |

**SMBusTable: 1:1 PLL Output Divider Register (Rev H and higher)**

| Byte 19 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | 1:1 PLL OutDiv 3 | PLL 2 Output Divider | RW | See Output Divider Table | | X |
| Bit 2 | | 1:1 PLL OutDiv 2 | PLL 2 Output Divider | RW | | | X |
| Bit 1 | | 1:1 PLL OutDiv 1 | PLL 2 Output Divider | RW | | | X |
| Bit 0 | | 1:1 PLL OutDiv 0 | PLL 2 Output Divider | RW | | | X |

**SMBusTable: Reserved Register**

| Byte 20 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | RESERVED | | | | | 0 |
| Bit 2 | | RESERVED | | | | | 0 |
| Bit 1 | | RESERVED | | | | | 0 |
| Bit 0 | | RESERVED | | | | | 0 |

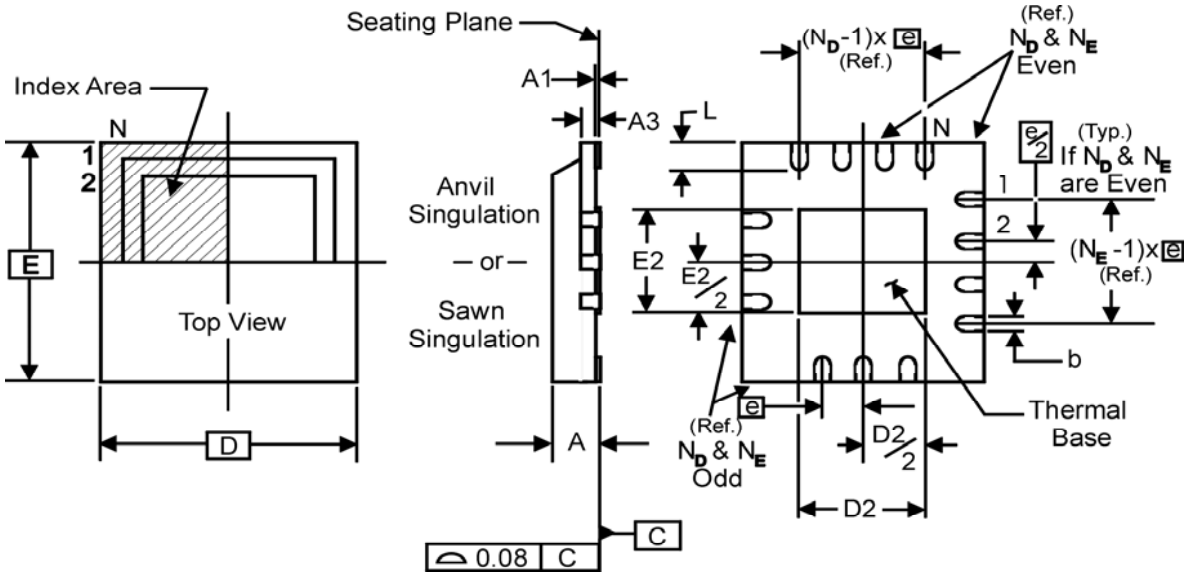
**SMBusTable: Test Byte Register**

| Byte 21 | Test | Test Function | Type | Test Result | PWD |
|---|---|---|---|---|---|
| Bit 7 | ` | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 6 | | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 5 | | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 4 | | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 3 | | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 2 | | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 1 | | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 0 | | ICS ONLY TEST | RW | Reserved | 0 |

**Note: Do NOT write to Bit 21. Erratic device operation will result!**

**Output Divider Table Rev H Devices only**

| Byte 13(3:0) Byte 19(3:0) | Divider Value |
|---|---|
| 0000 | 2 |
| 0001 | 3 |
| 0010 | 5 |
| 0011 | NA |
| 0100 | 4 |
| 0101 | 6 |
| 0110 | 10 |
| 0111 | NA |
| 1000 | 8 |
| 1001 | 12 |
| 1010 | 20 |
| 1011 | NA |
| 1100 | NA |
| 1101 | nA |
| 1110 | NA |
| 1111 | NA |

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**QUAD FLAT / NO LEAD PLASTIC PACKAGE**

DIMENSIONS

| SYMBOL | MIN. | MAX. |
|---|---|---|
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |

DIMENSIONS

| SYMBOL | ICS 72L TOLERANCE |
|---|---|
| N | 72 |
| $N_D$ | 18 |
| $N_E$ | 18 |
| D x E BASIC | 10.00 x 10.00 |
| D2 MIN. / MAX. | 5.75 / 6.15 |
| E2 MIN. / MAX. | 5.75 / 6.15 |
| L MIN. / MAX. | 0.3 / 0.5 |

Reference: JEDEC Publication 95, MO-220

## Ordering Information

**ICS9FG1901yKLF-T**

Example:

**ICS XXXX y K - LF T**

**Designation for tape and reel packaging**
**Lead Free, RoHS Compliant (Optional)**

**Package Type**
K = MLF

**Revision Designator** (will not correlate with datasheet revision)

**Device Type (consists of 3 or 4 digit numbers)**

**Prefix**
ICS, AV = Standard Device

0962E—01/02/07

## Revision History

| Rev. | Issue Date | Description | Page # |
|---|---|---|---|
| A | 4/25/2005 | 1. Added Symbol "A" to Dimensions table.<br>2. Preliminary Release. | 15 |
| B | 12/19/2005 | 1. Rearranged page 1 to enlarge Pin Configuration | 1 |
| C | 6/14/2006 | 1. Updated TBD to actual values.<br>2. Added PLL BW and Peaking Table.<br>3. Updated Skew specs.<br>4. Updated Paddle Dimensions. | Various |
| D | 8/17/2006 | Final Release. | - |
| E | 1/2/2007 | 1. Added Output Dividers to Bytes 13 and 19 for Rev H devices.<br>2. Changed PLL1 and PLL2 naming to 1:1 and Gearing PLL | Various |

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