



**THE DATASHEET OF
74HC2G125DC,125**





74HC2G125; 74HCT2G125

Dual buffer/line driver; 3-state

Rev. 7 — 16 November 2023

Product data sheet

1. General description

The 74HC2G125; 74HCT2G125 are dual buffer/line drivers with 3-state outputs controlled by the output enable inputs (\overline{nOE}). Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC2G125: CMOS level
 - For 74HCT2G125: TTL level
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standard: JESD7A (4.5 V to 5.5 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC2G125DP 74HCT2G125DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC2G125DC 74HCT2G125DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

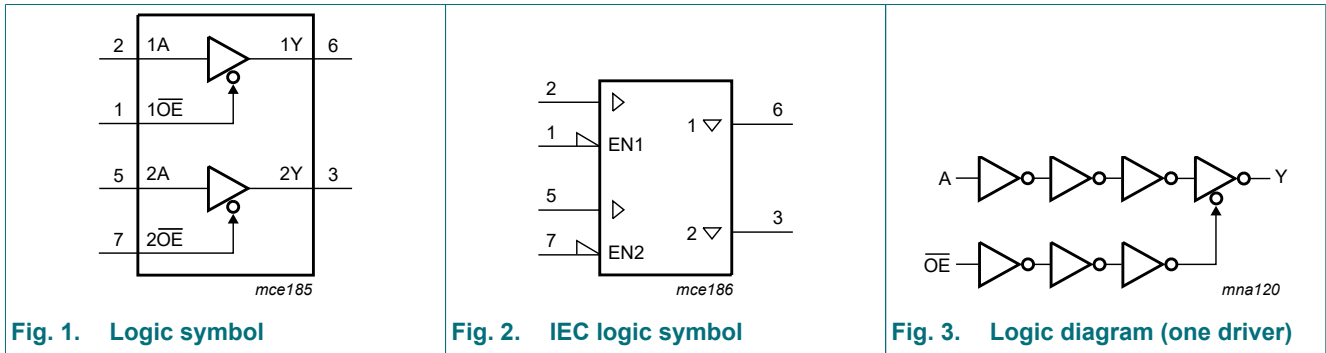
4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74HC2G125DP	H25
74HCT2G125DP	T25
74HC2G125DC	H25
74HCT2G125DC	T25

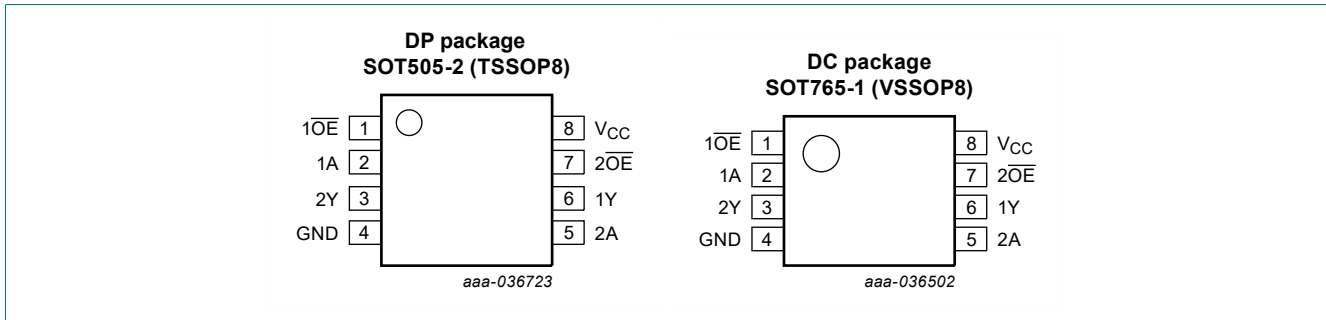
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input (active LOW)
1A, 2A	2, 5	data input
GND	4	ground (0 V)
1Y, 2Y	6, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$ [1]	-	35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G125			74HCT2G125			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$			$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$		Unit
			Min	Typ	Max	Min	Max	
74HC2G125								
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	V

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±5.0	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	μA
C _I	input capacitance		-	1.0	-	-	-	pF
C _O	output capacitance		-	1.5	-	-	-	pF
74HCT2G125								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		I _O = -20 μA	4.4	4.5	-	4.4	-	V
		I _O = -6.0 mA	3.84	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		I _O = 20 μA	-	0	0.1	-	0.1	V
		I _O = 6.0 mA	-	0.16	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±5.0	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	375	-	410	μA
C _I	input capacitance		-	1.0	-	-	-	pF
C _O	output capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
74HC2G125								
t_{pd}	propagation delay	nA to nY; see Fig. 4 [2]						
		$V_{CC} = 2.0$ V	-	35	115	-	135	ns
		$V_{CC} = 4.5$ V	-	11	23	-	27	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	10	-	-	-	ns
		$V_{CC} = 6.0$ V	-	8	20	-	23	ns
t_{en}	enable time	nOE to nY; see Fig. 5 [2]						
		$V_{CC} = 2.0$ V	-	40	115	-	135	ns
		$V_{CC} = 4.5$ V	-	11	23	-	27	ns
		$V_{CC} = 6.0$ V	-	8	20	-	23	ns
t_{dis}	disable time	nOE to nY; see Fig. 5 [2]						
		$V_{CC} = 2.0$ V	-	24	125	-	150	ns
		$V_{CC} = 4.5$ V	-	12	25	-	30	ns
		$V_{CC} = 6.0$ V	-	10	21	-	26	ns
t_t	transition time	see Fig. 4 [2]						
		$V_{CC} = 2.0$ V	-	18	75	-	90	ns
		$V_{CC} = 4.5$ V	-	6	15	-	18	ns
		$V_{CC} = 6.0$ V	-	5	13	-	15	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = \text{GND to } V_{CC}$ [3]						
		output enabled	-	11	-	-	-	pF
		output disabled	-	1	-	-	-	pF
74HCT2G125								
t_{pd}	propagation delay	nA to nY; see Fig. 4 [2]						
		$V_{CC} = 4.5$ V	-	15	31	-	38	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	12	-	-	-	ns
t_{en}	enable time	nOE to nY; see Fig. 5; $V_{CC} = 4.5$ V [2]	-	15	35	-	42	ns
t_{dis}	disable time	nOE to nY; see Fig. 5; $V_{CC} = 4.5$ V [2]	-	15	31	-	38	ns
t_t	transition time	see Fig. 4; $V_{CC} = 4.5$ V [2]	-	6	15	-	18	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = \text{GND to } V_{CC} - 1.5$ V [3]						
		output enabled	-	11	-	-	-	pF
		output disabled	-	1	-	-	-	pF

[1] All typical values are measured at $T_{amb} = 25\text{ °C}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{en} is the same as t_{PZL} and t_{PZH} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_t is the same as t_{THL} and t_{TLH} .

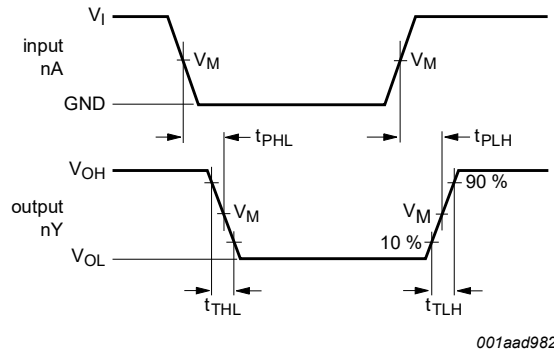
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz;

C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

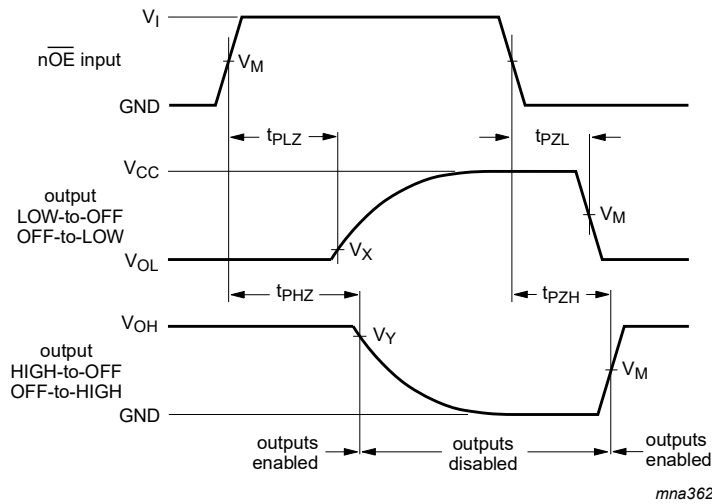
11.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Propagation delays data input (nA) to output (nY)



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC2G125	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
74HCT2G125	1.3 V	1.3 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

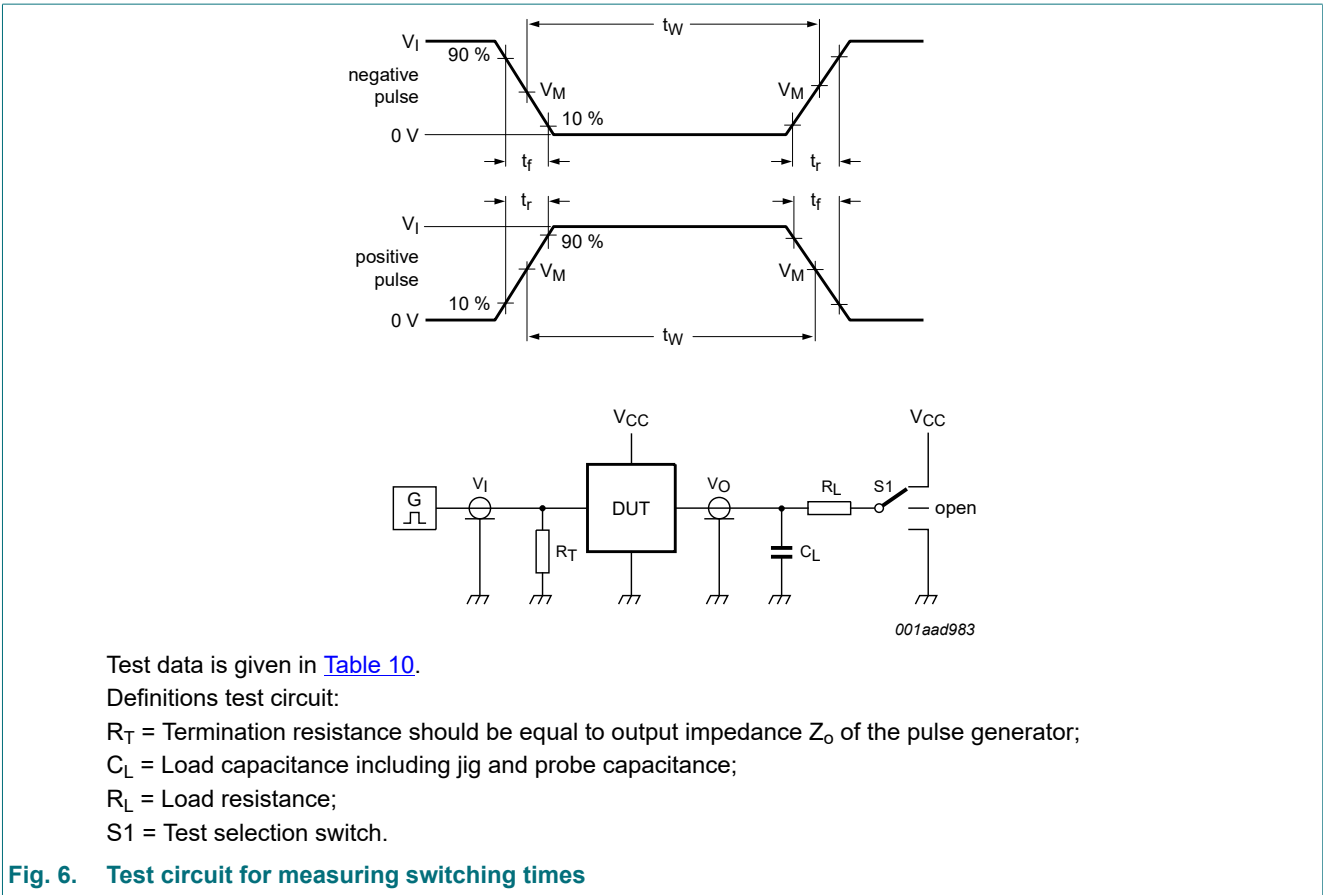


Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC2G125	V_{CC}	≤ 6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT2G125	3 V	≤ 6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

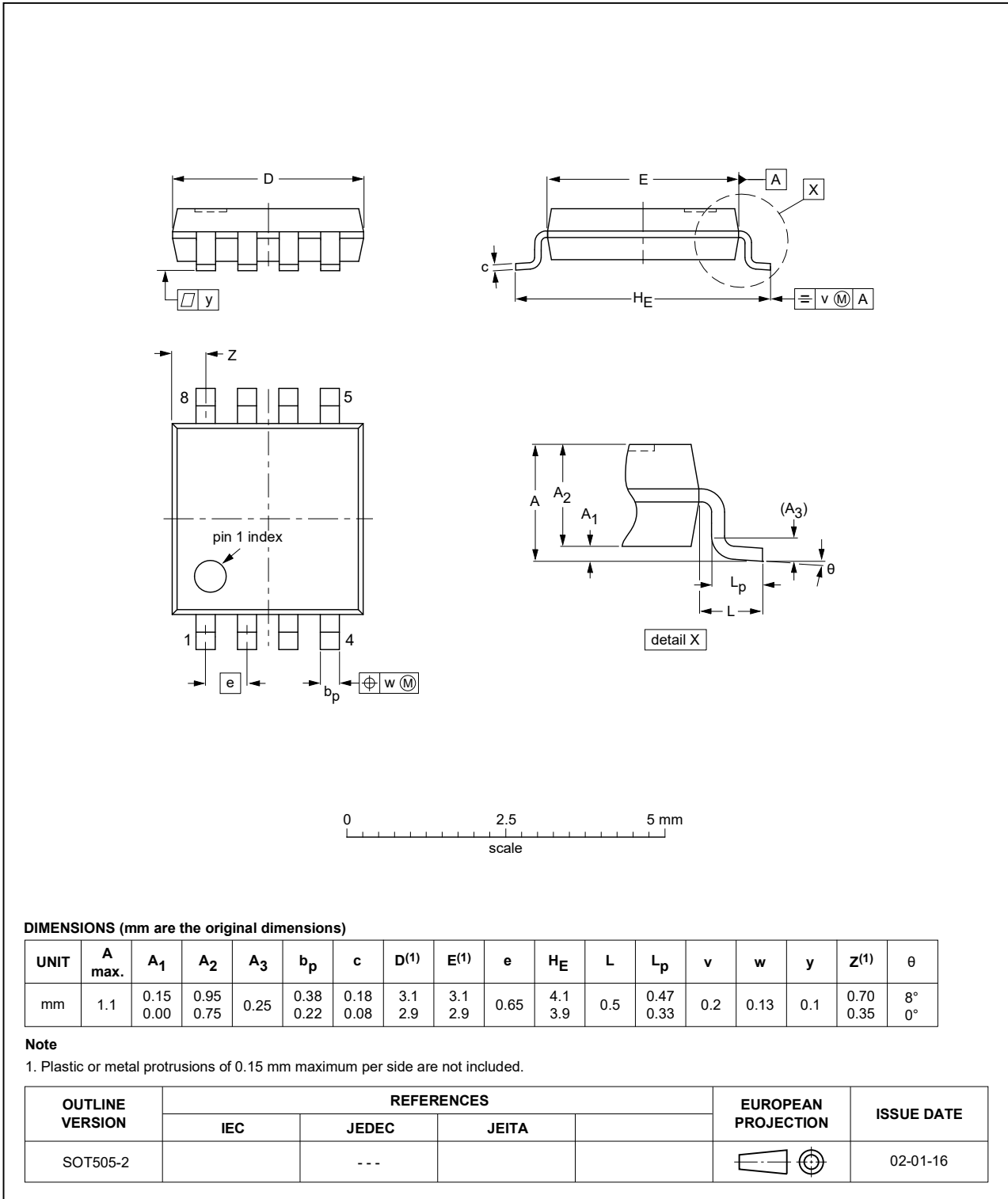


Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G125 v.7	20231116	Product data sheet	-	74HC_HCT2G125 v.6
Modifications:	<ul style="list-style-type: none"> • Section 2 updated. • Section 2: ESD specification updated according to the latest JEDEC standard. • Section 8: P_{tot} and derating values for P_{tot} total power dissipation updated. 			
74HC_HCT2G125 v.6	20181101	Product data sheet	-	74HC_HCT2G125 v.5
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC2G125GD and 74HCT2G125GD (SOT996-2/XSON8) removed. 			
74HC_HCT2G125 v.5	20140317	Product data sheet	-	74HC_HCT2G125 v.4
Modifications:	<ul style="list-style-type: none"> • For type numbers 74HC2G125GD and 74HCT2G125GD XSON8U has changed to XSON8. 			
74HC_HCT2G125 v.4	20080704	Product data sheet	-	74HC_HCT2G125 v.3
74HC_HCT2G125 v.3	20060102	Product data sheet	-	74HC_HCT2G125 v.2
74HC_HCT2G125 v.2	20030303	Product specification	-	74HC_HCT2G125 v.1
74HC_HCT2G125 v.1	20030131	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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