## Overview

This data sheet covers the electrical AC and DC specifications for four temperature grades of devices (part number prefixes MPF050, MPF100, MPF200, MPF300, and MPF500). AC and DC electrical characteristics and parametric values, unless otherwise noted, apply to all temperature grade devices. For example, worst-case STD speed grade applies to all temperature grade devices and –1 speed grade applies to all temperature grade devices except Military. In addition, Low-Power (L) devices are equivalent in performance to STD speed grade devices where offered. Users are expected to close timing using SmartTime for the speed and temperate grade of the device chosen.

**Table 1.** PolarFire Minimum and Maximum Junction Temperatures by Temperature Grade

| Temperature Grade | Minimum Junction Temperature | Maximum Junction Temperature |
|---|---|---|
| Extended Commercial (E) | 0°C | 100°C |
| Industrial (I) | –40°C | 100°C |
| Automotive AECQ-100 (T2) | –40°C | 125°C |
| Military (M) | –55°C | 125°C |

**Table 2.** PolarFire Speed Grade Options by Temperature Grade

| Temperature Grade | Standard Speed Grade | –1 Speed Grade |
|---|---|---|
| Extended Commercial (E) | Available | Available |
| Industrial (I) | Available | Available |
| Automotive T2 (T2) | Available | Available |
| Military (M) | Available | Not Available |

**Table 3.** PolarFire Package Ball Composition by Temperature Grade

| Temperature Grade | Ball Material Composition | Package Decoupling Capacitor Solder Paste (FC484, FC784, FC1152) |
|---|---|---|
| Extended Commercial (E) | RoHS | RoHS |
| Industrial (I) | RoHS | RoHS |
| Automotive T2 (T2) | RoHS | RoHS |
| Military (M) | Lead, Tin | Lead, Tin |

PolarFire device programming functions (programming, verify, and digest check) are only allowed over the Industrial temperature range regardless of the temperature grade of the device selected. Retention characteristics for each temperature range explicitly describe the retention characteristics for that temperature-grade device. You cannot, for example, use the retention characteristics at 110°C and apply them to the Extended Commercial or Industrial devices with a maximum $T_J$ of 100°C. Retention characteristics for Military-grade devices and Automotive-grade devices at the absolute maximum junction temperature of 125°C can be profiled using the PolarFire Retention Calculator, which can be obtained under NDA in the Secure Document Extranet. Refer the Secure Document User Guide.


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# 1. References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PolarFire FPGA Product Overview
- PolarFire® FPGA Production Devices Errata
- ER0217: PolarFire FPGA Pre-Production Device Errata
- PolarFire FPGA Packaging and Pin Descriptions User Guide
- UG0726: PolarFire FPGA Board Design User Guide
- PolarFire Family I/O User Guide
- PolarFire Family Fabric User Guide
- PolarFire Family Programming User Guide
- PolarFire Family Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- PolarFire FPGA and PolarFire SoC FPGA Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- PolarFire Family Power-Up and Resets User Guide
- PolarFire Family Transceiver User Guide
- PolarFire Family PCI Express User Guide
- PolarFire Family FPGA Security User Guide
- PolarFire FPGA and PolarFire SoC FPGA Power Estimator User Guide


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# 2. Device Offering

Refer to section "PolarFire FPGA Device Offerings" in the PolarFire FPGA Product Overview.


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# 3. Silicon and Libero® Tool Status

There are three status levels:

- **Advanced** – Initial estimated information based on simulations.
- **Preliminary** – Information based on simulation and/or initial characterization.
- **Production** – Final production data.

The following tables list the status of the PolarFire FPGA silicon and Libero® Timing and Power tool.

**Table 3-1.** PolarFire FPGA Silicon Status

| Product | Silicon |
|---|---|
| MPF050T, TS, TL, TLS, TC | Production – all temperature grades |
| MPF100T, TS, TL, TLS, TC | Production – all temperature grades |
| MPF200T, TS, TL, TLS, TC | Production – all temperature grades |
| MPF300T, TS, TL, TLS, TC | Production – all temperature grades |
| MPF500T, TS, TL, TLS, TC | Production – all temperature grades |

**Note**: Refer to Device Offering for the list of available part numbers.

**Table 3-2.** PolarFire FPGA Tool Status

| Device | Status | Libero Version | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Timing | | | | Power | | | |
| | | Extended Commercial | | Industrial | | Extended Commercial | | Industrial | |
| | | STD | –1 | STD | –1 | STD | –1 | STD | –1 |
| MPF050T, TS, TL, TLS | Production $V_{DD}$ = 1.0V, 1.05V | 2022.2 | 2022.2 | 2022.2 | 2022.2 | 2022.2 | 2022.2 | 2022.2 | 2022.2 |
| MPF100T, TS, TL, TLS | Production $V_{DD}$ = 1.0V | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 |
| | Production $V_{DD}$ = 1.05V | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 |
| MPF200T, TS, TL, TLS | Production $V_{DD}$ = 1.0V | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 |
| | Production $V_{DD}$ = 1.05V | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 |
| MPF300T, TS, TL, TLS | Production $V_{DD}$ = 1.0V | 12.1 | 12.0 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 | 12.1 |
| | Production $V_{DD}$ = 1.05V | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 |
| MPF500T, TS, TL, TLS | Production $V_{DD}$ = 1.0V | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 |
| | Production $V_{DD}$ = 1.05V | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 | 12.2 |
| MPFxxxTC | Production $V_{DD}$ = 1.0V | 2025.1 | NA | 2025.1 | NA | 2025.1 | NA | 2025.1 | NA |
| | Production $V_{DD}$ = 1.05V | 2025.1 | NA | 2025.1 | NA | 2025.1 | NA | 2025.1 | NA |


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**Table 3-3.** Military

| Device | Status | Minimum Libero Version That Meets the Status Column | |
|---|---|---|---|
| | | Timing | Power |
| | | Military | Military |
| | | STD | STD |
| MPF200TS | Production $V_{DD}$ = 1.0V | 12.5 | 12.5 |
| | Production $V_{DD}$ = 1.05V | 12.5 | 12.5 |
| MPF300TS | Production $V_{DD}$ = 1.0V | 12.3 | 12.3 |
| | Production $V_{DD}$ = 1.05V | 12.5 | 12.5 |
| MPF500TS | Production $V_{DD}$ = 1.0V | 12.5 | 12.5 |
| | Production $V_{DD}$ = 1.05V | 12.5 | 12.5 |

**Table 3-4.** Automotive T2

| Device | Status | Libero Version | | | |
|---|---|---|---|---|---|
| | | Timing | | Power | |
| | | Automotive T2 | | Automotive T2 | |
| | | STD | –1 | STD | –1 |
| MPF050T | Production $V_{DD}$ = 1.0V | 2022.2 | 2022.2 | 2022.2 | 2022.2 |
| | Production $V_{DD}$ = 1.05V | 2022.2 | 2022.2 | 2022.2 | 2022.2 |
| MPF100T | Production $V_{DD}$ = 1.0V | 12.6 | 12.6 | 12.6 | 12.6 |
| | Production $V_{DD}$ = 1.05V | 12.6 | 12.6 | 12.6 | 12.6 |
| MPF200T | Production $V_{DD}$ = 1.0V | 12.6 | 12.6 | 12.6 | 12.6 |
| | Production $V_{DD}$ = 1.05V | 12.6 | 12.6 | 12.6 | 12.6 |
| MPF300T | Production $V_{DD}$ = 1.0V | 12.6 | 12.6 | 12.6 | 12.6 |
| | Production $V_{DD}$ = 1.05V | 12.6 | 12.6 | 12.6 | 12.6 |
| MPF500T | Production $V_{DD}$ = 1.0V | 2025.1 | 2025.1 | 2025.1 | 2025.1 |
| | Production $V_{DD}$ = 1.05V | 2025.1 | 2025.1 | 2025.1 | 2025.1 |
| MPFxxxTC | Production $V_{DD}$ = 1.0V | 2025.1 | NA | 2025.1 | NA |
| | Production $V_{DD}$ = 1.05V | 2025.1 | NA | 2025.1 | NA |


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# 4. DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

## 4.1. Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

**Table 4-1.** Absolute Maximum Rating[3]

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| FPGA core power supply | $V_{DD}$ | –0.5 | 1.13 | V |
| Transceiver Tx and Rx lanes supply | $V_{DDA}$ | –0.5 | 1.13 | V |
| Programming and HSIO receiver supply | $V_{DD18}$ | –0.5 | 2.0 | V |
| FPGA core and FPGA PLL high-voltage supply | $V_{DD25}$ | –0.5 | 2.7 | V |
| Transceiver PLL high-voltage supply | $V_{DDA25}$ | –0.5 | 2.7 | V |
| Transceiver reference clock supply | $V_{DD_XCVR_CLK}$ | –0.5 | 3.6 | V |
| Global $V_{REF}$ for transceiver reference clocks | $XCVR_{VREF}$ | –0.5 | 3.6 | V |
| HSIO DC I/O supply[2] | $V_{DDIx}$ | –0.5 | 2.0 | V |
| GPIO DC I/O supply[2] | $V_{DDIx}$ | –0.5 | 3.6 | V |
| Dedicated I/O DC supply for JTAG and SPI | $V_{DDI3}$ | –0.5 | 3.6 | V |
| GPIO auxiliary power supply for I/O bank x[2] | $V_{DDAUXx}$ | –0.5 | 3.6 | V |
| Maximum DC input voltage on GPIO[4] | $V_{IN}$ | –0.5 | 3.8 | V |
| Maximum DC input voltage on HSIO[4] | $V_{IN}$ | –0.5 | 2.2 | V |
| Transceiver receiver absolute input voltage | Transceiver $V_{IN}$ | –0.5 | 1.41 | V |
| Transceiver reference clock absolute input voltage | Transceiver REFCLK $V_{IN}$ | –0.5 | 3.6 | V |
| Storage temperature (ambient)[1] | $T_{STG}$ | –65 | 150 | °C |
| Junction temperature[1] | $T_J$ | –55 | 135 | °C |
| Maximum soldering temperature RoHS | $T_{SOLROHS}$ | — | 260 | °C |

1. See Table 5-67. FPGA and µPROM Programming Cycles vs. Retention Characteristics for retention time vs. temperature. The total time used in calculating the device retention includes the device operating temperature time and temperature during storage time.
2. The power supplies for a given I/O bank x are shown as $V_{DDIx}$ and $V_{DDAUXx}$.
3. Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 4-2. Recommended Operating Conditions is not implied. Stresses beyond those listed in the following table might cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
4. The absolute maximum $V_{IN}$ limits listed in this table apply to $T_{Jmax}$ = 135°C. For lower recommended operating junction temperatures (100°C and 125°C), refer to Maximum Allowed Overshoot and Undershoot.

## 4.2. Recommended Operating Conditions

The following table lists the recommended operating conditions.


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**Table 4-2.** Recommended Operating Conditions [8,9]

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| FPGA core supply at 1.0V mode[1, 6] | $V_{DD}$ | 0.97 | 1.00 | 1.03 | V | — |
| FPGA core supply at 1.05V mode[1, 6] | $V_{DD}$ | 1.02 | 1.05 | 1.08 | V | — |
| Transceiver Tx and Rx lanes supply (1.0V mode)[6, 7] | $V_{DDA}$ | 0.97 | 1.00 | 1.03 | V | When all lane rates are 10.3125 Gbps or less.[1] |
| Transceiver Tx and Rx lanes supply (1.05V mode)[6] | $V_{DDA}$ | 1.02 | 1.05 | 1.08 | V | Must when any lane rate is greater than 10.3125 Gbps. Lane rates 10.3125 Gbps or less may also be powered in 1.05V mode.[1] |
| Programming and HSIO receiver supply[6] | $V_{DD18}$ | 1.71 | 1.80 | 1.89 | V | — |
| FPGA core and FPGA PLL high-voltage supply[6] | $V_{DD25}$ | 2.425 | 2.50 | 2.575 | V | — |
| Transceiver PLL high-voltage supply[6] | $V_{DDA25}$ | 2.425 | 2.50 | 2.575 | V | — |
| Transceiver reference clock supply[6, 7] | $V_{DD_XCVR_CLK}$ | 3.135 | 3.3 | 3.465 | V | 3.3V nominal |
| | | 2.375 | 2.5 | 2.625 | V | 2.5V nominal |
| Global $V_{REF}$ for transceiver reference clocks[3] | $XCVR_{VREF}$ | Ground | — | $V_{DD_XCVR_CLK}$ | V | — |
| HSIO DC I/O supply[6] | $V_{DDIx}$ | 1.14 | Various | 1.89 | V | Allowed nominal options: 1.2V, 1.35V, 1.5V, and 1.8V[4, 5] |
| | | 1.14 | 1.2 | 1.26 | V | For DDR4 |
| | | 1.425 | 1.5 | 1.575 | V | For DDR3 |
| | | 1.14 | 1.2 | 1.26 | V | For LPDDR3 |
| | | 1.283 | 1.35 | 1.418 | V | For DDR3L |
| GPIO DC I/O supply[6] | $V_{DDIx}$ | 1.14 | Various | 3.465 | V | Allowed nominal options: 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V[2, 4, 5] |
| | | 1.425 | 1.5 | 1.575 | V | For DDR3 |
| Dedicated I/O DC supply for JTAG and SPI (GPIO bank 3)[6] | $V_{DDI3}$ | 1.71 | Various | 3.465 | V | Allowed nominal options: 1.8V, 2.5V, and 3.3V |


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**Table 4-2.** Recommended Operating Conditions [8,9] (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| GPIO auxiliary supply[6] | $V_{DDAUXx}$ | 3.135 | 3.3 | 3.465 | V | For I/O bank x with $V_{DDIx}$ = 3.3V nominal[2, 4, 5] |
| | | 2.375 | 2.5 | 2.625 | V | For I/O bank x with $V_{DDIx}$ = 2.5V nominal or lower[2, 4, 5] |
| Extended commercial temperature range[8] | $T_J$ | 0 | — | 100 | °C | — |
| Industrial temperature range[8] | $T_J$ | –40 | — | 100 | °C | — |
| Automotive T2 temperature range[8] | $T_J$ | –40 | — | 125 | °C | — |
| Military temperature range[8] | $T_J$ | –55 | — | 125 | °C | — |
| Extended commercial programming temperature range[8] | $T_{PRG}$ | 0 | — | 100 | °C | — |
| Industrial programming temperature range[8] | $T_{PRG}$ | –40 | — | 100 | °C | — |

1. $V_{DD}$ and $V_{DDA}$ can independently operate at 1.0V or 1.05V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if $V_{DDIx}$ is 2.5V nominal or 3.3V nominal, $V_{DDAUXx}$ must be connected to the $V_{DDIx}$ supply for that bank. If $V_{DDIx}$ for a given GPIO bank is <2.5V nominal, $V_{DDAUXx}$ per I/O bank must be powered at 2.5V nominal.
3. $XCVR_{VREF}$ globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near $V_{DD_XCVR_CLK}$/2V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as $V_{DDIx}$ and $V_{DDAUXx}$.
5. At power-up and power-down, the $V_{DDIx}$ and $V_{DDAUXx}$ supply sequencing can cause signal glitches. Refer to PolarFire Family User I/O User Guide and UG0726: PolarFire FPGA Board Design User Guide for detailed explanation and recommended steps.
6. The recommended power supply tolerances include DC offset of the supply plus any power supply ripple over the customer design frequencies of interest, as measured at the device package pins. An example for a valid power supply that meets the recommendations for the VDD supply is 1.0V ±10 mV or 1.05V ±10 mV for DC offset with an additional power supply ripple of ±20 mV for a total of 1.0V ±30 mV or 1.05V ±30 mV.
7. Both $V_{DDA}$ and $V_{DD_XCVR_CLK}$ supplies must be powered when any of the transceivers are used. $V_{DD_XCVR_CLK}$ must power on within the XCVR calibration time (as specified for the device in Libero). $V_{DDA}$ and $V_{DD_XCVR_CLK}$ must both then remain powered during operation. If $V_{DDA}$ needs to be powered down, $V_{DD_XCVR_CLK}$ must also be powered down. There is no required sequence for powering up or down $V_{DDA}$ and $V_{DD_XCVR_CLK}$.


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8. This product is designed and validated for operation within the junction temperature (Tj) range specified in the Recommended Operating Conditions in this data sheet. Device functionality and performance outside this recommended operating range are not supported. Customers should account for the temperature difference between ambient (Ta) and junction (Tj) in their thermal environment and specific use case, which may result in a different and typically narrower ambient (Ta) operating temperature range.
9. $V_{DD}$ and other voltage rails must be maintained within the specified operating voltage range throughout device operation. Any voltage ripple or spikes outside the specified operating voltage range could result in timing failures, I/O interface issues, and may trigger user voltage detectors. The power delivery network on the printed circuit board must be designed to meet this operating voltage specification. Refer to the PolarFire FPGA Board Design User Guide for more information.

### 4.2.1. DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

**Table 4-3.** DC Characteristics over Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| Input pin capacitance[1] | $C_{IN}$ (GPIO) Dedicated input pins | — | 5.6 | pf | — |
| | $C_{IN}$ (HSIO) | — | 2.8 | pf | — |
| Input or output leakage current per pin | $I_L$ (GPIO) | — | 10 | µA | I/O disabled, high—Z |
| | $I_L$ (HSIO) | — | 10 | µA | I/O disabled, high—Z |
| Pad pull-up when $V_{IN}$ = 0 | $I_{PU}$[2] | 137 | 220 | µA | $V_{DDIx}$ = 3.3V |
| Pad pull-up when $V_{IN}$ = 0 | | 102 | 166 | µA | $V_{DDIx}$ = 2.5V |
| Pad pull-up when $V_{IN}$ = 0 | | 68 | 115 | µA | $V_{DDIx}$ = 1.8V |
| Pad pull-up when $V_{IN}$ = 0 | | 51 | 88 | µA | $V_{DDIx}$ = 1.5V |
| Pad pull-up when $V_{IN}$ = 0 | | 29 | 73 | µA | $V_{DDIx}$ = 1.35V |
| Pad pull-up when $V_{IN}$ = 0 | | 16 | 46 | µA | $V_{DDIx}$ = 1.2V |
| Pad pull-down when $V_{IN}$ = 3.3V (GPIO only) | $I_{PD}$[3] | 65 | 187 | µA | $V_{DDIx}$ = 3.3V |
| Pad pull-down when $V_{IN}$ = 2.5V (GPIO only) | | 63 | 160 | µA | $V_{DDIx}$ = 2.5V |
| Pad pull-down when $V_{IN}$ = 1.8V | | 60 | 117 | µA | $V_{DDIx}$ = 1.8V |
| Pad pull-down when $V_{IN}$ = 1.5V | | 57 | 95 | µA | $V_{DDIx}$ = 1.5V |
| Pad pull-down when $V_{IN}$ = 1.35V | | 52 | 86 | µA | $V_{DDIx}$ = 1.35V |
| Pad pull-down when $V_{IN}$ = 1.2V | | 47 | 79 | µA | $V_{DDIx}$ = 1.2V |

1. Represents the die input capacitance at the pad (not the package).
2. Weak pullup resistance (RPU) = VDDI/IPU.
3. Weak pulldown resistance (RPD) = VIN/IPD.


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**Table 4-4.** Minimum and Maximum Rise and Fall Times

| Parameter | Symbol | Min | Max | Unit | Maximum Frequency | Condition |
|---|---|---|---|---|---|---|
| Input rise time[1,4]<br>Input fall time[1,4] | $T_{RISE}$<br>$T_{FALL}$ | 200 ps[2,3] | 10% signal period | ps | F ≤ 100 KHz | Min (10% signal period, 1 µs)[5] |
| | | | 12.5% signal period | ps | 100 KHz < F ≤ 400 KHz | Min (12.5% signal period, 300 ns)[6] |
| | | | 20% signal period | ps | 400 KHz < F ≤ 50 MHz | Min (20% signal period, 50 ns)[7] |
| | | | 4 | ns | 50 MHz < F ≤ 125 MHz | Not to exceed 4 ns[8] |
| | | | 50% signal period | ns | 125 MHz < F ≤ 800 MHz | Sawtooth waveform[9] |

1. Voltage ramp must be monotonic. For single-ended I/O standards, input rise time is specified from 10%–90% of $V_{DDIx}$ and input fall time is specified from 90%–10% of $V_{DDIx}$. For voltage referenced and differential I/O configurations, ramp times must always comply with I/O standard requirements to ensure compliance.
2. Input slew rates must be controlled to never exceed PAD overshoot/undershoot requirements. Input pad overshoot and undershoot specifications are shown in section Maximum Allowed Overshoot and Undershoot.
3. Rise and fall times in this table are for unterminated inputs. When inputs are terminated, minimum ramp time is not restricted. Recommended minimum ramp time is 25% of bit period, not to exceed a rate of 5 V/ns.
4. Ramp times must not exceed I/O standard requirements to ensure compliance.
5. For signal frequencies <100 KHz, maximum rise time is 1 µs. For example, if signal frequency (F) is 100 KHz, 10% of signal period is 1 µs. The maximum ramp time allowed is the 1 µs limit. However, if signal frequency is 10 KHz, then 10% of signal period is 10 µs which exceeds the maximum limit of 1 µs. The maximum ramp time allowed is therefore 1 µs.
6. For 100 KHz < signal frequencies ≤ 400 KHz, maximum rise time is 300 ns. For example, if signal frequency is 400 KHz, then 12.5% of signal period is 312.5 ns. The maximum ramp time allowed is 300 ns. If the signal frequency is 200 KHz, then 12.5% of signal period is 625 ns. The maximum ramp time allowed is therefore 300 ns.
7. For 400 KHz < signal frequencies ≤ 50 MHz, maximum rise time is 50 ns or 20% of signal period, whichever is less. For example, if signal frequency is 50 MHz, then 20% of signal period is 4 ns. The maximum ramp time allowed is therefore 4 ns, even if the max limit is 50 ns. If the signal frequency is 1 MHz, then 20% of signal period is 200 ns. The maximum ramp time allowed is therefore 50 ns.
8. For 50 MHz < signal frequencies ≤ 125 MHz, maximum rise time is 4 ns. For example, if signal frequency is 125 MHz, then the maximum ramp time allowed is 4 ns (sawtooth signal). If the signal frequency is 75 MHz, the maximum ramp time allowed at 75 MHz is still 4 ns.
9. For 125 MHz < signal frequencies ≤ 800 MHz, maximum rise time is 50% of signal frequency (sawtooth signal). For example, if signal frequency is 250 MHz, then the maximum ramp time allowed is 2 ns. If the signal frequency is 800 MHz, the maximum ramp time allowed is 0.625 ns.

### 4.2.2. Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage listed as follows. Input currents must be limited to less than 100 mA per latch-up specifications.

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.


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The following tables list the maximum AC input voltage ($V_{IN}$) overshoot duration for HSIO.

**Table 4-5.** Maximum Overshoot During Transitions for HSIO at $T_J$ = 100°C

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100°C | Condition (V) |
|---|---|
| 100 | 1.8 |
| 100 | 1.85 |
| 100 | 1.9 |
| 100 | 1.95 |
| 100 | 2 |
| 100 | 2.05 |
| 100 | 2.1 |
| 100 | 2.15 |
| 100 | 2.2 |
| 90 | 2.25 |
| 30 | 2.3 |
| 7.5 | 2.35 |
| 1.9 | 2.4 |

**Note:** Overshoot level is for $V_{DDI}$ at 1.8V.

**Table 4-6.** Maximum Overshoot During Transitions for HSIO at $T_J$ = 125°C

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 125°C | Condition (V) |
|---|---|
| 100 | 1.8 |
| 100 | 1.85 |
| 100 | 1.9 |
| 100 | 1.95 |
| 100 | 2 |
| 100 | 2.05 |
| 100 | 2.1 |
| 100 | 2.15 |
| 100 | 2.2 |
| 35 | 2.25 |
| 8 | 2.3 |
| 2 | 2.35 |
| 0.5 | 2.4 |

**Note:** Overshoot level is for $V_{DDI}$ at 1.8V.

The following table lists the maximum AC input voltage ($V_{IN}$) undershoot duration for HSIO.

**Table 4-7.** Maximum Undershoot During Transitions for HSIO at $T_J$ = 100°C

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100°C | Condition (V) |
|---|---|
| 100 | –0.05 |
| 100 | –0.1 |
| 100 | –0.15 |
| 100 | –0.2 |


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**Table 4-7.** Maximum Undershoot During Transitions for HSIO at $T_J$ = 100°C (continued)

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100°C | Condition (V) |
|---|---|
| 100 | –0.25 |
| 100 | –0.3 |
| 100 | –0.35 |
| 100 | –0.4 |
| 44 | –0.45 |
| 14 | –0.5 |
| 4.8 | –0.55 |
| 1.6 | –0.6 |

**Table 4-8.** Maximum Undershoot During Transitions for HSIO at $T_J$ = 125°C

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 125°C | Condition (V) |
|---|---|
| 100 | –0.05 |
| 100 | –0.1 |
| 100 | –0.15 |
| 100 | –0.2 |
| 100 | –0.25 |
| 100 | –0.3 |
| 86 | –0.35 |
| 26 | –0.4 |
| 8 | –0.45 |
| 2.6 | –0.5 |
| 0.8 | –0.55 |
| 0.3 | –0.6 |

The following table lists the maximum AC input voltage ($V_{IN}$) overshoot duration for GPIO.

**Table 4-9.** Maximum Overshoot During Transitions for GPIO at $T_J$ = 100°C

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100°C | Condition (V) |
|---|---|
| 100 | 3.8 |
| 100 | 3.85 |
| 100 | 3.9 |
| 100 | 3.95 |
| 70 | 4 |
| 50 | 4.05 |
| 33 | 4.1 |
| 22 | 4.15 |
| 14 | 4.2 |
| 9.8 | 4.25 |
| 6.5 | 4.3 |
| 4.4 | 4.35 |
| 3 | 4.4 |
| 2 | 4.45 |


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**Table 4-9.** Maximum Overshoot During Transitions for GPIO at $T_J$ = 100°C (continued)

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100°C | Condition (V) |
|---|---|
| 1.4 | 4.5 |
| 0.9 | 4.55 |
| 0.6 | 4.6 |

**Note:** Overshoot level is for $V_{DDI}$ at 3.3V.

**Table 4-10.** Maximum Overshoot During Transitions for GPIO at $T_J$ = 125°C

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 125°C | Condition (V) |
|---|---|
| 100 | 3.8 |
| 84 | 3.85 |
| 54 | 3.9 |
| 35 | 3.95 |
| 23 | 4 |
| 15 | 4.05 |
| 10 | 4.1 |
| 6.6 | 4.15 |
| 4.4 | 4.2 |
| 2.9 | 4.25 |
| 1.9 | 4.3 |
| 1.3 | 4.35 |
| 0.9 | 4.4 |
| 0.6 | 4.45 |
| 0.4 | 4.5 |
| 0.28 | 4.55 |
| 0.19 | 4.6 |

**Note:** Overshoot level is $V_{DDI}$ at 3.3V.

The following table lists the maximum AC input voltage ($V_{IN}$) undershoot duration for GPIO.

**Table 4-11.** Maximum Undershoot During Transitions for GPIO at $T_J$ = 100°C

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100°C | Condition (V) |
|---|---|
| 100 | –0.5 |
| 100 | –0.55 |
| 100 | –0.6 |
| 100 | –0.65 |
| 100 | –0.7 |
| 100 | –0.75 |
| 100 | –0.8 |
| 100 | –0.85 |
| 100 | –0.9 |
| 100 | –0.95 |
| 100 | –1 |
| 100 | –1.05 |


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**Table 4-11.** Maximum Undershoot During Transitions for GPIO at $T_J$ = 100°C (continued)

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100°C | Condition (V) |
|---|---|
| 100 | –1.1 |
| 100 | –1.15 |
| 100 | –1.2 |
| 69 | –1.25 |
| 45 | –1.3 |

**Table 4-12.** Maximum Undershoot During Transitions for GPIO at $T_J$ = 125°C

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 125°C | Condition (V) |
|---|---|
| 100 | –0.5 |
| 100 | –0.55 |
| 100 | –0.6 |
| 100 | –0.65 |
| 100 | –0.7 |
| 100 | –0.75 |
| 100 | –0.8 |
| 100 | –0.85 |
| 100 | –0.9 |
| 100 | –0.95 |
| 100 | –1 |
| 100 | –1.05 |
| 78 | –1.1 |
| 50 | –1.15 |
| 32 | –1.2 |
| 20 | –1.25 |
| 13 | –1.3 |

#### 4.2.2.1. Power Supply Ramp Times

The following table lists the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0V to the minimum recommended voltage as specified in the section Recommended Operating Conditions. All supplies must rise and fall monotonically.

**Table 4-13.** Power Supply Ramp Times

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| FPGA core supply | $V_{DD}$ | 0.2 | 50 | ms |
| Transceiver core supply | $V_{DDA}$ | 0.2 | 50 | ms |
| Must connect to 1.8V supply | $V_{DD18}$ | 0.2 | 50 | ms |
| Must connect to 2.5V supply | $V_{DD25}$ | 0.2 | 50 | ms |
| Must connect to 2.5V supply | $V_{DDA25}$ | 0.2 | 50 | ms |
| HSIO bank I/O power supplies | $V_{DDI[0,1,6,7]}$ | 0.2 | 50 | ms |
| GPIO bank I/O power supplies | $V_{DDI[2,4,5]}$ | 0.2 | 50 | ms |
| Bank 3 dedicated I/O buffers (GPIO) | $V_{DDI3}$ | 0.2 | 50 | ms |
| GPIO bank auxiliary power supplies | $V_{DDAUX[2,4,5]}$ | 0.2 | 50 | ms |
| Transceiver reference clock supply | $V_{DD_XCVR_CLK}$ | 0.2 | 50 | ms |
| Global $V_{REF}$ for transceiver reference clocks | $XCVR_{VREF}$ | 0.2 | 50 | ms |


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**Note:** For proper operation of programming recovery mode, if a $V_{DD}$ supply brown-out occurs during programming, a minimum supply ramp down time for only the $V_{DD}$ supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

#### 4.2.2.2. Hot Socketing

The following table lists the hot socketing DC characteristics over recommended operating conditions.

**Table 4-14.** Hot Socketing DC Characteristics over Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Current per transceiver Rx input pin (P or N single-ended)[1, 2] | $I_{XCVRRX_HS}$ | — | — | ±4 | mA | $V_{DDA}$ = 0V |
| Current per transceiver Tx output pin (P or N single-ended)[3] | $I_{XCVRTX_HS}$ | — | — | ±10 | mA | $V_{DDA}$ = 0V |
| Current per transceiver reference clock input pin (P or N single-ended)[4] | $I_{XCVRREF_HS}$ | — | — | ±1 | mA | $V_{DD_XCVR_CLK}$ = 0V |
| Current per GPIO pin (P or N single-ended)[5] | $I_{GPIO_HS}$ | — | — | ±1 | mA | $V_{DDIx}$ = 0V |
| Current per HSIO pin (P or N single-ended) | — | — | — | — | — | Hot socketing is not supported in HSIO. |

1. Assumes device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1V pk–pk) that is toggling at any rate with PRBS7 data.
2. Each P and N transceiver input has less than the specified maximum input current.
3. Each P and N transceiver output is connected to a 40Ω resistor (50Ω CML termination—20% tolerance) to the maximum allowed output voltage ($V_{DDAmax}$ + 0.3V = 1.4V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC-coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
4. $V_{DD_XCVR_CLK}$ is powered down and the device is driven to –0.3V < $V_{IN}$ < $V_{DD_XCVR_CLK}$.
5. $V_{DDIx}$ is powered down and the device is driven to –0.3V < $V_{IN}$ < GPIO $V_{DDImax}$.

**Note:** The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, and DEVRST_N. Weak pull-up (as specified in GPIO) is always enabled.

## 4.3. Input and Output

The following section describes DC I/O levels, differential and complementary differential DC I/O levels, HSIO and GPIO on-die termination specifications, and LVDS specifications.

### 4.3.1. DC Input and Output Levels

The following tables list the DC I/O levels.

**Table 4-15.** DC Input Levels[3]

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$ [1] Max (V) |
|---|---|---|---|---|---|---|---|
| PCI | 3.15 | 3.3 | 3.45 | –0.3 | 0.3 × $V_{DDI}$ | 0.5 × $V_{DDI}$ | 3.45 |
| LVTTL | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS33 | 3.15 | 3.3 | 3.45 | –0.3 | 0.8 | 2 | 3.45 |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 2.625 |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.89 |


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**Table 4-15.** DC Input Levels[3] (continued)

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$ [1] Max (V) |
|---|---|---|---|---|---|---|---|
| LVCMOS15 | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.575 |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{DDI}$ | 0.65 × $V_{DDI}$ | 1.26 |
| SSTL25I[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL25II[2] | 2.375 | 2.5 | 2.625 | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 2.625 |
| SSTL18I[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL18II[2] | 1.71 | 1.8 | 1.89 | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 1.89 |
| SSTL15I | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| SSTL15II | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| SSTL135I | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| SSTL135II | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| HSTL15I | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| HSTL15II | 1.425 | 1.5 | 1.575 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.575 |
| HSTL135I | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| HSTL135II | 1.283 | 1.35 | 1.418 | –0.3 | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | 1.418 |
| HSTL12I | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.26 |
| HSTL12II | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.26 |
| HSUL18I | 1.71 | 1.8 | 1.89 | –0.3 | 0.3 × $V_{DDI}$ | 0.7 × $V_{DDI}$ | 1.89 |
| HSUL18II | 1.71 | 1.8 | 1.89 | –0.3 | 0.3 × $V_{DDI}$ | 0.7 × $V_{DDI}$ | 1.89 |
| HSUL12I | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 1.26 |
| POD12I | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | 1.26 |
| POD12II | 1.14 | 1.2 | 1.26 | –0.3 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | 1.26 |

1. GPIO $V_{IH}$ max is 3.45V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.
2. For external stub-series resistance. This resistance is on-die for GPIO.
3. PolarFire FPGA inputs are designed to support mixing assignment for certain I/O standards, allowing I/O using compatible standards to be placed in the same I/O bank. Refer to the description of the mixed I/O receiver capability in PolarFire® FPGA Family User I/O User Guide.

**Note:** 3.3V and 2.5V are only supported in GPIO banks.

**Table 4-16.** DC Output Levels

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$ [2,6] mA | $I_{OH}$ [2,6] mA |
|---|---|---|---|---|---|---|---|
| PCI[1] | 3.15 | 3.3 | 3.45 | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | 1.5 | 0.5 |
| LVTTL | 3.15 | 3.3 | 3.45 | 0.4 | 2.4 | Refer to Note 2 | |
| LVCMOS33 | 3.15 | 3.3 | 3.45 | 0.4 | $V_{DDI}$ – 0.4 | | |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | 0.4 | $V_{DDI}$ – 0.4 | | |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | 0.45 | $V_{DDI}$ – 0.45 | | |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | 0.25 × $V_{DDI}$ | 0.75 × $V_{DDI}$ | | |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | 0.25 × $V_{DDI}$ | 0.75 × $V_{DDI}$ | | |


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**Table 4-16.** DC Output Levels (continued)

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$ [2,6] mA | $I_{OH}$ [2,6] mA |
|---|---|---|---|---|---|---|---|
| SSTL25I[3] | 2.375 | 2.5 | 2.625 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | 8.1 |
| SSTL25II[3] | 2.375 | 2.5 | 2.625 | $V_{TT}$ – 0.810 | $V_{TT}$ + 0.810 | 16.2 | 16.2 |
| SSTL18I[3] | 1.71 | 1.8 | 1.89 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | 6.7 |
| SSTL18II[3] | 1.71 | 1.8 | 1.89 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 13.4 | 13.4 |
| SSTL15I[4] | 1.425 | 1.5 | 1.575 | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| SSTL15II[4] | 1.425 | 1.5 | 1.575 | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |
| SSTL135I[4] | 1.283 | 1.35 | 1.418 | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| SSTL135II[4] | 1.283 | 1.35 | 1.418 | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |
| HSTL15I | 1.425 | 1.5 | 1.575 | 0.4 | $V_{DDI}$ – 0.4 | 8 | 8 |
| HSTL15II | 1.425 | 1.5 | 1.575 | 0.4 | $V_{DDI}$ – 0.4 | 16 | 16 |
| HSTL135I[4] | 1.283 | 1.35 | 1.418 | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/50 | ($V_{DDI}$ – $V_{OH}$)/50 |
| HSTL135II[4] | 1.283 | 1.35 | 1.418 | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}$/25 | ($V_{DDI}$ – $V_{OH}$)/25 |
| HSTL12I[4] | 1.14 | 1.2 | 1.26 | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/50 | ($V_{DDI}$ – $V_{OH}$)/50 |
| HSTL12II[4] | 1.14 | 1.2 | 1.26 | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/25 | ($V_{DDI}$ – $V_{OH}$)/25 |
| HSUL18I[4] | 1.71 | 1.8 | 1.89 | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/55 | ($V_{DDI}$ – $V_{OH}$)/55 |
| HSUL18II[4] | 1.71 | 1.8 | 1.89 | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/25 | ($V_{DDI}$ – $V_{OH}$)/25 |
| HSUL12I[4] | 1.14 | 1.2 | 1.26 | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}$/40 | ($V_{DDI}$ – $V_{OH}$)/40 |
| POD12I[4,5] | 1.14 | 1.2 | 1.26 | 0.5 × $V_{DDI}$ | — | $V_{OL}$/48 | ($V_{DDI}$ – $V_{OH}$)/48 |
| POD12II[4,5] | 1.14 | 1.2 | 1.26 | 0.5 × $V_{DDI}$ | — | $V_{OL}$/34 | ($V_{DDI}$ – $V_{OH}$)/34 |

1. Drive strengths per PCI specification V/I curves.
2. Refer to PolarFire Family I/O User Guide for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. $I_{OL}/I_{OH}$ units for impedance standards in amps (not mA).
5. $V_{OH_MAX}$ based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all I/Os within a lane is limited as follows:
   a. HSIO lane: 120 mA per 12 I/O buffers.
   b. GPIO lane: 160 mA per 12 I/O buffers.

**Note:** 3.3V and 2.5V are only supported in GPIO banks.

### 4.3.2. Differential DC Input and Output Levels

The following tables list the differential DC I/O levels.

**Table 4-17.** Differential DC Input Levels

| I/O Standard | Bank Type | $V_{ICM_RANGE}$ Libero Setting | $V_{ICM}$ [1,3] Min (V) | $V_{ICM}$ [1,3] Typ (V) | $V_{ICM}$ [1,3] Max (V) | $V_{ID}$ [2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| LVDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS25 [7] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |


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**Table 4-17.** Differential DC Input Levels (continued)

| I/O Standard | Bank Type | $V_{ICM_RANGE}$ Libero Setting | $V_{ICM}$ [1,3] Min (V) | $V_{ICM}$ [1,3] Typ (V) | $V_{ICM}$ [1,3] Max (V) | $V_{ID}$ [2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| LVDS18G[4] | GPIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS18 [7] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS18 | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| RSDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| MINILVDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| SUBLVDS33 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS18[5] | HSIO | Mid (default) | 0.6 | 0.9 | 1.65 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| PPDS25 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| PPDS18[5] | HSIO | Mid (default) | 0.6 | 0.8 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| SLVS33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |
| SLVS25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |


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**Table 4-17.** Differential DC Input Levels (continued)

| I/O Standard | Bank Type | $V_{ICM_RANGE}$ Libero Setting | $V_{ICM}$ [1,3] Min (V) | $V_{ICM}$ [1,3] Typ (V) | $V_{ICM}$ [1,3] Max (V) | $V_{ID}$ [2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| SLVS18[5] | HSIO | Mid (default) | 0.6 | 1.00 | 1.65 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.3 |
| HCSL33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |
| HCSL25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |
| HCSL18[5] | HSIO | Mid (default) | 0.6 | 1.0 | 1.65 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.55 | 1.1 |
| BUSLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.1 | $V_{DDIn}$ |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.1 | $V_{DDIn}$ |
| MLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.35 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.35 | 2.4 |
| LVPECL33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| LVPECLE33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| MIPI25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.05 | 0.2 | 0.3 |

1. $V_{ICM}$ is the input Common mode.
2. $V_{ID}$ is the input differential voltage.
3. $V_{ICM}$ rules are as follows:
   a. GPIO $V_{ICM}$ must be less than $V_{DDI}$ – 0.4V;
   b. HSIO $V_{ICM}$ must be less than $V_{DDI}$ – 0.24V;
   c. $V_{ICM} + V_{ID}/2$ must be $<V_{DDI} + 0.4V$;
   d. $V_{ICM} - V_{ID}/2$ must be >VSS – 0.3V;
   e. Any differential input with $V_{ICM}$ ≤0.6 V requires the low Common mode setting in Libero ($V_{ICM_RANGE}$ = Low).
4. $V_{DDI}$ = 1.8V, $V_{DDAUX}$ = 2.5V.
5. HSIO receiver only.
6. GPIO receiver only.
7. LVDS25 (GPIO), LVDS18G (GPIO), and LVDS18 (HSIO) configurations should be used in conjunction with I/O CDR when implementing SGMII receivers.

**Table 4-18.** Differential DC Output Levels

| I/O Standard | Bank Type | $V_{OCM}$ [1] Min (V) | $V_{OCM}$ Typ (V) | $V_{OCM}$ Max (V) | $V_{OD}$ [2] Min (V) | $V_{OD}$ [2] Typ (V) | $V_{OD}$ [2] Max (V) |
|---|---|---|---|---|---|---|---|
| LVDS33 | GPIO | 1.125 | 1.2 | 1.375 | 0.25 | 0.35 | 0.45 |
| LVDS25 [4] | GPIO | 1.125 | 1.2 | 1.375 | 0.25 | 0.35 | 0.45 |
| LVDS18G[4] | GPIO | 1.125 | 1.2 | 1.375 | 0.25 | 0.35 | 0.45 |


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**Table 4-18.** Differential DC Output Levels (continued)

| I/O Standard | Bank Type | $V_{OCM}$ [1] Min (V) | $V_{OCM}$ Typ (V) | $V_{OCM}$ Max (V) | $V_{OD}$ [2] Min (V) | $V_{OD}$ [2] Typ (V) | $V_{OD}$ [2] Max (V) |
|---|---|---|---|---|---|---|---|
| LCMDS33 | GPIO | 0.45 | 0.6 | 0.7 | 0.25 | 0.35 | 0.45 |
| LCMDS25 | GPIO | 0.45 | 0.6 | 0.7 | 0.25 | 0.35 | 0.45 |
| RSDS33 | GPIO | 1.125 | 1.2 | 1.375 | 0.17 | 0.2 | 0.23 |
| RSDS25 | GPIO | 1.125 | 1.2 | 1.375 | 0.17 | 0.2 | 0.23 |
| MINILVDS33 | GPIO | 1.125 | 1.2 | 2.375 | 0.3 | 0.4 | 0.6 |
| MINILVDS25 | GPIO | 1.125 | 1.2 | 2.375 | 0.3 | 0.4 | 0.6 |
| SUBLVDS33 | GPIO | 0.8 | 0.9 | 1.0 | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | 0.8 | 0.9 | 1.0 | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | 0.05 | 0.8 | 1.4 | 0.17 | 0.2 | 0.23 |
| PPDS25 | GPIO | 0.05 | 0.8 | 1.4 | 0.17 | 0.2 | 0.23 |
| SLVSE15[3] | GPIO, HSIO | 0.1 | 0.2 | 0.3 | 0.12 | 0.135 | 0.15 |
| BUSLVDSE25[3] | GPIO | 1.15 | 1.25 | 1.31 | 0.24 | 0.262 | 0.272 |
| MLVDSE25[3] | GPIO | 1.15 | 1.25 | 1.31 | 0.396 | 0.442 | 0.453 |
| LVPECLE33[3] | GPIO | 1.51 | 1.65 | 1.74 | 0.664 | 0.722 | 0.755 |
| MIPIE25 [3] | GPIO | 0.15 | 0.2 | 0.25 | 0.14 | 0.2 | 0.27 |

1. $V_{OCM}$ is the output Common mode voltage.
2. $V_{OD}$ is the output differential voltage.
3. Emulated output only, using external resistors.
4. LVDS25 and LVDS18G configuration should be used when implementing SGMII transmitters.

### 4.3.3. Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

**Table 4-19.** Complementary Differential DC Input Levels

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{ICM}$ [1,3] Min (V) | $V_{ICM}$ [1,3] Typ (V) | $V_{ICM}$ [1,3] Max (V) | $V_{ID}$ [2] Min (V) | $V_{ID^2}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| SSTL25I | 2.375 | 2.5 | 2.625 | 1.164 | 1.250 | 1.339 | 0.1 | $V_{DDAUX}$ (GPIO) |
| SSTL25II | 2.375 | 2.5 | 2.625 | 1.164 | 1.250 | 1.339 | 0.1 | $V_{DDAUX}$ (GPIO) |
| SSTL18I | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL18II | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL15I | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL15II | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL135I | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |
| SSTL135II | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |
| HSTL15I | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| HSTL15II | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| HSTL135I | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |
| HSTL135II | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |


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**Table 4-19.** Complementary Differential DC Input Levels (continued)

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{ICM}$ [1,3] Min (V) | $V_{ICM}$ [1,3] Typ (V) | $V_{ICM}$ [1,3] Max (V) | $V_{ID}$ [2] Min (V) | $V_{ID}$[2] Max (V) |
|---|---|---|---|---|---|---|---|---|
| HSTL12I | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 | $V_{DDI}$ (HSIO) |
| HSTL12II | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 | $V_{DDI}$ (HSIO) |
| HSUL18I | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDI}$ (HSIO) |
| HSUL18II | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDI}$ (HSIO) |
| HSUL12I | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 | $V_{DDI}$ (HSIO) |
| POD12I | 1.14 | 1.2 | 1.26 | 0.787 | 0.840 | 0.895 | 0.1 | $V_{DDI}$ (HSIO) |
| POD12II | 1.14 | 1.2 | 1.26 | 0.787 | 0.840 | 0.895 | 0.1 | $V_{DDI}$ (HSIO) |

1. $V_{ICM}$ is the input Common mode voltage.
2. $V_{ID}$ is the input differential voltage.
3. $V_{ICM}$ rules are as follows:
   a. $V_{ICM}$ must be less than $V_{DDI}$ – 0.4V;
   b. $V_{ICM} + V_{ID}/2$ must be $<V_{DDI} + 0.4V$;
   c. $V_{ICM} – V_{ID}/2$ must be >VSS – 0.3V.

**Table 4-20.** Complementary Differential DC Output Levels

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Min (V) | $V_{OL}$ Max (V) | $V_{OH}$ [1,3] Min (V) | $I_{OL}$ [2] Min (mA) | $I_{OH}$ [2] Min (mA) |
|---|---|---|---|---|---|---|---|---|
| SSTL25I | 2.375 | 2.5 | 2.625 | — | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | 8.1 |
| SSTL25II | 2.375 | 2.5 | 2.625 | — | $V_{TT}$ – 0.810 | $V_{TT}$ + 0.810 | 16.2 | 16.2 |
| SSTL18I | 1.71 | 1.8 | 1.89 | — | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | 6.7 |
| SSTL18II | 1.71 | 1.8 | 1.89 | — | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 13.4 | 13.4 |
| SSTL15I[4] | 1.425 | 1.5 | 1.575 | — | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} – V_{OH})/40$ |
| SSTL15II[4] | 1.425 | 1.5 | 1.575 | — | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}/34$ | $(V_{DDI} – V_{OH})/34$ |
| SSTL135I[4] | 1.283 | 1.35 | 1.418 | — | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} – V_{OH})/40$ |
| SSTL135II[4] | 1.283 | 1.35 | 1.418 | — | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}/34$ | $(V_{DDI} – V_{OH})/34$ |
| HSTL15I | 1.425 | 1.5 | 1.575 | — | 0.4 | $V_{DDI}$ – 0.4 | 8 | 8 |
| HSTL15II | 1.425 | 1.5 | 1.575 | — | 0.4 | $V_{DDI}$ – 0.4 | 16 | 16 |
| HSTL135I[4] | 1.283 | 1.35 | 1.418 | — | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}/50$ | $(V_{DDI} – V_{OH})/50$ |
| HSTL135II[4] | 1.283 | 1.35 | 1.418 | — | 0.2 × $V_{DDI}$ | 0.8 × $V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} – V_{OH})/25$ |
| HSTL12I[4] | 1.14 | 1.2 | 1.26 | — | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}/50$ | $(V_{DDI} – V_{OH})/50$ |
| HSTL12II[4] | 1.14 | 1.2 | 1.26 | — | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} – V_{OH})/25$ |
| HSUL18I[4] | 1.71 | 1.8 | 1.89 | — | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}/55$ | $(V_{DDI} – V_{OH})/55$ |
| HSUL18II[4] | 1.71 | 1.8 | 1.89 | — | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} – V_{OH})/25$ |
| HSUL12I[4] | 1.14 | 1.2 | 1.26 | — | 0.1 × $V_{DDI}$ | 0.9 × $V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} – V_{OH})/40$ |
| POD12I[3,4] | 1.14 | 1.2 | 1.26 | — | 0.5 × $V_{DDI}$ | — | $V_{OL}/48$ | $(V_{DDI} – V_{OH})/48$ |
| POD12II[3,4] | 1.14 | 1.2 | 1.26 | — | 0.5 × $V_{DDI}$ | — | $V_{OL}/34$ | $(V_{DDI} – V_{OH})/34$ |

1. $V_{OH}$ is the single-ended high-output voltage.
2. The total DC sink/source current of all I/Os within a lane is limited as follows:


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a. HSIO lane: 120 mA per 12 I/O buffers.
b. GPIO lane: 160 mA per 12 I/O buffers.

3. $V_{OH_MAX}$ is based on external pull-up termination (pseudo-open drain).
4. $I_{OL}/I_{OH}$ units for impedance standards are in amps (not mA).

### 4.3.4. HSIO On-Die Termination

The following tables list the on-die termination calibration accuracy specifications for the HSIO bank.

**Table 4-21.** Single-Ended (Internal Parallel) Thevenin Termination

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8V/1.5V/1.35V/1.2V |
| –40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8V |
| –40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8V |
| –20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5V/1.35V |
| –20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5V/1.35V |
| –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5V/1.35V |
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5V/1.35V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5V/1.35V |
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2V |

**Note:** Thevenin impedance is calculated based on independent P and N as measured at 50% of $V_{DDI}$. For 50Ω/75Ω/150Ω cases, the nearest supported values of 40Ω/60Ω/120Ω are used.

**Table 4-22.** Single-Ended (Internal Parallel) Termination to $V_{DDI}$

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 34 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 48 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 80 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2V |

**Note:** Measured at 80% of $V_{DDI}$.

**Table 4-23.** Single-Ended (Internal Parallel) Termination to $V_{SS}$

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.8V/1.5V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.8V/1.5V |
| –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2V |
| –20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2V |

**Note:** Measured at 50% of $V_{DDI}$.


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### 4.3.5. GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for the GPIO bank.

**Table 4-24.** On-Die Termination Calibration Accuracy Specifications for GPIO Bank

| Parameter | Description | Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential termination[1] | Internal differential termination | –20 | 100 | 20 | Ω | $V_{ICM}$ < 0.8V[6] |
| | | –20 | 100 | 40 | Ω | 0.6V < $V_{ICM}$ < 1.65V[6] |
| | | –20 | 100 | 80 | Ω | 1.4V < $V_{ICM}$ [6] |
| Single-ended Thevenin termination[2, 3] | Internal parallel Thevenin termination | –40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8V/1.5V |
| | | –40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8V |
| | | –40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8V |
| | | –20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5V |
| | | –20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5V |
| | | –20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5V |
| | | –20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5V |
| | | –20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5V |
| Single-ended termination to $V_{SS}$[4, 5] | Internal parallel termination to $V_{SS}$ | –20 | 120 | 20 | Ω | $V_{DDI}$ = 2.5V/1.8V/1.5V/1.2V |
| | | –20 | 240 | 20 | Ω | $V_{DDI}$ = 2.5V/1.8V/1.5V/1.2V |

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of $V_{DDI}$.
3. For 50Ω/75Ω/150Ω cases, the nearest supported values of 40Ω/60Ω/120Ω are used.
4. Measured at 50% of $V_{DDI}$.
5. Supported terminations vary with the I/O type regardless of $V_{DDI}$ nominal voltage. Refer to Libero for available combinations and default settings.
6. When $V_{ICM}$ complies with more than one range, use the maximum percentage tolerance of the two ranges.

### 4.3.6. I/O Hysteresis

The following table lists the I/O input hysteresis characteristics for HSIO and GPIO over recommended operating conditions.

**Table 4-25.** Input Hysteresis Characteristics over Recommended Operating Conditions

| Bank Type | I/O Standard | Hysteresis (min) | Units |
|---|---|---|---|
| GPIO | LVCMOS33 | 180 | mV |
| GPIO | LVCMOS25 | 135 | mV |
| HSIO | LVCMOS18 | 50 | mV |
| HSIO | LVCMOS15 | 50 | mV |


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# 5. AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire FPGA device.

## 5.1. I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

### 5.1.1. Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP

The following table provides information about the methodology for input delay measurement.

**Table 5-1.** Input Delay Measurement Methodology

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3, 4] | $V_{REF}$[1, 5] | Unit |
|---|---|---|---|---|---|---|---|---|
| PCI | PCIE 3.3V | 0 | $V_{DDI}$ | — | — | $V_{DDI}/2$ | — | V |
| LVTTL | LVTTL 3.3V | 0 | $V_{DDI}$ | — | — | $V_{DDI}/2$ | — | V |
| LVCMOS33 | LVCMOS 3.3V | 0 | $V_{DDI}$ | — | — | $V_{DDI}/2$ | — | V |
| LVCMOS25 | LVCMOS 2.5V | 0 | $V_{DDI}$ | — | — | $V_{DDI}/2$ | — | V |
| LVCMOS18 | LVCMOS 1.8V | 0 | $V_{DDI}$ | — | — | $V_{DDI}/2$ | — | V |
| LVCMOS15 | LVCMOS 1.5V | 0 | $V_{DDI}$ | — | — | $V_{DDI}/2$ | — | V |
| LVCMOS12 | LVCMOS 1.2V | 0 | $V_{DDI}$ | — | — | $V_{DDI}/2$ | — | V |
| SSTL25I | SSTL 2.5V Class I | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | — | — | $V_{REF}$ | 1.25 | V |
| SSTL25II | SSTL 2.5V Class II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | — | — | $V_{REF}$ | 1.25 | V |
| SSTL18I | SSTL 1.8V Class I | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | — | — | $V_{REF}$ | 0.90 | V |
| SSTL18II | SSTL 1.8V Class II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | — | — | $V_{REF}$ | 0.90 | V |
| SSTL15I | SSTL 1.5V Class I | $V_{REF}$ – .175 | $V_{REF}$ + .175 | — | — | $V_{REF}$ | 0.75 | V |
| SSTL15II | SSTL 1.5V Class II | $V_{REF}$ – .175 | $V_{REF}$ + .175 | — | — | $V_{REF}$ | 0.75 | V |
| SSTL135I | SSTL 1.35V Class I | $V_{REF}$ – .16 | $V_{REF}$ + .16 | — | — | $V_{REF}$ | 0.675 | V |
| SSTL135II | SSTL 1.35V Class II | $V_{REF}$ – .16 | $V_{REF}$ + .16 | — | — | $V_{REF}$ | 0.675 | V |
| HSTL15I | HSTL 1.5V Class I | $V_{REF}$ – .5 | $V_{REF}$ + .5 | — | — | $V_{REF}$ | 0.75 | V |
| HSTL15II | HSTL 1.5V Class II | $V_{REF}$ – .5 | $V_{REF}$ + .5 | — | — | $V_{REF}$ | 0.75 | V |
| HSTL135I | HSTL 1.35V Class I | $V_{REF}$ – .45 | $V_{REF}$ + .45 | — | — | $V_{REF}$ | 0.675 | V |
| HSTL135II | HSTL 1.35V Class II | $V_{REF}$ – .45 | $V_{REF}$ + .45 | — | — | $V_{REF}$ | 0.675 | V |
| HSTL12I | HSTL 1.2V Class I | $V_{REF}$ – .4 | $V_{REF}$ + .4 | — | — | $V_{REF}$ | 0.60 | V |
| HSTL12II | HSTL 1.2V Class II | $V_{REF}$ – .4 | $V_{REF}$ + .4 | — | — | $V_{REF}$ | 0.60 | V |
| HSUL18I | HSUL 1.8V Class I | $V_{REF}$ – .54 | $V_{REF}$ + .54 | — | — | $V_{REF}$ | 0.90 | V |
| HSUL18II | HSUL 1.8V Class II | $V_{REF}$ – .54 | $V_{REF}$ + 0.54 | — | — | $V_{REF}$ | 0.90 | V |
| HSUL12I | HSUL 1.2V | $V_{REF}$ – .22 | $V_{REF}$ + .22 | — | — | $V_{REF}$ | 0.60 | V |
| POD12I | Pseudo-Open Drain (POD) logic 1.2V Class I | $V_{REF}$ – .15 | $V_{REF}$ + .15 | — | — | $V_{REF}$ | 0.84 | V |
| POD12II | POD 1.2V Class II | $V_{REF}$ – .15 | $V_{REF}$ + .15 | — | — | $V_{REF}$ | 0.84 | V |
| LVDS33 | Low-Voltage Differential Signaling (LVDS) 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| LVDS25 | LVDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| LVDS18 | LVDS 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |


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**Table 5-1.** Input Delay Measurement Methodology (continued)

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3, 4] | $V_{REF}$[1, 5] | Unit |
|---|---|---|---|---|---|---|---|---|
| LCMDS33 | Low-Common mode differential signaling (LCMDS) 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| LCMDS25 | LCMDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| LCMDS18 | LCMDS 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| RSDS33 | RSDS 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| RSDS25 | RSDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| RSDS18 | RSDS 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| MINILVDS33 | Mini-LVDS 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| MINILVDS25 | Mini-LVDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| MINILVDS18 | Mini-LVDS 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| SUBLVDS33 | Sub-LVDS 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | — | V |
| SUBLVDS25 | Sub-LVDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | — | V |
| SUBLVDS18 | Sub-LVDS 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | — | V |
| PPDS33 | Point-to-point differential signaling 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | — | V |
| PPDS25 | PPDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | — | V |
| PPDS18 | PPDS 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | — | V |
| SLVS33 | Scalable low-voltage signaling 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.200 | 0 | — | V |
| SLVS25 | SLVS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.200 | 0 | — | V |
| SLVS18 | SLVS 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.200 | 0 | — | V |
| HCSL33 | High-speed current steering logic (HCSL) 3.3V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.350 | 0 | — | V |
| HCSL25 | HCSL 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.350 | 0 | — | V |
| HCSL18 | HCSL 1.8V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.350 | 0 | — | V |
| BLVDSE25[6] | Bus LVDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| MLVDSE25[6] | Multipoint LVDS 2.5V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| LVPECL33 | Low-voltage positive emitter coupled logic | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.650 | 0 | — | V |
| LVPECLE33[6] | Low-voltage positive emitter coupled logic | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.650 | 0 | — | V |
| SSTL25I | Differential SSTL 2.5V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| SSTL25II | Differential SSTL 2.5V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | — | V |
| SSTL18I | Differential SSTL 1.8V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | — | V |
| SSTL18II | Differential SSTL 1.8V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | — | V |
| SSTL15I | Differential SSTL 1.5V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.750 | 0 | — | V |
| SSTL15II | Differential SSTL 1.5V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.750 | 0 | — | V |
| SSTL135I | Differential SSTL 1.35V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.675 | 0 | — | V |
| SSTL135II | Differential SSTL 1.35V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.675 | 0 | — | V |
| HSTL15I | Differential HSTL 1.5V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.750 | 0 | — | V |
| HSTL15II | Differential HSTL 1.5V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.750 | 0 | — | V |
| HSTL135I | Differential HSTL 1.35V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.675 | 0 | — | V |
| HSTL135II | Differential HSTL 1.35V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.675 | 0 | — | V |
| HSTL12I | Differential HSTL 1.2V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.600 | 0 | — | V |


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**Table 5-1.** Input Delay Measurement Methodology (continued)

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3, 4] | $V_{REF}$[1, 5] | Unit |
|---|---|---|---|---|---|---|---|---|
| HSTL12II | Differential HSTL 1.2V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.600 | 0 | — | V |
| HSUL18I | Differential HSUL 1.8V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | — | V |
| HSUL18II | Differential HSUL 1.8V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | — | V |
| HSUL12I | Differential HSUL 1.2V | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.600 | 0 | — | V |
| POD12I | Differential POD 1.2V Class I | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.840 | 0 | — | V |
| POD12II | Differential POD 1.2V Class II | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.840 | 0 | — | V |
| MIPI25 | Mobile Industry Processor Interface | $V_{ICM}$ – .125 | $V_{ICM}$ + .125 | 0.250 | 0.200 | 0 | — | V |

1. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst-case of these measurements. $V_{REF}$ values listed are typical. Input waveform switches between $V_{IL}$ and $V_{IH}$. All rise and fall rates must be 1V/ns for non-mixed mode input buffers as one-third the minimum period for mixed-mode input buffers.
2. Differential receiver standards all use 250 mV $V_{ID}$ for timing. $V_{ICM}$ is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the $V_{REF}$/$V_{MEAS}$ parameters found in IBIS models or shown in the Figure 5-1. Output Delay Measurement—Single-Ended Test Setup.
6. Emulated bidirectional interface.

### 5.1.2. Output Delay Measurement Methodology

The following section provides information about the methodology for output delay measurement.

**Table 5-2.** Output Delay Measurement Methodology

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| PCI | PCIE 3.3V | 25 | 10 | 1.65 | — |
| LVTTL | LVTTL 3.3V | 1M | 0 | 1.65 | — |
| LVCMOS33 | LVCMOS 3.3V | 1M | 0 | 1.65 | — |
| LVCMOS25 | LVCMOS 2.5V | 1M | 0 | 1.25 | — |
| LVCMOS18 | LVCMOS 1.8V | 1M | 0 | 0.90 | — |
| LVCMOS15 | LVCMOS 1.5V | 1M | 0 | 0.75 | — |
| LVCMOS12 | LVCMOS 1.2V | 1M | 0 | 0.60 | — |
| SSTL25I | Stub-series terminated logic 2.5V Class I | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL25II | SSTL 2.5V Class II | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL18I | SSTL 1.8V Class I | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL18II | SSTL 1.8V Class II | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL15I | SSTL 1.5V Class I | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL15II | SSTL 1.5V Class II | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL135I | SSTL 1.35V Class I | 50 | 0 | $V_{REF}$ | 0.675 |
| SSTL135II | SSTL 1.35V Class II | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL15I | High-Speed Transceiver Logic (HSTL) 1.5V Class I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL15II | HSTL 1.5V Class II | 50 | 0 | $V_{REF}$ | 0.75 |


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**Table 5-2.** Output Delay Measurement Methodology (continued)

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| HSTL135I | HSTL 1.35V Class I | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL135II | HSTL 1.35V Class II | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL12I | HSTL 1.2V Class I | 50 | 0 | $V_{REF}$ | 0.6 |
| HSTL12II | HSTL 1.2V Class II | 50 | 0 | $V_{REF}$ | 0.6 |
| HSUL18I | High-speed unterminated logic 1.8V Class I | 50 | 0 | $V_{REF}$ | 0.9 |
| HSUL18II | HSUL 1.8V Class II | 50 | 0 | $V_{REF}$ | 0.9 |
| HSUL12I | HSUL 1.2V Class I | 50 | 0 | $V_{REF}$ | 0.6 |
| POD12I | Pseudo-Open Drain (POD) logic 1.2V Class I | 50 | 0 | $V_{REF}$ | 0.84 |
| POD12II | POD 1.2V Class II | 50 | 0 | $V_{REF}$ | 0.84 |
| LVDS33 | LVDS 3.3V | 100 | 0 | 0[1] | 0 |
| LVDS25 | LVDS 2.5V | 100 | 0 | 0[1] | 0 |
| LCMDS33 | Low-Common Mode Differential Signaling (LCMDS) 3.3V | 100 | 0 | 0[1] | 0 |
| LCMDS25 | LCMDS 2.5V | 100 | 0 | 0 | 0 |
| RSDS33 | Reduced swing differential signaling 3.3V | 100 | 0 | 0[1] | 0 |
| RSDS25 | RSDS 2.5V | 100 | 0 | 0[1] | 0 |
| MINILVDS33 | Mini-LVDS 3.3V | 100 | 0 | 0[1] | 0 |
| MINILVDS25 | Mini-LVDS 2.5V | 100 | 0 | 0[1] | 0 |
| SUBLVDS33 | Sub-LVDS 3.3V | 100 | 0 | 0[1] | 0 |
| SUBLVDS25 | Sub-LVDS 2.5V | 100 | 0 | 0[1] | 0 |
| PPDS33 | Point-to-point differential signaling 3.3V | 100 | 0 | 0[1] | 0 |
| PPDS25 | PPDS 2.5V | 100 | 0 | 0[1] | 0 |
| SLVS33 | Scalable low-voltage signaling 3.3V | 100 | 0 | 0[1] | 0 |
| SLVS25 | SLVS 2.5V | 100 | 0 | 0[1] | 0 |
| SLVSE15 | SLVS 1.5V | 100 | 0 | 0[1] | 0 |
| HCSL33 | High-speed current steering logic 3.3V | 100 | 0 | 0[1] | 0 |
| HCSL25 | HCSL 2.5V | 100 | 0 | 0[1] | 0 |
| BUSLVDSE25 | Bus LVDS | 100 | 0 | 0[1] | 0 |
| MLVDSE25 | Multipoint LVDS 2.5V | 100 | 0 | 0[1] | 0 |
| LVPECLE33 | Low-voltage positive emitter-coupled logic | 100 | 0 | 0[1] | 0 |
| MIPIE25 | Mobile industry processor interface 2.5V | 100 | 0 | 0[1] | 0 |
| SSTL25I | Differential SSTL 2.5V Class I | 50 | 0 | 0[1] | 0 |
| SSTL25II | Differential SSTL 2.5V Class II | 50 | 0 | 0[1] | 0 |
| SSTL18I | Differential SSTL 1.8V Class I | 50 | 0 | 0[1] | 0 |
| SSTL18II | Differential SSTL 1.8V Class II | 50 | 0 | 0[1] | 0 |
| SSTL15I | Differential SSTL 1.5V Class I | 50 | 0 | 0[1] | 0 |
| SSTL15II | Differential SSTL 1.5V Class II | 50 | 0 | 0[1] | 0 |
| SSTL135I | Differential SSTL 1.35V Class I | 50 | 0 | 0[1] | 0 |
| SSTL135II | Differential SSTL 1.35V Class II | 50 | 0 | 0[1] | 0 |
| HSTL15I | Differential HSTL 1.5V Class I | 50 | 0 | 0[1] | 0 |


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**Table 5-2.** Output Delay Measurement Methodology (continued)

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| HSTL15II | Differential HSTL 1.5V Class II | 50 | 0 | 0[1] | 0 |
| HSTL135I | Differential HSTL 1.35V Class I | 50 | 0 | 0[1] | 0 |
| HSTL135II | Differential HSTL 1.35V Class II | 50 | 0 | 0[1] | 0 |
| HSTL12I | Differential HSTL 1.2V Class I | 50 | 0 | 0[1] | 0 |
| HSTL12II | Differential HSTL 1.2V Class II | 50 | 0 | 0[1] | 0 |
| HSUL18I | Differential HSUL 1.8V Class I | 50 | 0 | 0[1] | 0 |
| HSUL18II | Differential HSUL 1.8V Class II | 50 | 0 | 0[1] | 0 |
| HSUL12I | Differential HSUL 1.2V Class I | 50 | 0 | 0[1] | 0 |
| POD12I | Differential POD 1.2V Class II | 50 | 0 | 0[1] | 0 |
| POD12II | Differential POD 1.2V Class II | 50 | 0 | 0[1] | 0 |

1. The value given is the differential output voltage.

**Figure 5-1.** Output Delay Measurement—Single-Ended Test Setup

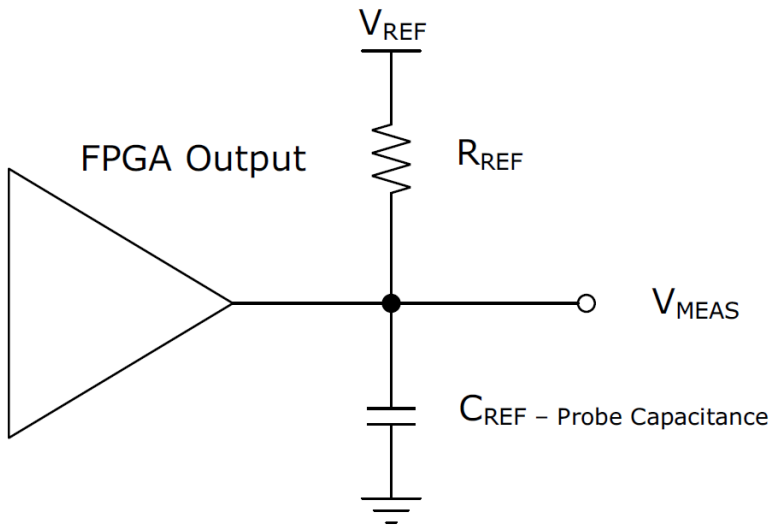
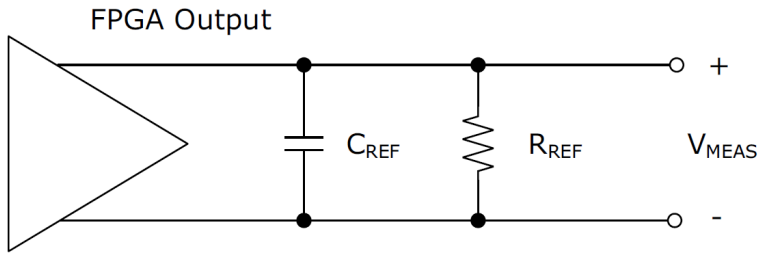



**Figure 5-2.** Output Delay Measurement—Differential Test Setup




### 5.1.3. Input Buffer Speed

The following tables describe input buffer speed.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.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–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-3.** HSIO Maximum Input Buffer Speed

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVDS18 | 1250 | 1250 | Mbps |
| LCMDS18 | 1250 | 1250 | Mbps |
| HCSL18 | 800 | 800 | Mbps |
| RSDS18 | 800 | 800 | Mbps |
| MINILVDS18 | 800 | 800 | Mbps |
| SUBLVDS18 | 900 | 900 | Mbps |
| PPDS18 | 800 | 800 | Mbps |
| SLVS18 | 1200 | 1200 | Mbps |
| SSTL18I | 800 | 1066 | Mbps |
| SSTL18II | 800 | 1066 | Mbps |
| SSTL15I | 1066 | 1333 | Mbps |
| SSTL15II | 1066 | 1333 | Mbps |
| SSTL135I | 1066 | 1333 | Mbps |
| SSTL135II | 1066 | 1333 | Mbps |
| HSTL15I | 900 | 1100 | Mbps |
| HSTL15II | 900 | 1100 | Mbps |
| HSTL135I | 1066 | 1066 | Mbps |
| HSTL135II | 1066 | 1066 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL12I | 1066 | 1333 | Mbps |
| HSTL12I | 1066 | 1266 | Mbps |
| HSTL12II | 1066 | 1266 | Mbps |
| POD12I | 1333 | 1600 | Mbps |
| POD12II | 1333 | 1600 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |
| LVCMOS12 (8 mA) | 300 | 300 | Mbps |

**Notes:**

- Performance is achieved with $V_{ID}$ ≥200 mV.
- LVDS18 configuration should be used in conjunction with I/O CDR when implementing SGMII receivers.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.


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**Table 5-4.** GPIO Maximum Input Buffer Speed[1, 2, 4]

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVDS18G/LVDS25/LVDS33/LCMDS25/LCMDS33 | 1250 | 1600 | Mbps |
| RSDS25/RSDS33 | 800 | 800 | Mbps |
| MINILVDS25/MINILVDS33 | 800 | 800 | Mbps |
| SUBLVDS25/SUBLVDS33 | 800 | 800 | Mbps |
| PPDS25/PPDS33 | 800 | 800 | Mbps |
| SLVS25/SLVS33 | 1200 | 1200 | Mbps |
| SLVSE15 | 800 | 800 | Mbps |
| HCSL25/HCSL33 | 800 | 800 | Mbps |
| BUSLVDSE25 | 800 | 800 | Mbps |
| MLVDSE25 | 800 | 800 | Mbps |
| LVPECL33 | 800 | 800 | Mbps |
| SSTL25I | 800 | 800 | Mbps |
| SSTL25II | 800 | 800 | Mbps |
| SSTL18I | 800 | 800 | Mbps |
| SSTL18II | 800 | 800 | Mbps |
| SSTL15I | 800 | 1066 | Mbps |
| SSTL15II | 800 | 1066 | Mbps |
| HSTL15I | 800 | 900 | Mbps |
| HSTL15II | 800 | 900 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| PCI | 500 | 500 | Mbps |
| LVTTL | 500 | 500 | Mbps |
| LVCMOS33 | 500 | 500 | Mbps |
| LVCMOS25 | 500 | 500 | Mbps |
| LVCMOS18 | 500 | 500 | Mbps |
| LVCMOS15 | 500 | 500 | Mbps |
| LVCMOS12 | 300 | 300 | Mbps |
| MIPI25[3] | 1000 | 1500 | Mbps |

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with $V_{ID}$ ≥200 mV.
3. $V_{ID}$ ≥ 200 mV, $V_{ICM}$ ≥100 mV, $T_j$= 0.4 UI.
4. LVDS25 configuration should be used in conjunction with I/O CDR when implementing SGMII receivers.

### 5.1.4. Output Buffer Speed

The following tables describe output buffer speed.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.


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–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-5.** HSIO Maximum Output Buffer Speed

| Standard | STD | –1 | Unit |
|---|---|---|---|
| SSTL18I | 800 | 1066 | Mbps |
| SSTL18II | 800 | 1066 | Mbps |
| SSTL18I (differential) | 800 | 1066 | Mbps |
| SSTL18II (differential) | 800 | 1066 | Mbps |
| SSTL15I | 1066 | 1333 | Mbps |
| SSTL15II | 1066 | 1333 | Mbps |
| SSTL15I (differential) | 1066 | 1333 | Mbps |
| SSTL15II (differential) | 1066 | 1333 | Mbps |
| SSTL135I | 1066 | 1333 | Mbps |
| SSTL135II | 1066 | 1333 | Mbps |
| SSTL135I (differential) | 1066 | 1333 | Mbps |
| SSTL135II (differential) | 1066 | 1333 | Mbps |
| HSTL15I | 900 | 1100 | Mbps |
| HSTL15II | 900 | 1100 | Mbps |
| HSTL15I (differential) | 900 | 1100 | Mbps |
| HSTL15II (differential) | 900 | 1100 | Mbps |
| HSTL135I | 1066 | 1066 | Mbps |
| HSTL135II | 1066 | 1066 | Mbps |
| HSTL135I (differential) | 1066 | 1066 | Mbps |
| HSTL135II (differential) | 1066 | 1066 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL18I (differential) | 400 | 400 | Mbps |
| HSUL18II (differential) | 400 | 400 | Mbps |
| HSUL12I | 1066 | 1333 | Mbps |
| HSUL12I (differential) | 1066 | 1333 | Mbps |
| HSTL12I | 1066 | 1266 | Mbps |
| HSTL12II | 1066 | 1266 | Mbps |
| HSTL12I (differential) | 1066 | 1266 | Mbps |
| HSTL12II (differential) | 1066 | 1266 | Mbps |
| POD12I | 1333 | 1600 | Mbps |
| POD12II | 1333 | 1600 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |
| LVCMOS12 (8 mA) | 250 | 300 | Mbps |

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.


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–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-6.** GPIO Maximum Output Buffer Speed

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVDS18G | 1250 | 1250 | Mbps |
| LVDS25/LCMDS25 | 1250 | 1250 | Mbps |
| LVDS33/LCMDS33 | 1250 | 1600 | Mbps |
| RSDS25 | 800 | 800 | Mbps |
| MINILVDS25 | 800 | 800 | Mbps |
| SUBLVDS25 | 800 | 800 | Mbps |
| PPDS25 | 800 | 800 | Mbps |
| SLVSE15 | 500 | 500 | Mbps |
| BUSLVDSE25 | 500 | 500 | Mbps |
| MLVDSE25 | 500 | 500 | Mbps |
| LVPECLE33 | 500 | 500 | Mbps |
| SSTL25I | 800 | 800 | Mbps |
| SSTL25II | 800 | 800 | Mbps |
| SSTL25I (differential) | 800 | 800 | Mbps |
| SSTL25II (differential) | 800 | 800 | Mbps |
| SSTL18I | 800 | 800 | Mbps |
| SSTL18II | 800 | 800 | Mbps |
| SSTL18I (differential) | 800 | 800 | Mbps |
| SSTL18II (differential) | 800 | 800 | Mbps |
| SSTL15I | 800 | 1066 | Mbps |
| SSTL15II | 800 | 1066 | Mbps |
| SSTL15I (differential) | 800 | 1066 | Mbps |
| SSTL15II (differential) | 800 | 1066 | Mbps |
| HSTL15I | 900 | 900 | Mbps |
| HSTL15II | 900 | 900 | Mbps |
| HSTL15I (differential) | 900 | 900 | Mbps |
| HSTL15II (differential) | 900 | 900 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL18I (differential) | 400 | 400 | Mbps |
| HSUL18II (differential) | 400 | 400 | Mbps |
| PCI | 500 | 500 | Mbps |
| LVTTL (20 mA) | 500 | 500 | Mbps |
| LVCMOS33 (20 mA) | 500 | 500 | Mbps |
| LVCMOS25 (16 mA) | 500 | 500 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |


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**Table 5-6.** GPIO Maximum Output Buffer Speed (continued)

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVCMOS12 (8 mA) | 250 | 300 | Mbps |
| MIPIE25 | 1000 | 1000 | Mbps |

**Note:** LVDS25 configuration should be used when implementing SGMII transmitters.

### 5.1.5. Maximum PHY Rate for Memory Interface IP

The following tables describe the maximum PHY rate for memory interface IP.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-7.** Maximum PHY Rate for Memory Interfaces IP for HSIO Banks

| Memory Standard | Gearing Ratio | $V_{DDAUX}$ | $V_{DDI}$ | STD (Mbps) Min | STD (Mbps) Max | –1 (Mbps) Min | –1 (Mbps) Max | Fabric Clock STD Min (MHz) | Fabric Clock STD Max (MHz) | Fabric Clock –1 Min (MHz) | Fabric Clock –1 Max (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR4 | 8:1 | 1.8V | 1.2V | 800 | 1333 | 800 | 1600 | 100 | 167 | 100 | 200 |
| DDR3 | 8:1 | 1.8V | 1.5V | 800 | 1067 | 800 | 1333 | 100 | 133 | 100 | 167 |
| DDR3L | 8:1 | 1.8V | 1.35V | 800 | 1067 | 800 | 1333 | 100 | 133 | 100 | 167 |
| LPDDR3 | 8:1 | 1.8V | 1.2V | 800 | 800 | 800 | 1333 | 100 | 100 | 100 | 167 |
| QDRII+ | 8:1 | 1.8V | 1.5V | 500 | 900 | 500 | 1100 | 62.5 | 112.5 | 62.5 | 137.5 |
| RLDRAM3[1] | 8:1 | 1.8V | 1.35V | — | 1067 | — | 1067 | — | 133 | — | 133 |
| RLDRAM3[1] | 4:1 | 1.8V | 1.35V | — | 667 | — | 800 | — | 167 | — | 200 |
| RLDRAM3[1] | 2:1 | 1.8V | 1.35V | — | 333 | — | 400 | — | 167 | — | 200 |
| RLDRAMII[1] | 8:1 | 1.8V | 1.8V | — | 800 | — | 1067 | — | 100 | — | 133 |
| RLDRAMII[1] | 4:1 | 1.8V | 1.8V | — | 667 | — | 800 | — | 167 | — | 200 |
| RLDRAMII[1] | 2:1 | 1.8V | 1.8V | — | 333 | — | 400 | — | 167 | — | 200 |

1. Simulation data only. Microchip does not provide a soft controller for RLDRAMII and RLDRAM3.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-8.** Maximum PHY Rate for Memory Interfaces IP for GPIO Banks

| Memory Standard | Gearing Ratio | $V_{DDAUX}$ | $V_{DDI}$ | STD (Mbps) Min | STD (Mbps) Max | –1 (Mbps) Min | –1 (Mbps) Max | Fabric Clock STD Min (MHz) | Fabric Clock STD Max (MHz) | Fabric Clock –1 Min (MHz) | Fabric Clock –1 Max (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR3 | 8:1 | 2.5V | 1.5V | 800 | 800 | 800 | 1067 | 100 | 100 | 100 | 133 |


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**Table 5-8.** Maximum PHY Rate for Memory Interfaces IP for GPIO Banks (continued)

| Memory Standard | Gearing Ratio | $V_{DDAUX}$ | $V_{DDI}$ | STD (Mbps) Min | STD (Mbps) Max | –1 (Mbps) Min | –1 (Mbps) Max | Fabric Clock STD Min (MHz) | Fabric Clock STD Max (MHz) | Fabric Clock –1 Min (MHz) | Fabric Clock –1 Max (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| QDRII+ | 8:1 | 2.5V | 1.5V | 500 | 900 | 500 | 900 | 62.5 | 112.5 | 62.5 | 112.5 |
| RLDRAMII[1] | 4:1 | 2.5V | 1.8V | — | 800 | — | 800 | — | 200 | — | 200 |
| RLDRAMII[1] | 2:1 | 2.5V | 1.8V | — | 400 | — | 400 | — | 200 | — | 200 |

1. Simulation data only. RLDRAMII is currently not supported with a soft IP controller.

## 5.1.6. User I/O Switching Characteristics

The following section describes user I/O switching characteristics. The following interface names are described in the PolarFire Family I/O User Guide.

### 5.1.6.1. I/O Digital

The following tables describe I/O digital.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-9.** I/O Digital Receive Single-Data Rate Switching Characteristics[1]

| Parameter | Interface Name | Topology | I/O Type | STD (MHz) | –1 (MHz) | STD (Mbps) | –1 (Mbps) | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|
| Input $F_{MAX}$ | RX_SDR_G_A | Rx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, aligned |
| Input $F_{MAX}$ | RX_SDR_R_A | Rx SDR | HSIO, GPIO | 250 | 250 | 250 | 250 | From a regional clock source, aligned |
| Input $F_{MAX}$ | RX_SDR_G_C | Rx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, centered |
| Input $F_{MAX}$ | RX_SDR_R_C | Rx SDR | HSIO, GPIO | 250 | 250 | 250 | 250 | From a regional clock source, centered |

1. Unless otherwise noted, all data rates listed are achieved with static IOD tap settings.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-10.** I/O Digital Receive Double Data Rate Switching Characteristics[1,2]

| Parameter | Interface Name | Topology | I/O Type | STD (MHz) | –1 (MHz) | STD (Mbps) | –1 (Mbps) | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|
| Input $F_{MAX}$ | RX_DDR_G_A | Rx DDR | HSIO | 335 | 345 | 670 | 690 | From a global clock source, aligned |
| | | | GPIO | 310 | 325 | 620 | 650 | |
| Input $F_{MAX}$ | RX_DDR_R_A | Rx DDR | HSIO | 250 | 250 | 500 | 500 | From a regional clock source, aligned |
| | | | GPIO | 250 | 250 | 500 | 500 | |


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**Table 5-10.** I/O Digital Receive Double Data Rate Switching Characteristics[1,2] (continued)

| Parameter | Interface Name | Topology | I/O Type | STD (MHz) | –1 (MHz) | STD (Mbps) | –1 (Mbps) | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|
| Input $F_{MAX}$ | RX_DDR_G_C | Rx DDR | HSIO | 335 | 345 | 670 | 690 | From a global clock source, centered |
| | | | GPIO | 310 | 325 | 620 | 650 | |
| Input $F_{MAX}$ | RX_DDR_R_C | Rx DDR | HSIO | 250 | 250 | 500 | 500 | From a regional clock source, centered |
| | | | GPIO | 250 | 250 | 500 | 500 | |
| Input $F_{MAX}$ 2:1 | RX_DDRX_B_G_A | Rx DDR Digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, aligned, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |
| Input $F_{MAX}$ 4:1 | RX_DDRX_B_G_A | Rx DDR Digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, aligned, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |
| Input $F_{MAX}$ 3.5:1 | RX_DDRX_B_G_FA | Rx DDR Digital mode for fractional | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, aligned, global fabric clock, fractional input |
| | | | GPIO | 320 | 320 | 640 | 640 | |
| Input $F_{MAX}$ 2:1 | RX_DDRX_B_G_C | Rx DDR Digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, centered, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |
| Input $F_{MAX}$ 4:1<br>Input $F_{MAX}$ 5:1 | RX_DDRX_B_G_C | Rx DDR Digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, centered, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |
| Input $F_{MAX}$ 4:1 | RX_DDRX_B_G_DYN_MIPI[3] | Rx DDR Digital mode for MIPI | GPIO | 500[4] | 750[4] | 1000[4] | 1500[4] | From a HS_IO_CLK clock source, centered, global fabric clock |
| Input $F_{MAX}$ 2:1 | RX_DDRX_B_R_A | Rx DDR Digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, aligned, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |
| Input $F_{MAX}$ 4:1<br>Input $F_{MAX}$ 5:1 | RX_DDRX_B_R_A | Rx DDR Digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, aligned, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |
| Input $F_{MAX}$ 2:1 | RX_DDRX_B_R_C | Rx DDR Digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, centered, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |
| Input $F_{MAX}$ 4:1<br>Input $F_{MAX}$ 5:1 | RX_DDRX_B_R_C | Rx DDR Digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, centered, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |

1. A centered clock-to-data interface can be created with a negedge launch of the data.
2. Unless otherwise noted, all data rates listed are achieved with static IOD tap settings.
3. Data rates listed are achieved using dynamic training.


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4. $V_{ID} \geq 200$ mV, $V_{ICM} \geq 100$ mV, $T_j = 0.4$ UI.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-11.** I/O Digital Transmit Single Data Rate Switching Characteristics[2]

| Parameter | Interface Name | Topology | I/O Type | STD (MHz) | –1 (MHz) | STD (Mbps) | –1 (Mbps) | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|
| Output $F_{MAX}$ | TX_SDR_G_A | Tx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, aligned[1] |
| | TX_SDR_G_C | Tx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, centered[1] |

1. A centered clock-to-data interface can be created with a negedge launch of the data.
2. Unless otherwise noted, all data rates listed are achieved with static IOD tap settings.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-12.** I/O Digital Transmit Double Data Rate Switching Characteristics

| Parameter | Interface Name | Topology | I/O Type | STD (MHz) | –1 (MHz) | STD (Mbps) | –1 (Mbps) | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|
| Output $F_{MAX}$ | TX_DDR_G_A | Tx DDR | HSIO, GPIO | 500 | 500 | 1000 | 1000 | From a global clock source, aligned |
| | TX_DDR_G_C | Tx DDR | HSIO, GPIO | 500 | 500 | 1000 | 1000 | From a global clock source, centered |
| Output $F_{MAX}$ 2:1 | TX_DDRX_B_A | Tx DDR digital mode | HSIO | 400 | 500 | 800 | 1000 | From a HS_IO_CLK clock source, aligned |
| Output $F_{MAX}$ 4:1<br>Output $F_{MAX}$ 5:1 | TX_DDRX_B_A | Tx DDR digital mode | HSIO | 667 | 800 | 1333 | 1600 | From a HS_IO_CLK clock source, aligned |
| Output $F_{MAX}$ 2:1 | TX_DDRX_B_C | Tx DDR digital mode | HSIO | 400 | 500 | 800 | 1000 | From a HS_IO_CLK clock source, centered with PLL |
| Output $F_{MAX}$ 4:1<br>Output $F_{MAX}$ 5:1 | TX_DDRX_B_C | Tx DDR digital mode | HSIO | 667 | 800 | 1333 | 1600 | From a HS_IO_CLK clock source, centered with PLL |
| Output $F_{MAX}$ 2:1 | TX_DDRX_B_A | Tx DDR digital mode | GPIO | 400 | 500 | 800 | 1000 | From a HS_IO_CLK clock source, aligned |
| Output $F_{MAX}$ 4:1<br>Output $F_{MAX}$ 5:1 | TX_DDRX_B_A | Tx DDR digital mode | GPIO | 625 | 800 | 1250 | 1600 | From a HS_IO_CLK clock source, aligned |
| Output $F_{MAX}$ 2:1 | TX_DDRX_B_C | Tx DDR digital mode | GPIO | 400 | 500 | 800 | 1000 | From a HS_IO_CLK clock source, centered with PLL |
| Output $F_{MAX}$ 4:1<br>Output $F_{MAX}$ 5:1 | TX_DDRX_B_C | Tx DDR digital mode | GPIO | 625 | 800 | 1250 | 1600 | From a HS_IO_CLK clock source, centered with PLL |


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**Table 5-12.** I/O Digital Transmit Double Data Rate Switching Characteristics (continued)

| Parameter | Interface Name | Topology | I/O Type | STD (MHz) | –1 (MHz) | STD (Mbps) | –1 (Mbps) | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|
| Output $F_{MAX}$ 4:1 | TX_DDRX_B_C_MIPI | Tx DDR digital mode for MIPI | GPIO | 500 | 500 | 1000 | 1000 | From a HS_IO_CLK clock source, centered with PLL |

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-13.** Programmable Delay

| Parameter | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit |
|---|---|---|---|---|---|---|---|
| In delay, out delay, DLL delay, PLL delay step sizes | 12.7 | 30 | 35 | 12.7 | 25 | 29.5 | ps |

**Note:** Refer to Libero timing reports for configuration-specific intrinsic and incremental delays.

**Figure 5-3.** LVDS Jitter Tolerance Plot

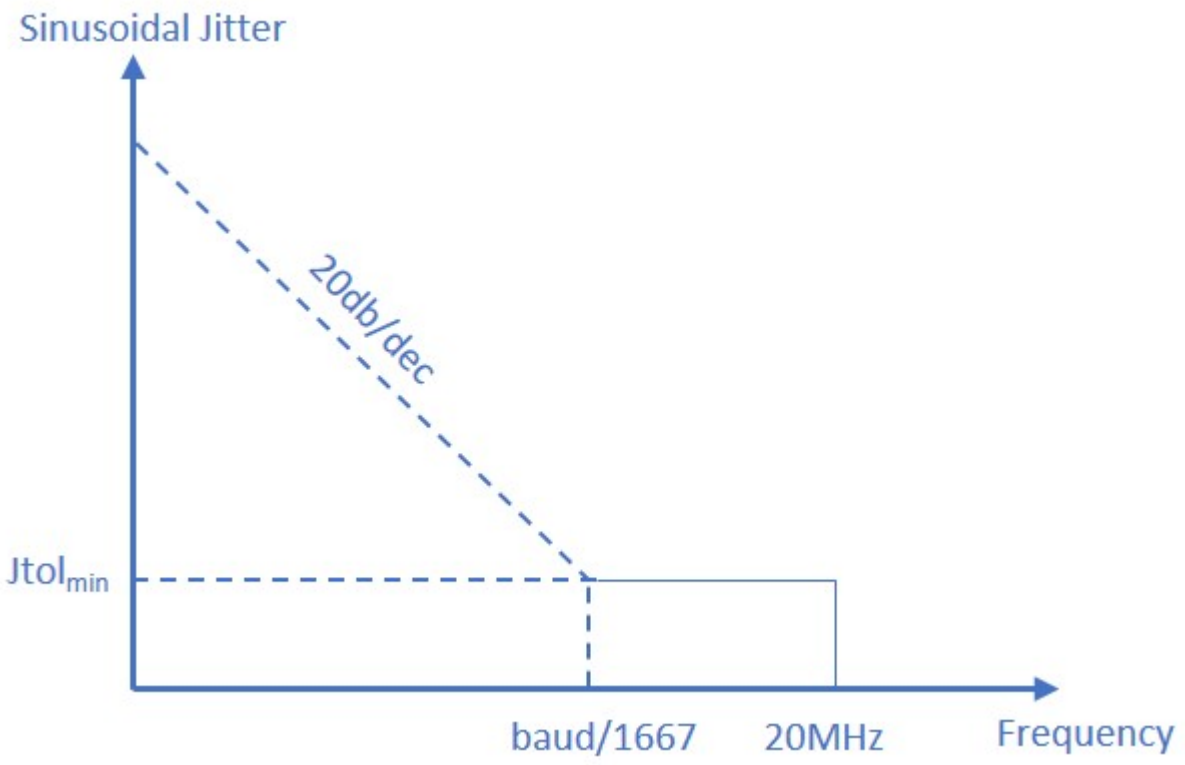


**Table 5-14.** I/O CDR Switching Characteristics

| Buffer Type | I/O Configuration | Min Data Rate (Mbps) | Max Data Rate (Mbps) | Max Tx to Rx Frequency Offset (ppm) | $Jtol_{min}$ (UI) |
|---|---|---|---|---|---|
| HSIO[1, 2] | LVDS18 | 266 | 1250 | ±200 | 0.08 |
| HSIO[1, 2] | LVDS18 | 266 | 1250 | ±100 | 0.1 |


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**Table 5-14.** I/O CDR Switching Characteristics (continued)

| Buffer Type | I/O Configuration | Min Data Rate (Mbps) | Max Data Rate (Mbps) | Max Tx to Rx Frequency Offset (ppm) | $Jtol_{min}$ (UI) |
|---|---|---|---|---|---|
| GPIO[1, 3] | LVDS25 | 266 | 1250 | ±100 | 0.1 |
| GPIO[1, 3] | LVDS18G | 266 | 1250 | ±100 | 0.1 |

1. Jitter tolerance of applied sinusoidal jitter from 1 KHz to 120 MHz, as shown in Figure 5-3. LVDS Jitter Tolerance Plot. It is measured in addition to a stressed eye of $T_j$ = 0.24 UI with $V_{ICM}$ of 1.25V and $V_{IDmin}$ of 250 mV, with the CDR operating at a rate of 1250 Mbps plus or minus the ppm offset listed.
2. HSIO LVDS uses an external 100Ω differential termination resistor. For more information, see LVDS specification in Table 4-17. Differential DC Input Levels.
3. GPIO LVDS uses an internal 100Ω differential termination resistor. For more information, see LVDS specification in Table 4-17. Differential DC Input Levels.

## 5.2. Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

### 5.2.1. Clocking

The following table describes clocking specifications.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-15.** Global and Regional Clock Characteristics (–55°C to 125°C)

| Parameter | Symbol | $V_{DD}$ = 1.0V STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V STD | $V_{DD}$ = 1.05V –1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Global clock $F_{MAX}$ | $F_{MAXG}$ | 500 | 500 | 500 | 500 | MHz | — |
| Regional clock $F_{MAX}$ | $F_{MAXR}$ | 375 | 375 | 375 | 375 | MHz | Transceiver interfaces only |
| | $F_{MAXR}$ | 250 | 250 | 250 | 250 | MHz | All other interfaces |
| Global clock duty cycle distortion | $T_{DCDG}$ | 190 | 190 | 190 | 190 | ps | At 500 MHz |
| Regional clock duty cycle distortion | $T_{DCDR}$ | 120 | 120 | 120 | 120 | ps | At 250 MHz |

The following table describes clocking specifications from –40°C to 100°C.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.


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**Table 5-16.** High-Speed I/O Clock Characteristics (–55°C to 125°C)

| Parameter | Symbol | $V_{DD}$ = 1.0V STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V STD | $V_{DD}$ = 1.05V –1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| High-speed I/O clock $F_{MAX}$ | $F_{MAXB}$ | 1000 | 1250 | 1000 | 1250 | MHz | HSIO and GPIO |
| High-speed I/O clock skew[1] | $F_{SKEWB}$ | 30 | 20 | 30 | 20 | ps | HSIO without bridging |
| | $F_{SKEWB}$ | See note 3 | | | | ps | HSIO with bridging |
| | $F_{SKEWB}$ | 45 | 35 | 45 | 35 | ps | GPIO without bridging |
| | $F_{SKEWB}$ | 75 | 60 | 75 | 60 | ps | GPIO with bridging |
| High-speed I/O clock duty cycle distortion[2] | $T_{DCB}$ | 90 | 90 | 90 | 90 | ps | HSIO without bridging |
| | $T_{DCB}$ | 115 | 115 | 115 | 115 | ps | HSIO with bridging |
| | $T_{DCB}$ | 90 | 90 | 90 | 90 | ps | GPIO without bridging |
| | $T_{DCB}$ | 115 | 115 | 115 | 115 | ps | GPIO with bridging |

1. $F_{SKEWB}$ is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other because they are fed by the same or adjacent clock-tree branches. Use the Libero SmartTime Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.
3. See Table 5-17. HSIO Clock Skew with Bridging (–55°C to 125°C).

The following table describes high-speed I/O clock skew ($F_{SKEWB}$) with bridging from –40°C to 100°C.

**Note:** $F_{SKEWB}$ is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Libero SmartTime Timing Analyzer tool to evaluate clock skew specific to the design.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-17.** HSIO Clock Skew with Bridging (–55°C to 125°C)

| Device | Total I/O Banks | Bridging Source | $V_{DD}$ = 1.0V STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|---|---|
| MPF050T | 1 | NNW[1] | 40 | 30 | 40 | 30 | ps |
| | 1 | NNE[2] | 40 | 30 | 40 | 40 | ps |
| MPF100T | 2 | NNW[1] | 120 | 80 | 120 | 80 | ps |
| | 2 | NNE[2] | 110 | 70 | 110 | 70 | ps |


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**Table 5-17.** HSIO Clock Skew with Bridging (–55°C to 125°C) (continued)

| Device | Total I/O Banks | Bridging Source | $V_{DD}$ = 1.0V STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|---|---|
| MPF200T | 2 | NNW[1] | 120 | 80 | 120 | 80 | ps |
| | 2 | NNE[2] | 110 | 70 | 110 | 70 | ps |
| MPF300T | 3 | NNW[1] | 120 | 80 | 120 | 80 | ps |
| | 3 | NNE[2] | 280 | 200 | 280 | 200 | ps |
| MPF500T | 3 | NNW[1] | 125 | 85 | 125 | 85 | ps |
| | 3 | NNE[2] | 300 | 220 | 300 | 220 | ps |

1. NNW source designates bridging that originates from the north-west corner or PIOs inside I/O bank 0 (the most western I/O bank at the north edge).
2. NNE source designates bridging that originates from the north-east corner or PIOs inside I/O bank 1 (the most eastern I/O bank at the north edge).

### 5.2.2. PLL

The following table describes PLL.

**Table 5-18.** PLL Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Input clock frequency (Integer mode) | $F_{INI}$ | 1 | — | 1250 | MHz | — |
| Input clock frequency (Fractional mode) | $F_{INF}$ | 10 | — | 1250 | MHz | — |
| Minimum reference or feedback pulse width[1] | $F_{INPULSE}$ | 200 | — | — | ps | — |
| Frequency at the Frequency Phase Detector (PFD) (Integer mode) | $F_{PHDETI}$ | 1 | — | 312 | MHz | — |
| Frequency at the PFD (Fractional mode) | $F_{PHDETF}$ | 10 | — | 225 | MHz | — |
| Allowable input duty cycle | $F_{INDUTY}$ | 25 | — | 75 | % | — |
| Maximum input period clock jitter (reference and feedback clocks)[2] | $F_{MAXINJ}$ | — | 120 | 1000 | ps | — |
| PLL VCO frequency | $F_{VCO}$ | 800 | — | 5000 | MHz | — |
| Loop bandwidth (Int)[3] | $F_{BW}$ | $F_{PHDET}$/55 | $F_{PHDET}$/44 | $F_{PHDET}$/30 | MHz | — |
| Loop bandwidth (FRAC)[3] | $F_{BW}$ | $F_{PHDET}$/91 | $F_{PHDET}$/77 | $F_{PHDET}$/56 | MHz | — |
| Static phase offset of the PLL outputs[4] | $T_{SPO}$ | — | — | Max (±60 ps, ±0.5 degrees) | ps | — |


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**Table 5-18.** PLL Electrical Characteristics (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| PLL output period jitter[10, 11] | $T_{OUTJITTER}$ | — | — | ±0.0125*output_ period | ps | 1.5 MHz ≤ $F_{OUT}$ < 15 MHz |
| | | — | — | 135 | ps | $F_{OUT}$ ≥ 15 MHz |
| | | — | — | ±67.5 | ps | |
| | | — | — | 16.67 | ns | 0.05MHz ≤ $F_{OUT}$ < 1.5MHz |
| | | — | — | ±8.335 | ns | |
| PLL output duty cycle precision | $T_{OUTDUTY}$ | 48 | — | 54 | % | — |
| PLL lock time[5] | $T_{LOCK}$ | — | — | Max (6.0 µs, 625 PFD cycles) | µs | — |
| PLL unlock time[6] | $T_{UNLOCK}$ | 2 | — | 8 | PFD cycles | — |
| PLL output frequency | $F_{OUT}$ | 0.050 | — | 1250 | MHz | — |
| Minimum power-down pulse width | $T_{MPDPW}$ | 1 | — | — | µs | — |
| Maximum delay in the feedback path[7] | $F_{MAXDFB}$ | — | — | 1.5 | PFD cycles | — |
| Spread spectrum modulation spread[8] | Mod_Spread | 0.1 | — | 3.1 | % | — |
| Spread spectrum modulation frequency[9] | Mod_Freq | $F_{PHDETF}$/ (128x63) | 32 | $F_{PHDETF}$/(128) | KHz | — |

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = 01 for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = 00 and can be increased if BW_PROP_CTRL = 10 and will be at the highest value if BW_PROP_CTRL = 11.
4. Maximum (±3 Sigma) phase error between any two outputs with nominally aligned phases.
5. PFD cycles is REFDIV/$F_{IN[I/F]}$. For example, REFDIV = 1, $F_{INI}$ = 25 MHz, lock time = Max (6.0 µs, 625 * 1/25 MHz) = 25µs.
6. Unlock occurs if two cycles slip within two PFD cycles.
7. Maximum propagation delay of external feedback path in Deskew mode.
8. Programmable capability for depth of down spread or center spread modulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).
10. Period jitter is measured at the output of the device using HSUL12 output buffers and includes the jitter effects of the reference clock source, PLL, clock routing networks, and output buffer. PLL is configured with internal feedback enabled and in integer mode. FPGA fabric is active during testing (75% utilization).
11. Jitter characteristics for protocol-specific industry standards are met due to improved input clock path and/or optimized VCO rates used. Contact technical support for protocol specific characterization reports.

**Note:** In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.


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### 5.2.3. DLL

The following table provides information about DLL.

**Table 5-19.** DLL Electrical Characteristics

| Parameter[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input reference clock frequency | $F_{INF}$ | 133 | — | 800 | MHz |
| Input feedback clock frequency | $F_{INFDBF}$ | 133 | — | 800 | MHz |
| Primary output clock frequency | $F_{OUTPF}$ | 133 | — | 800 | MHz |
| Secondary output clock frequency[2] | $F_{OUTSF}$ | 33.3 | — | 800 | MHz |
| Input clock cycle-to-cycle jitter | $F_{INJ}$ | — | — | 200 | ps |
| Output clock cycle-to-cycle jitter (with clean input clock) | $T_{OUTJITTERCC}$ | — | — | Max (250 ps, 15% of clock period) | ps |
| Output clock period jitter (with clean input clock) | $T_{OUTJITTERP}$ | — | — | Max (300 ps, 20% of clock period) | ps |
| Output clock-to-clock skew between two outputs with the same phase settings | $T_{SKEW}$ | — | — | ±150 | ps |
| DLL lock time | $T_{LOCK}$ | 16 | — | 16K | Reference clock cycles |
| Minimum reset pulse width | $T_{MRPW}$ | 3 | — | — | ns |
| Minimum input pulse width[3] | $T_{MIPW}$ | 20 | — | — | ns |
| Minimum input clock pulse width high | $T_{MPWH}$ | 400 | — | — | ps |
| Minimum input clock pulse width low | $T_{MPWL}$ | 400 | — | — | ps |
| Delay step size | $T_{DEL}$ | 12.7 | 30 | 35 | ps |
| Maximum delay block delay[4] | $T_{DELMAX}$ | 1.8 | | 4.8 | ns |
| Output clock duty cycle (with 50% duty cycle input)[5] | $T_{DUTY}$ | 40 | — | 60 | % |
| Output clock duty cycle (with 50% duty cycle input)[6] | $T_{DUTY50}$ | 45 | — | 55 | % |

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.
6. With duty cycle correction enabled.

### 5.2.4. RC Oscillators

The following tables describe internal RC clock resources for user designs. They also describe system design with RF front-end information about emitters generated on-chip to support programming operations.

**Table 5-20.** 2 MHz RC Oscillator Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | $RC_{2FREQ}$ | — | 2 | — | MHz | –55°C ≤ Tj ≤ 125°C |
| Accuracy | $RC_{2FACC}$ | –6.5 | — | +6.5 | % | –40°C ≤ Tj ≤ 100°C |
| | | –10 | — | +10 | % | –40°C ≤ Tj ≤ 125°C |
| | | –10 | — | +10 | % | –55°C ≤ Tj ≤ 125°C |
| Duty cycle | $RC_{2DC}$ | 46 | — | 54 | % | –55°C ≤ Tj ≤ 125°C |


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**Table 5-20.** 2 MHz RC Oscillator Electrical Characteristics (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Peak-to-peak output period jitter | $RC_{2PJIT}$ | — | 5 | 10 | ns | –55°C ≤ Tj ≤ 125°C |
| Peak-to-peak output cycle-to-cycle jitter | $RC_{2CJIT}$ | — | 5 | 10 | ns | –55°C ≤ Tj ≤ 125°C |
| Operating current ($V_{DD25}$) | $RC_{2IVPPA}$ | — | — | 60 | µA | –55°C ≤ Tj ≤ 125°C |
| Operating current ($V_{DD}$) | $RC_{2IVDD}$ | — | — | 2.6 | µA | –55°C ≤ Tj ≤ 125°C |

**Table 5-21.** 160 MHz RC Oscillator Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating frequency | $RC_{SCFREQ}$ | — | 160 | — | MHz | –55°C ≤ Tj ≤ 125°C |
| Accuracy | $RC_{SCFACC}$ | –6.5 | — | +6.5 | % | –40°C ≤ $T_j$ ≤ 100°C |
| | | –10 | — | +10 | % | –40°C ≤ Tj ≤ 125°C |
| | | –10 | — | +10 | % | –55°C ≤ Tj ≤ 125°C |
| Duty cycle | $RC_{SCDC}$ | 47 | — | 52 | % | –55°C ≤ Tj ≤ 125°C |
| Peak-to-peak output period jitter | $RC_{SCPJIT}$ | — | — | 600 | ps | –55°C ≤ Tj ≤ 125°C |
| Peak-to-peak output cycle-to-cycle jitter | $RC_{SCCJIT}$ | — | — | 172 | ps | –55°C ≤ Tj ≤ 125°C |
| Operating current ($V_{DD25}$) | $RC_{SCVPPA}$ | — | — | 599 | µA | –55°C ≤ Tj ≤ 125°C |
| Operating current ($V_{DD18}$) | $RC_{SCVPP}$ | — | — | 0.1 | µA | –55°C ≤ Tj ≤ 125°C |
| Operating current ($V_{DD}$) | $RC_{SCVDD}$ | — | — | 60.7 | µA | –55°C ≤ Tj ≤ 125°C |

## 5.2.5. Clock Jitter

Global clock, output clock, and transceiver clock jitter specifications are listed in this section. PLL jitter, DLL jitter, and RC oscillator jitter specifications are referenced in their respective sections.

**Table 5-22.** Period Jitter for Global Clocks[6, 7]

Global clocks are clock nets distributed throughout the FPGA using global networks. Jitter specifications listed in this table are applicable to –STD and –1 speed grade for all temperature grades.

| Parameter | Global Clock Period Jitter | | | | | Unit |
|---|---|---|---|---|---|---|
| % FF used (of total FFs in device)[1,2] | 0% | 15% | 25% | 50% | 75% | % |
| Average toggle rate[3] | — | 30% | 30% | 30% | 30% | % |
| Effective FF toggle %[4] | 0% | 4.5% | 7.5% | 15.0% | 22.5% | % |
| Max period jitter (absolute) | See Note 5 | 29 | 54 | 168 | 227 | ps |
| Max period jitter (peak to peak) | See Note 5 | ±14.5 | ±27 | ±84 | ±113.5 | ps |

1. % Flip-Flop (FF) used is defined as the percentage of total device FFs that are switching in the largest clock domain within the FPGA (including synchronous and divided clocks).
2. The 50% and 75% FF used per clock domain are only shown to illustrate the impact of high utilization on a global clock net jitter. Typical designs are expected to have less than 25% FF used per clock domain (as defined in the preceeding note).


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3. Measured jitter is generated at varying % FF used levels with a switching rate of 30%.
4. Effective FF toggle % is the product of % FF used and average toggle rate. In Table 5-22, jitter is specified for an average toggle rate of 30%. To determine jitter for a given combination, multiply FF used and average toggle rate then use the linear interpolation equation as shown in Figure 5-4.
5. Use PLL, DLL, 160 MHz RC Osc jitter specifications, or input jitter specifications, as applicable.
6. Refer to Table 5-23 for formulas to calculate period jitter as a function of the clocking topology.
7. For further details, see the PolarFire Family Clocking Resources Users Guide (section Global Net Clock Jitter).

**Figure 5-4.** Global Clock Period Jitter vs Effective FF Toggle Percentage

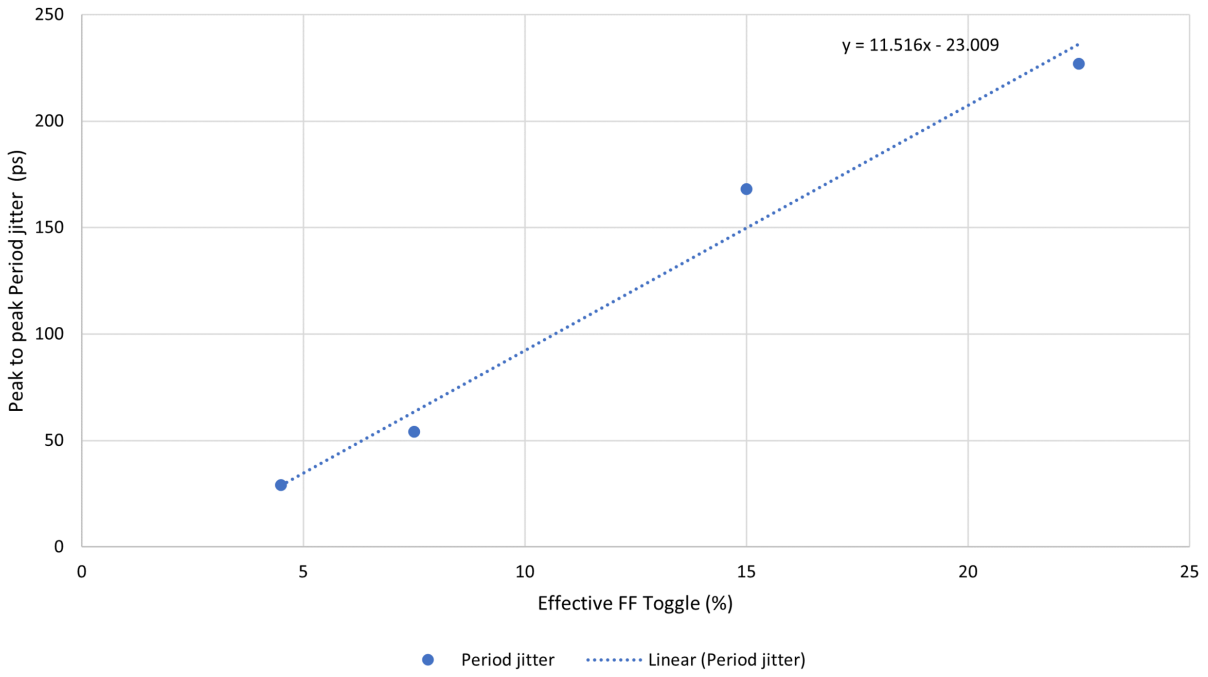


**Table 5-23.** Period Jitter Formula for Global Clocks[6, 7, 8, 9]

| Topology | Formula |
|---|---|
| Inbuf → CCC → PLL → Global | Max (PLL jitter, Global clock jitter) |
| Inbuf → CCC → Global | Max (Input jitter, Global clock jitter) |
| Global → CCC → PLL → Global | Max (PLL jitter, Global clock jitter) |
| Global → CCC → Global | Global clock jitter |
| TX clock → CCC → PLL → Global | Max (PLL jitter, Global clock jitter) |
| TX clock → Global → CCC → PLL → Global | Max (PLL jitter, Global clock jitter) |
| TX clock → Regional → CCC → PLL | Max (PLL jitter, Global clock jitter) |
| RX clock → CCC → PLL → Global | Max (PLL jitter, Global clock jitter) |
| RX clock → Global → CCC → PLL → Global | Max (PLL jitter, Global clock jitter) |
| RX clock → Regional → CCC→ PLL | Max (PLL jitter, Global clock jitter) |
| 2 MHz / 160 MHz RCOsc → CCC → Global | Max (RCOSC jitter, Global clock jitter) |


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**Table 5-23.** Period Jitter Formula for Global Clocks[6, 7, 8, 9] (continued)

| Topology | Formula |
|---|---|
| 160 MHz RCOsc → CCC → PLL → Global [1] | Max (PLL jitter, Global clock jitter) |
| Inbuf → CCC → DLL → Global [2] | Max (Input jitter + DLL jitter, Global clock jitter) |
| Inbuf → CCC → DLL → PLL → Global [2,3] | Max (PLL jitter, Global clock jitter) |
| Inbuf → CCC → PLL → DLL → Global | Max (DLL jitter, Global clock jitter) |

1. The 2 MHz RCOsc should not be used as reference clock of PLLs. The 160 MHz oscillator should be used instead for better PLL input jitter immunity.
2. Input jitter is additive to DLL output jitter. It should not exceed the maximum DLL input jitter allowed. Refer to Table 5-19 for information on jitter specifications.
3. When cascading DLL into PLL, DLL output frequency should be limited such that the PLL input jitter requirement is met. Refer to Table 5-18 and Table 5-19 for information on jitter specifications.

**Table 5-24.** Period Jitter for External Output Clocks[6, 7, 8, 9]

External output clocks are generated within the FPGA, routed through global networks and propagated outside of the FPGA by means of HSIO or GPIO output buffers. Jitter specifications listed in this table are applicable to –STD and –1 speed grade for all temperature grades.

| Parameter | External Output Clock Period Jitter | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| % FF used (of total FFs in device)[1,2] | 0% | 14% | 23% | 47% | 56% | 75% | % |
| Average toggle rate[3] | — | 30% | 30% | 30% | 30% | 30% | % |
| Effective FF toggle %[4] | 0% | 4.2% | 6.9% | 14.1% | 16.8% | 22.5% | % |
| Max period jitter (absolute) | See Note 5 | 334 | 466 | 800 | 924 | 1140 | ps |
| Max period jitter (peak to peak) | See Note 5 | ±167 | ±233 | ±400 | ±462 | ±570 | ps |

1. % Flip-Flop (FF) used is defined as the percentage of total device FFs that are switching in the largest clock domain within the FPGA (including synchronous and divided clocks).
2. The 50% and 75% FF used per clock domain are only shown to illustrate the impact of high utilization on a global clock net jitter. Typical designs are expected to have less than 25% FF used per clock domain (as defined in the preceding note).
3. Measured jitter is generated at varying % FF used levels with a switching rate of 30%.
4. Effective FF toggle % is the product of % FF used and average toggle rate. In Table 5-24, jitter is specified for an average toggle rate of 30%. To determine jitter for a given combination, multiply FF used and average toggle rate then use the linear interpolation equation as shown in Figure 5-5.
5. Use PLL, DLL, 160 MHz RC Osc jitter specifications, or input jitter specifications, as applicable.
6. All measurements were taken by observing the clock jitter from an FPGA output pin.
7. Refer to Table 5-25 for formulas to calculate period jitter as a function of the clocking topology.
8. For clock forwarded interfaces such as DDRx where both data and clock are sent from the same clock domain, this external jitter component should be ignored. Output jitter should be taken from the interface specification.


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9. For further details, see the PolarFire Family Clocking Resources Users Guide (section Global Net Clock Jitter).


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**Figure 5-5.** External Output Clock Period Jitter vs Effective FF Toggle Percentage

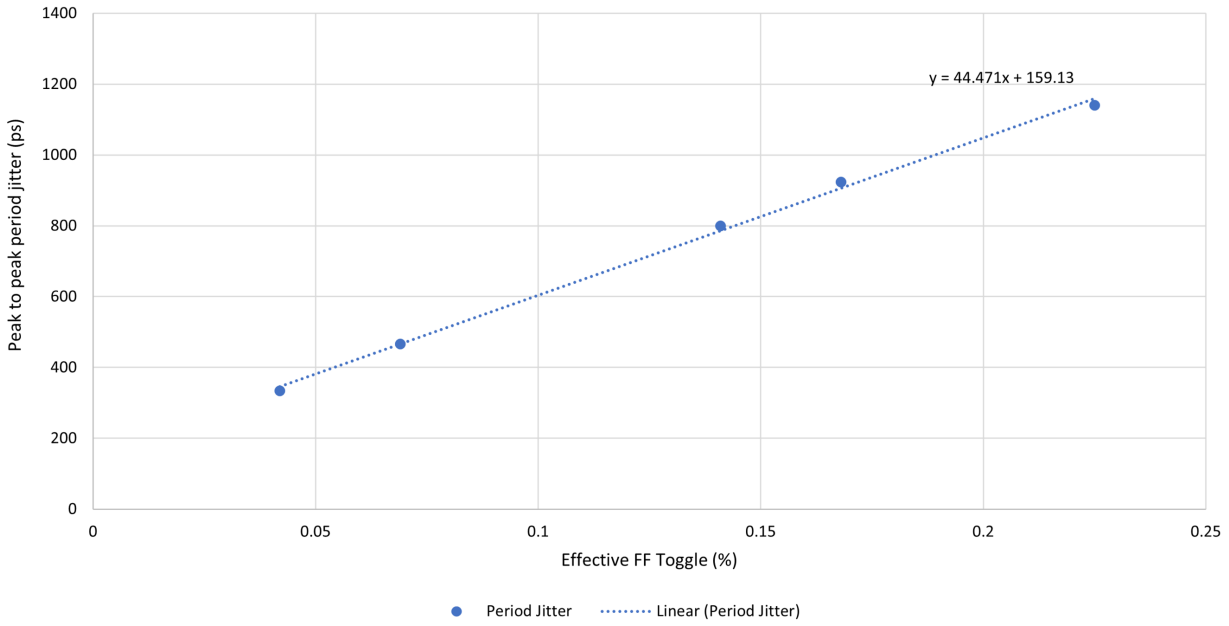


**Table 5-25.** Period Jitter Formula for External Output Clocks

| Topology | Formula |
|---|---|
| Inbuf → CCC → PLL → Global → Outbuf | Max (PLL jitter, External output clock jitter) |
| Inbuf → CCC → Global → Outbuf | Max (Input jitter, External output clock jitter) |
| Global → CCC → PLL → Global → Outbuf | Max (PLL jitter, External output clock jitter) |
| Global → CCC → Global → Outbuf | External output clock jitter |
| TX clock → CCC → PLL → Global → Outbuf | Max (PLL jitter, External output clock jitter) |
| TX clock → Global → CCC → PLL → Global → Outbuf | Max (PLL jitter, External output clock jitter) |
| TX clock → Regional → CCC → PLL → Outbuf | Max (PLL jitter, External output clock jitter) |
| RX clock → CCC → PLL → Global → Outbuf | Max (PLL jitter, External output clock jitter) |
| RX clock → Global → CCC → PLL → Global → Outbuf | Max (PLL jitter, External output clock jitter) |
| RX clock → Regional → CCC→ PLL→ Outbuf | Max (PLL jitter, External output clock jitter) |
| 2 MHz / 160 MHz RCOsc → CCC → Global → Outbuf | Max (RCOsc jitter, External output clock jitter) |
| 160 MHz RCOsc → CCC → PLL → Global → Outbuf [1] | Max (PLL jitter, External output clock jitter) |
| Inbuf → CCC → DLL → Global → Outbuf [2] | Max (Input jitter + DLL jitter, External output clock jitter) |
| Inbuf → CCC → DLL → PLL → Global → Outbuf [2,3] | Max (PLL jitter, External output clock jitter) |
| Inbuf → CCC→ PLL → DLL → Global → Outbuf | Max (DLL jitter, External output clock jitter) |

1. The 2 MHz RCOsc should not be used as reference clock of PLLs. The 160 MHz oscillator should be used instead for better PLL input jitter immunity.
2. Input jitter is additive to DLL output jitter. It should not exceed the maximum DLL input jitter allowed. Refer to Table 5-19 for information on jitter specifications.
3. When cascading DLL into PLL, DLL output frequency should be limited such that the PLL input jitter requirement is met. Refer to Table 5-18 and Table 5-19 for information on jitter specifications.


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**Table 5-26.** Period Jitter for Transceiver Clocks[5, 6]

Transceiver clocks are generated within the FPGA and routed to/from transceiver TX and RX through global networks. Jitter specifications listed in this table are applicable to –STD and –1 speed grade for all temperature grades.

| Parameter | Transceiver Clock Period Jitter | | | | | Unit |
|---|---|---|---|---|---|---|
| % FF used (of total FFs in device)[1,2] | 0% | 15% | 25% | 50% | 75% | % |
| Average toggle rate[3] | — | 30% | 30% | 30% | 30% | % |
| Effective FF toggle %[4] | 0% | 4.5% | 7.5% | 15.0% | 22.5% | % |
| Maximum TX clock period jitter (absolute) | 60 | 89 | 114 | 228 | 287 | ps |
| Maximum TX clock period jitter (peak to peak) | ±30 | ±44.5 | ±57 | ±114 | ±143.5 | ps |
| Maximum RX clock period jitter (absolute) | 200 | 229 | 254 | 368 | 427 | ps |
| Maximum RX clock period jitter (peak to peak) | ±100 | ±114.5 | ±127 | ±184 | ±213.5 | ps |

1. % Flip-Flop (FF) used is defined as the percentage of total device FFs that are switching in the largest clock domain within the FPGA (including synchronous and divided clocks).
2. The 50% and 75% FF used per clock domain are only shown to illustrate the impact of high utilization on a global clock net jitter. Typical designs are expected to have less than 25% FF used per clock domain (as defined in the preceding note).
3. Measured jitter is generated at varying % FF used levels with a switching rate of 30%.
4. Effective FF toggle % is the product of % FF used and average toggle rate. In Table 5-26, jitter is specified for an average toggle rate of 30%. To determine jitter for a given combination, multiply FF used and average toggle rate then use the linear interpolation equation as shown in Figure 5-6.
5. Refer to Table 5-27 for formulas to calculate period jitter as a function of the clocking topology.
6. For further details, see the PolarFire Family Transceiver User Guide (section Global Net Clock Jitter).


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**Figure 5-6.** Transceiver Clock Period vs Effective FF Toggle Percentage

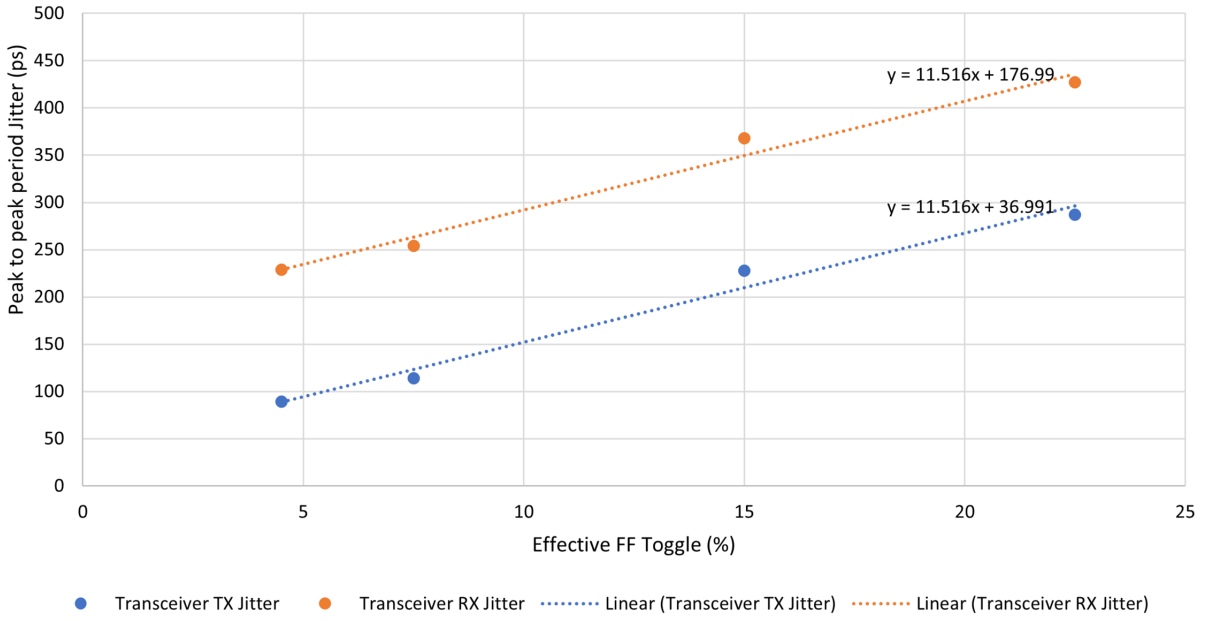


**Table 5-27.** Period Jitter Formula for Transceiver Clocks[1, 2]

| Topology | Formula |
|---|---|
| TX clock → Global | TX clock jitter |
| TX clock → Regional | TX clock jitter |
| RX clock → Global | RX clock jitter |
| RX clock → Regional | RX clock jitter |

1. All measurements were taken by observing the clock jitter from an FPGA output pin.
2. Refer to Table 5-25 for formulas to calculate period jitter as a function of the clocking topology.

## 5.3. Fabric Specifications

The following section describes specifications for the fabric.

### 5.3.1. Math Blocks

The following table lists the maximum operating frequency ($F_{MAX}$) of the math block in the extended commercial temperature range (0°C to 100°C).

**Table 5-28.** Math Block Performance Extended Commercial Range (0°C to 100°C)

| Modes | $V_{DD}$ = 1.0V –STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V –STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|
| 18 × 18 multiplication | 370 | 470 | 440 | 500 | MHz |
| 18 × 18 multiplication summed with 48-bit input | 370 | 470 | 440 | 500 | MHz |
| 18 × 19 multiplier pre-adder ROM mode | 365 | 465 | 435 | 500 | MHz |
| Two 9 × 9 multiplication | 370 | 470 | 440 | 500 | MHz |
| 9 × 9 dot product (DOTP) | 370 | 470 | 440 | 500 | MHz |
| Complex 18 × 19 multiplication | 360 | 455 | 430 | 500 | MHz |


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The following table lists the maximum operating frequency ($F_{MAX}$) of the math block in the industrial temperature range (–40°C to 100°C).

**Table 5-29.** Math Block Performance Industrial Range (–40°C to 100°C)

| Modes | $V_{DD}$ = 1.0V –STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V –STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|
| 18 × 18 multiplication | 365 | 465 | 435 | 500 | MHz |
| 18 × 18 multiplication summed with 48-bit input | 365 | 465 | 435 | 500 | MHz |
| 18 × 19 multiplier pre-adder ROM mode | 355 | 460 | 430 | 500 | MHz |
| Two 9 × 9 multiplication | 365 | 465 | 435 | 500 | MHz |
| 9 × 9 DOTP | 365 | 465 | 435 | 500 | MHz |
| Complex 18 × 19 multiplication | 350 | 450 | 425 | 500 | MHz |

The following table lists the maximum operating frequency ($F_{MAX}$) of the math block in the Automotive T2 temperature range (–40°C to 125°C).

**Table 5-30.** Math Block Performance Automotive T2 Range (–40°C to 125°C)

| Modes | $V_{DD}$ = 1.0V –STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V –STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|
| 18 × 18 multiplication | 365 | 465 | 435 | 500 | MHz |
| 18 × 18 multiplication summed with 48-bit input | 365 | 465 | 435 | 500 | MHz |
| 18 × 19 multiplier pre-adder ROM mode | 355 | 460 | 430 | 500 | MHz |
| Two 9 × 9 multiplication | 365 | 465 | 435 | 500 | MHz |
| 9 × 9 DOTP | 365 | 465 | 435 | 500 | MHz |
| Complex 18 × 19 multiplication | 350 | 450 | 425 | 500 | MHz |

The following table lists the maximum operating frequency ($F_{MAX}$) of the math block in the Military temperature range (–55°C to 125°C).

**Table 5-31.** Math Block Performance Military Range (–55°C to 125°C)

| Modes | $V_{DD}$ = 1.0V –STD | $V_{DD}$ = 1.05V –STD | Unit |
|---|---|---|---|
| 18 × 18 multiplication | 360 | 435 | MHz |
| 18 × 18 multiplication summed with 48-bit input | 360 | 435 | MHz |
| 18 × 19 multiplier pre-adder ROM mode | 355 | 430 | MHz |
| Two 9 × 9 multiplication | 360 | 435 | MHz |
| 9 × 9 DOTP | 360 | 435 | MHz |
| Complex 18 × 19 multiplication | 345 | 425 | MHz |

### 5.3.2. SRAM Blocks

The following table lists the maximum operating frequency ($F_{MAX}$) of the LSRAM block for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.


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**Table 5-32.** LSRAM Performance Industrial Temperature Range (–55°C to 125°C)

| $V_{DD}$ = 1.0V –STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V –STD | $V_{DD}$ = 1.05V –1 | Unit | Condition |
|---|---|---|---|---|---|
| 343 | 428 | 343 | 428 | MHz | Two-port, all supported widths, pipelined, simple-write, and write-feed-through |
| 309 | 428 | 309 | 428 | MHz | Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through |
| 343 | 428 | 343 | 428 | MHz | Dual-port, all supported widths, pipelined, simple-write, and write-feed-through |
| 309 | 428 | 309 | 428 | MHz | Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through |
| 343 | 428 | 343 | 428 | MHz | Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through |
| 279 | 295 | 279 | 295 | MHz | Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through |
| 343 | 428 | 343 | 428 | MHz | Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through |
| 196 | 285 | 240 | 285 | MHz | Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through |
| 240 | 285 | 240 | 285 | MHz | Two-port, all supported widths, pipelined, and read-before-write |
| 240 | 285 | 240 | 285 | MHz | Two-port, all supported widths, non-pipelined, and read-before-write |
| 240 | 285 | 240 | 285 | MHz | Dual-port, all supported widths, pipelined, and read-before-write |
| 240 | 285 | 240 | 285 | MHz | Dual-port, all supported widths, non-pipelined, and read-before-write |
| 240 | 285 | 240 | 285 | MHz | Two-port pipelined ECC mode, pipelined, and read-before-write |
| 198 | 240 | 198 | 240 | MHz | Two-port non-pipelined ECC mode, pipelined, and read-before-write |
| 240 | 285 | 240 | 285 | MHz | Two-port pipelined ECC mode, non-pipelined, and read-before-write |
| 193 | 240 | 193 | 240 | MHz | Two-port non-pipelined ECC mode, non-pipelined, and read-before-write |

The following table lists the maximum operating frequency ($F_{MAX}$) of the µSRAM block for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-33.** µSRAM Performance

| Parameter | Symbol | $V_{DD}$ = 1.0V –STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V –STD | $V_{DD}$ = 1.05V –1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Operating frequency | $F_{MAX}$ | 400 | 415 | 450 | 480 | MHz | Write-port |
| Read access time | Tac | — | 2 | — | 2 | ns | Read-port |

The following table lists the maximum operating frequency ($F_{MAX}$) of the µPROM block for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.


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–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-34.** µPROM Performance

| Parameter | Symbol | $V_{DD}$ = 1.0V –STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V –STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|---|
| Read access time | Tac | 10 | 10 | 10 | 10 | ns |

## 5.4. Transceiver Switching Characteristics

This section describes transceiver switching characteristics. This section is not applicable to PolarFire Core family of FPGAs that do not feature transceiver functionality. Refer to the PPAT for transceiver pin termination guidelines.

### 5.4.1. Transceiver Performance

The following table describes transceiver performance.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-35.** PolarFire Transceiver and TxPLL Performance

| Parameter | Symbol | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Tx data rate[1,2] | $F_{TXRate}$ | 0.25 | — | 10.3125 | 0.25 | — | 12.7 | Gbps |
| Tx OOB (serializer bypass) data rate | $F_{TXRateOOB}$ | DC | — | 1.5 | DC | — | 1.5 | Gbps |
| Rx data rate when AC coupled[2] | $F_{RxRateAC}$ | 0.25 | — | 10.3125 | 0.25 | — | 12.7 | Gbps |
| Rx data rate when DC coupled | $F_{RxRateDC}$ | 0.25 | — | 3.2 | 0.25 | — | 3.2 | Gbps |
| Rx OOB (deserializer bypass) data rate | $F_{TXRateOOB}$ | DC | — | 1.25 | DC | — | 1.25 | Gbps |
| TxPLL output frequency[3] | $F_{TXPLL}$ | 1.6 | — | 5.1563 | 1.6 | — | 6.35 | GHz |
| Rx CDR mode | $F_{RXCDR}$ | 0.25 | — | 10.3125 | 0.25 | — | 10.3125 | Gbps |
| Rx DFE and CDR auto-calibration modes[2] | $F_{RXAUTOCAL}$ | 3.0 | — | 10.3125 | 3.0 | — | 12.7 | Gbps |
| Rx Eye Monitor mode [2] | $F_{RXEyeMon}$ | 3.0 | — | 10.3125 | 3.0 | — | 12.7 | Gbps |
| EQ far-end loopback data rate | $F_{EQFELPB}$ | 0.25 | — | 1.25 | 0.25 | — | 1.25 | Gbps |
| EQ near-end loopback data rate | $F_{EQNELPB}$ | 0.25 | — | 10.3125 | 0.25 | — | 10.3125 | Gbps |
| CDR far-end parallel loopback data rate[6] | $F_{CDRFELPB}$ | 0.00625[5] | — | 312.5 | — | — | 312.5 | MHz |
| PCS reset minimum pulse width | $MPW_{PCS_RESET}$ | 16 | — | — | 16 | — | — | [Tx\|Rx]_CLK Cycles[4] |
| PMA reset minimum pulse width | $MPW_{PMA_RESET}$ | 16 | — | — | 16 | — | — | [Tx\|Rx]_CLK Cycles[4] |

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.
2. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.


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4. Minimum pulse width should reference TX_CLK when Tx only or both Tx and Rx are used. Reference RX_CLK if only Rx is used.
5. In 40-bit wide parallel mode.
6. The CDR far-end parallel loopback is clocked by the recovered clock of the CDR. The bandwidth of this loopback is equivalent to the clock multiplied by the data width.

### 5.4.2. Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-36.** PolarFire Transceiver Reference Clock AC Requirements

| Parameter | Symbol | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Reference clock input rate[1, 2] | $F_{TXREFCLK}$ | 20 | — | 400 | 20 | — | 400 | MHz |
| Reference clock input rate[1, 2, 3] | $F_{XCVRREFCLKMAX\ CASCADE}$ | 20 | — | 156.3 | 20 | — | 156.3 | MHz |
| Reference clock rate at the Tx PLL PFD[4] | $F_{TXREFCLKPFD}$ | 20 | — | 156.3 | 20 | — | 175 | MHz |
| Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4] | $F_{TXREFCLKPFD10G}$ | 75 | — | 156.3 | 75 | — | 175 | MHz |
| Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5] | $F_{TXREFPN}$ | — | — | –110 | — | — | –110 | dBc/Hz |
| Phase noise at 10 KHz | $F_{TXREFPN}$ | — | — | –110 | — | — | –110 | dBc/Hz |
| Phase noise at 100 KHz | $F_{TXREFPN}$ | — | — | –115 | — | — | –115 | dBc/Hz |
| Phase noise at 1 MHz | $F_{TXREFPN}$ | — | — | –135 | — | — | –135 | dBc/Hz |
| Reference clock input rise time (10%–90%)[8] | $T_{REFRISE}$ | — | 200 | 500 | — | 200 | 500 | ps |
| Reference clock input fall time (90%–10%)[8] | $T_{REFFALL}$ | — | 200 | 500 | — | 200 | 500 | ps |
| Reference clock rate at RX CDR | $F_{RXREFCLKCDR}$ | 20 | — | 156.3 | 20 | — | 156.3 | MHz |
| Reference clock duty cycle | $T_{REFDUTY}$ | 40 | — | 60 | 40 | — | 60 | % |


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**Table 5-36.** PolarFire Transceiver Reference Clock AC Requirements (continued)

| Parameter | Symbol | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Spread spectrum modulation spread[6] | Mod_Spread | 0.1 | — | 3.1 | 0.1 | — | 3.1 | % |
| Spread spectrum modulation frequency[7] | Mod_Freq | TxREF CLKPFD/ (128) | 32 | TxREF CLKPFD/ (128*63) | TxREF CLKPFD/ (128) | 32 | TxREF CLKPFD/ (128*63) | KHz |

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. To calculate the $F_{TXREFPN}$ phase noise requirement at frequencies other than 156 MHz, use the following formula: $F_{TXREFPN}$ at f(MHz) = $F_{TXREFPN}$ at 156 MHz + 20*log(f/156)
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).
8. If increased Tx total jitter is acceptable, the maximum reference clock input rise/fall times may be increased beyond the maximum shown in this table when using single-ended configurations (LVCMOS and LVTTL). Refer to Table 5-42 for total jitter specifications as a function of reference clock input rise/fall time.

### 5.4.3. Transceiver Reference Clock I/O Standards

The following differential I/O standards are supported as transceiver reference clocks.

- LVDS25/33
- HCLS25 (for PCIe)
- RSDS25/33
- MINILVDS25/33
- SUBLVDS25/33
- PPDS25/33
- SLVS25/33
- BUSLVDS25
- MLVDS25
- LVPECL33
- MIPI25

For DC input levels, see Differential DC Input and Output Levels.

The transceiver reference clock differential receiver supports $V_{ICM}$ Common mode. If increased Tx total jitter is acceptable, the maximum reference clock input rise/fall times may be increased beyond the maximum specification shown in Table 5-36 when using single-ended configurations (LVCMOS and LVTTL). Refer to Table 5-42 for jitter specification as a function of reference clock input rise/fall time.

**Note:** The amount of jitter from the input receiver increases at Common modes of less 0.2V or greater than $XCVR_{VREF}$ –0.4V. Therefore, for improved SerDes operation, it is recommended that the


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$V_{CM}$ of the signal into the SerDes reference clock input be at a minimum of 0.2V and below $XCVR_{VREF}$ –0.4V.

The following single-ended I/O standards are supported as transceiver reference clocks.

- LVTTL
- LVCMOS33
- LVCMOS25
- LVCMOS18
- SSTL25I/II
- SSTL18I/II
- HSUL18I/II

For DC input levels, see section DC Input and Output Levels.

**Note:** Generally, Hysteresis = OFF is recommended. In extremely high noise systems with degraded reference clock input, Hysteresis = ON may improve results.

### 5.4.4. Transmitter Performance

The following tables describe performance of the transmitter.

**Table 5-37.** Transceiver Reference Clock Input Termination

| Parameter | Symbol | Min (%) | Typ (Ω) | Max (%) | Condition | Notes |
|---|---|---|---|---|---|---|
| Single-ended Thevenin termination | RefTerm | –40 | 50 | +20 | VDDI = 1.8V/ 1.5V | Thevenin impedance is calculated based on independent P and N as measured at 50% of VDDI.<br>For 50Ω/75Ω/ 150Ω cases, the nearest supported values of 40Ω/60Ω/120Ω are used. |
| | | –40 | 75 | +20 | VDDI = 1.8V | |
| | | –40 | 150 | +20 | VDDI = 1.8V/ 1.5V | |
| Differential termination | RefDiffTerm | –20 | 100[1] | +20 | VICM < 0.8V | Measured across P to N with 400 mV bias.<br>When VICM complies with more than one range, use the maximum percentage tolerance of the two ranges. |
| | | –20 | 100 | +40 | 0.6V < VICM < 1.65V | |
| | | –20 | 100 | +80 | 1.4V < VICM | |
| Power-up termination | — | — | >50K | — | — | — |

1. Measured at $V_{CM}$ = 1.2V and $V_{ID}$ = 350 mV.

**Note:** All pull-ups are disabled at power-up to allow hot plug capability.

The following tables describe the PolarFire transceiver user interface clocks.


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**Note:** Unless specified, all modes are non-deterministic. For more information, see PolarFire Family Transceiver User Guide.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-38.** Transceiver TX_CLK Range (Nondeterministic PCS Mode with Global or Regional Fabric Clocks)

| Mode | STD Min | STD Max | –1 Min | –1 Max | Unit |
|---|---|---|---|---|---|
| 8-bit, max data rate = 1.6 Gbps | — | 200 | — | 200 | MHz |
| 10-bit, max data rate = 1.6 Gbps | — | 160 | — | 160 | MHz |
| 16-bit, max data rate = 4.8 Gbps | — | 300 | — | 300 | MHz |
| 20-bit, max data rate = 6.0 Gbps | — | 300 | — | 300 | MHz |
| 32-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 325 | — | 325 | MHz |
| 40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 260 | — | 320 | MHz |
| 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 165 | — | 200 | MHz |
| 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 130 | — | 160 | MHz |
| Fabric pipe mode 32-bit, max data rate = 6.0 Gbps | — | 150 | — | 150 | MHz |

1. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-39.** Transceiver RX_CLK Range (Non-Deterministic PCS Mode with Global or Regional Fabric Clocks)

| Mode | STD Min | STD Max | –1 Min | –1 Max | Unit |
|---|---|---|---|---|---|
| 8-bit, max data rate = 1.6 Gbps | — | 200 | — | 200 | MHz |
| 10-bit, max data rate = 1.6 Gbps | — | 160 | — | 160 | MHz |
| 16-bit, max data rate = 4.8 Gbps | — | 300 | — | 300 | MHz |
| 20-bit, max data rate = 6.0 Gbps | — | 300 | — | 300 | MHz |
| 32-bit, max data rate = 10.3125 Gbps | — | 325 | — | 325 | MHz |
| 40-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 260 | — | 320 | MHz |
| 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 165 | — | 200 | MHz |
| 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 130 | — | 160 | MHz |
| Fabric pipe mode 32-bit, max data rate = 6.0 Gbps | — | 150 | — | 150 | MHz |

1. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.


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**Table 5-40.** Transceiver TX_CLK Range (Deterministic PCS Mode with Regional Fabric Clocks)

| Mode | STD Min | STD Max | –1 Min | –1 Max | Unit |
|---|---|---|---|---|---|
| 8-bit, max data rate = 1.6 Gbps | — | 200 | — | 200 | MHz |
| 10-bit, max data rate = 1.6 Gbps | — | 160 | — | 160 | MHz |
| 16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1) | — | 225 | — | 266 | MHz |
| 20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1) | — | 225 | — | 266 | MHz |
| 32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1) | — | 225 | — | 266 | MHz |
| 40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1] | — | 225 | — | 266 | Mhz |
| 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 165 | — | 200 | MHz |
| 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 130 | — | 160 | MHz |

1. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.

–STD speed grade is offered for Extended Commercial (E), Industrial (I), Military (M), and Automotive (T2) temperature grades.

–1 speed grade is offered for Extended Commercial (E), Industrial (I), and Automotive (T2) temperature grades only.

**Table 5-41.** Transceiver RX_CLK Range (Deterministic PCS Mode with Regional Fabric Clocks)

| Mode | STD Min | STD Max | –1 Min | –1 Max | Unit |
|---|---|---|---|---|---|
| 8-bit, max data rate = 1.6 Gbps | — | 200 | — | 200 | MHz |
| 10-bit, max data rate = 1.6 Gbps | — | 160 | — | 160 | MHz |
| 16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1) | — | 225 | — | 266 | MHz |
| 20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1) | — | 225 | — | 266 | MHz |
| 32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1) | — | 225 | — | 266 | MHz |
| 40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1] | — | 225 | — | 266 | MHz |
| 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 165 | — | 200 | MHz |
| 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | — | 130 | — | 160 | MHz |

1. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.

**Table 5-42.** PolarFire Transceiver Transmitter Characteristics[14]

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential termination | $V_{OTERM}$ | 68 | 85 | 102 | Ω | 85Ω setting |
| | $V_{OTERM}$ | 80 | 100 | 120 | Ω | 100Ω setting |
| | $V_{OTERM}$ | 120 | 150 | 180 | Ω | 150Ω setting |
| Common mode voltage[1] | $V_{OCM}$ | 0.44 × $V_{DDA}$ | 0.525 × $V_{DDA}$ | 0.59 × $V_{DDA}$ | V | DC coupled 50% setting |
| | $V_{OCM}$ | 0.52 × $V_{DDA}$ | 0.6 × $V_{DDA}$ | 0.66 × $V_{DDA}$ | V | DC coupled 60% setting |
| | $V_{OCM}$ | 0.61 × $V_{DDA}$ | 0.7 × $V_{DDA}$ | 0.75 × $V_{DDA}$ | V | DC coupled 70% setting |
| | $V_{OCM}$ | 0.63 × $V_{DDA}$ | 0.8 × $V_{DDA}$ | 0.83 × $V_{DDA}$ | V | DC coupled 80% setting |


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**Table 5-42.** PolarFire Transceiver Transmitter Characteristics[14] (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Rise time[2] | $T_{TxRF}$ | 40 | — | 61 | ps | 20% to 80% |
| Fall time[2] | | 39 | — | 58 | ps | 80% to 20% |
| Differential peak-to-peak amplitude | $V_{ODPP}$ | 1080 | 1140 | 1320 | mV | 1000 mV setting |
| | $V_{ODPP}$ | 1010 | 1060 | 1220 | mV | 800 mV setting |
| | $V_{ODPP}$ | 550 | 580 | 670 | mV | 500 mV setting |
| | $V_{ODPP}$ | 465 | 490 | 560 | mV | 400 mV setting |
| | $V_{ODPP}$ | 350 | 370 | 425 | mV | 300 mV setting |
| | $V_{ODPP}$ | 250 | 260 | 300 | mV | 200 mV setting |
| | $V_{ODPP}$ | 150 | 160 | 185 | mV | 100 mV setting |
| Transmit lane P to N skew[3] | $T_{OSKEW}$ | — | 8 | 15 | ps | — |
| Lane to lane transmit skew[4] | $T_{LLSKEW}$ | — | — | 75 | ps | Single PLL, 2–4 bonded lanes, 8–40-bit fabric width[10] |
| | | — | — | 8 | UI | Single PLL, 2–4 bonded lanes, 64–80-bit fabric width[11] |
| | | — | — | 8 + Refclk skew | UI | Multiple PLL, 2–4 bonded lanes, 8–40-bit fabric width[11, 12] |
| | | — | — | 32 + Refclk skew | UI | Multiple PLL, 2–4 bonded lanes, 64–80-bit fabric width[11, 12] |
| Electrical idle transition entry time[7] | TTxEITrEntry | — | — | 20 | ns | — |
| Electrical idle transition exit time[7] | TTxEITrExit | — | — | 19 | ns | — |
| Electrical idle amplitude | VTxEIpp | — | — | 7 | mV | — |
| TXPLL lock time | $T_{TXLock}$ | — | — | 1600 | PFD cycles | — |
| Digital PLL lock time[8] | $T_{DPLLLock}$ | — | — | 75,000 | REFCLK UIs | Frequency lock |
| | | — | — | 150,000 | REFCLK UIs | Phase lock |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.22<br>0.1 | UI<br>UI | Data rate ≥10.3125 Gbps to 12.7 Gbps[9] (Tx $V_{CO}$ rate 5.16 GHz to 6.35 GHz)<br>TxPLL in Integer mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.28<br>0.1 | UI<br>UI | Data rate ≥10.3125 to 12.7 Gbps[9] (Tx $V_{CO}$ rate 5.16 GHz to 6.35 GHz)<br>TxPLL in Fractional mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.22<br>0.09 | UI<br>UI | Data rate ≥8.5 Gbps to 10.3125 Gbps (Tx $V_{CO}$ rate 4.25 GHz to 5.16 GHz)<br>TxPLL in Integer mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.28<br>0.09 | UI<br>UI | Data rate ≥8.5 Gbps to 10.3125 Gbps (Tx $V_{CO}$ rate 4.25 GHz to 5.16 GHz)<br>TxPLL in Fractional mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5,6] | $T_J$<br>$T_{DJ}$ | — | — | 0.21<br>0.09 | UI<br>UI | Data rate ≥5.0 Gbps to 8.5 Gbps (Tx $V_{CO}$ rate 2.5 GHz to 4.25 GHz)<br>TxPLL in Integer mode |


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**Table 5-42.** PolarFire Transceiver Transmitter Characteristics[14] (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.25<br>0.09 | UI<br>UI | Data rate ≥5.0 Gbps to 8.5 Gbps (Tx $V_{CO}$ rate 2.5 GHz to 4.25 GHz)<br>TxPLL in Fractional mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.17<br>0.03 | UI<br>UI | Data rate ≥1.6 Gbps to 5.0 Gbps (Tx $V_{CO}$ rate 1.6 GHz to 2.5 GHz)<br>TxPLL in Integer mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.2<br>0.03 | UI<br>UI | Data rate ≥1.6 Gbps to 5.0 Gbps (Tx $V_{CO}$ rate 1.6 GHz to 2.5 GHz)<br>TxPLL in Fractional mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.08<br>0.02 | UI<br>UI | Data rate ≥ 800 Mbps to 1.6 Gbps (Tx $V_{CO}$ rate 1.6 GHz)<br>TxPLL in Integer mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.11<br>0.02 | UI<br>UI | Data rate ≥ 800 Mbps to 1.6 Gbps (Tx $V_{CO}$ rate 1.6 GHz)<br>TxPLL in Fractional mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.05<br>0.01 | UI<br>UI | Data rate = 250 Mbps to 800 Mbps (Tx $V_{CO}$ rate 1.48 GHz to 1.6 GHz)<br>TxPLL in Integer mode |
| Total jitter[5, 6, 13]<br>Deterministic jitter[5, 6] | $T_J$<br>$T_{DJ}$ | — | — | 0.06<br>0.01 | UI<br>UI | Data rate = 250 Mbps to 800 Mbps (Tx $V_{CO}$ rate 1.48 GHz to 1.6 GHz)<br>TxPLL in Fractional mode |

1. Increased DC Common mode settings above 50% reduce allowed $V_{OD}$ output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same TxPLL. Multiple PLL applies to N lanes using multiple TxPLLs from different quad locations.
5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher $V_{CO}$ rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a $10^{-12}$ Bit Error Rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
8. FTxRefClk = 75 MHz with typical settings.
9. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.
10. Transmit alignment in this case will automatically align upon the Tx PLL obtaining lock. For details on transmit alignment, see PolarFire Family Transceiver User Guide.
11. In order to obtain the required alignment for these configurations, an FPGA fabric Tx alignment circuit must be implemented. For details on transmit alignment, see PolarFire Family Transceiver User Guide.
12. Refclk skew is the amount of skew between the reference clocks of the two PLL.
13. Jitter decomposition can be found in the protocol characterization reports.
14. Tx total jitter (Tj) is quoted for reference clock rise and fall times as specified in Table 5-36. If increased Tj is acceptable, the maximum reference clock input rise/fall times may be increased


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beyond the maximum specification shown in Table 5-36 when using single-ended configurations (LVCMOS and LVTTL).

a. Tj increases by 8% for 0.5 ns < $T_{RISE}/T_{FALL}$ ≤ 2.0 ns.

b. Tj increases by 25% for 2.0 ns < $T_{RISE}/T_{FALL}$ ≤ 5.0 ns.

c. Tj increases by 35% for 0.5 ns < $T_{RISE}/T_{FALL}$ ≤ 5.0 ns.

### 5.4.5. Receiver Performance

The following table describes performance of the receiver.

**Table 5-43.** PolarFire Transceiver Receiver Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{IN}$ | 0 | — | $V_{DDA}$ + 0.3 | V | — |
| Differential peak-to-peak amplitude | $V_{IDPP}$ | 140 | — | 1250 | mV | — |
| Differential termination | $V_{ITERM}$ | 68 | 85 | 102 | Ω | 85Ω setting |
| | | 80 | 100 | 120 | Ω | 100Ω setting |
| | | 120 | 150 | 180 | Ω | 150Ω setting |
| Common mode voltage [1] | $V_{ICMDC}$ | 0.7 × $V_{DDA}$ | — | 0.9 × $V_{DDA}$ | V | DC coupled |
| Exit electrical idle detection time | $T_{EIDET}$ | — | 50 | 100 | ns | — |
| Run length of Consecutive Identical Digits (CID) | $C_{ID}$ | — | — | 200 | UI | — |
| CDR frequency tolerance[2] | $F_{LRTOL}$ | –11700 | — | +11700 | ppm of line rate | Enhanced Receiver Management is disabled [14] |
| CDR lock-to-data time[13] | $T_{LTD}$ | 512 * $CDR_{REFDIV}$ | — | 1024 * $CDR_{REFDIV}$ | $CDR_{REFCLK}$ cycles | Enhanced Receiver Management is disabled [14] |
| | | (1900/$T_{CDRREF}$) + (512 + (1020 * ($W_{XCVRFABRX}$/$CDR_{FBDIV}$)) * $CDR_{REFDIV}$) | — | (5200/$T_{CDRREF}$) + (1024 + (6380 * ($W_{XCVRFABRX}$/$CDR_{FBDIV}$)) * $CDR_{REFDIV}$) | $CDR_{REFCLK}$ cycles | Enhanced Receiver Management is enabled [14] |
| CDR lock-to-ref time[13] | $T_{LTF}$ | (1000/$T_{CDRREF}$) + (1024 * $CDR_{REFDIV}$) | — | (13000/$T_{CDRREF}$) + (1536 * $CDR_{REFDIV}$) | $CDR_{REFCLK}$ cycles | — |
| High-gain lock time | $T_{HGLT}$ | 10.8 | — | — | ns | For Burst Mode Receiver (BMR) |
| High-gain state time[12] | $T_{HGSTATE}$ | — | — | 3264 | ns | For Burst Mode Receiver (BMR) |


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**Table 5-43.** PolarFire Transceiver Receiver Characteristics (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Loss-of-signal detect (peak detect range setting= high)[9,10] | $V_{DETHIGH}$ | 145 | — | 295 | mV | Setting = 3 |
| | | 155 | — | 340 | mV | Setting = 4 |
| | | 180 | — | 365 | mV | Setting = 5 |
| | | 195 | — | 375 | mV | Setting = 6 |
| | | 210 | — | 385 | mV | Setting = 7 |
| Loss-of-signal detect (peak detect range setting= low)[9,10] | $V_{DETLOW}$ | 65 | — | 175 | mV | Setting = PCIe[3, 7] |
| | | 95 | — | 190 | mV | Setting = SATA[4, 8] |
| | | 75 | — | 170 | mV | Setting = 1 |
| | | 95 | — | 185 | mV | Setting = 2 |
| | | 100 | — | 190 | mV | Setting = 3 |
| | | 140 | — | 210 | mV | Setting = 4 |
| | | 155 | — | 240 | mV | Setting = 5 |
| | | 165 | — | 245 | mV | Setting = 6 |
| | | 170 | — | 250 | mV | Setting = 7 |
| Sinusoidal jitter tolerance | $T_{SJTOL}$ | 0.34 | — | — | UI | >8.5 Gbps –12.7 Gbps[5, 11] |
| | | 0.43 | — | — | UI | >8.0–8.5 Gbps[5] |
| | | 0.45 | — | — | UI | >3.2–8.0 Gbps[5] |
| | | 0.45 | — | — | UI | >1.6 to 3.2 Gbps[5] |
| | | 0.42 | — | — | UI | >0.8 to 1.6 Gbps[5] |
| | | 0.41 | — | — | UI | 250 to 800 Mbps[5] |
| Total jitter tolerance with stressed eye | $T_{TJTOLSE}$ | 0.65 | — | — | UI | 3.125 Gbps[5] |
| | | 0.65 | — | — | UI | 6.25 Gbps[6] |
| | | 0.7 | — | — | UI | 10.3125 Gbps[6] |
| | | 0.7 | — | — | UI | 12.7 Gbps[6, 11] |
| Sinusoidal jitter tolerance with stressed eye | $T_{SJTOLSE}$ | 0.1 | — | — | UI | 3.125 Gbps[5] |
| | | 0.05 | — | — | UI | 6.25 Gbps[6] |
| | | 0.05 | — | — | UI | 10.3125 Gbps[6] |
| | | 0.05 | — | — | UI | 12.7 Gbps[6, 11] |
| CTLE DC gain (all stages, max settings) | — | 0.1 | — | 10 | dB | — |
| CTLE AC gain (all stages, max settings) | — | 0.05 | — | 16 | dB | — |
| DFE AC gain (per 5 stages, max settings) | — | 0.05 | — | 7.5 | dB | — |


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**Table 5-43.** PolarFire Transceiver Receiver Characteristics (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Auto adaptive calibration time (CTLE) | $T_{CTLE}$ | 12 | — | 45 | ms | — |
| Auto adaptive calibration time (CTLE+DFE) | $T_{CTLE+DFE}$ | — | 1.4 | — | s | — |
| Enhanced receiver management control clock input (CTRL_CLK) | $F_{ERMCTRLCLK}$ | 38.4 | 40 | 41.6 | MHz | — |

1. Valid at 3.2 Gbps and below.
2. Data vs Rx reference clock frequency.
3. Achieves compliance with PCIe electrical idle detection.
4. Achieves compliance with SATA OOB specification.
5. Rx jitter values based on Bit Error Ratio (BER) of 10–12, AC-coupled input with 400 mV $V_{ID}$, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.
6. Rx jitter values based on Bit Error Ratio (BER) of 10–12, AC-coupled input with 400 mV $V_{ID}$, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
7. For PCIe: Low Threshold Setting = 0, High Threshold Setting = 2.
8. For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
9. Loss of signal is valid for data rates of 1 Gbps to 5 Gbps for PRBS7 (8B/10B) or PRBS31 (64b/6xb) data formats. It is also valid for detection of SATA out-of-band signals at data rates up to 6 Gbps. If the default settings for the low threshold (0x0) and high threshold (0x2) using the low range option for the peak detector are used, then the Rx $V_{Amplitude}$ pk-pk (outside of data eye) at the receiver input package pins must be a minimum of 300 mV for short reach (6.5 dB insertion loss at 5 GHz) applications, 350 mV for medium reach (17.0 dB insertion loss at 5 GHz) applications, and 450 mV for long reach (25.0 dB insertion loss at 5 GHz) applications—generally the settings are less limiting than what is required for good BER operation of the SerDes. Note that if the option to force CDR Lock2Ref upon Rx Idle is set (default at data rates of 5 Gbps and below), this minimum $V_{Amplitude}$ pk-pk must be enforced for proper CDR operation.
10. Detect values measured at 1.5 Gbps with PRBS7 data pattern.
11. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.
12. $T_{HGSTATE}$ is based on the condition where the CDR was in lock (to reference or data) for at least 5.2 µs before moving to the high-gain state. At this point, if the receive data is outside the ppm tolerance of the CDR, the CDR will unlock after the time specified by the parameter.
13. The following definitions apply:
    a. $T_{CDRREF}$ is the transceiver CDR reference clock period in nanoseconds.
    b. $W_{XCVRFABRX}$ is the parallel interface width of the transceiver receive fabric interface.
    c. $CDR_{FBDIV}$ is the feedback divider of the transceiver.
    d. $CDR_{CDRREFDIV}$ is the reference divider of the transceiver CDR.
14. For details on the Enhanced Receiver Management feature, refer to the PolarFire Family Transceiver User Guide.


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### 5.4.6. Transceiver and Receiver Return Loss Characteristics

This section describes transmitter and receiver return loss characteristics compliant with OIF-CEI-03.1.

**Figure 5-7.** Differential Return Loss

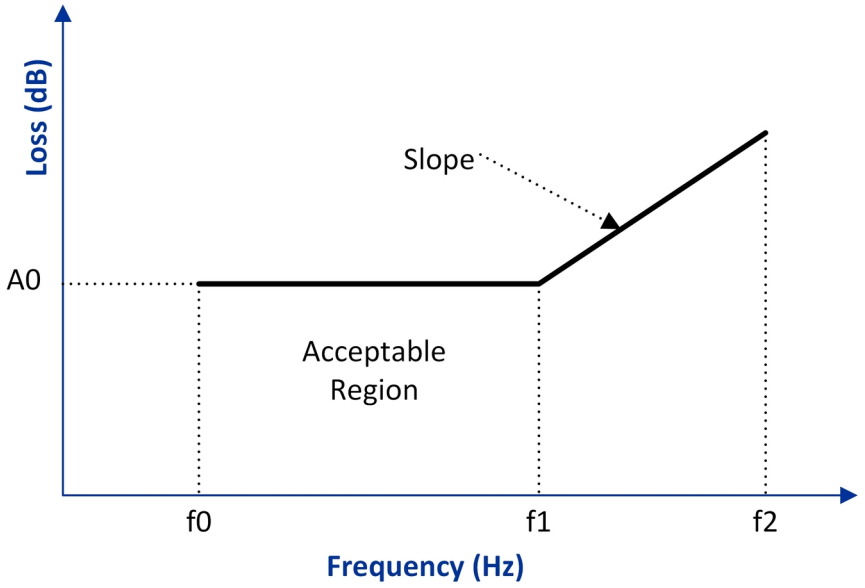


**Table 5-44.** Differential Return Loss

| Parameter | Value | Unit |
|---|---|---|
| A0 | –8 | dB |
| f0 | 100 | MHz |
| f1 | (3/4) * T_Baud | Hz |
| f2 | T_Baud | Hz |
| Slope | 16.6 | dB/dec |


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**Figure 5-8.** Common Mode Return Loss

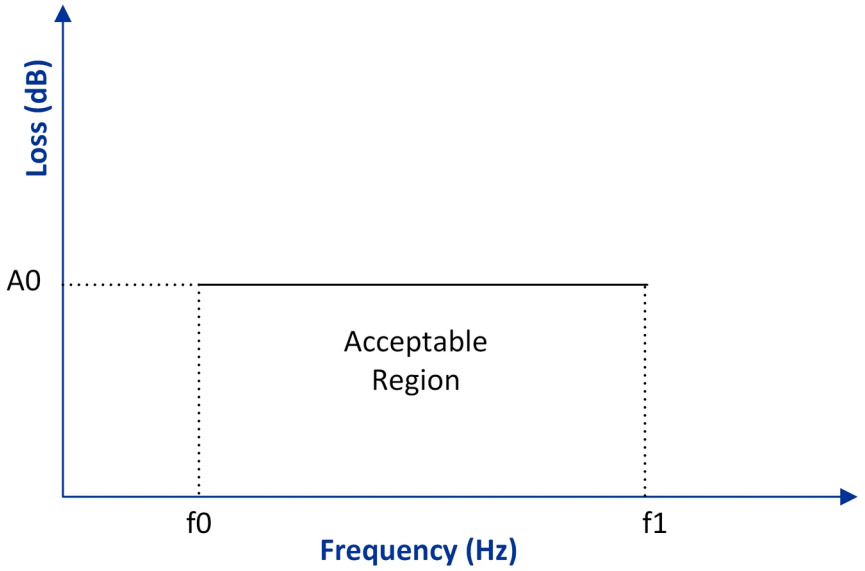


**Table 5-45.** Common Mode Return Loss

| Parameter | Value | Unit |
|---|---|---|
| A0 | –6 | dB |
| f0 | 100 | MHz |
| f1 | (3/4) * T_Baud | Hz |

## 5.5. Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics. This section is not applicable to PolarFire Core family of FPGAs that do not feature transceiver functionality. Refer to the PPAT for transceiver pin termination guidelines.

### 5.5.1. PCI Express

The following tables describe the PCI Express.

**Table 5-46.** PCI Express Gen1

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 2.5 Gbps | — | 0.25 | UI |
| Receiver jitter tolerance | 2.5 Gbps | 0.4 | — | UI |

**Note:** With add-in card, as specified in PCI Express CEM Rev 2.0.

**Table 5-47.** PCI Express Gen2

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 5.0 Gbps | — | 0.35 | UI |
| Receiver jitter tolerance | 5.0 Gbps | 0.4 | — | UI |

**Note:** With add-in card as specified in PCI Express CEM Rev 2.0.


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### 5.5.2. Interlaken

The following table describes Interlaken.

**Table 5-48.** Interlaken

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 6.375 Gbps | — | 0.3 | UI |
| | 10.3125 Gbps | — | 0.3 | UI |
| | 12.7 Gbps[1, 2] | — | 0.3 | UI |
| Receiver jitter tolerance | 6.375 Gbps | 0.6 | — | UI |
| | 10.3125 Gbps | 0.65 | — | UI |
| | 12.7 Gbps[1, 2] | 0.65 | — | UI |

1. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.
2. Supported on –1 speed grade only.

### 5.5.3. 10GbE (10GBASE-R and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

**Table 5-49.** 10GbE (10GBASE-R)

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 10.3125 Gbps | — | 0.28 | UI |
| Receiver jitter tolerance | 10.3125 Gbps | 0.7 | — | UI |

The following table describes 10GbE (10GBASE-KR).

**Table 5-50.** 10GbE (10GBASE-KR)

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 10.3125 Gbps | — | 0.28 | UI |
| Receiver jitter tolerance (SJ) | 10.3125 Gbps | 0.115 | — | UI |
| Receiver jitter tolerance (RJ) | 10.3125 Gbps | 0.13 | — | UI |
| Receiver jitter tolerance (DCD) | 10.3125 Gbps | 0.035 | — | UI |

The following table describes 10GbE (XAUI).

**Table 5-51.** 10GbE (XAUI)

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter (near end) | 3.125 Gbps | — | 0.35 | UI |
| Total transmit jitter (far end) | — | — | 0.55 | UI |
| Receiver jitter tolerance | 3.125 Gbps | 0.65 | — | UI |

The following table describes 10GbE (RXAUI).


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**Table 5-52.** 10GbE (RXAUI)

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter (near-end) | 6.25 Gbps | — | 0.35 | UI |
| Total transmit jitter (far-end) | 6.25 Gbps | — | 0.55 | UI |
| Receiver jitter tolerance | 6.25 Gbps | 0.65 | — | UI |

### 5.5.4. 1GbE (1000BASE-X)

The following table describes 1GbE (1000BASE-X).

**Table 5-53.** 1GbE (1000BASE-X)

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 1.25 Gbps | — | 0.24 | UI |
| Receiver jitter tolerance | 1.25 Gbps | 0.749 | — | UI |

### 5.5.5. SGMII and QSGMII

The following table describes SGMII.

**Table 5-54.** SGMII

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 1.25 Gbps | — | 0.24 | UI |
| Receiver jitter tolerance | 1.25 Gbps | 0.749 | — | UI |

The following table describes QSGMII.

**Table 5-55.** QSGMII

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 5.0 Gbps | — | 0.3 | UI |
| Receiver jitter tolerance | 5.0 Gbps | 0.65 | — | UI |

### 5.5.6. CPRI

The following table describes CPRI.

**Table 5-56.** CPRI

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 0.6144 Gbps | — | 0.35 | UI |
| | 1.2288 Gbps | — | 0.35 | UI |
| | 2.4576 Gbps | — | 0.35 | UI |
| | 3.0720 Gbps | — | 0.35 | UI |
| | 4.9152 Gbps | — | 0.3 | UI |
| | 6.1440 Gbps | — | 0.3 | UI |
| | 8.11008 Gbps | — | 0.335 | UI |
| | 9.8304 Gbps | — | 0.335 | UI |


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**Table 5-56.** CPRI (continued)

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Receive jitter tolerance | 0.6144 Gbps | 0.75 | — | UI |
| | 1.2288 Gbps | 0.75 | — | UI |
| | 2.4576 Gbps | 0.75 | — | UI |
| | 3.0720 Gbps | 0.75 | — | UI |
| | 4.9152 Gbps | 0.7 | — | UI |
| | 6.1440 Gbps | 0.7 | — | UI |
| | 8.11008 Gbps | 0.7 | — | UI |
| | 9.8304 Gbps | 0.7 | — | UI |

### 5.5.7. JESD204B

The following table describes JESD204B.

**Table 5-57.** JESD204B

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 3.125 Gbps | — | 0.35 | UI |
| | 6.25 Gbps | — | 0.3 | UI |
| | 12.5 Gbps[1, 2] | — | 0.3 | UI |
| Receive jitter tolerance | 3.125 Gbps | 0.56 | — | UI |
| | 6.25 Gbps | 0.6 | — | UI |
| | 12.5 Gbps[1, 2] | 0.7 | — | UI |

1. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.
2. Supported on –1 speed grade only.

### 5.5.8. Display Port

The following table describes Display Port.

**Table 5-58.** Display Port

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 1.62 Gbps | Test point: TP2 | — | 0.27 | UI |
| | 2.7 Gbps | Test point: TP2 | — | 0.42 | UI |
| | 5.4 Gbps | Test point: TP3_EQ | — | 0.62[1] | UI |
| | 8.1 Gbps | Test point: TP3_CTLE | — | 0.47 | UI |
| Total receive jitter tolerance | 1.62 Gbps | SJ at 20 MHz | 0.747 | — | UI |
| | 2.7 Gbps | SJ at 100 MHz | 0.491 | — | UI |
| | 5.4 Gbps | SJ at 10 MHz | 0.636 | — | UI |
| | | SJ at 100 MHz | 0.62 | — | UI |
| | 8.1 Gbps | SJ at 15 MHz | 0.62 | — | UI |

1. Total transmit jitter includes 0.04 UI from cable crosstalk effect.


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### 5.5.9. Serial RapidIO

The following table describes Serial RapidIO.

**Table 5-59.** Serial RapidIO

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 1.25 Gbps | — | — | 0.35 | UI |
| | 2.5 Gbps | — | — | 0.35 | UI |
| | 3.125 Gbps | — | — | 0.35 | UI |
| | 5.0 Gbps | — | — | 0.3 | UI |
| | 6.25 Gbps | — | — | 0.3 | UI |
| | 10.3125 Gbps | — | — | 0.28 | UI |
| Receive jitter tolerance | 1.25 Gbps | — | 0.65 | — | UI |
| | 2.5 Gbps | — | 0.65 | — | UI |
| | 3.125 Gbps | — | 0.65 | — | UI |
| | 5.0 Gbps | Short reach | 0.6 | — | UI |
| | | Long reach | 0.95 | — | UI |
| | 6.25 Gbps | Short reach | 0.6 | — | UI |
| | | Long reach | 0.95 | — | UI |
| | 10.3125 Gbps | Short reach | 0.62 | — | UI |

### 5.5.10. SDI

The following table describes SDI.


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**Table 5-60.** SDI

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 270 Mbps | Timing jitter (10 Hz–27 MHz) | — | 0.2 | UI |
| | | Alignment jitter (1 KHz–27 MHz) | — | 0.2 | UI |
| | 1.485 Gbps | Timing jitter (10 Hz–148.5 MHz) | — | 1.0 | UI |
| | | Alignment jitter (100 KHz–148.5 MHz) | — | 0.2 | UI |
| | 2.97 Gbps | Timing jitter (10 Hz–297 MHz) | — | 2.0 | UI |
| | | Alignment jitter (100 KHz–297 MHz) | — | 0.3 | UI |
| | 5.94 Gbps | Timing jitter (10 Hz–594 MHz) | — | 2.0 | UI |
| | | Alignment jitter (100 KHz–594 MHz) | — | 0.3 | UI |
| | 11.88 Gbps | Timing jitter (10 Hz–1188 MHz) | — | 2.0 | UI |
| | | Alignment jitter (100 KHz–1188 MHz) | — | 0.3 | UI |
| Receive jitter tolerance | 270 Mbps | Alignment jitter | 0.2 | — | UI |
| | 1.485 Gbps | Alignment jitter | 0.2 | — | UI |
| | 2.97 Gbps | Alignment jitter | 0.3 | — | UI |
| | 5.94 Gbps | Alignment jitter | 0.3 | — | UI |
| | 11.88 Gbps | Alignment jitter | 0.3 | — | UI |

## 5.5.11. OTN

The following table describes OTN.

**Table 5-61.** OTN

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 2.66 Gbps | 3 dB BW: 5 KHz to 20 MHz | — | 0.3 | UI |
| | | 3 dB BW: 1 MHz to 20 MHz | — | 0.1 | UI |
| | 10.70 Gbps[2] | 3 dB BW: 20 KHz to 80 MHz | — | 0.3 | UI |
| | | 3 dB BW: 4 MHz to 80 MHz | — | 0.1 | UI |
| | 11.09 Gbps[1] | 3 dB BW: 20 KHz to 80 MHz | — | 0.3 | UI |
| | | 3 dB BW: 4 MHz to 80 MHz | — | 0.1 | UI |
| Receive jitter tolerance | 2.66 Mbps | SJ at 5 KHz | 1.5 | — | UI |
| | | SJ at 20 MHz | 0.15 | — | UI |
| | 10.70 Gbps[2] | SJ at 20 KHz | 1.5 | — | UI |
| | | SJ at 80 MHz | 0.15 | — | UI |
| | 11.09 Gbps[1, 2] | SJ at 20 KHz | 1.5 | — | UI |
| | | SJ at 80 MHz | 0.15 | — | UI |


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1. For data rates greater than 10.3125 Gbps, $V_{DDA}$ must be set to 1.05V mode. See supply tolerance in the section Recommended Operating Conditions.
2. Supported on –1 speed grade only.

### 5.5.12. Fiber Channel

The following table describes Fiber Channel.

**Table 5-62.** Fiber Channel

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 1.0625 Gbps | — | — | 0.23 | UI |
| | 2.125 Gbps | — | — | 0.33 | UI |
| | 4.25 Gbps | — | — | 0.52 | UI |
| | 8.5 Gbps | — | — | 0.31 | UI |
| Receive jitter tolerance | 1.0625 Gbps | 0.68 | — | — | UI |
| | 2.125 Gbps | 0.62 | — | — | UI |
| | 4.24 Gbps | 0.62 | — | — | UI |
| | 8.5 Gbps | 0.71 | — | — | UI |

### 5.5.13. HiGig and HiGig+

The following table describes HiGig and HiGig+.

**Table 5-63.** HiGig and HiGig+

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 3.75 Gbps | Near-end | — | 0.35 | UI |
| | 3.75 Gbps | Far-end | — | 0.55 | UI |
| Receive jitter tolerance | 3.75 Gbps | — | 0.65 | — | UI |

### 5.5.14. HiGig II

The following table describes HiGig II.

**Table 5-64.** HiGig II

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 6.875 Gbps | Near-end | — | 0.35 | UI |
| | 6.875 Gbps | Far-end | — | 0.55 | UI |
| Receive jitter tolerance | 6.875 Gbps | — | 0.65 | — | UI |

### 5.5.15. FireWire IEEE® 1394

The following table describes FireWire IEEE® 1394.

**Table 5-65.** FireWire IEEE® 1394

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 196.608 Mbps | S200 Near-end[1] | — | 200 | ps |
| | 393.22 Mbps | S400 Near-end[2] | — | 516 | ps |
| | 786.43 Mbps | S800 Near-end[2, 3] | — | 200 | ps |


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**Table 5-65.** FireWire IEEE® 1394 (continued)

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Receive jitter tolerance | 196.608 Mbps | S200[1] | 500 | — | ps |
| | 393.22 Mbps | S400[2] | 1025 | — | ps |
| | 786.43 Mbps | S800[2] | 375 | — | ps |

1. DS mode.
2. Beta mode.
3. PolarFire complies with 1394 S800 electrical requirements with the exception of Tx eye requirement. For more details, refer to the PolarFire FPGA FireWire Characterization Report.

### 5.5.16. SLVS-EC

The following table describes SLVS-EC.

**Table 5-66.** SLVS-EC

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 2.376 Gbps | — | — | 0.4 | UI |
| Receive jitter tolerance | 2.376 Gbps | 0.15 SJ at 2 MHz | 0.5 | — | UI |
| | 5.0 Gbps | 0.15 SJ at 4 MHz | 0.5 | — | UI |

## 5.6. Non-Volatile Characteristics

The following section describes non-volatile characteristics.

### 5.6.1. FPGA and µPROM Programming Cycle and Retention

The following table describes FPGA and µPROM programming cycle and retention characteristics. Programming, zeroization, and verify operations all count as a programming cycle.

Retention characteristics for Military-grade devices and Automotive-grade devices at the absolute maximum junction temperature of 125°C can be profiled using the PolarFire Retention Calculator, which can be obtained under NDA in the Secure Document Extranet. Refer the Secure Document User Guide.

**Table 5-67.** FPGA and µPROM Programming Cycles vs. Retention Characteristics[1]

| Programming $T_J$ | Programming Cycles, Max | Retention Years | Retention Years at $T_J$ |
|---|---|---|---|
| 0°C to 85°C | 1000 | 20 | 85°C |
| 0°C to 100°C | 500 | 20 | 100°C |
| –20°C to 100°C | 500 | 20 | 100°C |
| –40°C to 100°C | 500 | 20 | 100°C |
| –40°C to 85°C | 1000 | 16 | 100°C |
| –40°C to 55°C | 2000 | 12 | 100°C |
| –40°C to 100°C | 500 | 20 | 100°C |
| –40°C to 100°C | 500 | 10 | 110°C |
| –40°C to 100°C | 500 | Note 2 | 125°C |

**Notes:**

1. Power supplied to the device must be valid during programming operations such as programming and verify. Programming recovery mode is available only for in-application programming mode and requires an external SPI Flash.


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2. Contact technical support at microchip.com/support.

### 5.6.2. FPGA Programming Time

The following tables describe FPGA programming time. For allowable programming junction temperature ($T_J$), see previous table FPGA and µPROM Programming Cycles vs. Retention Characteristics.

**Table 5-68.** SPI Initiator and Auto-Update Programming Time (IAP)

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | $T_{PROG}$ | MPF050T, TL, TS, TLS, TC | 23.4 | 29.2 | s |
| | | MPF100T, TL, TS, TLS, TC | 17 | 31.3 | s |
| | | MPF200T, TL, TS, TLS, TC | 17 | 31.3 | s |
| | | MPF300T, TL, TS, TLS, TC | 26 | 40 | s |
| | | MPF500T, TL, TS, TLS, TC | 31 | 46.3 | s |

**Table 5-69.** SPI Target Programming Time

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | $T_{PROG}$ | MPF050T, TL, TS, TLS, TC[1, 2] | 26.6 | 29.7 | s |
| | | MPF100T, TL, TS, TLS, TC[1, 2] | 27 | 36.3 | s |
| | | MPF200T, TL, TS, TLS, TC[1, 2] | 41 | 55 | s |
| | | MPF300T, TL, TS, TLS, TC[1, 2] | 50 | 66 | s |
| | | MPF500T, TL, TS, TLS, TC[1, 2] | 90 | 118.8 | s |

1. SmartFusion® 2 as SPI Initiator with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.
2. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel® i7 at 3.6 GHz, 32 GB RAM, Windows® 10.


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**Table 5-70.** JTAG Programming Time

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | $T_{PROG}$ | MPF050T, TL, TS, TLS, TC[1] | 27.2 | 30.8 | s |
| | | MPF100T, TL, TS, TLS, TC[1] | 35 | 46.2 | s |
| | | MPF200T, TL, TS, TLS, TC[1] | 56 | 74.8 | s |
| | | MPF300T, TL, TS, TLS, TC[1] | 95 | 125.4 | s |
| | | MPF500T, TL, TS, TLS, TC[1] | 122 | 161.7 | s |

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel® i7 at 3.6 GHz, 32 GB RAM, Windows® 10.

### 5.6.3. FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

**Table 5-71.** Initialization Client Sizes

| Device | Plaintext | Ciphertext |
|---|---|---|
| MPF050T, TL, TS, TLS, TC | 706KB | 729 KB |
| MPF100T, TL, TS, TLS, TC | 1580 KB | 1630 KB |
| MPF200T, TL, TS, TLS, TC | 2916 KB | 3006 KB |
| MPF300T, TL, TS, TLS, TC | 4265 KB | 4403 KB |
| MPF500T, TL, TS, TLS, TC | 6835 KB | 7045 KB |

**Note:** Worst case initializing all fabric LSRAM, USRAM, and UPROM.

**Table 5-72.** Bitstream Sizes

| File | Devices | FPGA | Security | SNVM (all pages) | FPGA+ SNVM | SNVM+ Sec | FPGA+ SNVM+ Sec |
|---|---|---|---|---|---|---|---|
| SPI | MPF050T, TL, TS, TLS, TC | 1593 KB | — | 59.7 KB | 1643 KB | — | — |
| DAT | MPF050T, TL, TS, TLS, TC | 1594 KB | 8 KB | 61.2 KB | 1645 KB | — | 1650 KB |
| SPI | MPF100T, TL, TS, TLS, TC | 3400 KB | — | 59.7 KB | 3500 KB | — | — |
| DAT | MPF100T, TL, TS, TLS, TC | 3400 KB | 7.6 KB | 61.2 KB | 3500 KB | 66.3 KB | 3500 KB |
| SPI | MPF200T, TL, TS, TLS, TC | 5900 KB | — | 59.7 KB | 5900 KB | — | — |
| DAT | MPF200T, TL, TS, TLS, TC | 5900 KB | 7.6 KB | 61.2 KB | 6000 KB | 66.3 KB | 6000 KB |
| SPI | MPF300T, TL, TS, TLS, TC | 9300 KB | — | 59.7 KB | 9600 KB | — | — |
| DAT | MPF300T, TL, TS, TLS, TC | 9300 KB | 7.6 KB | 61.2 KB | 9600 KB | 66.3 KB | 9600 KB |
| SPI | MPF500T, TL, TS, TLS, TC | 14300 KB | — | 59.7 KB | 14400 KB | — | — |


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**Table 5-72.** Bitstream Sizes (continued)

| File | Devices | FPGA | Security | SNVM (all pages) | FPGA+ SNVM | SNVM+ Sec | FPGA+ SNVM+ Sec |
|---|---|---|---|---|---|---|---|
| DAT | MPF500T, TL, TS, TLS, TC | 14300 KB | 7.6 KB | 61.2 KB | 14400 KB | 66.3 KB | 14400 KB |

### 5.6.4. Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag. Digests are operational only from –40°C to 100°C.

**Table 5-73.** Maximum Number of Digest Cycles

| Retention Since Programmed (N = Number Digests During that Time)[1] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Storage and Operating $T_J$ | N ≤300 | N = 500 | N = 1000 | N = 1500 | N = 2000 | N = 4000 | N = 6000 | Unit | Retention |
| –40 to 100 | 20 × LF | 17 × LF | 12 × LF | 10 × LF | 8 × LF | 4 × LF | 2 × LF | °C | Years |
| 0 to 100 | 20 × LF | 17 × LF | 12 × LF | 10 × LF | 8 × LF | 4 × LF | 2 × LF | °C | Years |
| –40 to 85 | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 16 × LF | 8 × LF | 4 × LF | °C | Years |
| –40 to 55 | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | °C | Years |
| –40 to 110 | 10 × LF | 8.5 × LF | 6 × LF | 5 × LF | 4 × LF | 2 × LF | 1 × LF | °C | Years |
| –40 to 125 | Note 2 | | | | | | | | |
| –55 to 110 | 10 × LF | 8.5 × LF | 6 × LF | 5 × LF | 4 × LF | 2 × LF | 1 × LF | °C | Years |
| –55 to 125 | Note 2 | | | | | | | | |

1. LF = Lifetime Factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.
2. Contact technical support at microchip.com/support.

**Table 5-74.** FPGA Programming Cycles Lifetime Factor

| Programming $T_J$ | Programming Cycles | LF |
|---|---|---|
| –40°C to 100°C | 500 | 1 |
| –40°C to 85°C | 1000 | 0.8 |
| –40°C to 55°C | 2000 | 0.6 |

**Notes:**

- The maximum number of accumulated device digest cycles is 100K. The maximum number of digests is 10K cycles between programming non-volatile data (fabric sNVM, user keys, user locks, and so on).
- Digests are operational only over the –40°C to 100°C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures ($T_J$).
- **Example 1:** 500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40°C to 85°C $T_J$. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.


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- **Example 2:** One programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40°C to 100°C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

### 5.6.5. Digest Time

The following table describes digest time.

**Table 5-75.** Digest Times

| Parameter | Devices | Typ | Max | Unit | Libero Description |
|---|---|---|---|---|---|
| Setup time | All | 2 | — | µs | — |
| Fabric digest run time | MPF050T, TL, TS, TLS, TC | 962 | 1203.8 | ms | Fabric digest |
| | MPF100T, TL, TS, TLS, TC | 880 | 1137.5 | ms | Fabric digest |
| | MPF200T, TL, TS, TLS, TC | 1005 | 1337.5 | ms | Fabric digest |
| | MPF300T, TL, TS, TLS, TC | 1503.9 | 1977.5 | ms | Fabric digest |
| | MPF500T, TL, TS, TLS, TC | 2085 | 2687.5 | ms | Fabric digest |
| UFS CC digest run time | MPF050T, TL, TS, TLS, TC | 34 | 43.8 | µs | Fabric digest |
| | MPF100T, TL, TS, TLS, TC | 33.5 | 43.8 | µs | Fabric digest |
| | MPF200T, TL, TS, TLS, TC | 33.5 | 43.8 | µs | Fabric digest |
| | MPF300T, TL, TS, TLS, TC | 33.5 | 43.8 | µs | Fabric digest |
| | MPF500T, TL, TS, TLS, TC | 33.5 | 43.8 | µs | Fabric digest |
| sNVM digest run time[1] | MPF050T, TL, TS, TLS, TC | 4.54 | 6.3 | ms | sNVM digest |
| | MPF100T, TL, TS, TLS, TC | 4.5 | 6.3 | ms | sNVM digest |
| | MPF200T, TL, TS, TLS, TC | 4.5 | 6.3 | ms | sNVM digest |
| | MPF300T, TL, TS, TLS, TC | 4.5 | 6.3 | ms | sNVM digest |
| | MPF500T, TL, TS, TLS, TC | 4.5 | 6.3 | ms | sNVM digest |
| UFS UL digest run time | MPF050T, TL, TS, TLS, TC | 47 | 61.3 | µs | Security digest |
| | MPF100T, TL, TS, TLS, TC | 47 | 61.3 | µs | Security digest |
| | MPF200T, TL, TS, TLS, TC | 47 | 61.3 | µs | Security digest |
| | MPF300T, TL, TS, TLS, TC | 47 | 61.3 | µs | Security digest |
| | MPF500T, TL, TS, TLS, TC | 47 | 61.3 | µs | Security digest |
| User key digest run time[2] | MPF050T, TL, TS, TLS, TC | 631.5 | 790 | µs | Security digest |
| | MPF100T, TL, TS, TLS, TC | 526 | 680 | µs | Security digest |
| | MPF200T, TL, TS, TLS, TC | 526 | 680 | µs | Security digest |
| | MPF300T, TL, TS, TLS, TC | 526 | 680 | µs | Security digest |
| | MPF500T, TL, TS, TLS, TC | 526 | 680 | µs | Security digest |
| UFS UPERM digest run time | MPF050T, TL, TS, TLS, TC | 34 | 43.8 | µs | Standalone digest |
| | MPF100T, TL, TS, TLS, TC | 33.2 | 43.8 | µs | Standalone digest |
| | MPF200T, TL, TS, TLS, TC | 33.2 | 43.8 | µs | Standalone digest |
| | MPF300T, TL, TS, TLS, TC | 33.2 | 43.8 | µs | Standalone digest |
| | MPF500T, TL, TS, TLS, TC | 33.2 | 43.8 | µs | Standalone digest |


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**Table 5-75.** Digest Times (continued)

| Parameter | Devices | Typ | Max | Unit | Libero Description |
|---|---|---|---|---|---|
| Factory digest run time | MPF050T, TL, TS, TLS, TC | 494 | 621.3 | µs | Standalone digest |
| | MPF100T, TL, TS, TLS, TC | 494 | 638.8 | µs | Standalone digest |
| | MPF200T, TL, TS, TLS, TC | 494 | 638.8 | µs | Standalone digest |
| | MPF300T, TL, TS, TLS, TC | 494 | 638.8 | µs | Standalone digest |
| | MPF500T, TL, TS, TLS, TC | 494 | 638.8 | µs | Standalone digest |

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

**Note:** These times do not include the power-up to functional timing overhead when using digest checks on power-up.

### 5.6.6. Zeroization Time

The time taken to zeroize any or all configuration elements in response to a tamper event is detailed in this section.

**Table 5-76.** Zeroization Mode: Like New

| Parameter | MPF050T | | MPF100T | | MPF200T | | MPF300T | | MPF500T | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | | |
| Time to enter zeroization | 6.9 | 7.6 | 7.3 | 8.0 | 7.3 | 8.0 | 7.2 | 8.0 | 7.5 | 8.3 | ms | Zeroization-In-Progress (ZIP) flag is set |
| Time to destroy the data[1] | 442.4 | 486.7 | 473.2 | 520.5 | 464.6 | 511 | 469.1 | 516 | 478.4 | 526.2 | ms | Data erased, one scrubbing |
| Time to scrub the data (like new)[2] | 6.9 | 7.6 | 7.4 | 8.2 | 7.3 | 8 | 7.4 | 8.1 | 7.5 | 8.2 | s | Full scrubbing |
| Total time to zeroize (like new)[3] | 8.7 | 9.6 | 8.8 | 9.7 | 8.7 | 9.6 | 9.3 | 10.2 | 10.6 | 11.7 | s | Verification complete |

**Table 5-77.** Zeroization Mode: Non-Recoverable

| Parameter | MPF050T | | MPF100T | | MPF200T | | MPF300T | | MPF500T | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | | |
| Time to enter zeroization | 7.1 | 7.8 | 7.5 | 8.3 | 7.5 | 8.3 | 7.5 | 8.2 | 7.7 | 8.5 | ms | Zeroization-In-Progress (ZIP) flag is set |


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**Table 5-77.** Zeroization Mode: Non-Recoverable (continued)

| Parameter | MPF050T | | MPF100T | | MPF200T | | MPF300T | | MPF500T | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | | |
| Time to destroy the data[1] | 462.5 | 508.7 | 494.6 | 544.1 | 485.9 | 534.5 | 490.8 | 539.8 | 500.4 | 550.5 | ms | Data erased, one scrubbing |
| Time to scrub the data (non-recoverable)[2] | 7.9 | 8.7 | 8.5 | 9.3 | 8.3 | 9.2 | 8.4 | 9.2 | 8.5 | 9.4 | s | Full scrubbing |
| Total time to zeroize (non-recoverable)[3] | 9.7 | 10.7 | 9.9 | 10.9 | 9.8 | 10.7 | 10.4 | 11.4 | 10.8 | 11.8 | s | Verification complete |

**Note:**

1. Time to enter zeroization, erase fabric, and scrub pNVM once.
2. Time to enter zeroization, erase fabric and scrub pNVM once, and a full scrub of the pNVM and fabric.
3. Time to enter zeroization, erase fabric and scrub pNVM once, and a full scrub of the pNVM and fabric, and verify.

### 5.6.7. Verify Time

The following tables describe verify time.

**Table 5-78.** Standalone Fabric Verify Times

| Parameter | Devices | Max | Unit |
|---|---|---|---|
| Standalone verification over JTAG | MPF050T, TL, TS, TLS, TC[1] | 13.75 | s |
| | MPF100T, TL, TS, TLS, TC[1] | 41.25 | s |
| | MPF200T, TL, TS, TLS, TC[1] | 66.25 | s |
| | MPF300T, TL, TS, TLS, TC[1] | 112.5 | s |
| | MPF500T, TL, TS, TLS, TC[1] | 142.5 | s |
| Standalone verification over SPI | MPF050T, TL, TS, TLS, TC[2] | 15 | s |
| | MPF100T, TL, TS, TLS, TC[2] | 30 | s |
| | MPF200T, TL, TS, TLS, TC[2] | 46.25 | s |
| | MPF300T, TL, TS, TLS, TC[2] | 68.75 | s |
| | MPF500T, TL, TS, TLS, TC[2] | 111.25 | s |

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel® i7 at 3.6 GHz, 32 GB RAM, Windows® 10.
2. SmartFusion® 2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

**Notes:**


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- Standalone verify is limited to 2,000 total verify hours over the industrial –40°C to 100°C temperature. For example, 2,000 hours = 7.2M seconds. The MPF300T device has a 90-second verify time over JTAG. This equates to 80,000 verify operations for the life of the MPF300T device.
- Use the digest system service for verify times greater than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

**Table 5-79.** Verify Time by Programming Hardware

| Devices | IAP | FlashPro4 | FlashPro5 | BP | Silicon Sculptor | Units |
|---|---|---|---|---|---|---|
| MPF050T, TL, TS, TLS, TC | 5 | 15.2 | 15.2 | — | — | s |
| MPF100T, TL, TS, TLS, TC | 6 | 42 | 33 | — | — | s |
| MPF200T, TL, TS, TLS, TC | 9 | 67 | 53 | — | — | s |
| MPF300T, TL, TS, TLS, TC | 14 | 95 | 90 | — | — | s |
| MPF500T, TL, TS, TLS, TC | 15 | 169 | 114 | — | — | s |

**Notes:**

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel® i7 at 3.6 GHz, 32 GB RAM, Windows® 10.

**Table 5-80.** Verify System Services

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| In-application verify by index | $T_{IAP_Ver_Index}$ | 44H | MPF050T, TL, TS, TLS, TC | 5.26 | 5.61 | s |
| | | | MPF100T, TL, TS, TLS, TC | 5.9 | 6.6 | s |
| | | | MPF200T, TL, TS, TLS, TC | 8.2 | 9.59 | s |
| | | | MPF300T, TL, TS, TLS, TC | 12.4 | 13.85 | s |
| | | | MPF500T, TL, TS, TLS, TC | 13.4 | 14.91 | s |
| In-application verify by SPI address | $T_{IAP_Ver_Addr}$ | 45H | MPF050T, TL, TS, TLS, TC | 5.26 | 5.6 | s |
| | | | MPF100T, TL, TS, TLS, TC | 5.9 | 6.6 | s |
| | | | MPF200T, TL, TS, TLS, TC | 8.2 | 9.59 | s |
| | | | MPF300T, TL, TS, TLS, TC | 12.4 | 13.85 | s |
| | | | MPF500T, TL, TS, TLS, TC | 13.4 | 14.91 | s |


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### 5.6.8. Authentication Time

The following tables describe authentication system service time.

**Table 5-81.** Authentication Services

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Bitstream authentication | $T_{BIT_AUTH}$ | 23H | MPF050T, TL, TS, TLS, TC | 1.1 | 1.4 | s |
| | | | MPF100T, TL, TS, TLS, TC | 2.1 | 3 | s |
| | | | MPF200T, TL, TS, TLS, TC | 3.3 | 4.6 | s |
| | | | MPF300T, TL, TS, TLS, TC | 4.9 | 6.8 | s |
| | | | MPF500T, TL, TS, TLS, TC | 7.6 | 9.8 | s |
| IAP image authentication | $T_{IAP_AUTH}$ | 22H | MPF050T, TL, TS, TLS, TC | **1.1** | 1.4 | s |
| | | | MPF100T, TL, TS, TLS, TC | 2.1 | 3 | s |
| | | | MPF200T, TL, TS, TLS, TC | 3.3 | 4.6 | s |
| | | | MPF300T, TL, TS, TLS, TC | 4.9 | 6.8 | s |
| | | | MPF500T, TL, TS, TLS, TC | 7.6 | 9.8 | s |

### 5.6.9. Secure NVM Performance

The following table describes secure NVM performance.

**Table 5-82.** sNVM Read/Write Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Plain text programming | — | 7 | 7.2 | 9.9 | ms | — |
| Authenticated text programming | — | 7.2 | 7.4 | 11.8 | ms | — |
| Authenticated and encrypted text programming | — | 7.2 | 7.4 | 11.8 | ms | — |
| Authentication R/W 1st access from power-up overhead | $T_{PUF_OVHD}$ | 10 | 13 | 138.8 | ms | From $T_{FAB_READY}$ |
| Plain text read | — | 8 | 8.5 | 11.3 | µs | — |
| Authenticated text read | — | 113 | 114.5 | 148.8 | µs | — |
| Authenticated and decrypted text read | — | 159 | 161 | 208.8 | µs | — |


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**Notes:**

- Page size = 256 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- $T_{PUF_OVHD}$ is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

### 5.6.10. Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

**Table 5-83.** sNVM Programming Cycles vs. Retention Characteristics[1]

| Programming Temperature | Programming Cycles per Page, Max | Programming Cycles per Block, Max | Retention Years |
|---|---|---|---|
| –40°C to 100°C | 10,000 | 100,000 | 20 |
| –40°C to 85°C | 10,000 | 100,000 | 20 |
| –40°C to 55°C | 10,000 | 100,000 | 20 |
| –40°C to 125°C | 10,000 | 100,000 | Note 2 |
| –55°C to 125°C | 10,000 | 100,000 | Note 2 |

**Notes:**

1. Page size = 256 bytes. Block size = 56 KBytes.
2. Contact technical support at microchip.com/support.

## 5.7. System Services

This section describes system switching and throughput characteristics.

### 5.7.1. System Services Throughput Characteristics

The following table describes system services throughput characteristics.

**Table 5-84.** System Services Throughput Characteristics[6]

| Parameter | Symbol | Service ID | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Serial number | $T_{Serial}$ | 00H | 65 | 86.3 | µs | — |
| User code | $T_{User}$ | 01H | 2.2 | 2.9 | µs | — |
| Design information | $T_{Design}$ | 02H | 3.6 | 4.8 | µs | — |
| Device certificate | $T_{Cert}$ | 03H | 255 | 331.3 | ms | — |
| Read digests | $T_{digest_read}$ | 04H | 252 | 328.8 | µs | — |
| Query security locks | $T_{sec_Query}$ | 05H | 80 | 105 | µs | — |
| Read debug information | $T_{Rd_debug}$ | 06H | 37 | 48.8 | µs | — |
| Reserved | — | 07H–0FH | — | — | — | — |
| Secure NVM write plain text | $T_{SNVM_Wr_Plain}$ | 10H | — | — | — | Note 1 |
| Secure NVM write authenticated plain text | $T_{SNVM_Wr_Auth}$ | 11H | — | — | — | Note 1 |


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**Table 5-84.** System Services Throughput Characteristics[6] (continued)

| Parameter | Symbol | Service ID | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Secure NVM write authenticated cipher text | $T_{SNVM_Wr_Cipher}$ | 12H | — | — | — | Note 1 |
| Reserved | — | 13H–17H | — | — | — | — |
| Secure NVM read | $T_{SNVM_Rd}$ | 18H | — | — | — | Note 1 |
| Digital signature service raw | $T_{SIG_RAW}$ | 19H | 174 | 226.3 | ms | — |
| Digital signature service DER | $T_{SIG_DER}$ | 1AH | 174 | 226.3 | ms | — |
| Reserved | — | 1BH–1FH | — | — | — | — |
| PUF emulation | $T_{Challenge}$ | 20H | 11.2 | 14.6 | ms | — |
| Nonce service | $T_{Nonce}$ | 21H | 10.7 | 13.9 | ms | — |
| Bitstream authentication | $T_{BIT_AUTH}$ | 22H | — | — | — | Note 4 |
| IAP Image authentication | $T_{IAP_AUTH}$ | 23H | — | — | — | Note 4 |
| Reserved | — | 26H–3FH | — | — | — | — |
| In-application programming by index | $T_{IAP_Prg_Index}$ | 42H | — | — | — | Note 2 |
| In-application programming by SPI address | $T_{IAP_Prg_Addr}$ | 43H | — | — | — | Note 2 |
| In-application verify by index | $T_{IAP_Ver_Index}$ | 44H | — | — | — | Note 5 |
| In-application verify by SPI address | $T_{IAP_Ver_Addr}$ | 45H | — | — | — | Note 5 |
| Auto update | $T_{AutoUpdate}$ | 46H | — | — | — | Note 2 |
| Digest check | $T_{digest_chk}$ | 47H | — | — | — | Note 3 |

1. See Table 5-82.
2. See Table 5-68.
3. See Table 5-75.
4. See Table 5-81.
5. See Table 5-80.
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

## 5.8. Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, PF_SPI, system controller, and temper detectors and dynamic reconfiguration.

### 5.8.1. UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.


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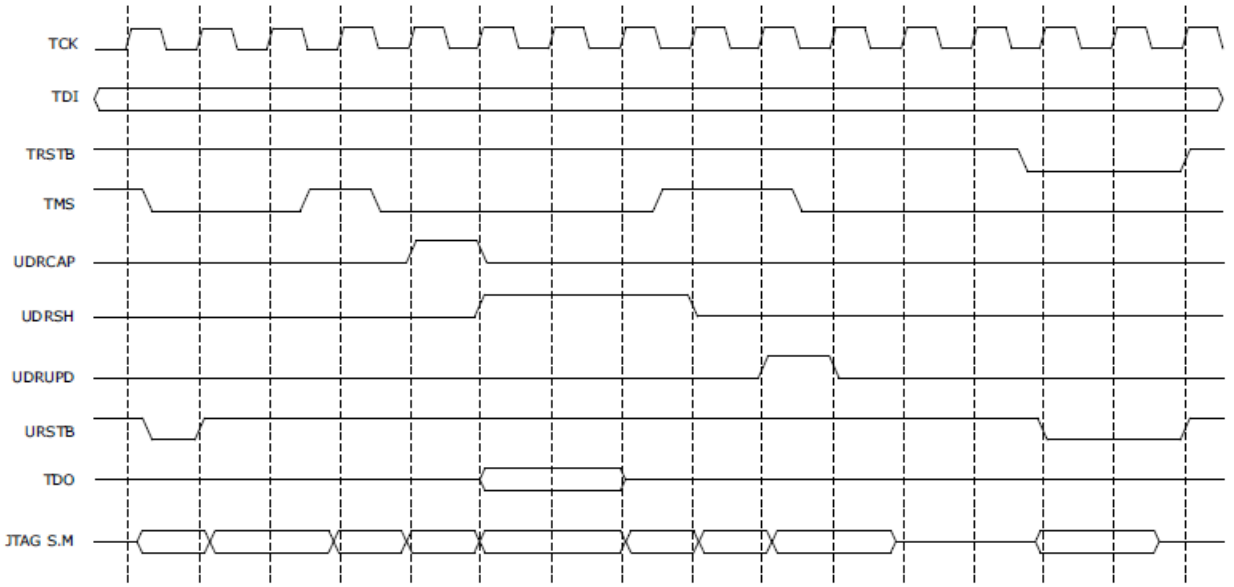
**Table 5-85.** UJTAG Performance Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| TCK frequency | $F_{TCK}$ | — | — | 25 | MHz | — |

**Figure 5-9.** UJTAG Timing Diagram




### 5.8.2. UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

**Table 5-86.** UJTAG Security Performance Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| TCK frequency | $F_{TCK}$ | — | — | — | MHz | — |

### 5.8.3. PF_SPI Initiator Programming Switching Characteristics

The following section describes characteristics of PF_SPI initiator programming switching.

**Table 5-87.** SPI Initiator Programming Performance Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| SCK frequency | $F_{SCK}$ | — | — | 20 | MHz | — |

### 5.8.4. Tamper Detectors

The following section describes tamper detectors.

**Table 5-88.** ADC Conversion Rate

| Parameter | Description | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| $T_{CONV1}$ | Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0. | 350 | — | 470 | µs |
| $T_{CONVN}$ | Time between subsequent channel conversions. | — | 480 | — | µs |
| $T_{SETUP}$ | Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs. | 0 | — | — | ns |
| $T_{VALID}$ [2] | Width of the valid pulse. | 1.5 | — | 2.5 | µs |


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**Table 5-88.** ADC Conversion Rate (continued)

| Parameter | Description | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| $T_{RATE}$ | Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter. | — | Rate × 32 | — | µs |

1. Min, Typ, and Max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

**Note:** Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

**Table 5-89.** Temperature and Voltage Sensor Electrical Characteristics

| Parameter | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Temperature sensing range | –55 | — | 125 | °C | — |
| Temperature sensing accuracy | –10 | — | 10 | °C | — |
| Voltage sensing range | 0.9 | — | 2.8 | V | — |
| Voltage sensing accuracy | –3.0 | — | 3.0 | % | — |

**Table 5-90.** Tamper Macro Timing Characteristics—Flags and Clearing

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| From event detection to flag generation | $T_{JTAG_ACTIVE}$ [1] | 28 | 35 | ns |
| | $T_{MESH_ERR}$ [1] | 1.8 | 2.5 | µs |
| | $T_{CLK_GLITCH}$ [1] | — | 50 | ns |
| | $T_{CLK_FREQ}$ [1] | — | 4 | µs |
| | $T_{LOW_VDD}$ [1, 3] | 70 | 1000 | µs |
| | $T_{HIGH_VDD18}$ [1, 3] | 85 | 1000 | µs |
| | $T_{HIGH_VDD25}$ [1, 3] | 130 | 1000 | µs |
| | $T_{SECDEC}$ [1] | — | 5 | ns |
| | $T_{DRI_ERR}$ [1] | 14 | 18 | µs |
| | $T_{WDOG}$ [1] | — | 5 | ns |
| | $T_{LOCK_ERR}$ [1] | — | 5 | ns |


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**Table 5-90.** Tamper Macro Timing Characteristics—Flags and Clearing (continued)

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Time from system controller instruction execution to flag generation | $T_{INST_BUF_ACCESS}$ [1, 2] | 4 | 5 | µs |
| | $T_{INST_DEBUG}$ [1, 2] | 3.3 | 4 | µs |
| | $T_{INST_CHK_DIGEST}$ [1, 2] | 1.8 | 3 | µs |
| | $T_{INST_EC_SETUP}$ [1, 2] | 1.8 | 2 | µs |
| | $T_{INST_FACT_PRIV}$ [1, 2] | 3.8 | 5 | µs |
| | $T_{INST_KEY_VAL}$ [1, 2] | 2.5 | 3.5 | µs |
| | $T_{INST_MISC}$ [1, 2] | 1.5 | 2 | µs |
| | $T_{INST_PASSCODE_MATCH}$ [1, 2] | 2.5 | 3 | µs |
| | $T_{INST_PASSCODE_SETUP}$ [1, 2] | 4.2 | 5 | µs |
| | $T_{INST_PROG}$ [1, 2] | 3.8 | 4.5 | µs |
| | $T_{INST_PUB_INFO}$ [1, 2] | 4 | 4.5 | µs |
| | $T_{INST_ZERO_RECO}$ [1, 2] | 2.5 | 3 | µs |
| | $T_{INST_PASSCODE_FAIL}$ [1, 2] | 170 | 180 | µs |
| | $T_{INST_KEY_VAL_FAIL}$ [1, 2] | 92 | 110 | µs |
| | $T_{INST_UNUSED}$ [1, 2] | 4 | 5 | µs |
| Time from sending the CLEAR to deassertion on FLAG | $T_{CLEAR_FLAG}$ | 17 | 23 | ns |

1. The timing does not impact the user design, but it is useful for security analysis.
2. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.
3. Timing of these depends highly on supply ramp rate.

**Table 5-91.** Tamper Macro Response Timing Characteristics

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Time from triggering the response to all I/Os disabled | $T_{IO_DISABLE}$ | 45 | 63 | ns |
| Time from negation of RESPONSE to all I/Os re-enabled | $T_{CLR_IO_DISABLE}$ | 34 | 51 | ns |
| Time from triggering the response to security locked | $T_{LOCKDOWN}$ | — | 20 | ns |
| Time from negation of RESPONSE to earlier security unlock condition | $T_{CLR_LOCKDOWN}$ | — | 20 | ns |
| Time from triggering the response to device enters RESET | $T_{tr_RESET}$ | 11.7 | 14 | µs |
| Time from triggering the response to start of zeroization | $T_{tr_ZEROLISE}$ | 7.4 | 8.2 | ms |

### 5.8.5. System Controller Suspend Switching Characteristics

The following table describes the characteristics of system controller suspend switching.

**Table 5-92.** System Controller Suspend Entry and Exit Characteristics

| Parameter | Symbol | Definition | Typ | Max | Unit |
|---|---|---|---|---|---|
| Time from TRSTb falling edge to SUSPEND_EN signal assertion | $T_{suspend_Tr}$ [1, 2] | Suspend entry time from TRST_N assertion | 42 | 44 | ns |
| Time from TRSTb rising edge to ACTIVE signal assertion | $T_{suspend_exit}$ | Suspend exit time from TRST_N negation | 361 | 372 | ns |


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1. ACTIVE indicates that the system controller is inactive or active regardless of the state of SUSPEND_EN.
2. ACTIVE signal must never be asserted with SUSPEND_EN is asserted.

### 5.8.6. Dynamic Reconfiguration Interface

The following table provides interface timing information for the DRI, which is an embedded APB target interface within the FPGA fabric that does not use FPGA resources.

**Table 5-93.** Dynamic Reconfiguration Interface Timing Characteristics

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| PCLK frequency | $F_{PD_PCLK}$ | 200 | MHz |

### 5.8.7. User Voltage Detector Characteristics

The following table provides the electrical characteristics of the $V_{DD}$ (1.0V), $V_{DD18}$, and $V_{DD25}$ voltage detectors. For proper operation of the voltage detectors, $V_{DD}$ must be set to 1.0V.

When using user voltage detectors, it's recommended to design the board power supplies for the monitored rails with tighter tolerances than listed in Table 4-2. This margin will provide guard band and help prevent false tamper detection.

**Table 5-94.** User Voltage Detector Electrical Characteristics

| Parameter | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{DD_HIGH_DET}$ | 1.031 | — | 1.103 | V | Temp= –55°C to 125°C; VDD18 = 1.8V ±5%; VDD25= 2.5V ±3% |
| $V_{DD18_HIGH_DET}$ | 1.891 | — | 1.998 | V | Temp= –55°C to 125°C; VDD = 1.0V ±3%; VDD25= 2.5V ±3% |
| $V_{DD25_HIGH_DET}$ | 2.630 | — | 2.765 | V | Temp= –55°C to 125°C; VDD = 1.0V ±3%; VDD18= 1.8V ±5% |
| $V_{DD_LOW_DET}$ | 0.910 | — | 0.969 | V | Temp= –55°C to 125°C; VDD18 = 1.8V ±5%; VDD25= 2.5V ±3% |
| $V_{DD18_LOW_DET}$ | 1.560 | — | 1.640 | V | Temp= –55°C to 125°C; VDD = 1.0V ±3%; VDD25= 2.5V ±3% |
| $V_{DD25_LOW_DET}$ | 2.188 | — | 2.307 | V | Temp= –55°C to 125°C; VDD = 1.0V ±3%; VDD18= 1.8V ±5% |

## 5.9. Power-Up to Functional Timing

Microchip non-volatile FPGA technology offers the fastest boot-time of any mid-range FPGA in the market. The following tables describes both cold-boot (from power-on) and warm-boot (assertion of DEVRST_N pin or assertion of reset from the tamper macro) timing. The power-up diagrams assume all power supplies to the device are stable.

### 5.9.1. Power-On (Cold) Reset Initialization Sequence

The following cold reset timing diagram shows the initialization sequencing of the device.


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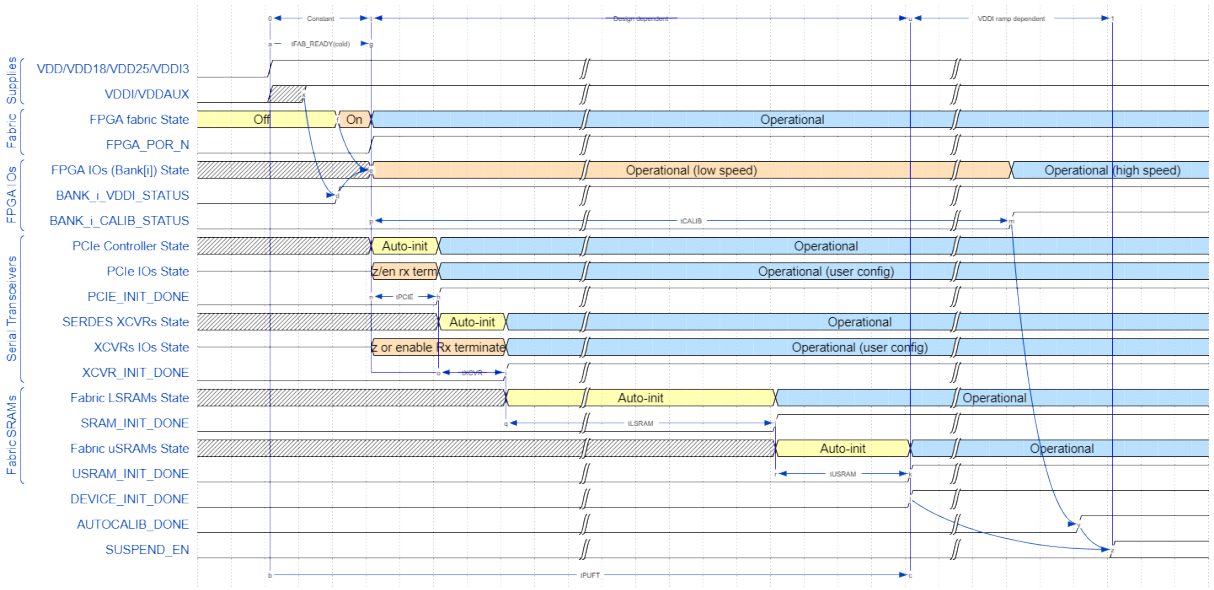
**Figure 5-10.** Cold Reset Timing




**Notes:**

- Figure 5-10 shows the case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25/VDDI3 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25/VDDI3 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25/VDDI3, then the I/O bank enable time is measured from the assertion of VDDI/VDDAUX and is not specified by the PUFT specification. In this case, I/O operation is indicated by the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation. Refer to Main Supplies for supplies that must always be on for proper startup.
- AUTOCALIB_DONE assertion indicates the completion of the I/O bank calibration controller enable sequence when auto-calibration is enabled. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert either before or after DEVICE_INIT_DONE, depending on the following:
  - The time from when VDD/VDD18/VDD25/VDDI3 are powered ON to when VDDI/VDDAUX are powered ON.

    Note: If any user-specified I/O banks are not powered ON within the auto-calibration timeout window, AUTOCALIB_DONE will not assert until after that timeout expires.
  - The specified ramp times of VDDI of each I/O bank enabled for auto-calibration.
  - The amount of auto-initialization to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If auto-calibration is enabled and an I/O bank's VDDI/VDDAUX is not powered ON within the auto-calibration timeout window, the bank will be approximately calibrated when VDDI/VDDAUX are later applied. For accurate calibration on these banks, it is necessary to initiate a re-calibration using CALIB_START from fabric.
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.
- The bank specific BANK_x_CALIB_STATUS signal is asserted when an I/O bank calibration has completed.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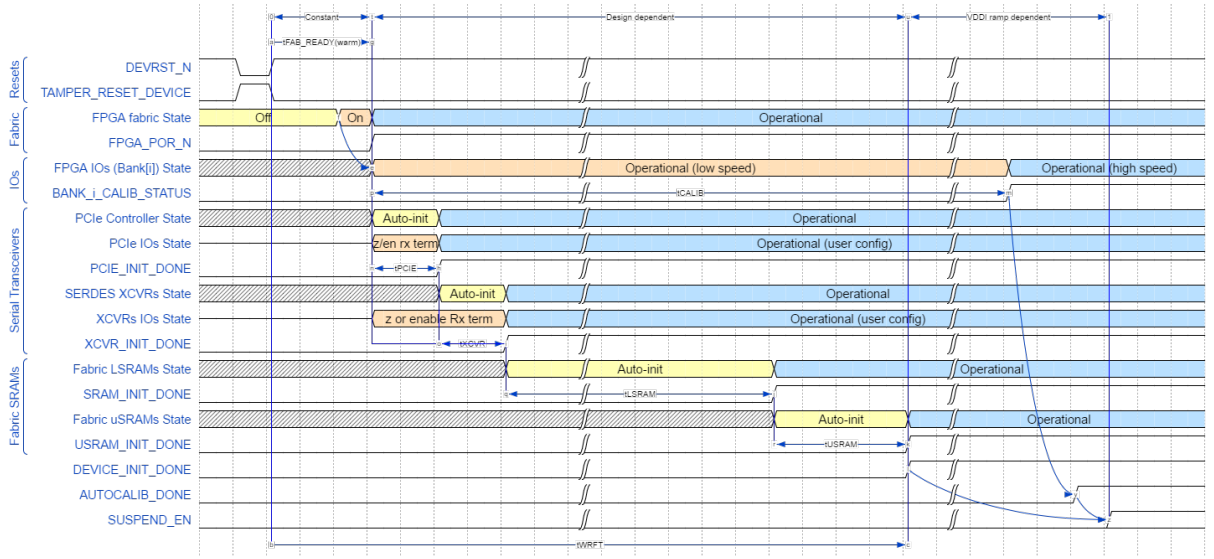
### 5.9.2. Warm Reset Initialization Sequence

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

**Figure 5-11.** Warm Reset Timing




### 5.9.3. Power-On Reset Voltages

The following sections describe the power-on reset voltages.

#### 5.9.3.1. Main Supplies

The start of power-up to functional time ($T_{PUFT}$) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25, VDDI3) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering ON the FPGA fabric and I/Os.

**Table 5-95.** POR Ref Voltages

| Supply | Power-On Reset Start Point (V) | Note |
|---|---|---|
| VDD | 0.95 | Applies to both 1.0V and 1.05V operation. |
| VDD18 | 1.71 | — |
| VDD25 | 2.25 | — |
| VDDI3 | Table 5-96 | — |

#### 5.9.3.2. I/O-Related Supplies

For the I/Os to become functional at low speed (sub-400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered ON.

**Table 5-96.** I/O-Related Supplies

| Supply | I/O Power-Up Start Point (V) |
|---|---|
| VDDI | 0.85 |
| VDDAUX | 1.6 |

There are no sequencing requirements for the power supplies. There are few sequences that can create temporary glitches on GPIO during initialization. Refer to UG0726: PolarFire FPGA Board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Design User Guide for more details. In order for the device to start initialization, VDDI3 must be powered before or at the same time as the other main supplies (VDD, VDD18, VDD25). The other I/O supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the I/O supplies of I/O banks remain powered OFF, with the exception of VDDI3).

### 5.9.4. User Design Dependence of Power-Up Times

Some phases of the device initialization are user design dependent, as the device automatically initializes certain resources to user-specified configurations if those resources are used in the design. It is necessary to compute the overall power-up to functional time by referencing the following tables and adding the relevant phases, according to the design configuration. The following equation refers to timing parameters specified in the above timing diagrams. Please note $T_{PCIE}$ , $T_{XCVR}$, $T_{LSRAM,}$ and $T_{USRAM}$ can be found in PolarFire Family Power-Up and Resets User Guide.

$T_{PUFT} = T_{FAB_READY(cold)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

$T_{WRFT} = T_{FAB_READY(warm)} + \max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$

**Note:** $T_{PCIE}$, $T_{XCVR}$, $T_{LSRAM}$, $T_{USRAM}$, and $T_{CALIB}$ are common to both cold and warm reset scenarios.

Auto-initialization of FPGA (if required) occurs in parallel with I/O calibration. The device may be considered fully functional only when the later of these two activities has finished, which may be either one, depending on the configuration, as may be calculated from the following tables. Note that I/O calibration may extend beyond $T_{PUFT}$ (as I/O calibration process is independent of main device power-on and is instead dependent on I/O bank supply relative power-on time and ramp times). The previous timing diagram for power-on initialization shows the earliest that I/Os could be enabled, if the I/O power supplies are powered on before or at the same time as the main supplies.

### 5.9.5. Cold Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the power supplies reaching the above trip point levels until the FPGA fabric is operational and the FPGA I/Os are functional for low-speed (sub-400 MHz) operation.

**Table 5-97.** Cold Boot

| Power-On (Cold) Reset to Fabric and I/O Operational | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Time when input pins start working – $T_{IN_ACTIVE(cold)}$ | 0.92 | 4.38 | 7.84 | ms |
| Time when weak pull-ups are enabled – $T_{PU_PD_ACTIVE(cold)}$ | 0.92 | 4.38 | 7.84 | ms |
| Time when fabric is operational – $T_{FAB_READY(cold)}$ | 0.95 | 4.41 | 7.87 | ms |
| Time when output pins start driving – $T_{OUT_ACTIVE(cold)}$ | 0.97 | 4.43 | 7.89 | ms |

### 5.9.6. Warm Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the negation of the warm reset event until the FPGA fabric is operational and the FPGA I/Os are functional for low-speed (sub-400 MHz) operation.

**Table 5-98.** Warm Boot

| Warm Reset to Fabric and I/O Operational | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Time when input pins start working – $T_{IN_ACTIVE(warm)}$ | 0.65 | 1.63 | 2.62 | ms |
| Time when weak pull-ups/pull-downs are enabled – $T_{PU_PD_ACTIVE(warm)}$ | 0.65 | 1.63 | 2.62 | ms |
| Time when fabric is operational – $T_{FAB_READY(warm)}$ | 0.68 | 1.66 | 2.65 | ms |
| Time when output pins start driving – $T_{OUT_ACTIVE(warm)}$ | 0.70 | 1.68 | 2.67 | ms |


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### 5.9.7. Miscellaneous Initialization Parameters

In the following table, $T_{FAB_READY}$ refers to either $T_{FAB_READY(cold)}$ or $T_{FAB_READY(warm)}$ as specified in the previous tables, depending on whether the initialization is occurring as a result of a cold or warm reset, respectively.

**Table 5-99.** Cold and Warm Boot

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| The time from $T_{FAB_READY}$ to ready to program through JTAG/ SPI-Target | — | 0 | 0 | 0 | ms | — |
| The time from $T_{FAB_READY}$ to auto-update start | — | — | $T_{PUF_OVHD}$ [1] | $T_{PUF_OVHD}$ [1] | ms | — |
| The time from $T_{FAB_READY}$ to programming recovery start | — | — | $T_{PUF_OVHD}$ [1] | $T_{PUF_OVHD}$ [1] | ms | — |
| The time from $T_{FAB_READY}$ to the tamper flags being available | $T_{TAMPER_READY}$ | 0 | 0 | 0 | ms | — |
| The time from $T_{FAB_READY}$ to the Athena Crypto co-processor being available (for S devices only) | $T_{CRYPTO_READY}$ | 0 | 0 | 0 | ms | — |

1. Programming depends on the PUF to power-up. Refer to $T_{PUF_OVHD}$ at section Secure NVM Performance.

### 5.9.8. I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

**Table 5-100.** I/O Initial Calibration Time (TCALIB)

| Ramp Time | Min (ms) | Max (ms) | Condition |
|---|---|---|---|
| 0.2 ms | 0.98 | 2.63 | Applies to HSIO and GPIO banks |
| 50 ms | 41.62 | 62.19 | Applies to HSIO and GPIO banks |

**Notes:**

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for I/O calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in section I/O-Related Supplies.

**Table 5-101.** I/O Fast Recalibration Time (TRECALIB)

| I/O Type | Min (ms) | Typ (ms) | Max (ms) | Condition |
|---|---|---|---|---|
| GPIO bank | 0.04 | 0.14 | 0.24 | GPIO configured for 3.3V operation |
| HSIO bank | 0.11 | 0.20 | 0.30 | HSIO configured for 1.8V operation |

**Note:** In order to obtain fast re-calibration, the user must assert the relevant calibration request signals from the FPGA fabric to the I/O bank controller (see PF_INIT_MONITOR IP).

## 5.10. Dedicated Pins

The following section describes the dedicated pins.

### 5.10.1. JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.


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**Table 5-102.** JTAG Electrical Characteristics

| Symbol | Description | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $T_{DISU}$ | TDI input setup time | 0.0 | — | — | ns | — |
| $T_{DIHD}$ | TDI input hold time | 2.0 | — | — | ns | — |
| $T_{TMSSU}$ | TMS input setup time | 1.5 | — | — | ns | — |
| $T_{TMSHD}$ | TMS input hold time | 1.5 | — | — | ns | — |
| $F_{TCK}$ | TCK frequency | — | — | 25 | MHz | — |
| $T_{TCKDC}$ | TCK duty cycle | 40 | — | 60 | % | — |
| $T_{TDOCQ}$ | TDO clock to Q out | — | — | 8.4 | ns | $C_{LOAD}$ = 40 pf |
| $T_{RSTBCQ}$ | TRSTB clock to Q out | — | — | 23.5 | ns | $C_{LOAD}$ = 40 pf |
| $T_{RSTBPW}$ | TRSTB min pulse width | 50 | — | — | ns | — |
| $T_{RSTBREM}$ | TRSTB removal time | 0.0 | — | — | ns | — |
| $T_{RSTBREC}$ | TRSTB recovery time | 12.0 | — | — | ns | — |
| $CIN_{TDI}$ | TDI input pin capacitance | — | — | 5.3 | pf | — |
| $CIN_{TMS}$ | TMS input pin capacitance | — | — | 5.3 | pf | — |
| $CIN_{TCK}$ | TCK input pin capacitance | — | — | 5.3 | pf | — |
| $CIN_{TRSTB}$ | TRSTB input pin capacitance | — | — | 5.3 | pf | — |

## 5.10.2. SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

**Table 5-103.** SPI Initiator Mode (PolarFire Initiator)[1]

| Parameter | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| SCK frequency | sp1i_sc | — | 20<br>40 | MHz | During Programming<br>During Initialization |
| SCK minimum pulse width high | sp2i_sc | SCK_period/2 | — | ns | — |
| SCK minimum pulse width low | sp3i_sc | SCK_period/2 | — | ns | — |
| Rise and fall time | sp4i_sc<br>sp5i_sc | — | — | ns | Refer to PolarFire IBIS models[3] |
| SCK to SDO | sp6i_sc | –2.0 | +3.0 | ns | — |
| SDI setup to SCK[2] | sp7i_sc | 10.0 | — | ns | — |
| SDI hold from SCK[2] | sp8i_sc | –1.0 | — | ns | — |

**Note:**

1. Parameters are referenced to the active edge of SCK, which depends on the configured SPI protocol (for example, Motorola SPI mode uses rising edge as active edge if SPO = 0).
2. SDI is clocked into SPI on active edge and clocked out on inactive edge. Therefore, SDO delay parameters are dependent on SCK frequency (nominally SCK_period/2).
3. For specific rise/fall times, board design considerations, and detailed output buffer resistances, use the corresponding IBIS models located online at IBIS Models: PolarFire.


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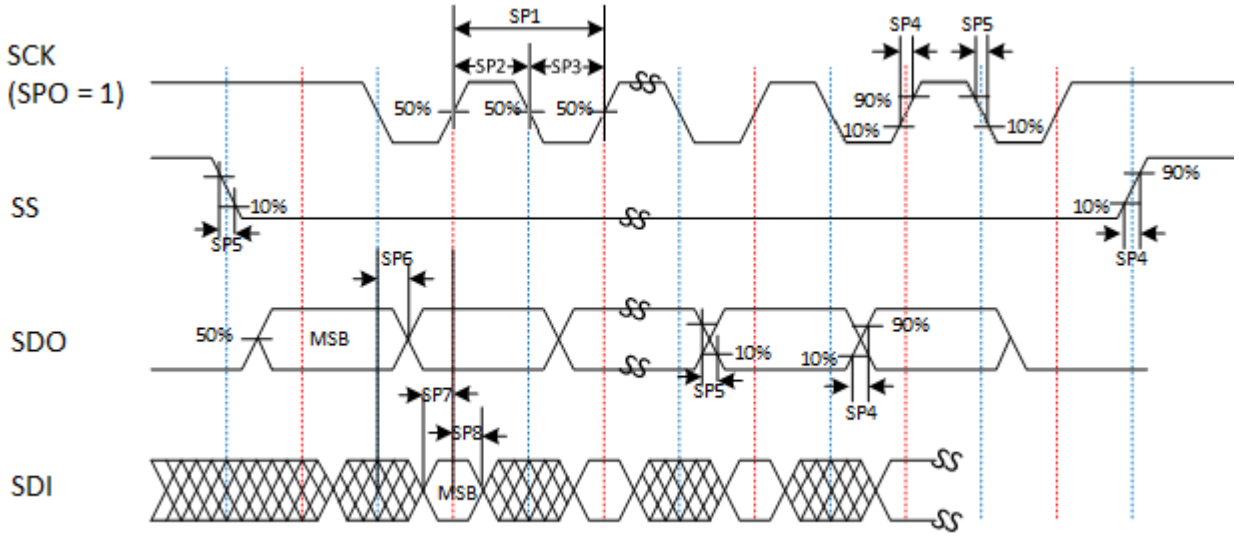
**Table 5-104.** SPI Target Mode (PolarFire Target)[1]

| Parameter | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| SCK frequency | sp1t_sc | — | 80 | MHz | — |
| SCK minimum pulse width high | sp2t_sc | SCK_period/2 | — | ns | — |
| SCK minimum pulse width low | sp3t_sc | SCK_period/2 | — | ns | — |
| Rise and fall time | sp4t_sc<br>sp5t_sc | — | — | ns | Refer to PolarFire IBIS models[3] |
| SCK to SDO | sp6t_sc | 0.0 | +8.0 | ns | — |
| SDI setup to SCK[2] | sp7t_sc | 2.0 | — | ns | — |
| SDI hold from SCK[2] | sp8t_sc | 2.0 | — | ns | — |

**Note:**

1. Parameters are referenced to the active edge of SCK, which depends on the configured SPI protocol (for example, Motorola SPI mode uses rising edge as active edge if SPO = 0).
2. SDI is clocked into SPI on active edge and clocked out on inactive edge. Therefore, SDO delay parameters are dependent on SCK frequency (nominally SCK_period/2).
3. For specific rise/fall times, board design considerations, and detailed output buffer resistances, use the corresponding IBIS models located online at IBIS Models: PolarFire.

**Figure 5-12.** SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)




## 5.10.3. SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

**Table 5-105.** SmartDebug Probe Performance Characteristics

| Parameter | Symbol | $V_{DD}$ = 1.0V STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|---|
| Maximum frequency of probe signal | $F_{MAX}$ | 100 | 100 | 100 | 100 | MHz |


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**Table 5-105.** SmartDebug Probe Performance Characteristics (continued)

| Parameter | Symbol | $V_{DD}$ = 1.0V STD | $V_{DD}$ = 1.0V –1 | $V_{DD}$ = 1.05V STD | $V_{DD}$ = 1.05V –1 | Unit |
|---|---|---|---|---|---|---|
| Minimum delay of probe signal | $T_{Min_delay}$ | — | — | — | — | ns |
| Maximum delay of probe signal | $T_{Max_delay}$ | — | — | — | — | ns |

### 5.10.4. DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

**Table 5-106.** DEVRST_N Electrical Characteristics[1]

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| DEVRST_N ramp time | $DR_{RAMP}$ | — | 10 | — | µs | DEVRST_N ramp must be monotonic and meet the rise and fall time requirement. |
| DEVRST_N assert time | $DR_{ASSERT}$ | 1 | — | — | µs | The minimum time for DEVRST_N assertion to be recognized. |
| DEVRST_N de-assert time | $DR_{DEASSERT}$ | 2.75 | — | — | ms | The minimum time DEVRST_N needs to be de-asserted before assertion. |

1. For regular IOs (GPIO and HSIO) rise and fall time requirements, refer to Table 4-4.

## 5.11. User Crypto

The following section describes user crypto.

### 5.11.1. TeraFire® 5200B Switching Characteristics

The following table describes TeraFire® 5200B switching characteristics.

**Table 5-107.** TeraFire® F5200B Switching Characteristics

| Parameter | Symbol | STD | – 1 | Unit | Condition |
|---|---|---|---|---|---|
| $F_{MAX}$ with DLL | $F_{MAX_DLL}$ | 189 | 189 | MHz | –55°C to 125°C |
| $F_{MIN}$ with DLL | $F_{MIN_DLL}$ | 125 | 125 | MHz | –55°C to 125°C |
| $F_{MAX}$ with DLL in Bypass mode | $F_{MAX_DLL_BYPASS}$ | 70 | 70 | MHz | –55°C to 125°C |
| $F_{MIN}$ with DLL in Bypass mode | $F_{MIN_DLL_BYPASS}$ | 0 | 0 | MHz | –55°C to 125°C |

### 5.11.2. TeraFire® 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire® 5200B throughput characteristics. Adding the 2 columns clock counts on any given row will yield the expected performance for that algorithm and message size.

**Note:** Throughput cycle count collected with Athena TeraFire Core and a soft RISC-V CPU running at 70 MHz.

**Table 5-108.** AES

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| AES-ECB-128 encrypt[1] | 128 | 511 | 1011 |
| | 64K | 48109 | 927 |


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**Table 5-108.** AES (continued)

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| AES-ECB-128 decrypt[1] | 128 | 557 | 1328 |
| | 64K | 48385 | 1282 |
| AES-ECB-256 encrypt[1] | 128 | 527 | 1333 |
| | 64K | 56301 | 1303 |
| AES-ECB-256 decrypt[1] | 128 | 589 | 1356 |
| | 64K | 56673 | 1410 |
| AES-CBC-256 encrypt[1] | 128 | 588 | 1316 |
| | 64K | 58691 | 1286 |
| AES-CBC-256 decrypt[1] | 128 | 617 | 1676 |
| | 64K | 56853 | 1730 |
| AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1921 | 1701 |
| | 64K | 58022 | 1640 |
| AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1969 | 1718 |
| | 64K | 58054 | 1803 |

1. With DPA counter measures.

**Table 5-109.** GMAC

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| AES-GCM-256[1], 128-bit tag, (message is only authenticated) | 128 | 1859 | 1752 |
| | 64K | 47659 | 1854 |

1. With DPA counter measures.

**Table 5-110.** HMAC

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| HMAC-SHA-256[1], 256-bit key | 512 | 7461 | 1616 |
| | 64K | 86319 | 1350 |
| HMAC-SHA-384[1], 384-bit key | 1024 | 13017 | 1438 |
| | 64K | 104055 | 1438 |

1. With DPA counter measures.

**Table 5-111.** CMAC

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| AES-CMAC-256[1] (message is only authenticated) | 128 | 446 | 8434 |
| | 64K | 45494 | 110209 |

1. With DPA counter measures.


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**Table 5-112.** KEY TREE

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| 128-bit nonce + 8-bit optype | — | 102457 | 2173 |
| 256-bit nonce + 8-bit optype | — | 103218 | 2359 |

**Table 5-113.** SHA

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| SHA-1[1] | 512 | 2370 | 816 |
| | 64K | 75528 | 709 |
| SHA-256[1] | 512 | 2500 | 656 |
| | 64K | 82704 | 656 |
| SHA-384[1] | 1024 | 4122 | 712 |
| | 64K | 98174 | 656 |
| SHA-512[1] | 1024 | 4122 | 652 |
| | 64K | 98174 | 653 |

1. With DPA counter measures.

**Table 5-114.** ECC

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| ECDSA SigGen, P-384/SHA-384[1] | 1024 | 12525647 | 5072 |
| | 8K | 12540387 | 5072 |
| ECDSA SigGen, P-384/SHA-384 | 1024 | 5502896 | 5071 |
| | 8K | 5513718 | 5071 |
| ECDSA SigVer, P-384/SHA-384[1] | 1024 | 6243821 | 4683 |
| | 8K | 6321110 | 4422 |
| ECDSA SigVer, P-384/SHA-384 | 1024 | 6243821 | 4422 |
| | 8K | 6321110 | 4422 |
| Key Agreement (KAS), P-384 | — | 5039125 | 10318 |
| Point Multiply, P-256[1] | — | 5177474 | 4434 |
| Point Multiply, P-384[1] | — | 12055519 | 5086 |
| Point Multiply, P-521[1] | — | 26889271 | 6470 |
| Point Addition, P-384 | — | 3018067 | 5303 |
| KeyGen (PKG), P-384 | — | 12052230 | 7909 |
| Point Verification, P-384 | — | 5091 | 3354 |

1. With DPA counter measures.

**Table 5-115.** IFC (RSA)

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| Encrypt, RSA-2048, e=65537 | 2048 | 436972 | 8287 |
| Encrypt, RSA-3072, e=65537 | 3072 | 962162 | 12063 |
| Decrypt, RSA-2048[1], CRT | 2048 | 26847616 | 15261 |


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**Table 5-115.** IFC (RSA) (continued)

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| Decrypt, RSA-3072[1], CRT | 3072 | 75168689 | 22488 |
| Decrypt, RSA-4096, CRT | 4096 | 88789629 | 23585 |
| Decrypt, RSA-3072, CRT | 3072 | 38202717 | 18838 |
| SigGen, RSA-3072/SHA-384[1] ,CRT, PKCS #1 V 1 1.5 | 1024 | 75156973 | 19562 |
| | 8K | 75222026 | 18880 |
| SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5 | 1024 | 148092303 | 13622 |
| | 8K | 148102319 | 13622 |
| SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5 | 1024 | 970959 | 11769 |
| | 8K | 981755 | 11769 |
| SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5 | 1024 | 443593 | 8490 |
| | 8K | 452751 | 8443 |
| SigGen, RSA-3072/SHA-384, ANSI X9.31 | 1024 | 147143879 | 13624 |
| | 8K | 147153109 | 13417 |
| SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31 | 1024 | 972788 | 11268 |
| | 8K | 983643 | 11215 |

1. With DPA counter measures.

**Table 5-116.** FFC (DH)

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| SigGen, DSA-3072/SHA-384[1] | 1024 | 27932434 | 13271 |
| | 8K | 27946636 | 13166 |
| SigGen, DSA-3072/SHA-384 | 1024 | 12086324 | 13028 |
| | 8K | 12097138 | 12862 |
| SigVer, DSA-3072/SHA-384 | 1024 | 24711796 | 14689 |
| | 8K | 24418930 | 14689 |
| SigVer, DSA-2048/SHA-256 | 1024 | 9673222 | 10717 |
| | 8K | 9803028 | 10717 |
| Key Agreement (KAS), DH-3072 (p=3072,security=256) | — | 4920705 | 9519 |
| Key Agreement (KAS), DH-3072 (p=3072,security=256)[1] | — | 78871914 | 9495 |

1. With DPA counter measures.

**Table 5-117.** NRBG

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| Instantiate: strength, s=256, 384-bit nonce, 384-bit personalization string | — | 18221 | 3076 |
| Reseed: no additional input, s=256 | — | 13585 | 1056 |


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**Table 5-117.** NRBG (continued)

| Modes | Message Size (Bits) | Athena TeraFire Crypto Core Clock-Cycles | RISC-V CPU Clock-Cycles |
|---|---|---|---|
| Reseed: 384-bit additional input, s=256 | — | 15922 | 995 |
| Generate: (no additional input), prediction resistance enabled, s=256 | 128 | 15262 | 1672 |
| | 8K | 27169 | 7837 |
| Generate: (no additional input), prediction resistance disabled, s=256 | 128 | 2138 | 781 |
| | 8K | 14045 | 7837 |
| Generate: (384-bit additional input), prediction resistance enabled, s=256 | 128 | 21299 | 1620 |
| | 8K | 33206 | 8563 |
| Generate: (384-bit additional input), prediction resistance disabled, s=256 | 128 | 11657 | 1507 |
| | 8K | 23564 | 8563 |
| Un-instantiate | — | 761 | 502 |


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# 6. Revision History

| Revision | Date | Description |
|---|---|---|
| G | 03/2026 | • Updated Transceiver Maximum $V_{IN}$ in Table 4-1.<br>• A note has been added to Table 4-1.<br>• Added VDDI tolerances for supported DDR interfaces in Table 4-2.<br>• A note has been added to Table 4-2.<br>• Notes about auto-calibration have been clarified in Power-On (Cold) Reset Initialization Sequence.<br>• PLL has been added to Table 5-13.<br>• The following sections have been updated: FPGA Programming Time, FPGA Bitstream Sizes, Digest Time, Zeroization Time, Verify Time, Authentication Time, Secure NVM Performance, and System Services Throughput Characteristics.<br>• A recommendation has been added to User Voltage Detector Characteristics, and Table 5-94 has been updated. |
| F | 05/2025 | • Added reference to PolarFire Core products (MPFxxxTC) in Silicon and Libero Tool Status, Transceiver Switching Characteristics, Transceiver Protocol Characteristics, FPGA Programming Time, FPGA Bitstream Sizes, Digest Time, Verify Time, and Authentication Time.<br>• Changed silicon status of MPF050 to "Production – all temperature grades" in Table 3-1.<br>• Added MPF500T offering in Table 3-4 Automotive T2.<br>• Updated note 7 under Recommended Operating Conditions for "XCVR calibration time".<br>• Added clarifying note 8 under Recommended Operating Conditions.<br>• Removed reference to PolarFire I/O Timing spreadsheet in User I/O Switching Characteristics.<br>• Corrected note under Transmitter Performance from "Untill specified" to "Unless specified".<br>• Updated notes under Power-On (Cold) Reset Initialization Sequence.<br>• Updated note under I/O Fast Recalibration Time (TRECALIB).<br>• SLVS18, SUBLVDS18 and SLVS25/33 Maximum input buffer speeds have been updated in Input Buffer Speed.<br>• Updated units from “ps” to “UI” in Table 5-66. |


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**Revision History** (continued)

| Revision | Date | Description |
|---|---|---|
| E | 04/2024 | • Added the MPF050T part number status to production.<br>• Added two notes to Table 4-3 to explain how weak pullup and weak pulldown resistors should be calculated.<br>• Corrected Note 6 of Table 4-4. The maximum time allowed was listed as 300 µs and should be 300 ns.<br>• Added HSIO clock skew with bridging for MPF050T device in Table 5-17.<br>• Added PLL output jitter specification for $F_{OUT}$ slower than 1.5 MHz in Table 5-18. Also clarified Note 5 and 6.<br>• Added footnote to Table 5-106.<br>• Updated the SPI Timing section for clarification. No changes to silicon have occurred. See SPI Switching Characteristics.<br>• Clarified Note 1 and condition in Table 5-106.<br>• Changed “CDR PPM tolerance” to “CDR frequency tolerance” for better clarity in Receiver Performance.<br>• Updated VDDI3 power-up requirements in section Power-Up to Functional Timing and I/O-Related Supplies.<br>• Updated Zeroization Time and User Voltage Detector Characteristics sections as per PCN.<br>• Updated Table 5-37.<br>• Updated RC Oscillators.<br>• Corrected item in Table 5-7. Fabric clock maximum frequency for LPDDR3 on -STD speed grade devices was listed as 133 MHz and should be 100 MHz.<br>• Updated Table 5-107 to support the full military range.<br>• Authentication Service IDs were swapped. Table 5-81 was updated.<br>• Corrected Table 3 for military grade devices to lead and tin.<br>• Redirected the Device Offering list to a separate document entitled PolarFire® FPGA Product Overview. |
| D | 05/2022 | • Listed part number prefixes that pertain to this document (MPF050T, MPF100T, MPF200T, MPF300T, and MPF500T) in the Overview. |
| C | 04/2022 | • Added a column to Table 5-75 to correlate individual digest times to the condensed digest times in Libero.<br>• Fixed a typo—added a parenthesis to the min and max CDR lock-to-data time in Table 5-43.<br>• Added a new section Clock Jitter for Customer Advisory Notice (CAN) Global Clock Jitter.<br>• Added a reference to footnote 8 in Table 5-36. |


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**Revision History** (continued)

| Revision | Date | Description |
|---|---|---|
| B | 10/2021 | • Added AECQ-100 to Table 1. PolarFire Minimum and Maximum Junction Temperatures by Temperature Grade.<br>• Added the MPF050 to Table 3-2. PolarFire FPGA Tool Status.<br>• Added note 3 under Table 4-1. Absolute Maximum Rating.<br>• Changed the name LVDS18 for GPIO to LVDS18G in Table 4-17. Differential DC Input Levels.<br>• Added a row for LVDS18G in Table 4-18. Differnetial DC Ouptut Level.<br>• Added a LVDS18G row to Table 5-4. GPIO Maximum Input Buffer Speed.<br>• Added a LVDS18G row to Table 5-6. GPIO Maximum Output Buffer Speed.<br>• Removed DDR3L from the footnote under Table 5-7. Maximum PHY Rate for Memory Interfaces IP for HSIO Banks.<br>• Added a LVDS18G row to Table 5-14. I/O CDR Switching Characteristics.<br>• Added footnote 8 under Table 5-30. PolarFire Transceiver Reference Clock AC Requirements that relaxes the reference clock requirements if additional jitter is acceptable.<br>• Changed references from VDDSREF to $XCVR_{VREF}$ in section Transceiver Reference Clock I/O Standards to align with Table 4-2. Recommended Operating Conditions.<br>• Added footnote 14 under Table 5-36. PolarFire Transcevier Transmitter Characteristics that relaxes the reference clock requirements if additional jitter is acceptable<br>• Clarified that programming, verify, and zeroization operations all count as a programming cycle. For more information, see section FPGA and µPROM Programming Cycle and Retention.<br>• Table 5-62. SPI Initiator and Auto-Update Programming Time (IAP) was updated to now reference auto-update programming times.<br>• Clarified Notes section under Table 5-74. Standalone Fabric Verify Times.<br>• Clarified table headers and notes in section User Crypto.<br>• Clarified that µPROM NVM characteristics are the same as the FPGA fabric as the µPROM is constructed from the same NVM switch. For more information, see section FPGA and µPROM Programming Cycle and Retention. |
| A | 02/2021 | • Updated document to Microchip template.<br>• Updated document number from DS51700141 to DS00003831.<br>• Added automotive and military temperature-grade specifications.<br>• Increased MIPI TX speeds from 800 Mbps to 1000 Mbps for STD speed grade.<br>• Removed digest junction temperature from the table Maximum Number of Digest Cycles as it has no effect on device retention.<br>• Added SDI 6G and 12G rates. |


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**Revision History** (continued)

| Revision | Date | Description |
|---|---|---|
| 1.8 | 11/2020 | • Added footnote 3 to clarify mixed I/O receiver capability for DC Input Levels.<br>• Clarified GPIO $V_{ICM}$ and HSIO $V_{ICM}$ rules in footnote 3 in Differential DC Input Levels.<br>• Added Input Hysteresis Characteristics over Recommended Operating Conditions.<br>• Added minimum DDR memory data rates to Maximum PHY Rate for Memory Interfaces IP for HSIO Banks and Maximum PHY Rate for Memory Interfaces IP for GPIO Banks.<br>• Corrected $F_{MAX}$ values for QDR memories from 113 MHz to 112.5 MHz in Maximum PHY Rate for Memory Interfaces IP for GPIO Banks.<br>• Added note to indicate which IOD delay setting was used to achieve the specifications for the following tables:<br>– I/O Digital Receive Single-Data Rate Switching Characteristics 1<br>– I/O Digital Receive Double Data Rate Switching Characteristics 4<br>– I/O Digital Transmit Single Data Rate Switching Characteristics 2<br>– I/O Digital Transmit Double Data Rate Switching Characteristics<br>• Included a +/- maximum specification in addition to the absolute maximum specification for "PLL ouput period jitter" in PLL Electrical Characteristics.<br>• Added footnote 11 to PLL Electrical Characteristics to direct customers to contact technical support for protocol-specific jitter characteristics.<br>• Updated values in LSRAM Performance Industrial Temperature Range (–55 °C to 125 °C) .<br>• Added transceiver loopback rates and two footnotes to PolarFire Transceiver and TXPLL Performance.<br>• Updated transceiver refclk inputs from 156 MHz to 156.3 MHz in PolarFire Transceiver Reference Clock AC Requirements.<br>• Added min/max specifications to "Differential termination" in PolarFire Transceiver Transmitter Characteristics and PolarFire Transceiver Receiver Characteristics.<br>• Made the following updates to Display Port:<br>– Added 8.1 Gbps data rates.<br>– Clarified total receive jitter tolerance for 5.4 Gbps data rate.<br>– Added footnote to total transmit jitter for 5.4 Gbps data rate max.<br>• Made the following updates to FireWire IEEE 1394:<br>– Added FireWire S200 specifications.<br>– Lowered FireWire S400 Tx jitter from 557 ps to 516 ps.<br>– Clarified FireWire S800 amplitude specification.<br>• Added SLVS-EC.<br>• Deleted Table 103 SPI Macro Interface Timing Characteristics and replaced with PF_SPI Master Programming Switching Characteristics. To determine timing of the user SPI macro from the fabric, please use SmartTime.<br>• Updated the signal name AVM_ACTIVE to SUSPEND_EN in Cold Reset Timing and Warm Reset Timing.<br>• Clarified device behavior in description underneath I/O-Related Supplies. |


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**Revision History** (continued)

| Revision | Date | Description |
|---|---|---|
| 1.7 | 12/2019 | • Updated table PolarFire FPGA Silicon Status. Libero 12.2 now contains production timing and power for all devices.<br>• Corrected footnote 5 in the table PolarFire Transceiver Reference Clock AC Requirements.<br>• Corrected footnote in the table sNVM Programming Cycles vs. Retention Characteristics.<br>• Added timing parameters to the table Master SPI Programming Time (IAP) and table Slave SPI Programming Time.<br>• Added 270 mbps rates to the section SDI.<br>• Added FireWire section.<br>• Added footnotes to the following tables:<br>– Recommended Operating Conditions<br>– I/O Digital Receive Double Data Rate Switching Characteristics<br>– I/O Digital Transmit Single Data Rate Switching Characteristics<br>– I/O Digital Transmit Double Data Rate Switching Characteristics<br>– HSIO Maximum Input Buffer Speed<br>– HSIO Maximum Output Buffer Speed<br>– GPIO Maximum Output Buffer Speed<br>– Programmable Delay<br>• Added MIPI data rates to the following tables:<br>– GPIO Maximum Input Buffer Speed<br>– GPIO Maximum Output Buffer Speed<br>• Updated MIPIE25 output DC specifications. |
| 1.6 | 06/2019 | • The parameter RX_DDRX_B_G_FA (for Video7 applications) was added. For more information, see table I/O Digital Receive Double-Data Rate Switching Characteristics.<br>• I/O CDR switching characteristics were added. For more information, see table I/O CDR Switching Characteristics.<br>• High-speed I/O clock skew with bridging was added. For more information, see table High-Speed I/O Clock Characteristics (–40 °C to 100 °C).<br>• PCS and PMA minimum reset pulse widths were added. For more information, see table PolarFire Transceiver and TXPLL Performance.<br>• Auto adaptive calibration was added to CDR lock times, Burst Mode Receiver (BMR) high-gain lock time, and BMR high-gain state time. For more information, see table PolarFire Transceiver Receiver Characteristics.<br>• Fiber channel rates were corrected. For more information, see table Fiber Channel.<br>• HiGig and HiGig+ specifications were updated. For more information, see table HiGig and HiGig+.<br>• HiGig II specifications were updated. For more information, see table HiGigII.<br>• The DEVRST_N parameter was correctly classified as ramp time. For more information, see section Dedicated Pins.<br>• Transmitter and receiver return loss characteristics were added. For more information, see section Transceiver Switching Characteristics.<br>• Voltage detector specifications were added and the voltage glitch detector was removed. For more information, see section User Voltage Detector Characteristics. |
| 1.5 | | • All tables have been reviewed and updated to reflect production silicon characteristics for the 200T, 200TL, 200TS, 200TLS, 100T, 100TL, 100TS, and 100TLS devices in all packages, speed grades, and temperature grades.<br>• The maximum transceiver reference clock input rate was changed from 800 MHz to 400 MHz due to a typo in version 1.4. For more information, see table PolarFire Transceiver Reference Clock AC Requirements. |


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**Revision History** (continued)

| Revision | Date | Description |
|---|---|---|
| 1.4 | 09/2018 | • All tables have been reviewed and updated to reflect production silicon characteristics for the 300T, 300TL, 300TS, and 300TLS devices in all packages, speed grades, and temperature grades. |
| 1.3 | 06/2018 | • The System Services section was updated.<br>• The Non-Volatile Characteristics section was updated.<br>• The Fabric Macros section was updated.<br>• The Transceiver Switching Characteristics section was updated. |
| 1.2 | 06/2018 | • The datasheet has moved to preliminary status. Every table has been updated. |
| 1.1 | 08/2017 | • LVDS specifications changed to 1.25G.<br>• LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps.<br>• A note was added indicting a zeroization cycle counts as a programming cycle.<br>• A note was added defining power down conditions for programming recovery conditions. |
| 1.0 | | Initial Revision |


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