THE DATASHEET OF

ICS952906AFLFT

Integrated Circuit Systems, Inc.

ICS952906A

Programmable Timing Control Hub™ for Next Gen P4™ processor

Recommended Application:

VIA VN800/CN700/P4M800 style chipset for P4 processor

Output Features:

- 3 - 0.7V current-mode differential CPU pairs
- 10 - PCI, 3 free running, 33MHz
- 2 - REF, 14.318MHz
- 3 - 3V66, 66.66MHz
- 1 - 48MHz
- 1 - 24/48MHz
- 2 - 25MHz @ 2.5V

Key Specifications:

- CPU/SRC outputs cycle-cycle jitter < 125ps
- 3V66 outputs cycle-cycle jitter < 250ps
- PCI outputs cycle-cycle jitter < 250ps
- CPU - AGP skew < +/- 350ps
- AGP-PCI skew between 1~3.5ns

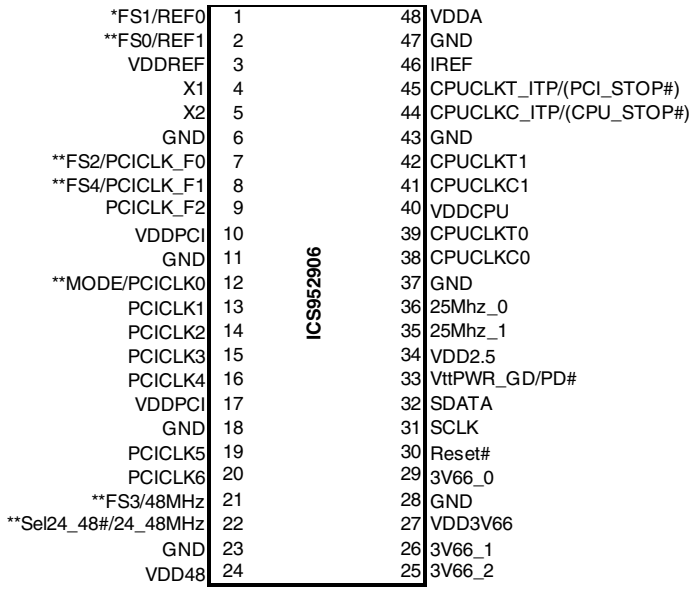
Features/Benefits:

- Programmable output frequency.
- Programmable asynchronous 3V66&PCI frequency.
- Programmable output divider ratios.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference input.

Functionality

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI
FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz
0	0	0	0	0	100.00	66.67	33.33
0	0	0	0	1	200.00	66.67	33.33
0	0	0	1	0	133.33	66.67	33.33
0	0	0	1	1	166.67	66.67	33.33
0	0	1	0	0	200.00	66.67	33.33
0	0	1	0	1	400.00	66.67	33.33
0	0	1	1	0	266.67	66.67	33.33
0	0	1	1	1	333.33	66.67	33.33
0	1	0	0	0	100.99	67.33	33.66
0	1	0	0	1	201.98	67.33	33.66
0	1	0	1	0	134.65	67.33	33.66
0	1	0	1	1	168.31	67.32	33.66
0	1	1	0	0	115.00	76.67	38.33
0	1	1	0	1	230.00	76.67	38.33
0	1	1	1	0	153.33	76.66	38.33
0	1	1	1	1	191.67	76.67	38.33
1	0	0	0	0	100.00	66.66	33.33
1	0	0	0	1	200.00	66.66	33.33
1	0	0	1	0	133.33	66.66	33.33
1	0	0	1	1	166.67	71.43	35.71
1	0	1	0	0	200.00	66.66	33.33
1	0	1	0	1	400.00	66.66	33.33
1	0	1	1	0	266.67	66.66	33.33
1	0	1	1	1	333.33	66.66	33.33
1	1	0	0	0	105.00	69.99	35.00
1	1	0	0	1	210.00	69.99	35.00
1	1	0	1	0	140.00	69.99	35.00
1	1	0	1	1	175.00	69.99	35.00
1	1	1	0	0	110.00	73.33	36.66
1	1	1	0	1	220.00	73.33	36.66
1	1	1	1	0	146.66	73.33	36.66
1	1	1	1	1	183.34	73.33	36.66

Pin Configuration



* This pin have 120K pull-up to VDD

** This pin have 120K pull-down to GND

48-pin SSOP & TSSOP

Pin Description

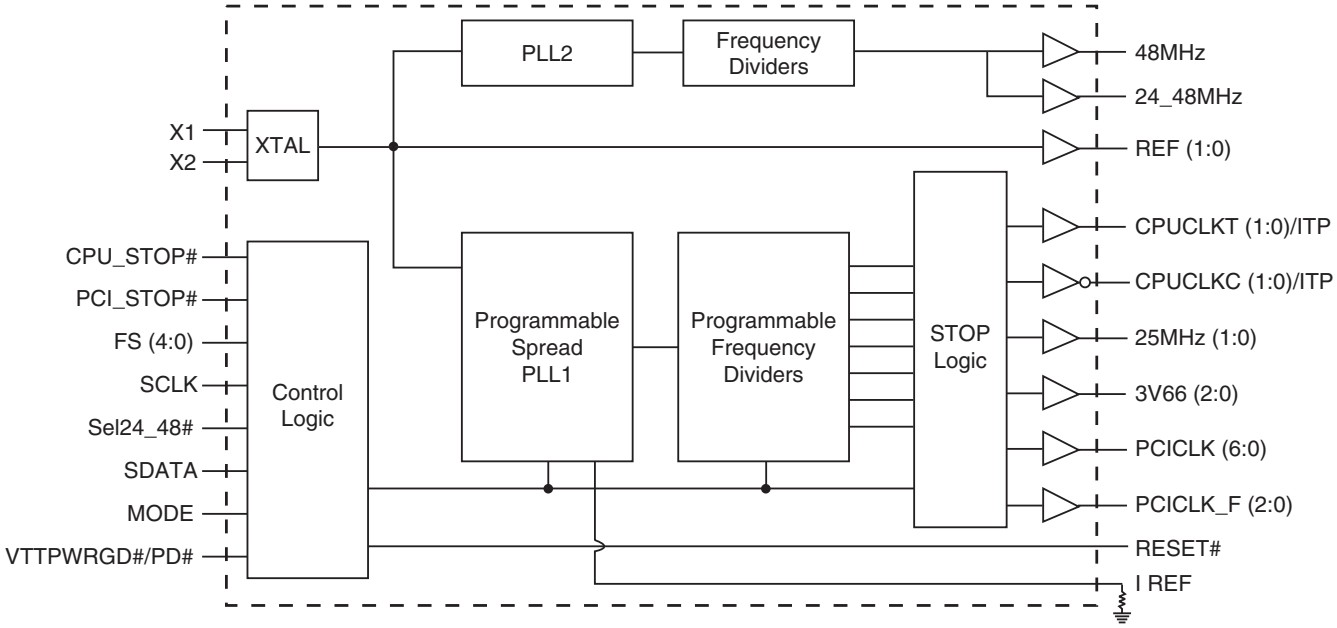
PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	*FS1/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
2	**FS0/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
3	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
4	X1	IN	Crystal input, Nominally 14.318MHz.
5	X2	OUT	Crystal output, Nominally 14.318MHz
6	GND	PWR	Ground pin.
7	**FS2/PCICLK_F0	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
8	**FS4/PCICLK_F1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
9	PCICLK_F2	OUT	Free running PCI clock not affected by PCI_STOP# .
10	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
11	GND	PWR	Ground pin.
12	**MODE/PCICLK0	I/O	Function select latch input pin, 0=Desktop Mode (pin 44/45 are outputs), 1=Mobile Mode (pin44/45 are STOP inputs) / PCI clock output.
13	PCICLK1	OUT	PCI clock output.
14	PCICLK2	OUT	PCI clock output.
15	PCICLK3	OUT	PCI clock output.
16	PCICLK4	OUT	PCI clock output.
17	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
18	GND	PWR	Ground pin.
19	PCICLK5	OUT	PCI clock output.
20	PCICLK6	OUT	PCI clock output.
21	**FS3/48MHz	I/O	Frequency select latch input pin / Fixed 48MHz clock output. 3.3V
22	**Sel24_48#/24_48MHz	I/O	Latched select input for 24/48MHz output / 24/48MHz clock output. 1=24MHz, 0 = 48MHz.
23	GND	PWR	Ground pin.
24	VDD48	PWR	Power pin for the 48MHz output.3.3V
25	3V66_2	OUT	3.3V 66.66MHz clock output
26	3V66_1	OUT	3.3V 66.66MHz clock output
27	VDD3V66	PWR	Power pin for the 3.3V 66MHz clocks.
28	GND	PWR	Ground pin.
29	3V66_0	OUT	3.3V 66.66MHz clock output
30	Reset#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
31	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
32	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
33	VttPWR_GD/PD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.
34	VDD2.5	PWR	Power supply, nominal 2.5V
35	25Mhz_1	OUT	25MHz clock output, 2.5V
36	25Mhz_0	OUT	25MHz clock output, 2.5V
37	GND	PWR	Ground pin.
38	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
39	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
40	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
41	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
43	GND	PWR	Ground pin.
44	CPUCLKC_ITP/(CPU_STOP#)	I/O	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / Stops all CPUCLK besides the free running clocks
45	CPUCLKT_ITP/(PCI_STOP#)	I/O	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / Stops all PCICLK besides the free running clocks
46	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
47	GND	PWR	Ground pin.
48	VDDA	PWR	3.3V power for the PLL core.

General Description

ICS952906A is a 48 pin clock chip for VIA VN800/CN700/P4M800 style chipsets. When used with a fanout DDR buffer, such as the 93788, it provides all the necessary clock signals for such a system.

The **ICS952906A** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
3	6	REF, Xtal
10, 17	11, 18	PCICLK outputs
24	23	48MHz Fix, Fix Digital, Fix analog
27	28	3V66 outputs
34	37	2.5V for 25MHz outputs
40	43	CPU outputs
48	47	CPU Analog, CPU digital

General I²C serial interface information for the ICS952906A

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table1: QuadRom Frequency Selection Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
0	0	0	0	0	0	0	100.00	66.67	33.33	0 to -0.5% Down
0	0	0	0	0	0	1	200.00	66.67	33.33	0 to -0.5% Down
0	0	0	0	0	1	0	133.33	66.67	33.33	0 to -0.5% Down
0	0	0	0	0	1	1	166.67	66.67	33.33	0 to -0.5% Down
0	0	0	0	1	0	0	200.00	66.67	33.33	0 to -0.5% Down
0	0	0	0	1	0	1	400.00	66.67	33.33	0 to -0.5% Down
0	0	0	0	1	1	0	266.67	66.67	33.33	0 to -0.5% Down
0	0	0	0	1	1	1	333.33	66.67	33.33	0 to -0.5% Down
0	0	0	1	0	0	0	100.99	67.33	33.66	0.25% Center
0	0	0	1	0	0	1	201.98	67.33	33.66	0.25% Center
0	0	0	1	0	1	0	134.65	67.33	33.66	0.25% Center
0	0	0	1	0	1	1	168.31	67.32	33.66	0.25% Center
0	0	0	1	1	0	0	115.00	76.67	38.33	No Spread
0	0	0	1	1	0	1	230.00	76.67	38.33	No Spread
0	0	0	1	1	1	0	153.33	76.66	38.33	No Spread
0	0	0	1	1	1	1	191.67	76.67	38.33	No Spread
0	0	1	0	0	0	0	100.00	66.66	33.33	0.25% Center
0	0	1	0	0	0	1	200.00	66.66	33.33	0.25% Center
0	0	1	0	0	1	0	133.33	66.66	33.33	0.25% Center
0	0	1	0	0	1	1	166.67	71.43	35.71	0.25% Center
0	0	1	0	1	0	0	200.00	66.66	33.33	0.25% Center
0	0	1	0	1	0	1	400.00	66.66	33.33	0.25% Center
0	0	1	0	1	1	0	266.67	66.66	33.33	0.25% Center
0	0	1	0	1	1	1	333.33	66.66	33.33	0.25% Center
0	0	1	1	0	0	0	105.00	69.99	35.00	No Spread
0	0	1	1	0	0	1	210.00	69.99	35.00	No Spread
0	0	1	1	0	1	0	140.00	69.99	35.00	No Spread
0	0	1	1	0	1	1	175.00	69.99	35.00	No Spread
0	0	1	1	1	0	0	110.00	73.33	36.66	No Spread
0	0	1	1	1	0	1	220.00	73.33	36.66	No Spread
0	0	1	1	1	1	0	146.66	73.33	36.66	No Spread
0	0	1	1	1	1	1	183.34	73.33	36.66	No Spread

Table1: QuadRom Frequency Selection Table (Continued)

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
0	1	0	0	0	0	0	103.00	68.66	34.33	No Spread
0	1	0	0	0	0	1	206.00	68.66	34.33	No Spread
0	1	0	0	0	1	0	137.33	68.66	34.33	No Spread
0	1	0	0	0	1	1	171.67	68.66	34.33	No Spread
0	1	0	0	1	0	0	228.89	68.66	34.33	No Spread
0	1	0	0	1	0	1	412.00	68.66	34.33	No Spread
0	1	0	0	1	1	0	274.67	68.66	34.33	No Spread
0	1	0	0	1	1	1	343.33	68.66	34.33	No Spread
0	1	0	1	0	0	0	105.00	69.99	35.00	No Spread
0	1	0	1	0	0	1	210.00	69.99	35.00	No Spread
0	1	0	1	0	1	0	140.00	69.99	35.00	No Spread
0	1	0	1	0	1	1	175.00	69.99	35.00	No Spread
0	1	0	1	1	0	0	233.33	69.99	35.00	No Spread
0	1	0	1	1	0	1	420.00	69.99	35.00	No Spread
0	1	0	1	1	1	0	280.00	69.99	35.00	No Spread
0	1	0	1	1	1	1	350.00	69.99	35.00	No Spread
0	1	1	0	0	0	0	107.00	71.33	35.66	No Spread
0	1	1	0	0	0	1	214.00	71.33	35.66	No Spread
0	1	1	0	0	1	0	142.66	71.33	35.66	No Spread
0	1	1	0	0	1	1	178.34	71.33	35.66	No Spread
0	1	1	0	1	0	0	237.78	71.33	35.66	No Spread
0	1	1	0	1	0	1	428.00	71.33	35.66	No Spread
0	1	1	0	1	1	0	285.34	71.33	35.66	No Spread
0	1	1	0	1	1	1	356.66	71.33	35.66	No Spread
0	1	1	1	0	0	0	110.00	73.33	36.66	No Spread
0	1	1	1	0	0	1	220.00	73.33	36.66	No Spread
0	1	1	1	0	1	0	146.66	73.33	36.66	No Spread
0	1	1	1	0	1	1	183.34	73.33	36.66	No Spread
0	1	1	1	1	0	0	244.44	73.33	36.66	No Spread
0	1	1	1	1	0	1	440.00	73.33	36.66	No Spread
0	1	1	1	1	1	0	293.34	73.33	36.66	No Spread
0	1	1	1	1	1	1	366.66	73.33	36.66	No Spread

Table1: QuadRom Frequency Selection Table (Continued)

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
1	0	0	0	0	0	0	95.00	63.33	31.66	No Spread
1	0	0	0	0	0	1	190.00	63.33	31.66	No Spread
1	0	0	0	0	1	0	126.66	63.33	31.66	No Spread
1	0	0	0	0	1	1	158.34	63.33	31.66	No Spread
1	0	0	0	1	0	0	211.11	63.33	31.66	No Spread
1	0	0	0	1	0	1	380.00	63.33	31.66	No Spread
1	0	0	0	1	1	0	253.34	63.33	31.66	No Spread
1	0	0	0	1	1	1	316.66	63.33	31.66	No Spread
1	0	0	1	0	0	0	90.00	59.99	30.00	No Spread
1	0	0	1	0	0	1	180.00	59.99	30.00	No Spread
1	0	0	1	0	1	0	120.00	59.99	30.00	No Spread
1	0	0	1	0	1	1	150.00	59.99	30.00	No Spread
1	0	0	1	1	0	0	200.00	59.99	30.00	No Spread
1	0	0	1	1	0	1	360.00	59.99	30.00	No Spread
1	0	0	1	1	1	0	240.00	59.99	30.00	No Spread
1	0	0	1	1	1	1	300.00	59.99	30.00	No Spread
1	0	1	0	0	0	0	85.00	56.66	28.33	No Spread
1	0	1	0	0	0	1	170.00	56.66	28.33	No Spread
1	0	1	0	0	1	0	113.33	56.66	28.33	No Spread
1	0	1	0	0	1	1	141.67	56.66	28.33	No Spread
1	0	1	0	1	0	0	188.89	56.66	28.33	No Spread
1	0	1	0	1	0	1	340.00	56.66	28.33	No Spread
1	0	1	0	1	1	0	226.67	56.66	28.33	No Spread
1	0	1	0	1	1	1	283.33	56.66	28.33	No Spread
1	0	1	1	0	0	0	80.00	53.33	26.66	No Spread
1	0	1	1	0	0	1	160.00	53.33	26.66	No Spread
1	0	1	1	0	1	0	106.66	53.33	26.66	No Spread
1	0	1	1	0	1	1	133.34	53.33	26.66	No Spread
1	0	1	1	1	0	0	177.78	53.33	26.66	No Spread
1	0	1	1	1	0	1	320.00	53.33	26.66	No Spread
1	0	1	1	1	1	0	213.34	53.33	26.66	No Spread
1	0	1	1	1	1	1	266.66	53.33	26.66	No Spread

Table1: QuadRom Frequency Selection Table (Continued)

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	AGP	PCI	Spread
		FS4	FS3	FS2	FS1	FS0	MHz	MHz	MHz	%
1	1	0	0	0	0	0	115.00	76.66	38.33	No Spread
1	1	0	0	0	0	1	230.00	76.66	38.33	No Spread
1	1	0	0	0	1	0	153.33	76.66	38.33	No Spread
1	1	0	0	0	1	1	191.67	76.66	38.33	No Spread
1	1	0	0	1	0	0	255.55	76.66	38.33	No Spread
1	1	0	0	1	0	1	460.00	76.66	38.33	No Spread
1	1	0	0	1	1	0	306.67	76.66	38.33	No Spread
1	1	0	0	1	1	1	383.33	76.66	38.33	No Spread
1	1	0	1	0	0	0	115.00	79.99	40.00	No Spread
1	1	0	1	0	0	1	230.00	79.99	40.00	No Spread
1	1	0	1	0	1	0	153.33	79.99	40.00	No Spread
1	1	0	1	0	1	1	191.67	79.99	40.00	No Spread
1	1	0	1	1	0	0	255.55	79.99	40.00	No Spread
1	1	0	1	1	0	1	460.00	79.99	40.00	No Spread
1	1	0	1	1	1	0	306.67	79.99	40.00	No Spread
1	1	0	1	1	1	1	383.33	79.99	40.00	No Spread
1	1	1	0	0	0	0	78.00	51.99	26.00	No Spread
1	1	1	0	0	0	1	156.00	51.99	26.00	No Spread
1	1	1	0	0	1	0	104.00	51.99	26.00	No Spread
1	1	1	0	0	1	1	130.00	51.99	26.00	No Spread
1	1	1	0	1	0	0	173.33	51.99	26.00	No Spread
1	1	1	0	1	0	1	312.00	51.99	26.00	No Spread
1	1	1	0	1	1	0	208.00	51.99	26.00	No Spread
1	1	1	0	1	1	1	260.00	51.99	26.00	No Spread
1	1	1	1	0	0	0	75.00	50.00	25.00	No Spread
1	1	1	1	0	0	1	150.00	50.00	25.00	No Spread
1	1	1	1	0	1	0	100.00	50.00	25.00	No Spread
1	1	1	1	0	1	1	125.00	50.00	25.00	No Spread
1	1	1	1	1	0	0	166.67	50.00	25.00	No Spread
1	1	1	1	1	0	1	300.00	50.00	25.00	No Spread
1	1	1	1	1	1	0	200.00	50.00	25.00	No Spread
1	1	1	1	1	1	1	250.00	50.00	25.00	No Spread

I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	FS6	Freq Select Bit 6	RW	See Table 1: QuadRom Frequency Selection Table		0
Bit 5	-	FS5	Freq Select Bit 5	RW			0
Bit 4	-	FS4	Freq Select Bit 4	RW			0
Bit 3	-	FS3	Freq Select Bit 3	RW			0
Bit 2	-	FS2	Freq Select Bit 2	RW			0
Bit 1	-	FS1	Freq Select Bit 1	RW			0
Bit 0	-	FS0	Freq Select Bit 0	RW			0

I²C Table: Spreading and Device Behavior Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS1	Spread Select 1**	RW	00 = 0.20%	10 = 0.35%	0
Bit 6	-	SS0	Spread Select 0**	RW	01 = 0.25%	Reserved	1
Bit 5	-	SS_EN	Spread Enable Control	RW	ON	OFF	1
Bit 4	-	WDS_EN	WD Soft Reset Enable	RW	ON	OFF	0
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	45, 44	CPUCLKT/C_ITP, CPU1T/C, CPU0T/C	Output Control	RW	Disable	Enable	1
Bit 1	42,41	CPUCLKT/C_1	Output Control	RW	Disable	Enable	1
Bit 0	39, 38	CPUCLKT/C_0	Output Control	RW	Disable	Enable	1

**** Spread programming only applies for ROM table entries 0001000 to 0001011 and 0010000 to 0010111**

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	36	25MHz_0	Output Control	RW	Disable	Enable	1
Bit 6	35	25MHz_1	Output Control	RW	Disable	Enable	1
Bit 5	-	CPUT Stop Mode	0: CPUT Driven during PD#; 1: Tri-stated	RW	Driven	Hi-Z	0
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	26	3V66_1	Output Control	RW	Disable	Enable	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	42,41	CPUCLKT/C_1	Output Stop Control	RW	Free Run	Stoppable	1
Bit 0	39, 38	CPUCLKT/C_0	Output Stop Control	RW	Free Run	Stoppable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	ASEL1	3V66/PCI Freq Select	RW	See Table 5: Async AGP/PCI Freq Table		0
Bit 6	20	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 5	19	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	16	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	15	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	14	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	13	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	12	PCICLK0	Output Control	RW	Disable	Enable	1

Table 5: Asynchronous 3V66/PCI Frequency Table

Byte6 Bit7	Byte3 Bit7	3V66/PCI Frequency
0	0	66.66/33.33
0	1	80.00/40.00
1	0	72.73/36.36

I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	48MHz_0 2x output drive	0=2x drive	RW	2x drive	normal	1
Bit 6	-	PCI ADIV	PCI Async Divider Cntr	RW	AGP/2	PLL3 Freq/24	0
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	29	3V66_0	Output Control	RW	Disable	Enable	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	9	PCICLK_F2	Output Control	RW	Disable	Enable	1
Bit 1	8	PCICLK_F1	Output Control	RW	Disable	Enable	1
Bit 0	7	PCICLK_F0	Output Control	RW	Disable	Enable	1

I²C Table: Reserved Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Mode Sel1	PLL Mode Selection Bits	RW	See Table 4: Mode Selection Table		0
Bit 5	-	Mode Sel0		RW			0
Bit 4	25	3V66_2	Output Control	RW	Disable	Enable	1
Bit 3	-	M PLL2 Div3	M Divider Programming bits for Async mode 2&3	RW	The decimal representation of M PLL2 Div (3:0) + 2 is equal to REF divider value for PLL2		X
Bit 2	-	M PLL2 Div2		RW			X
Bit 1	-	M PLL2 Div1		RW			X
Bit 0	-	M PLL2 Div0		RW			X

Table 4: Mode Selection Table

Mode	Standard Overclock Mode(I)	CPU Overclock Mode(II)	Graphic Overclock Mode(III)
IIC Control	Byte 5 bit(6:5) = 00	Byte 5 bit(6:5) = 01	Byte 5 bit(6:5) = 10
25MHz From?	PLL3	PLL3	PLL1
3V66/PCI From?	PLL1 (Needed to be align w/ CPU)	PLL3	PLL3
Spreading	CPU/3V66/PCI have spread	Only CPU clocks have spread.	Only CPU clocks have spread.

I²C Table: Vendor & Revision ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	ASEL0	3V66/PCI Freq Select	RW	See Table 5: Async AGP/PCI Freq Table		0
Bit 6	-	N PLL2 Div6	N Divider Programming bits for Async mode 2&3	RW	The decimal representation of N PLL2 Div (6:0) + 8 is equal to VCO divider value for PLL2.		X
Bit 5	-	N PLL2 Div5		RW			X
Bit 4	-	N PLL2 Div4		RW			X
Bit 3	-	N PLL2 Div3		RW			X
Bit 2	-	N PLL2 Div2		RW			X
Bit 1	-	N PLL2 Div1		RW			X
Bit 0	-	N PLL2 Div0		RW			X

I²C Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WD7	WD Timer Bit 7	RW	These bits represent X*290ms the watchdog timer waits before it goes to alarm mode. Default is 11 x 293ms = 3.2s.		0
Bit 6	-	WD6	WD Timer Bit 6	RW			0
Bit 5	-	WD5	WD Timer Bit 5	RW			0
Bit 4	-	WD4	WD Timer Bit 4	RW			0
Bit 3	-	WD3	WD Timer Bit 3	RW			1
Bit 2	-	WD2	WD Timer Bit 2	RW			0
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	R	Disable	Enable	0
Bit 5	-	WDFSEN	WD Safe Frequency Mode	RW	Latched FS/Byte0	WD B10 b(4:0)	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(8:0)+8] / [MDiv(6:0)+2]		X
Bit 6	-	M Div6	M Divider Programming bits	RW			X
Bit 5	-	M Div5		RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(8:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(8:0)+8] / [MDiv(6:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	Reserved	Reserved	R	-	-	0
Bit 5	-	SSP13	Spread Spectrum Programming b(13:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	25MHz Div3	25MHz Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-	25Mhz Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-	25MHz Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-	25MHz Div0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X
Bit 3	-	CPU Div3	CPUDivider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-	CPU Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	CPU Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	CPU Div0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	Reserved	Reserved	RW	-		-		X
Bit 6	-	Reserved		RW	-		-		X
Bit 5	-	Reserved		RW	-		-		X
Bit 4	-	Reserved		RW	-		-		X
Bit 3	-	3V66Div3	3V66/PCI Divider Ratio Programming Bits for Mode 1	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-	3V66Div2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	3V66Div1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	3V66Div0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	X
Bit 6	-	Reserved	Reserved	RW	-	-	X
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Group Skew Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	3V66Skw3	CPU-3V66 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	0
Bit 6	-	3V66Skw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	0
Bit 5	-	3V66Skw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 4	-	3V66Skw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0
Bit 3	-	PCISkw3	CPU-PCI 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 2	-	PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	1
Bit 1	-	PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 0	-	PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0

I²C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	PCISkw3	CPU-PCI F(2:0) 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 6	-	PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	1
Bit 5	-	PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 4	-	PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0
Bit 3	-	Reserved	Reserved	RW	-		-		0
Bit 2	-	Reserved	Reserved	RW	-		-		0
Bit 1	-	Reserved	Reserved	RW	-		-		0
Bit 0	-	Reserved	Reserved	RW	-		-		0

I²C Table: Slew Rate Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIFStr1	PCICLKF (2:0) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 6	-	PCIFStr0			01 = 0.75X	11 = 1.00X	1
Bit 5	-	PCIFStr1	PCICLK (6) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 4	-	PCIFStr0			01 = 0.75X	11 = 1.00X	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	AGPStr1	AGPCLK Strength Control	RW	00 = 0.70X	10 = 0.90X	1
Bit 0	-	AGPStr0		RW	01 = 0.80X	11 = 1.00X	1

I²C Table: Slew Rate Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REF_Slw	REF Slew Rate Control	RW	00 = Medium	10 = Strong	1
Bit 6	-			RW	01 = Weak	11 = N/A	0
Bit 5	-	PCIFStr1	PCICLK (5) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 4	-	PCIFStr0			01 = 0.75X	11 = 1.00X	1
Bit 3	-	PCIFStr1	PCICLK (4:2) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 2	-	PCIFStr0			01 = 0.75X	11 = 1.00X	1
Bit 1	-	PCIFStr1	PCICLK (1:0) Strength Control	RW	00 = 0.63X	10 = 0.88X	1
Bit 0	-	PCIFStr0			01 = 0.75X	11 = 1.00X	1

I²C Table: Output Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	48MHz_0	Output Control	RW	Disable	Enable	1
Bit 6	-	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 5	-	REF1	Output Control	RW	Disable	Enable	1
Bit 4	-	REF0	Output Control	RW	Disable	Enable	1
Bit 3	-	REF2	Output Control	RW	Disable	Enable	1
Bit 2	-	48MHz_1	Output Control	RW	Disable	Enable	1
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Read Back Register

Byte 24	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDHRB	WD Hard Alarm Status Read back	R	-	-	X
Bit 6	-	WDSRB	WD Soft Alarm Status Read back	R	-	-	X
Bit 5	-	Reserved	Reserved	R	-	-	0
Bit 4	-	FS4RB	FS4 Read back	R	-	-	X
Bit 3	-	FS3RB	FS3 Read back	R	-	-	X
Bit 2	-	FS2RB	FS2 Read back	R	-	-	X
Bit 1	-	FS1RB	FS1 Read back	R	-	-	X
Bit 0	-	FS0RB	FS0 Read back	R	-	-	X

Absolute Maximum Ratings

Core Operating Voltage . . . . . 4.6 V
I/O Operating Voltage 3.6V
Lo gic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3V +/-5%	2		V_{DD} + 0.3	V	
Input MID Voltage	V_{MID}	3.3V +/-5%	1		1.8	V	
Input Low Voltage	V_{IL}	3.3V +/-5%	V_{SS} -0.3		0.8	V	
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			350	mA	
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			35	mA	
		all differential pairs tri-stated			12	mA	
Input Frequency[3]	F_i	V_{DD} = 3.3 V		14.31818		MHz	3
Pin Inductance[1]	L_{pin}				7	nH	1
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization[1,2]	T_{STAB}	From VDD Power-Up or de-assertion of PD# to 1st clock.			1.8	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPU & SRC 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3V +/-5%; C_L =2pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1
Voltage Low	VLow		-150		150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			100	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			125	ps	1

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - 3V66

T_A = 0 - 70°C; V_{DD} = 3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Output High Current	I_{OH}	$V_{OH@MIN}$ = 1.0 V	-33			mA	
		$V_{OH@MAX}$ = 3.135 V			-33	mA	
Output Low Current	I_{OL}	$V_{OL@MIN}$ = 1.95 V	30			mA	
		$V_{OL@MAX}$ = 0.4 V			38	mA	
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Skew	t_{sk1}	V_T = 1.5 V			250	ps	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V 3V66			250	ps	1

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Output High Current	I_{OH}	$V_{OH@MIN}$ = 1.0 V	-33			mA	
		$V_{OH@MAX}$ = 3.135 V			-33	mA	
Output Low Current	I_{OL}	$V_{OL@MIN}$ = 1.95 V	30			mA	
		$V_{OL@MAX}$ = 0.4 V			38	mA	
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Skew	t_{sk1}	V_T = 1.5 V			500	ps	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V 3V66			250	ps	1

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - 48MHz, 24MHz

T_A = 0 - 70°C; V_{DD} = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-200		200	ppm	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Output High Current	I_{OH}	$V_{OH@MIN}$ = 1.0 V	-33			mA	
		$V_{OH@MAX}$ = 3.135 V			-33	mA	
Output Low Current	I_{OL}	$V_{OL@MIN}$ = 1.95 V	30			mA	
		$V_{OL@MAX}$ = 0.4 V			38	mA	
Edge Rate		Rising edge rate	1		2	V/ns	1
Edge Rate		Falling edge rate	1		2	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Long Term Jitter		125us period jitter (8kHz frequency modulation amplitude)			6	ns	1

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

Electrical Characteristics - REF-14.318MHz

T_A = 0 - 70°C; V_{DD} = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V	
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA	
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA	
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps	1
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			1000	ps	1

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

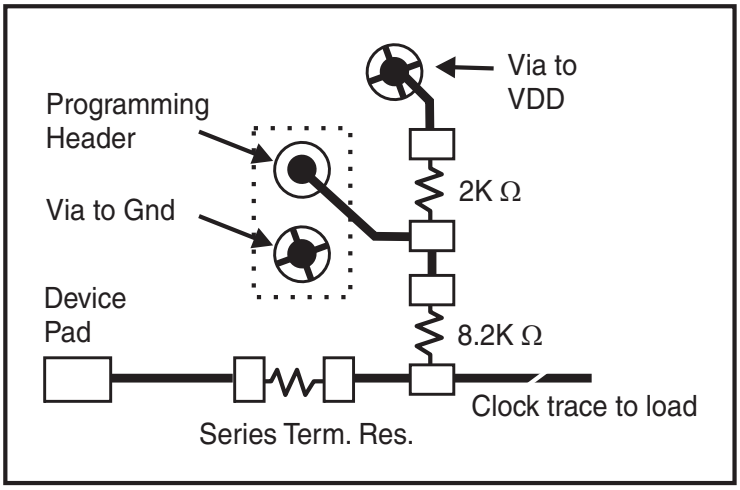
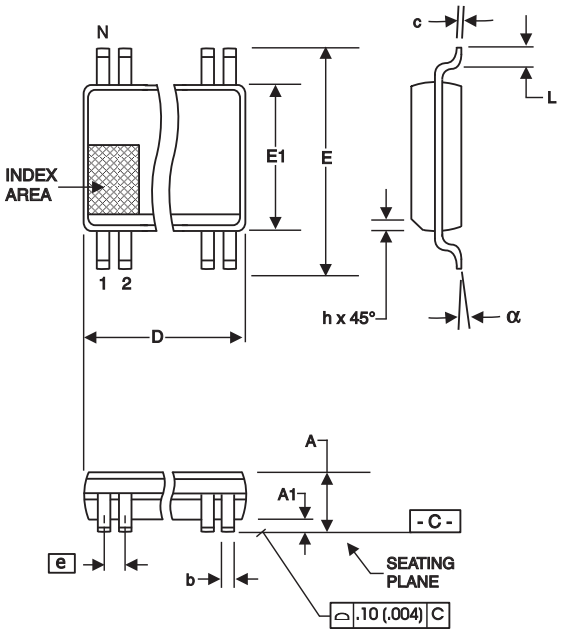


Fig. 1



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

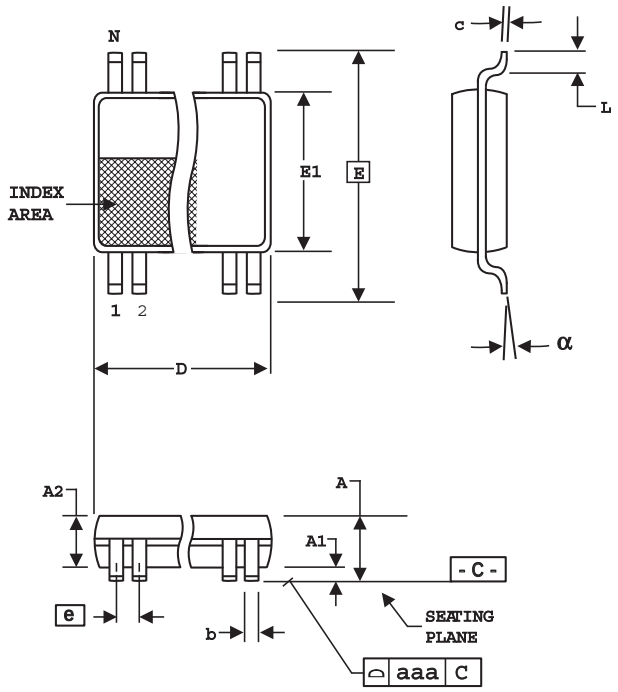
ICS952906AFLFT

Example:

ICS XXXX A F LF- T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator**
- **Device Type**
- **Prefix**
  ICS = Standard Device

1236A—08/06/07



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS952906AGLFT

Example:

ICS XXXX A G LF- T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator**
- **Device Type**
- **Prefix**
  ICS = Standard Device

1236A—08/06/07

Revision History

Rev.	Issue Date	Description	Page #
N/A	06/15/06	Initial Release	-
0.1	08/29/06	Updated I2C	13
A	08/06/07	1. Updated 48/24MHz Electrical Characteristics 2. Final release	19

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- Alternative Solution
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