

Product Overview

Qorvo's TGA2307 is a MMIC power amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. Operating from 5 – 6 GHz, the TGA2307 produces greater than 47 dBm of saturated output power with power-added efficiency greater than 40 % and large signal gain greater than 20 dB.

Both ports are fully matched to 50 ohms with integrated DC blocking capacitors thereby simplifying system integration. The TGA2307's performance makes it well suited for both commercial and military applications.

Lead-free and RoHS compliant.

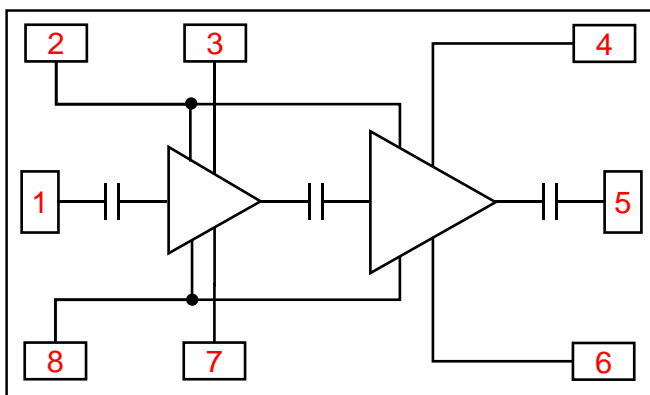


Key Features

- Frequency Range: 5.0 – 6.0 GHz
- Output Power ($P_{IN} = 27$ dBm): > 47 dBm
- Power Added Efficiency ($P_{IN} = 27$ dBm): > 40 %
- Small Signal Gain: > 26 dB
- Input Return Loss: > 18 dB
- Large Signal Gain ($P_{IN} = 27$ dBm): > 20 dB
- Bias Condition: $V_D = 28$ V, $I_{DQ} = 1000$ mA
- Chip Dimensions: 4.280 x 4.260 x 0.100 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- C-Band Radar
- Satellite Communication

Ordering Information

Part No.	Description
TGA2307	5.0 – 6.0 GHz 50 W GaN Power Amplifier
TGA2307S2	Samples (2 pcs.)
TGA2307EVB	Evaluation Board for TGA2307

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to +1 V
Peak Drain Current (I_D)	7.2 A
Gate Current (I_G)	See plot, pg. 11
Power Dissipation (P_{DISS}), 85°C	96 W
Input Power (P_{IN}), Pulsed, 50Ω, $V_D=28V$, $I_{DQ}=1000mA$, 85 °C	33 dBm
Input Power (P_{IN}), Pulsed, 3:1 VSWR, $V_D=28V$, $I_{DQ}=1000mA$, 85 °C	33 dBm
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	-65 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	28 V
Drain Current (I_{DQ})	1000 mA
Gate Voltage (V_G), Typical	-2.5 V
Operating Temperature	-40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

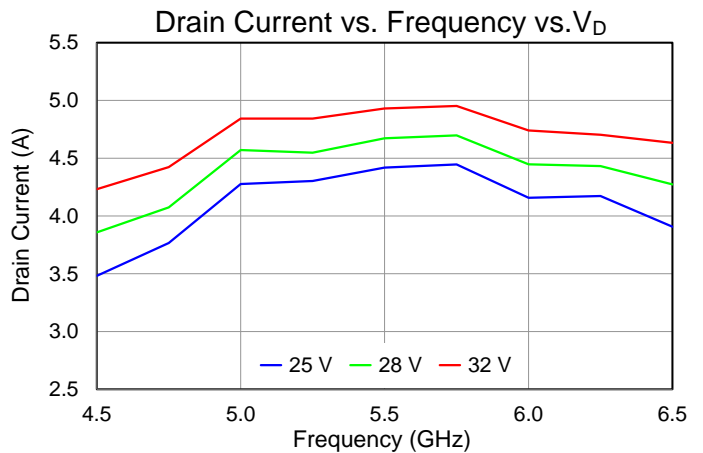
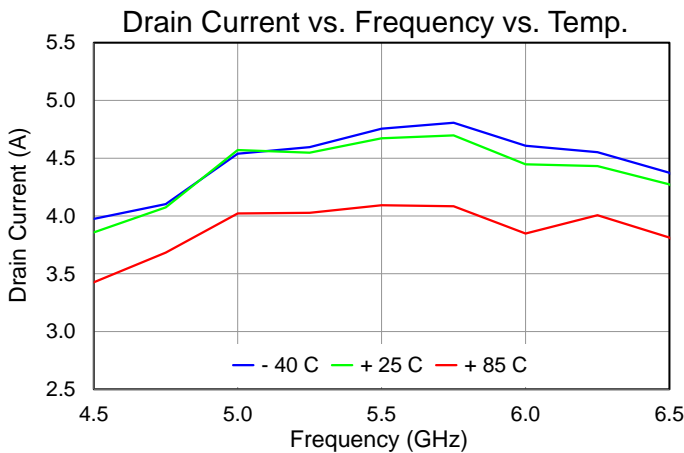
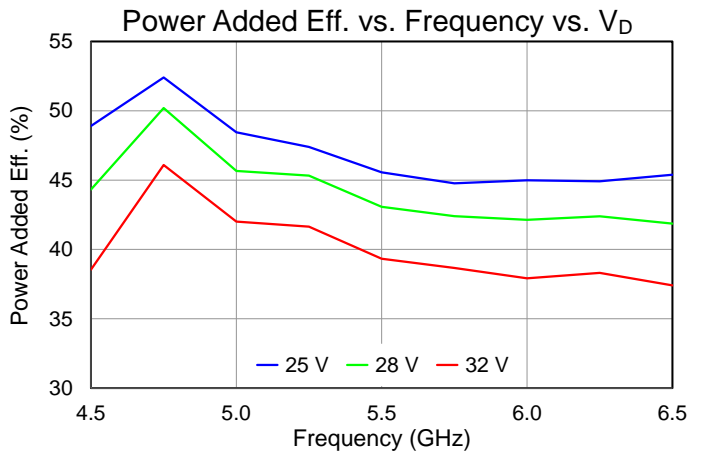
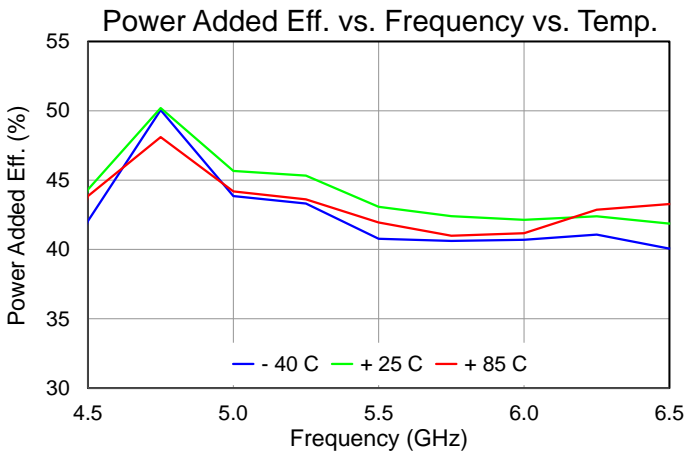
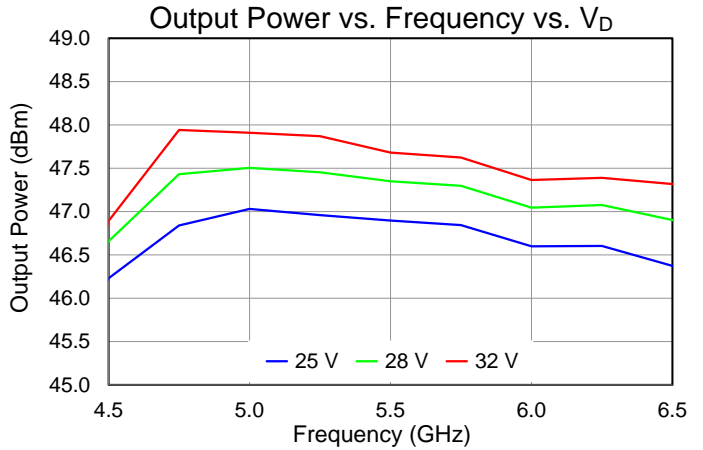
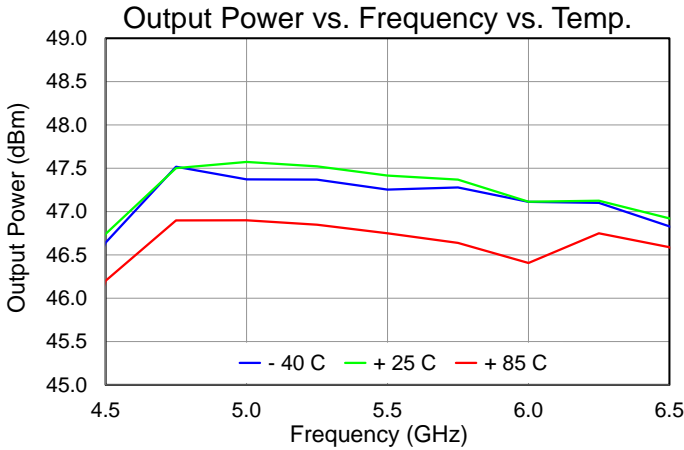
Electrical Specifications

Parameter		Min	Typ	Max	Units
Operational Frequency Range		5.0		6.0	GHz
Output Power ($P_{IN} = 27$ dBm)	5.0 GHz		47.6		dBm
	5.5 GHz		47.4		dBm
	6.0 GHz		47.1		dBm
Power Added Efficiency ($P_{IN} = 27$ dBm)	5.0 GHz		45.7		%
	5.5 GHz		43.1		%
	6.0 GHz		42.1		%
Small Signal Gain (CW) ($I_{DQ} = 500$ mA)	5.0 GHz		24.7		dB
	5.5 GHz		24.3		dB
	6.0 GHz		24.8		dB
Input Return Loss (CW) ($I_{DQ} = 500$ mA)	5.0 GHz		26		dB
	5.5 GHz		22		dB
	6.0 GHz		25		dB
Output Return Loss (CW) ($I_{DQ} = 500$ mA)	5.0 GHz		10		dB
	5.5 GHz		8		dB
	6.0 GHz		8		dB
2 nd Harmonic Performance			See plots pg. 7,8		
3 rd Harmonic Performance			See plots pg. 7,8		
Output Power Temp. Coeff. (85 – 25 °C, $P_{IN} = 27$ dBm))			-0.012		dB/°C
Sm. Signal Gain Temperature Coefficient (85 to -40 °C)			-0.044		dB/°C

Test conditions, unless otherwise noted: T = 25 °C, $V_D = 28$ V, $I_{DQ} = 1000$ mA, Typical, PW = 100 us, Duty Cycle = 10%

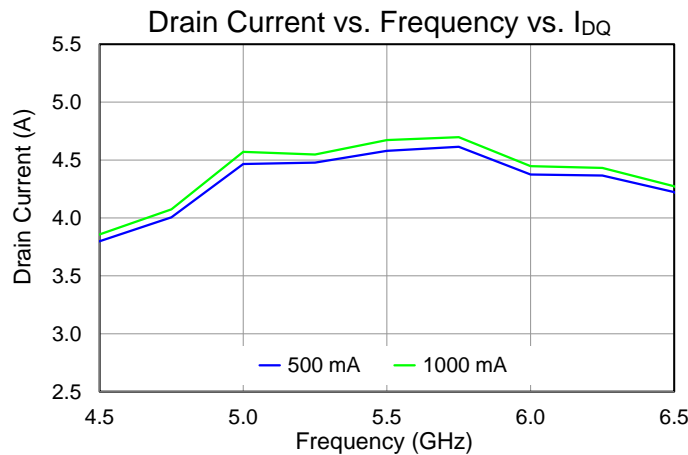
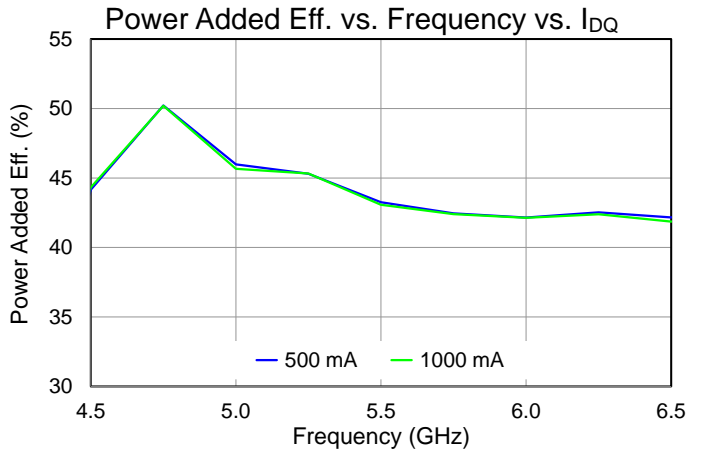
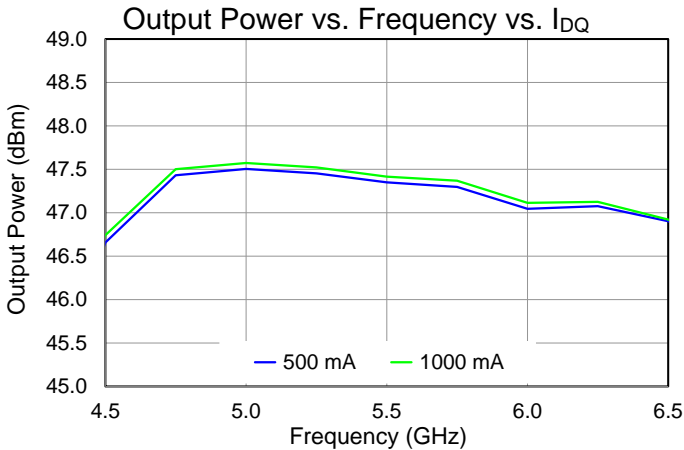
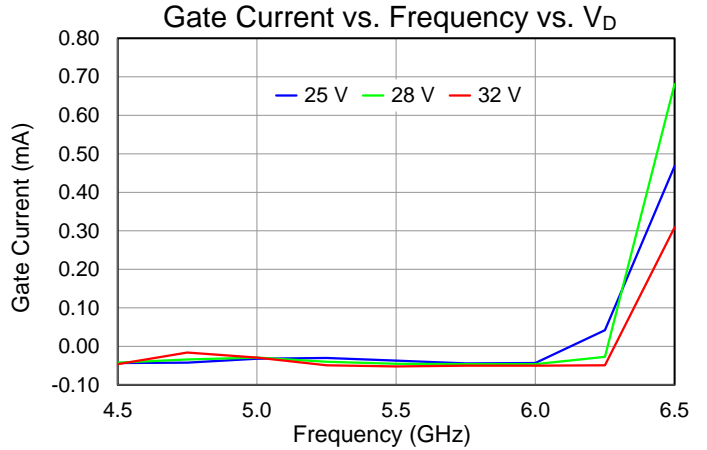
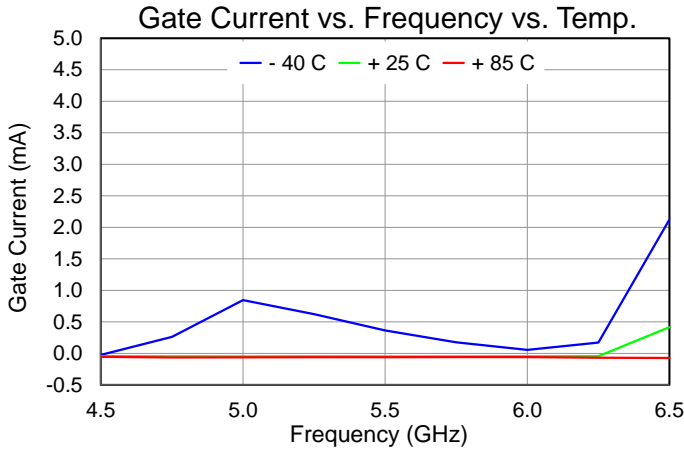
Performance Plots – Large Signal

Test conditions unless otherwise noted: $V_D = 28\text{ V}$, $I_{DQ} = 1000\text{ mA}$, $P_{IN} = 27\text{ dBm}$, $T = 25\text{ }^\circ\text{C}$, $PW = 100\text{ }\mu\text{s}$, Duty Cycle = 10%



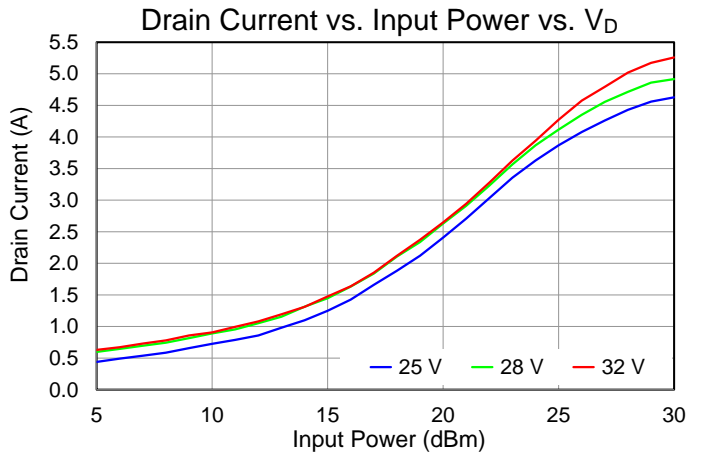
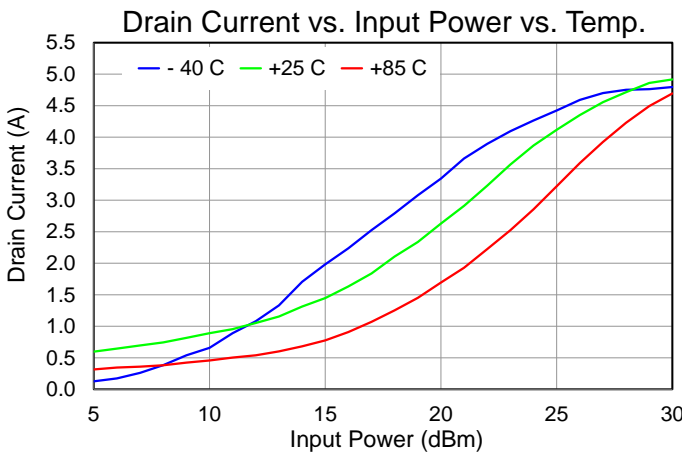
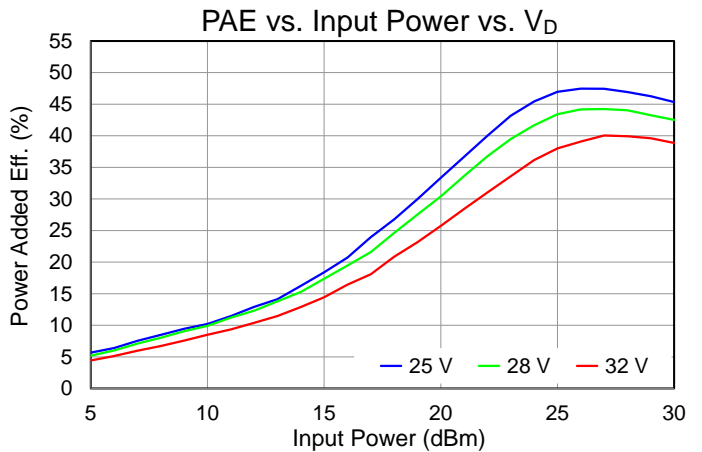
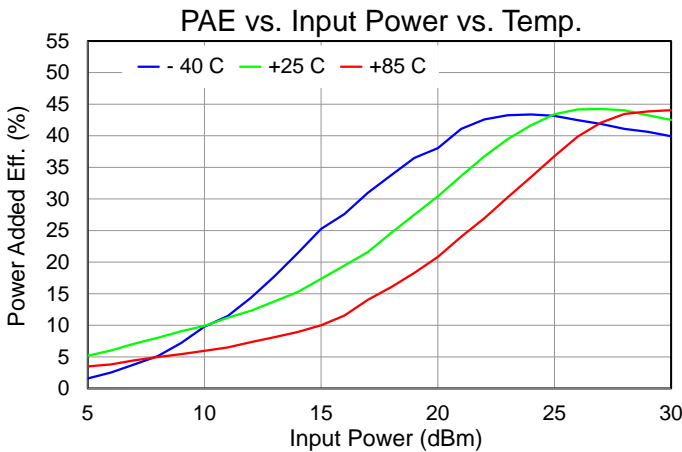
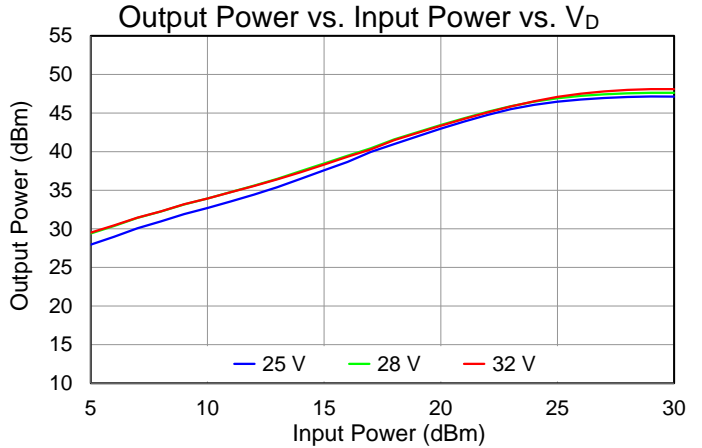
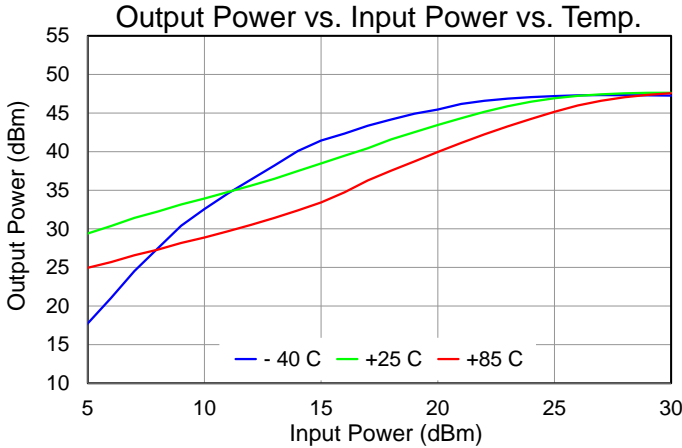
Performance Plots – Large Signal

Test conditions unless otherwise noted: $V_D = 28\text{ V}$, $I_{DQ} = 1000\text{ mA}$, $P_{IN} = 27\text{ dBm}$, $T = 25\text{ }^\circ\text{C}$, $PW = 100\text{ }\mu\text{s}$, Duty Cycle = 10%



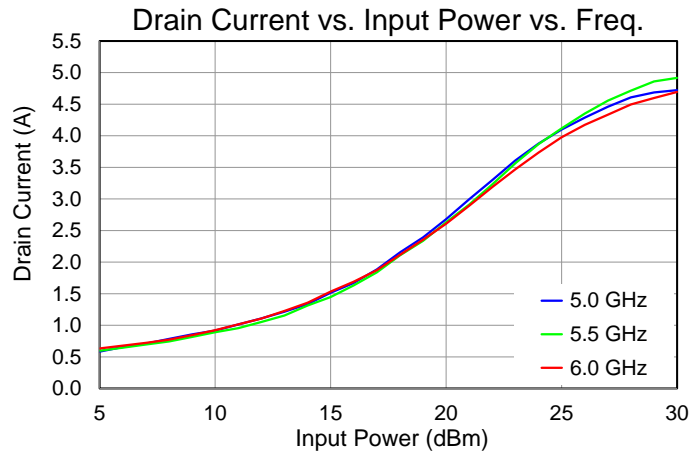
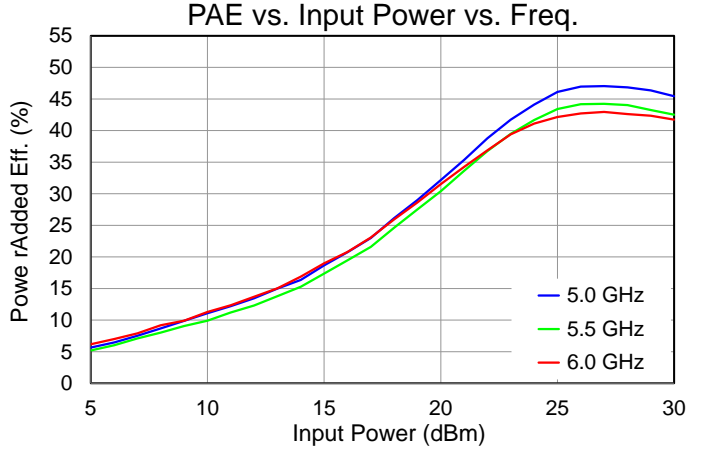
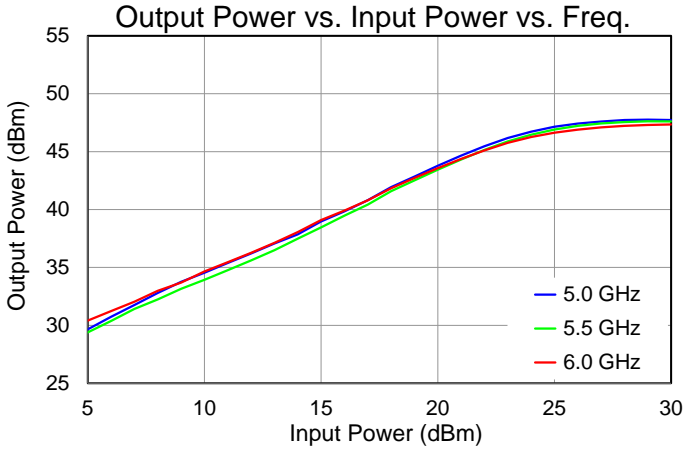
Performance Plots – Large Signal

Test conditions unless otherwise noted: $V_D = 28\text{ V}$, $I_{DQ} = 500\text{ mA}$, Freq. = 5.5 GHz, $T = 25\text{ }^\circ\text{C}$, PW = 100 us, Duty Cycle = 10%



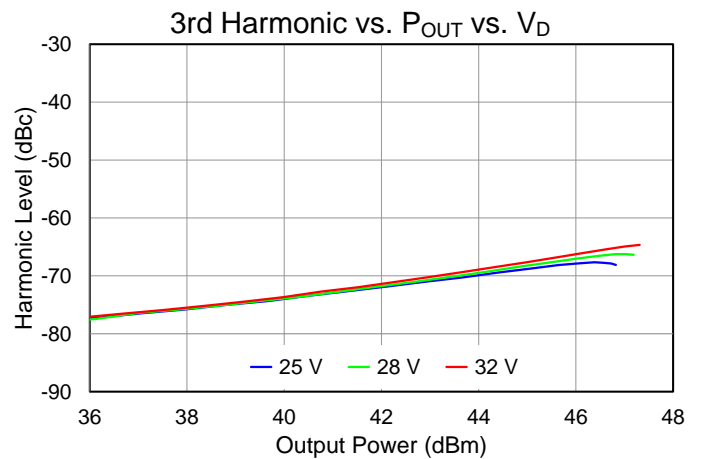
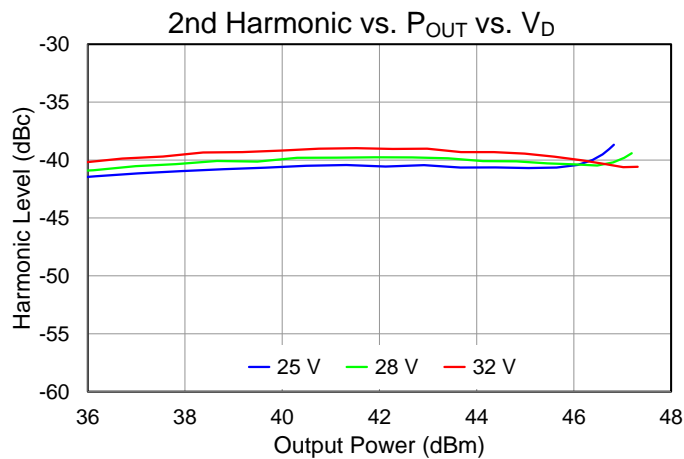
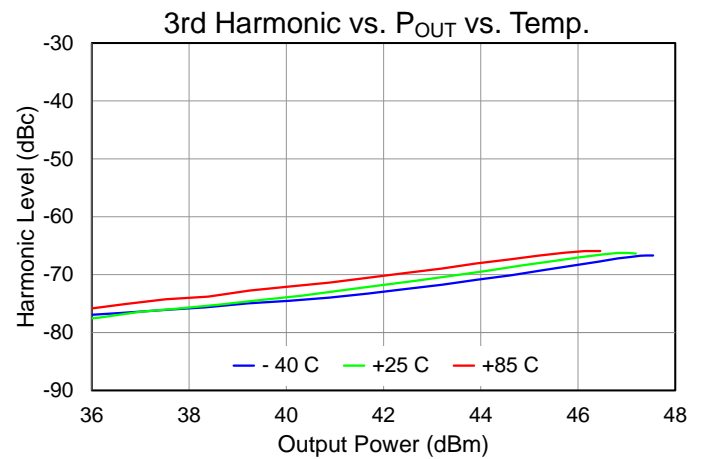
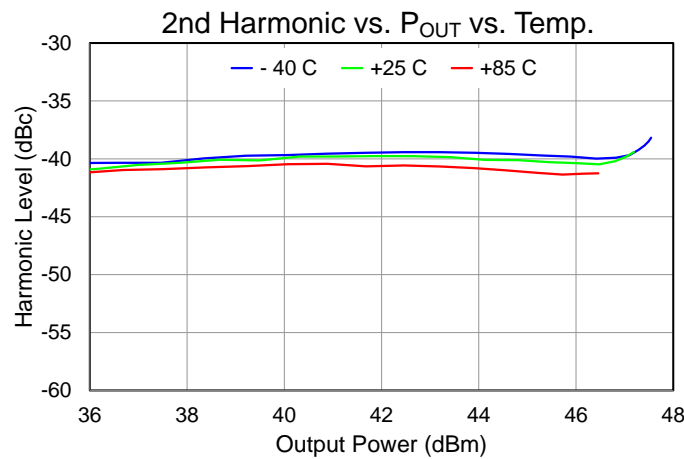
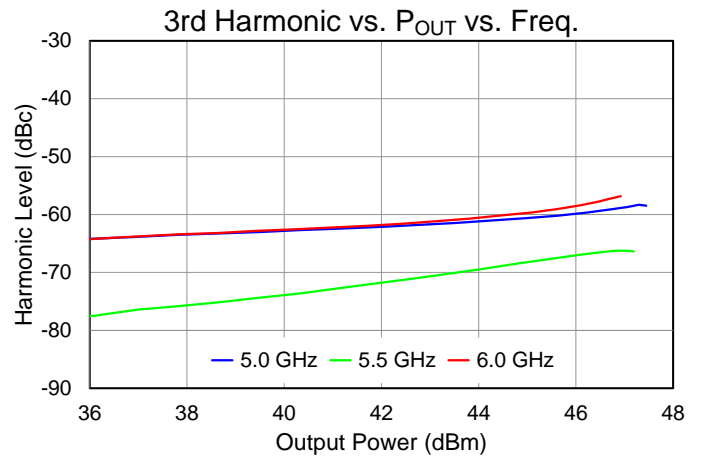
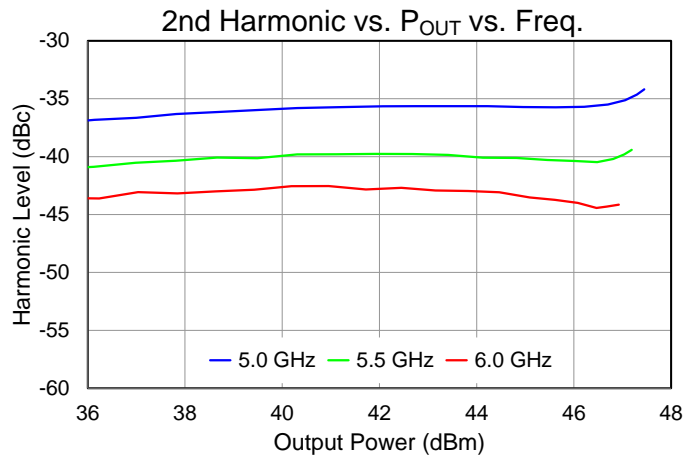
Performance Plots – Large Signal

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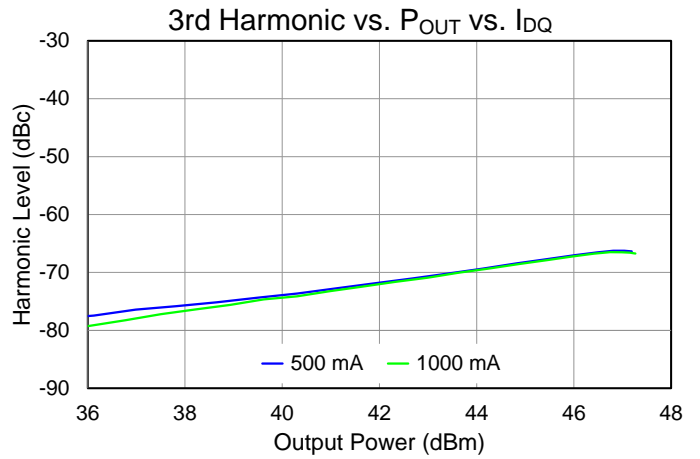
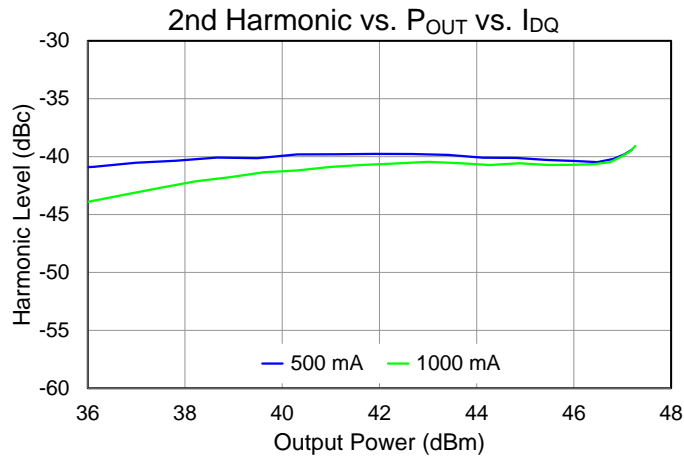
Performance Plots – Harmonics

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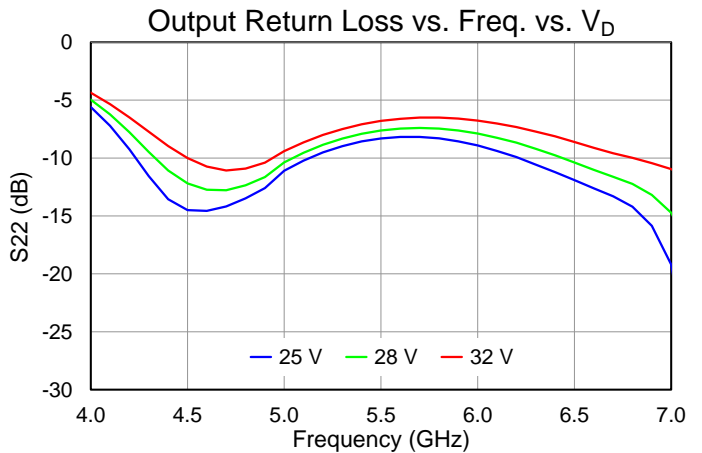
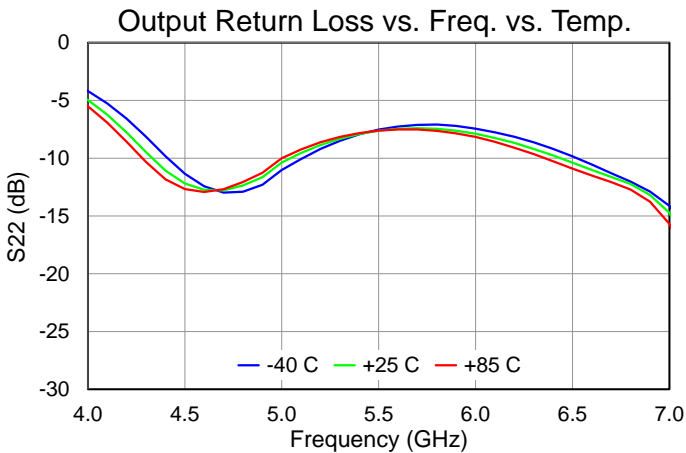
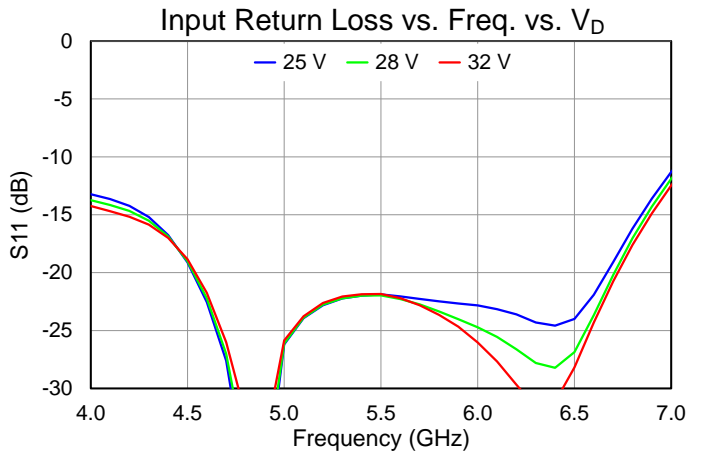
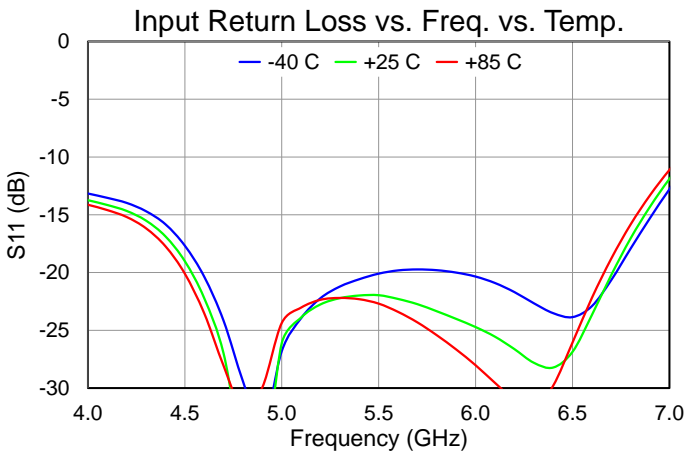
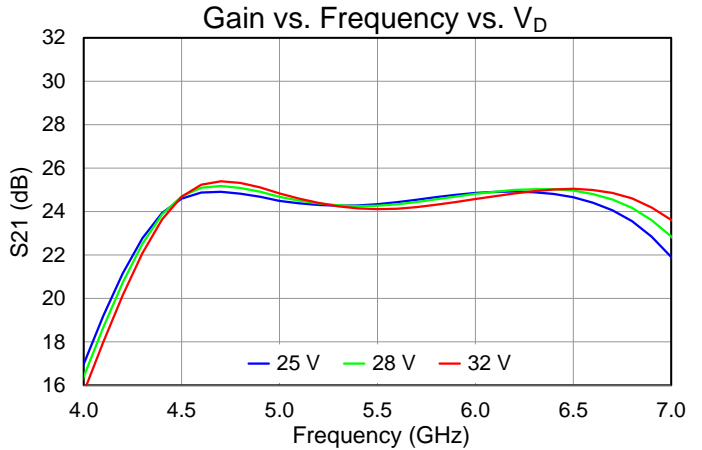
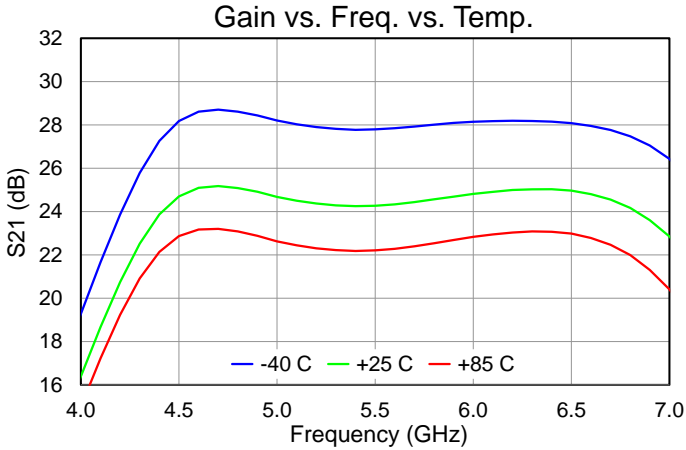
Performance Plots – Harmonics

Test conditions unless otherwise noted: $V_D = 28\text{ V}$, $I_{DQ} = 500\text{ mA}$, $P_{IN} = 27\text{ dBm}$, $PW = 100\text{ us}$, Duty Cycle = 10%



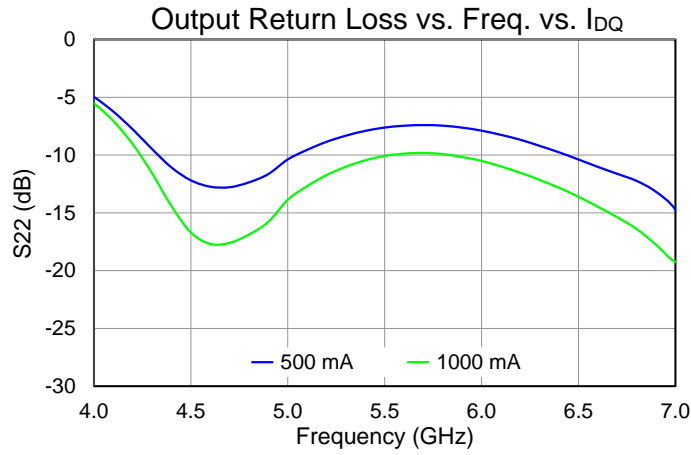
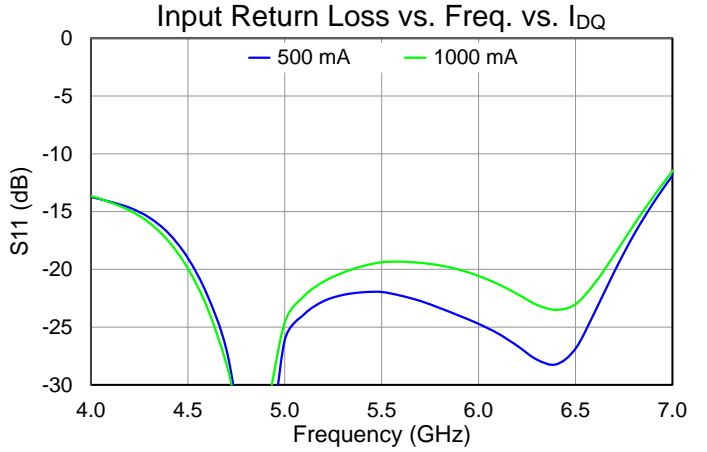
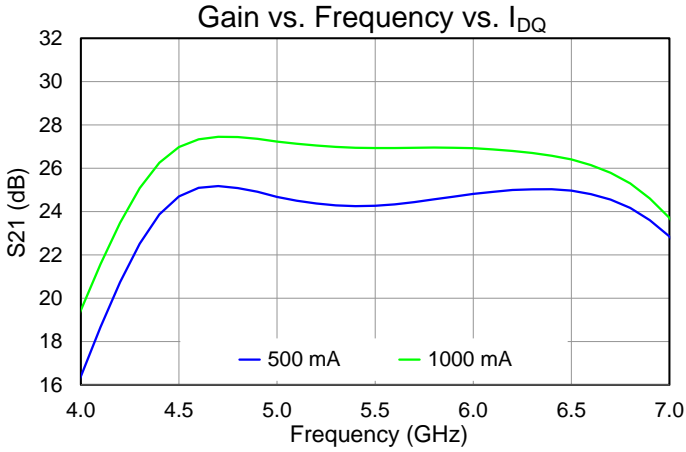
Performance Plots – Small Signal (CW)

Test conditions unless otherwise noted: $V_d = 28\text{ V}$, $I_{dq} = 500\text{ mA}$, $T = 25\text{ }^\circ\text{C}$



Performance Plots – Small Signal (CW)

Test conditions unless otherwise noted: $V_d = 28\text{ V}$, $I_{dq} = 500\text{ mA}$, $T = 25\text{ }^\circ\text{C}$



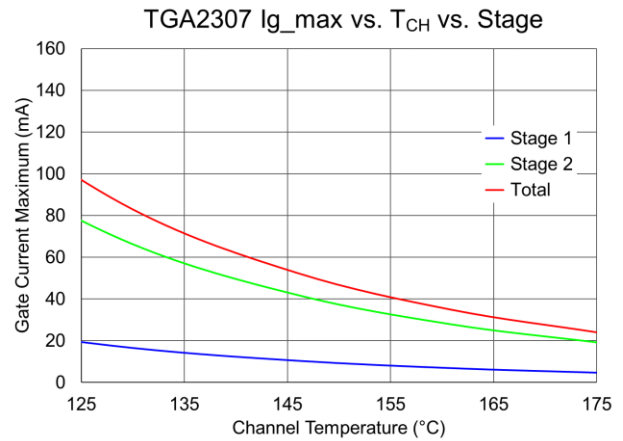
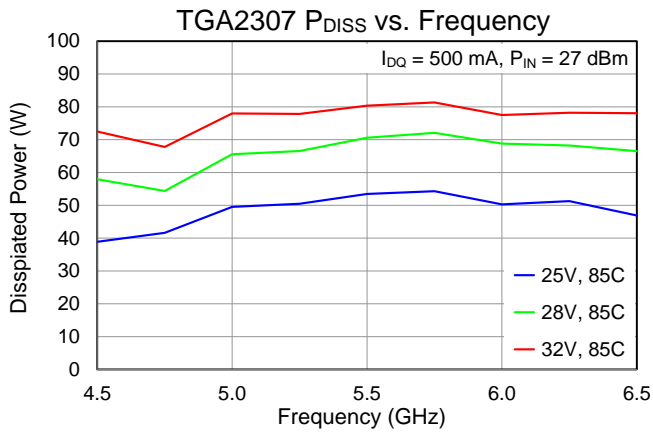
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{base} = 85\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{DQ} = 1.0\text{ A}$, $Freq = 5.75\text{ GHz}$, $I_{D_Drive} = 4.08\text{ A}$, $P_{IN} = 27\text{ dBm}$, $P_{OUT} = 46.6\text{ dBm}$, $P_{DISS} = 65.7\text{ W}$, $PW = 100\text{ }\mu\text{s}$, $DC = 10\%$	0.79	$^{\circ}\text{C/W}$
Channel Temperature, T_{CH} (Under RF)		137	$^{\circ}\text{C}$

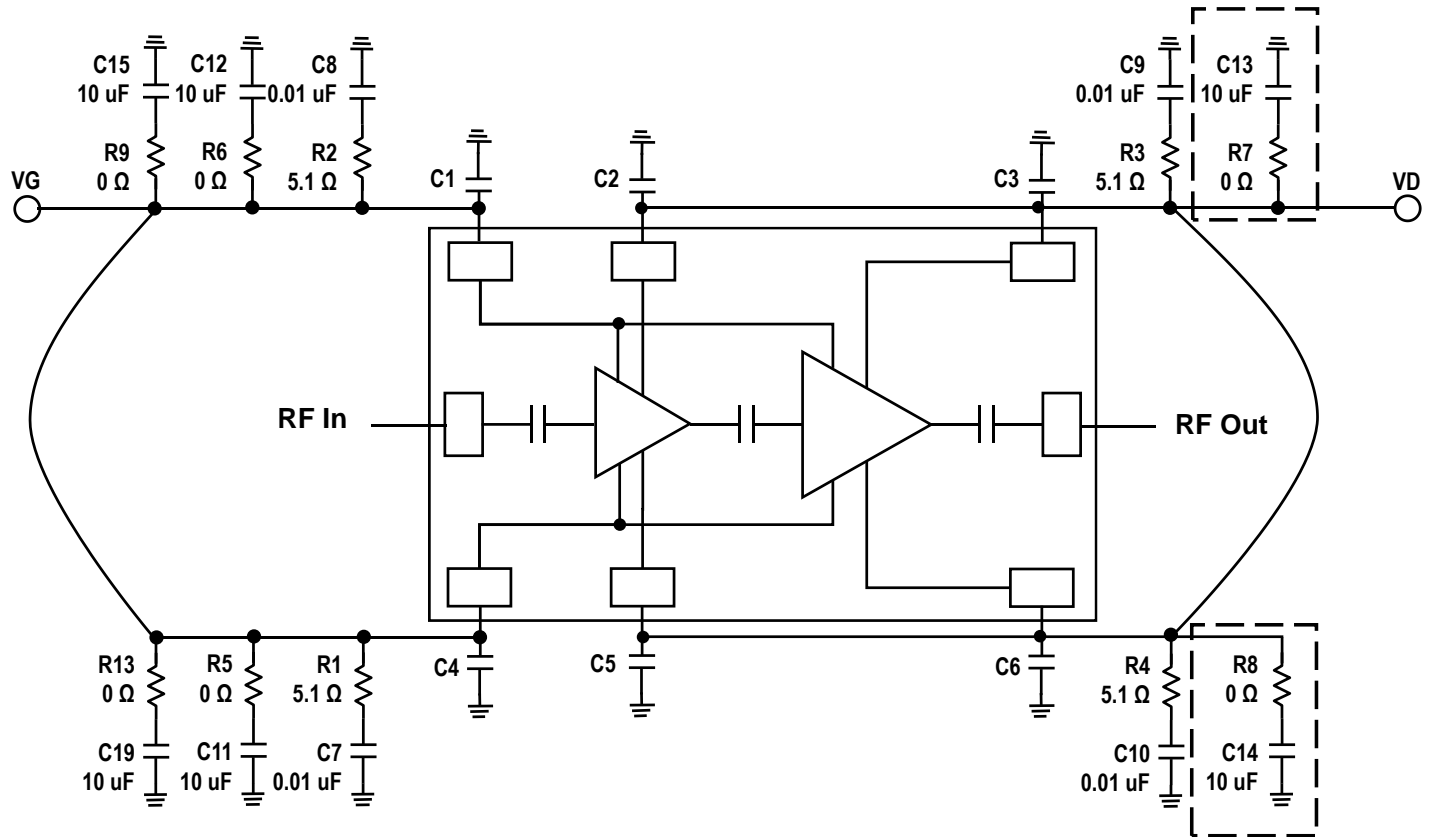
Notes:

1. Die mounted to 20 mil CuMo carrier plate with AuSn solder. Thermal resistance determined to the back of carrier (85 $^{\circ}\text{C}$).
2. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Power Dissipation and Maximum Gate Current



Applications Information and Bias Procedure



Notes:

1. V_G & V_D need to be biased from both sides.
2. R7, R8, C13, C14 should be added if the TGA2307 is to be used with a fixed voltage (non-pulsed) drain bias.

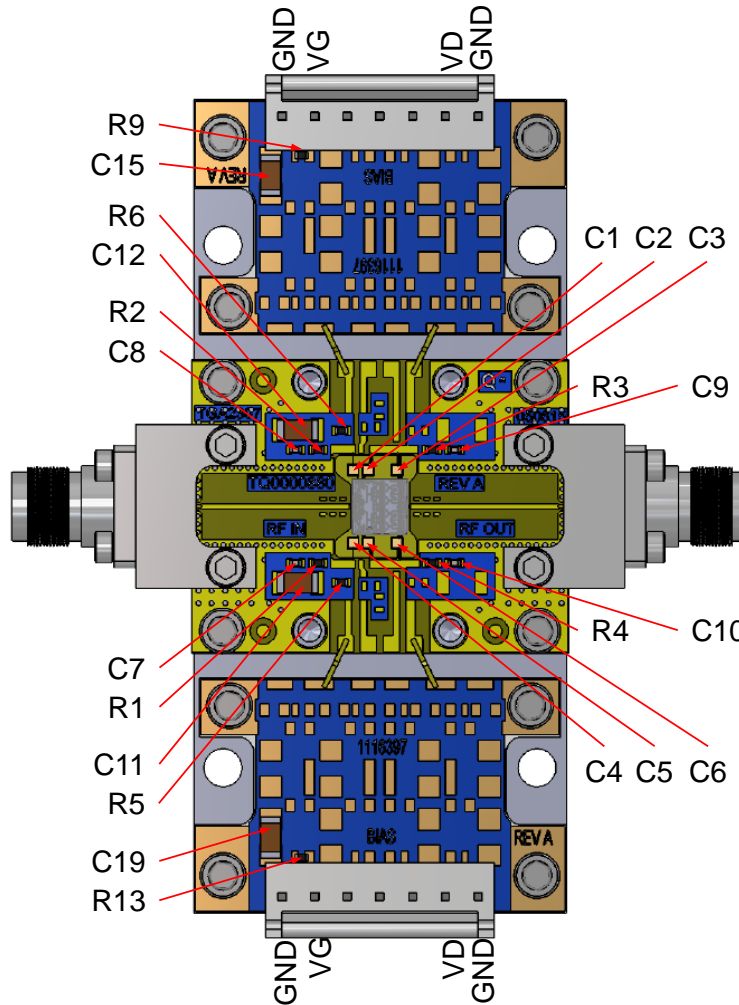
Bias-Up Procedure

1. Set I_D limit (CW) to 5500 mA, I_G limit to 140 mA
2. Set V_G to -5.0 V
4. Set V_D +28 V
5. Adjust V_G more positive until $I_{DQ} \approx 1000$ mA ($V_G \sim -2.8$ V Typical)
6. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0 V. Ensure $I_{DQ} \sim 0$ mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly



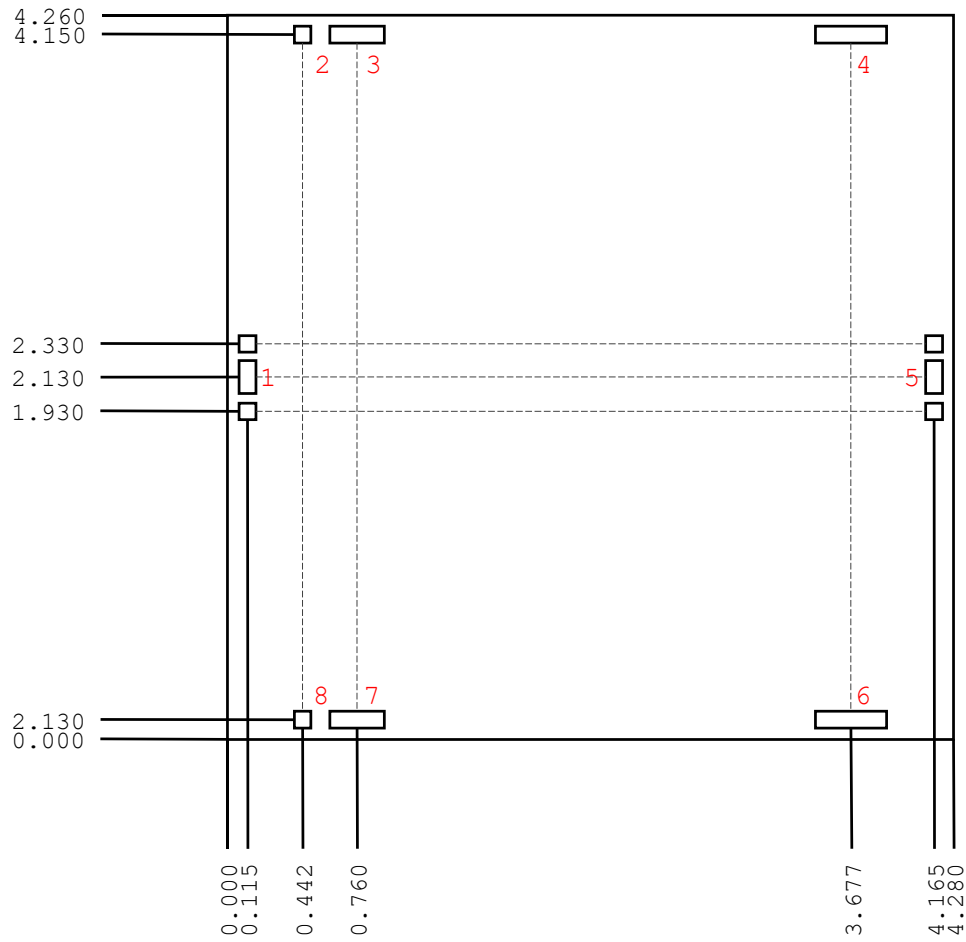
Notes:

- 1. V_G and V_D must be biased from both sides (top and bottom).

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1 – C6	100 pF // 10000 pF	CAP, 10000pF, ±20%, 50V, X7R, 30X30, SL	Presidio	MVB3030X103M2H5C1F
C7 – C10	0.1 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	Various	
C11, C12, C15, C19	10 uF	CAP, CER, 10UF, 25V, 20%, X5R, 1206	Various	
R1 – R4	0 Ohm	RES, 0 OHM, 5%, 0402	Various	
R5, R6, R9, R13	5.1 Ohm	RESISTOR, 5.1 OHM, 5%, 0402, SMD	Various	

Mechanical Information and Bond Pad Description



Units: millimeters
Thickness: 0.100
Die x,y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF IN	100 x 200	RF Input; matched to 50 Ω , DC blocked
2, 8	V _G	100 x 100	Gate voltage for stage 1. Bias network is required; see Application Circuit on page 12 as an example.
3, 7	V _{D1}	318 x 100	Drain voltage for stage 1. Bias network is required; see Application Circuit on page 12 as an example.
4, 6	V _{D2}	418 x 100	Drain voltage for stage 2. Bias network is required; see Application Circuit on page 12 as an example.
5	RF OUT	100 x 200	RF Output; matched to 50 Ω , DC blocked

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3–4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	ANSI/ESDA/JEDEC JS-001



Caution!
ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3–4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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