20 GHz to 54 GHz, GaAs, pHEMT, MMIC, 29 dBm (0.5 W) Power Amplifier

Data Sheet

ADPA7009CHIP

FEATURES

- **Output P1dB: 28.5 dBm typical at 24 GHz to 36 GHz**
- **P_{SAT}: 29 dBm typical at 24 GHz to 36 GHz**
- **Gain: 19.5 dB typical at 24 GHz to 36 GHz**
- **Input return loss: 17.5 dB typical at 24 GHz to 36 GHz**
- **Output return loss: 22.0 dB typical at 24 GHz to 36 GHz**
- **Output IP3: 35 dBm typical at 24 GHz to 36 GHz**
- **Supply voltage: 5 V typical at 750 mA**
- **50 Ω matched input and output**
- **Die size: 2.750 mm × 1.845 mm× 0.102 mm**

APPLICATIONS

- **Military and space**
- **Test instrumentation**
- **Satellite communications**

FUNCTIONAL BLOCK DIAGRAM

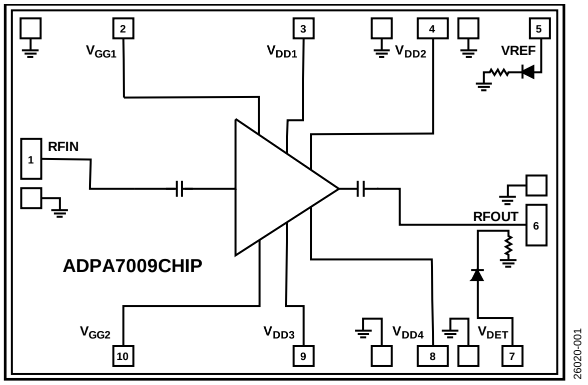

Figure 1.

GENERAL DESCRIPTION

The ADPA7009CHIP is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), 29 dBm saturated output power (0.5 W) distributed power amplifier that operates from 20 GHz to 54 GHz. The amplifier provides a gain of 19.5 dB, an output power for 1 dB compression (P1dB) of 28.5 dBm, and a typical output third-order intercept (IP3) of 35 dBm at 24 GHz to 36 GHz. The ADPA7009CHIP requires 750 mA from a 5 V supply voltage (V_{DD}) and features inputs and outputs that are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the RFIN and RFOUT pads connected via one 0.076 mm (3 mil) ribbon bond of 0.076 mm (3 mil) minimal length.

Rev. 0

Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

3/2021—Revision 0: Initial Version

SPECIFICATIONS

20 GHz TO 24 GHz FREQUENCY RANGE

T_A = 25°C, supply voltage (V_{DD}) = 5 V, I_{DQ} = 750 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust the gate voltage (V_{GGx}) from −1.5 V to 0 V to achieve I_{DQ} = 750 mA typical.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		24	GHz	
GAIN		14.5	17		dB	
Gain Flatness			±1.2		dB	
Gain Variation Over Temperature			0.033		dB/°C	
NOISE FIGURE			6.5		dB	
RETURN LOSS						
Input			15.0		dB	
Output			20.0		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	25	27.5		dBm	
Saturated Output Power	P_{SAT}		28.5		dBm	
Output Third-Order Intercept	IP3		32		dBm	Output power (P_{OUT}) per tone = 14 dBm with 1 MHz tone spacing
SUPPLY						
Quiescent Current	I_{DQ}		750		mA	Adjust V_{GGx} to achieve I_{DQ} = 750 mA typical
Voltage	V_{DD}	3	5		V	

24 GHz TO 36 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 750 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GGx} from −1.5 V to 0 V to achieve I_{DQ} = 750 mA typical.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		24		36	GHz	
GAIN		17.0	19.5		dB	
Gain Flatness			±1.1		dB	
Gain Variation Over Temperature			0.023		dB/°C	
NOISE FIGURE			5.5		dB	
RETURN LOSS						
Input			17.5		dB	
Output			22.0		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	26	28.5		dBm	
Saturated Output Power	P_{SAT}		29		dBm	
Output Third-Order Intercept	IP3		35		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
SUPPLY						
Quiescent Current	I_{DQ}		750		mA	Adjust V_{GGx} to achieve I_{DQ} = 750 mA typical
Voltage	V_{DD}	3	5		V	

36 GHz TO 50 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 750 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GGx} from −1.5 V to 0 V to achieve I_{DQ} = 750 mA typical.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		36		50	GHz	
GAIN		17.5	20.0		dB	
Gain Flatness			±1.1		dB	
Gain Variation Over Temperature			0.026		dB/°C	
NOISE FIGURE			6.0		dB	
RETURN LOSS						
Input			20		dB	
Output			20		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	22	25		dBm	
Saturated Output Power	P_{SAT}		27.0		dBm	
Output Third-Order Intercept	IP3		34.5		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
SUPPLY						
Quiescent Current	I_{DQ}		750		mA	Adjust V_{GGx} to achieve I_{DQ} = 750 mA typical
Voltage	V_{DD}	3	5		V	

50 GHz TO 54 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 750 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GGx} from −1.5 V to 0 V to achieve I_{DQ} = 750 mA typical.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		50		54	GHz	
GAIN			20.5		dB	
Gain Flatness			±0.85		dB	
Gain Variation Over Temperature			0.027		dB/°C	
NOISE FIGURE			6.0		dB	
RETURN LOSS						
Input			16.5		dB	
Output			20.0		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		24.0		dBm	
Saturated Output Power	P_{SAT}		26.0		dBm	
Output Third-Order Intercept	IP3		33		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
SUPPLY						
Quiescent Current	I_{DQ}		750		mA	Adjust V_{GGx} to achieve I_{DQ} = 750 mA typical
Voltage	V_{DD}	3	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DDx})	6.0 V
V_{GGx}	−1.6 V to 0 V
RF Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 85 mW/°C Above 85°C)	7.7 W
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T_J = 85°C, V_{DD} = 5 V, I_{DQ} = 750 mA)	129°C
Temperature Range	
Storage	−65°C to +150°C
Operating	−55°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the carrier or substrate on which the die is mounted. Careful attention is needed with each material used in the thermal path below the IC.

θ_{JC} is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
C-10-13	11.7	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA7009CHIP

Table 7. ADPA7009CHIP, 10-Pad Die

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

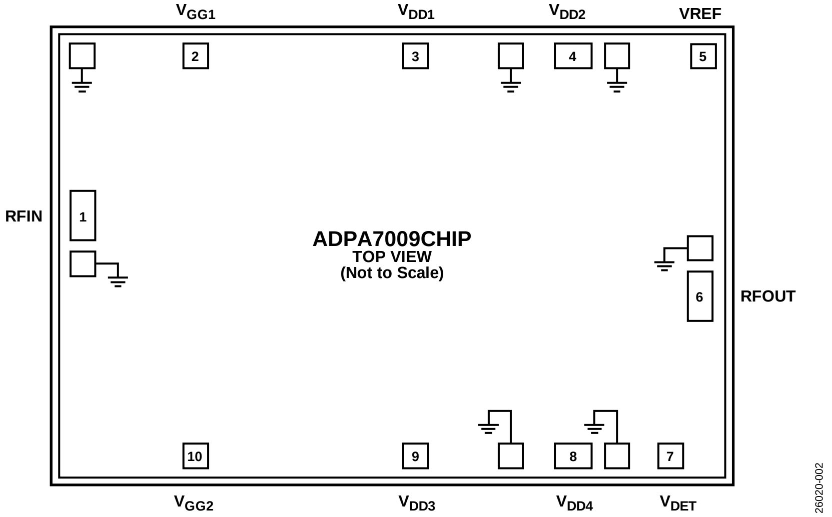


Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Signal Input. This pad is ac-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
2, 10	V_{GG1}, V_{GG2}	Amplifier Gate Controls. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required for these pads. Adjust V_{GGx} from −1.5 V to 0 V to achieve the desired quiescent current. See Figure 7 for the interface schematic.
3, 4, 8, 9	V_{DD1}, V_{DD2}, V_{DD4}, V_{DD3}	Drain Biases for the Amplifier. External bypass capacitors of 4.7 µF, 0.01 µF, and 100 pF are required for these pads. See Figure 9 for the interface schematic.
5	VREF	Reference Diode Voltage. Use this pad for temperature compensation of the VDET RF output power measurements. Used in combination with VDET, this voltage provides temperature compensation to the VDET RF output power measurements. See Figure 4 for the interface schematic.
6	RFOUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω. See Figure 8 for the interface schematic.
7	VDET	Detector Diode Used for Measuring the RF Output Power. Detection via this pad requires the application of a dc bias voltage through an external series resistor. Used in combination with VREF, the difference detector voltage, VREF − VDET, is a temperature compensated dc voltage proportional to the RF output power. See Figure 5 for the interface schematic.
Die Bottom	GND	Ground. The die bottom must be connected to RF and dc ground. See Figure 3 for the interface schematic.

INTERFACE SCHEMATICS

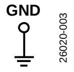


Figure 3. GND Interface Schematic

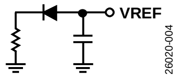


Figure 4. VREF Interface Schematic

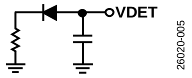


Figure 5. VDET Interface Schematic

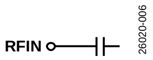


Figure 6. RFIN Interface Schematic

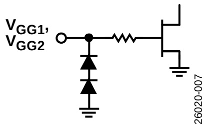


Figure 7. V_{GG1}, V_{GG2} Interface Schematic

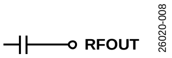


Figure 8. RFOUT Interface Schematic

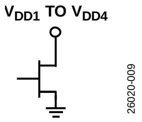


Figure 9. V_{DD1} to V_{DD4} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

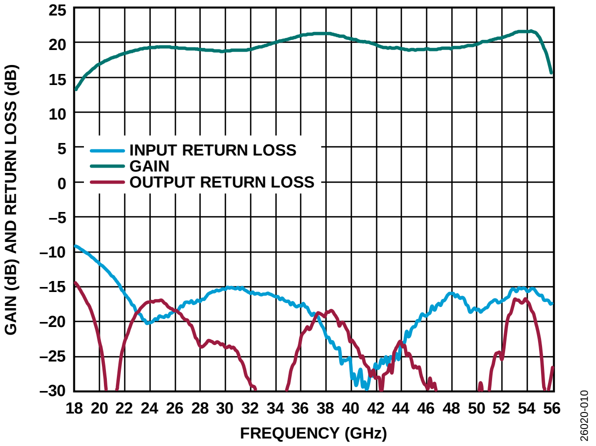


Figure 10. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 750 mA

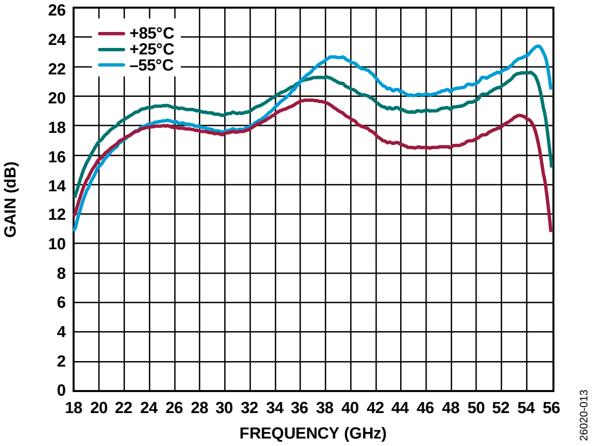


Figure 13. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA

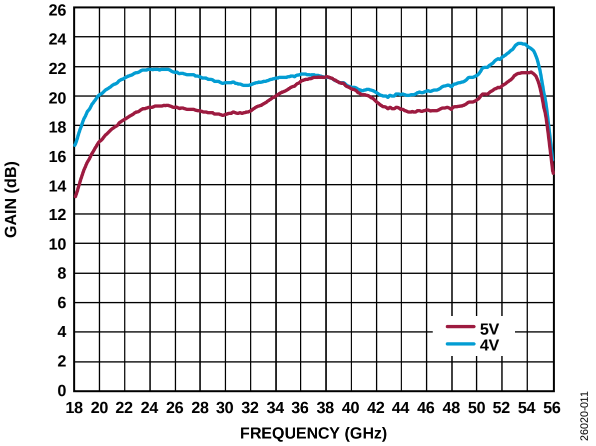


Figure 11. Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA

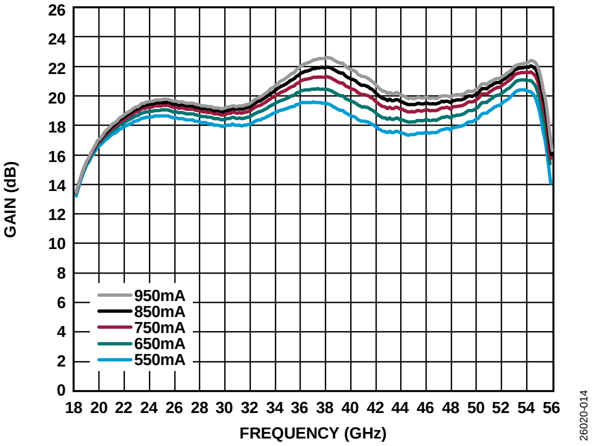


Figure 14. Gain vs. Frequency for Various I_{DQ} Currents, V_{DD} = 5 V

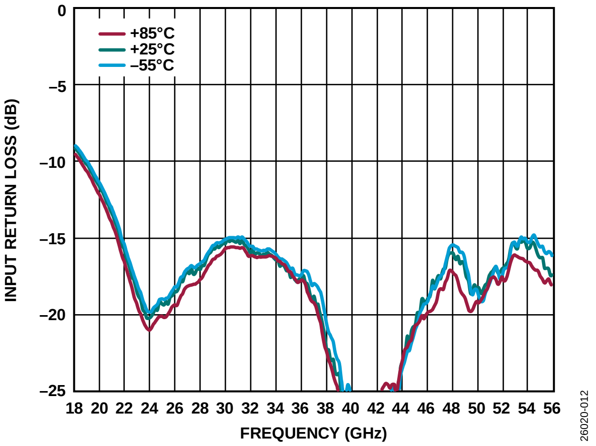


Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA

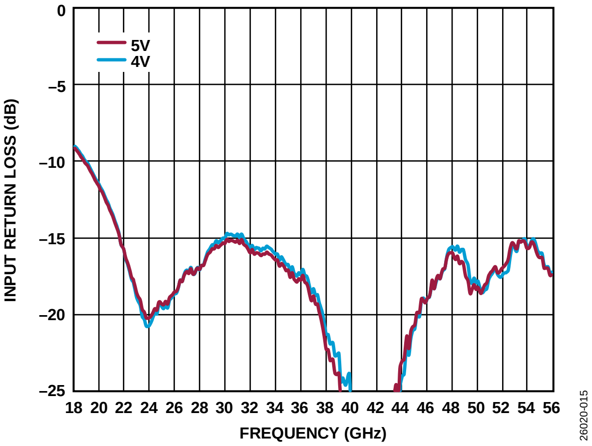


Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA

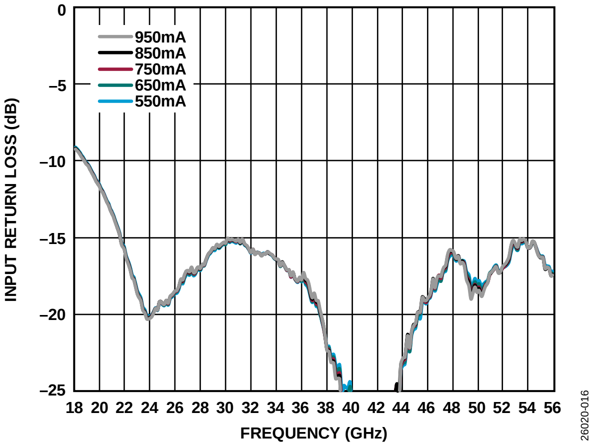


Figure 16. Input Return Loss vs. Frequency for Various I_{DQ} Currents, V_{DD} = 5 V

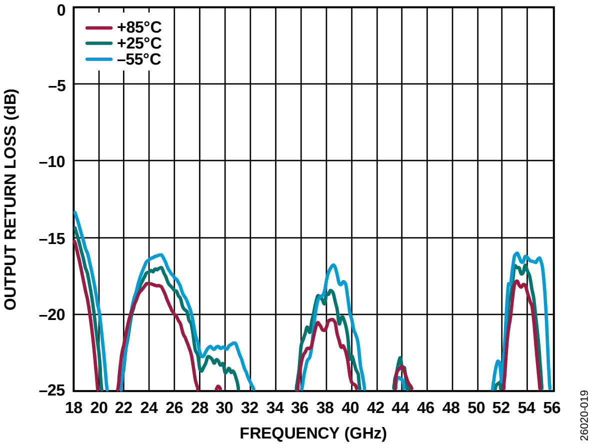


Figure 19. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA

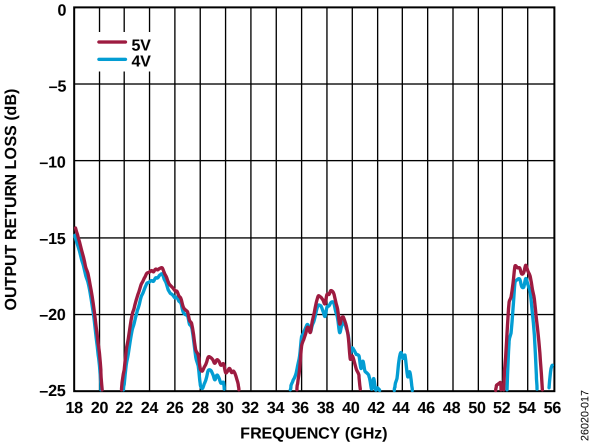


Figure 17. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA

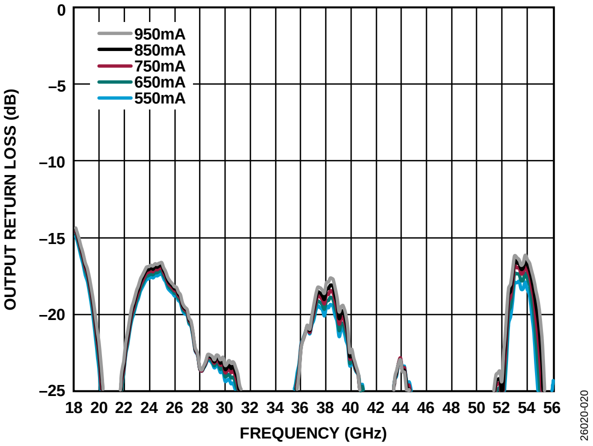


Figure 20. Output Return Loss vs. Frequency for Various I_{DQ} Currents, V_{DD} = 5 V

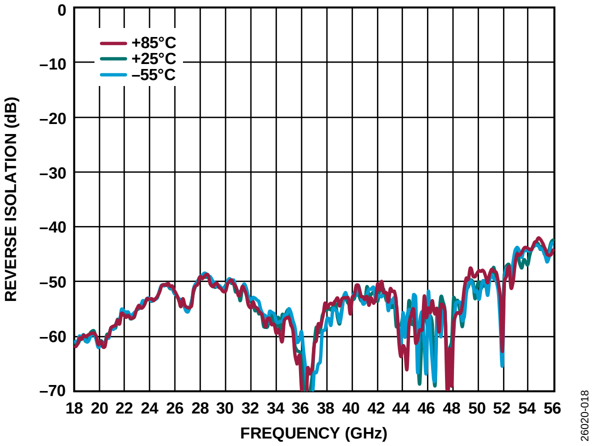


Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA

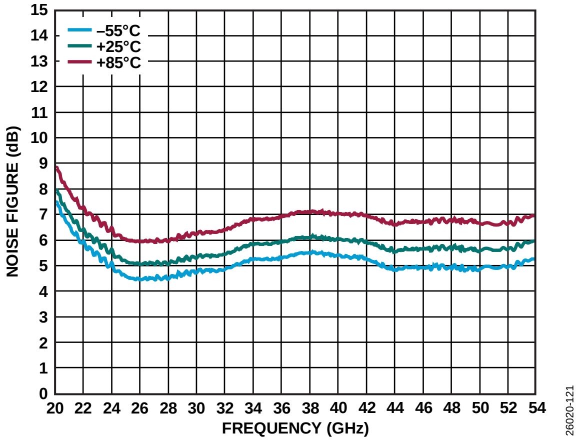


Figure 21. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA

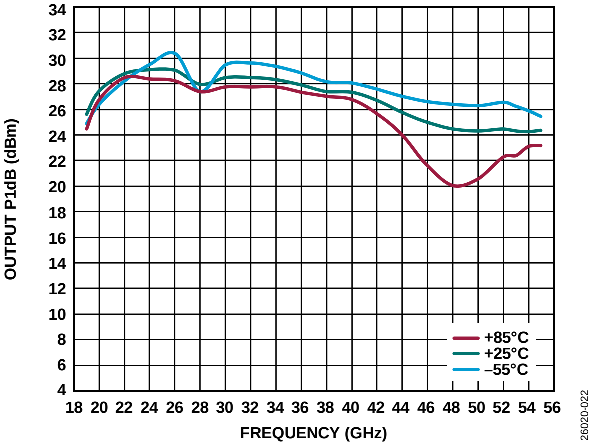


Figure 22. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA

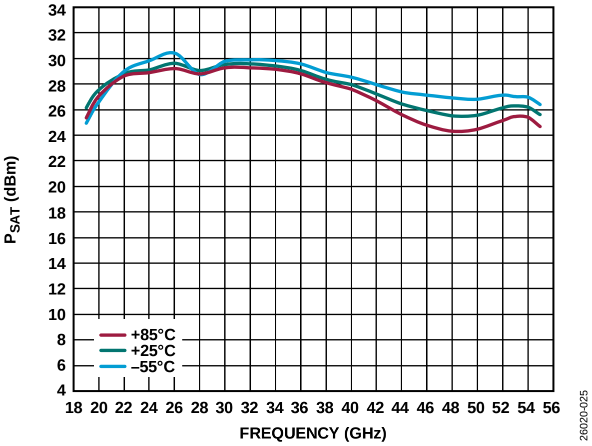


Figure 25. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA

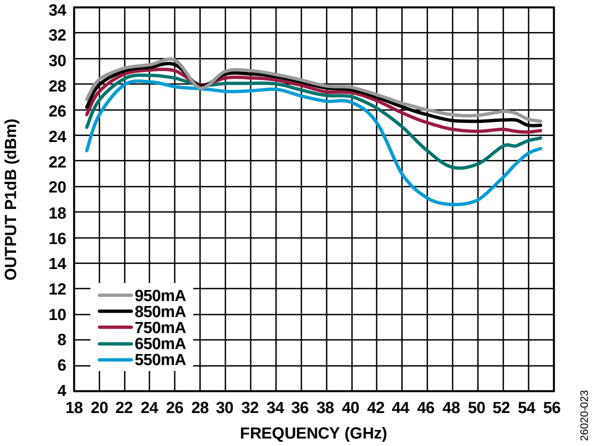


Figure 23. Output P1dB vs. Frequency for Various I_{DQ} Currents, V_{DD} = 5 V

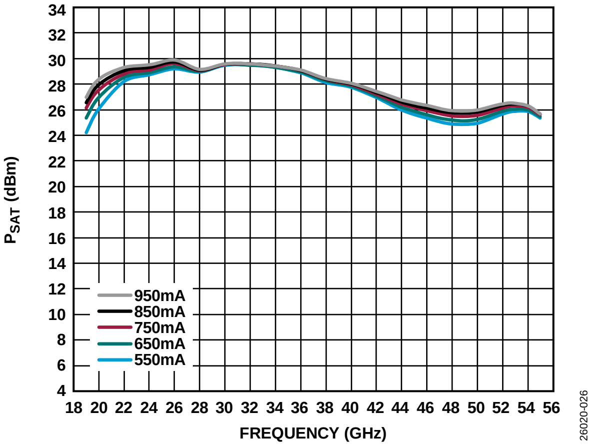


Figure 26. P_{SAT} vs. Frequency for Various I_{DQ} Currents, V_{DD} = 5 V

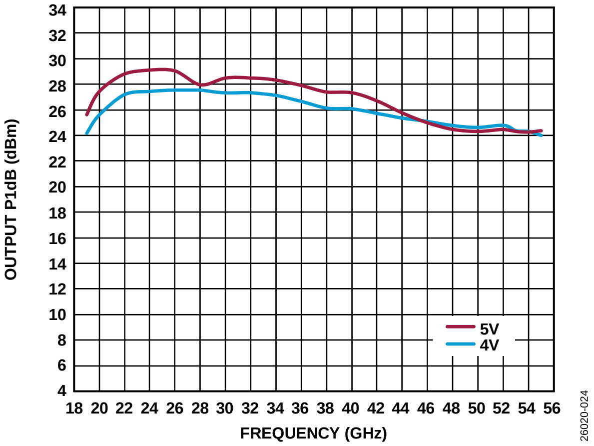


Figure 24. Output P1dB vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA

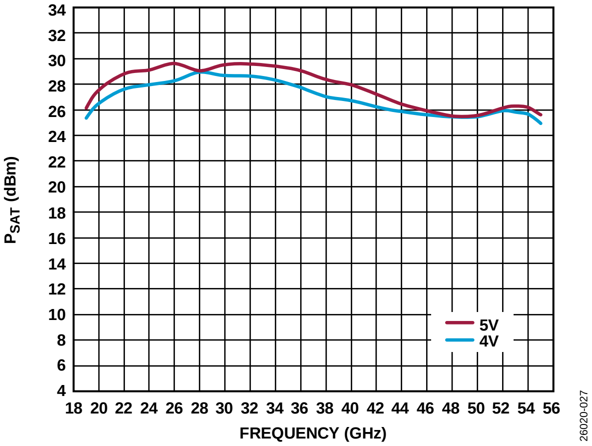


Figure 27. P_{SAT} vs. Frequency for Various Voltages, I_{DQ} = 750 mA

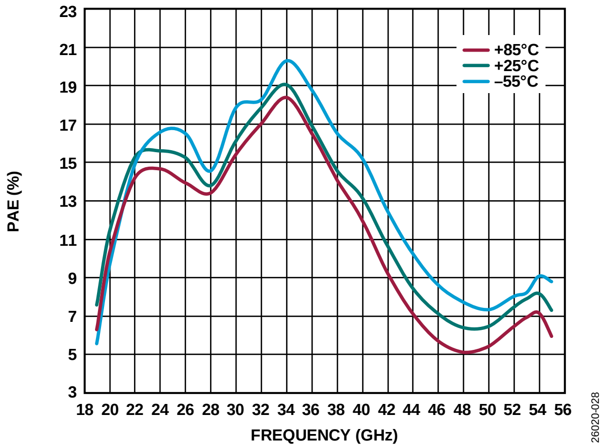


Figure 28. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 750 mA, PAE at P_{SAT} (dBm)

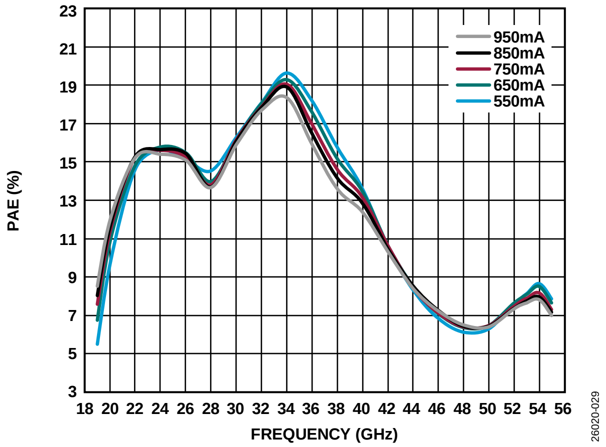


Figure 29. PAE vs. Frequency for Various I_{DQ} Currents, V_{DD} = 5 V, PAE at P_{SAT} (dBm)

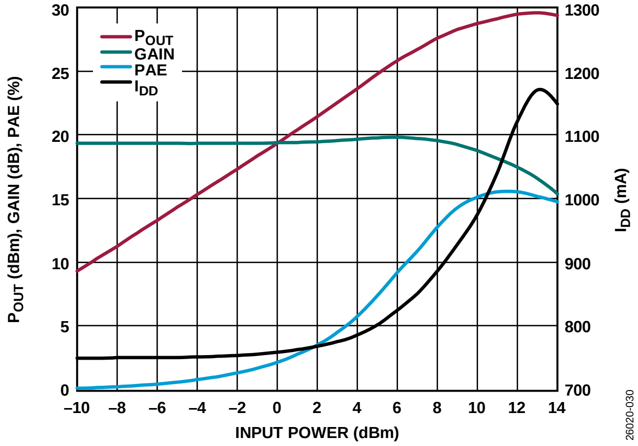


Figure 30. P_{OUT}, Gain, PAE, and Drain Current with RF Applied (I_{DD}) vs. Input Power, 26 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

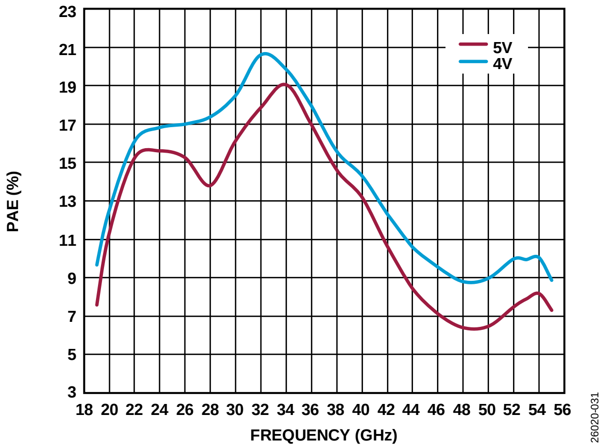


Figure 31. PAE vs. Frequency for Various Supply Voltages, I_{DQ} = 750 mA, PAE at P_{SAT} (dBm)

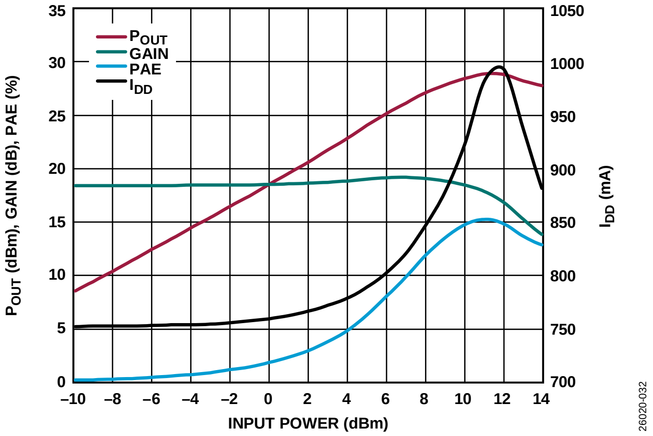


Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 22 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

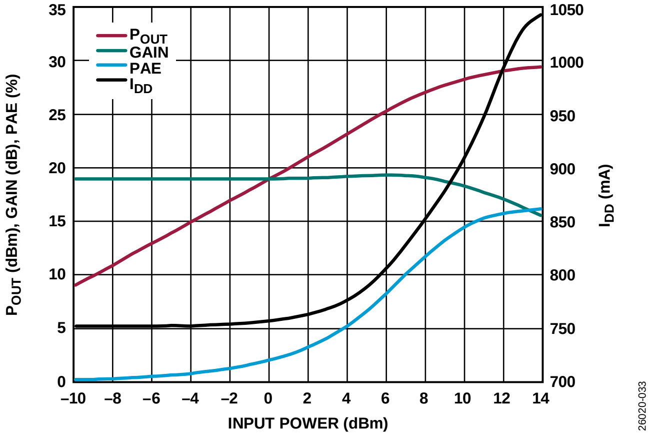


Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 30 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

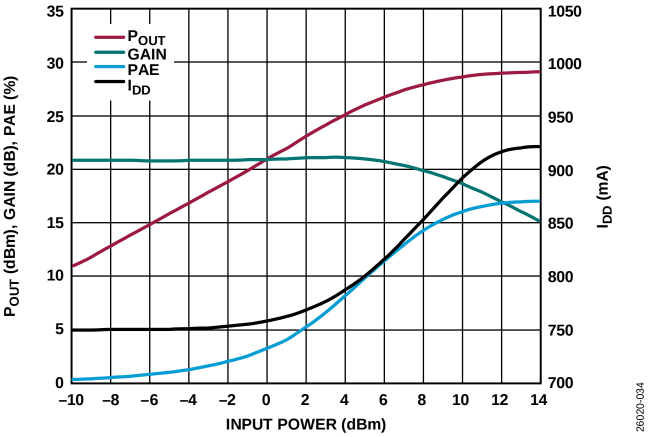


Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 36 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

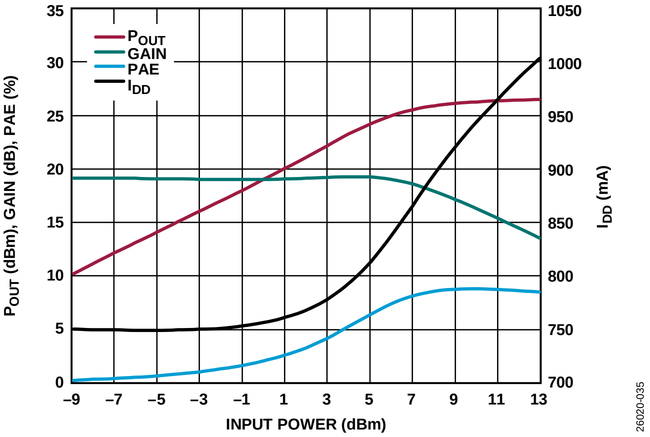


Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 44 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

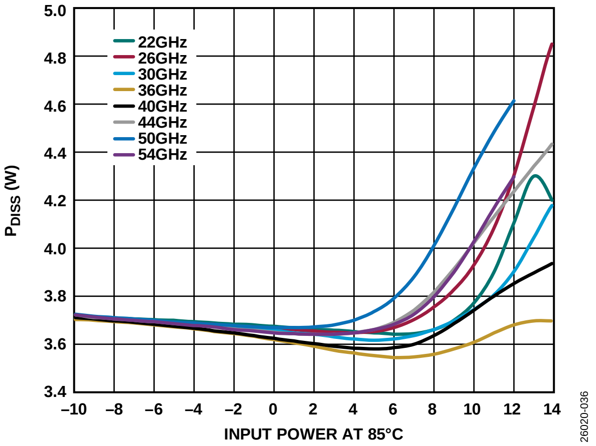


Figure 36. P_{DISS} vs. Input Power for Various Frequencies at T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 750 mA

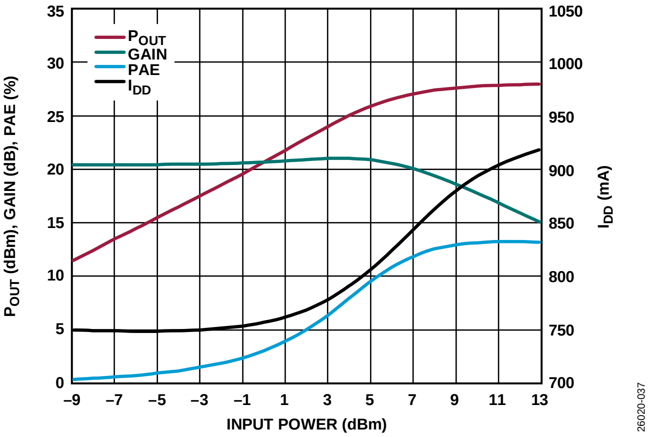


Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 40 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

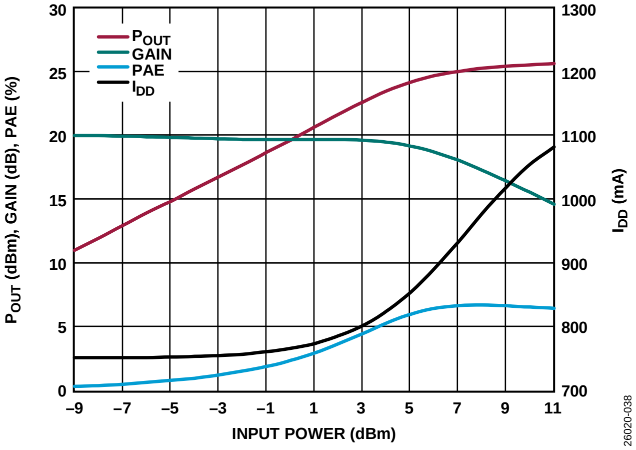


Figure 38. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 50 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

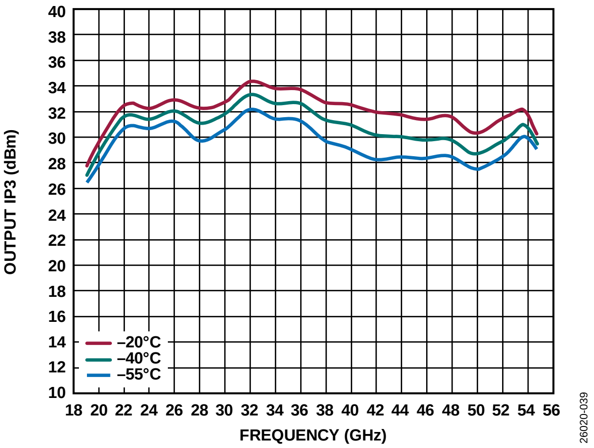


Figure 39. Output IP3 vs. Frequency at −20°C, −40°C, and −55°C, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 750 mA

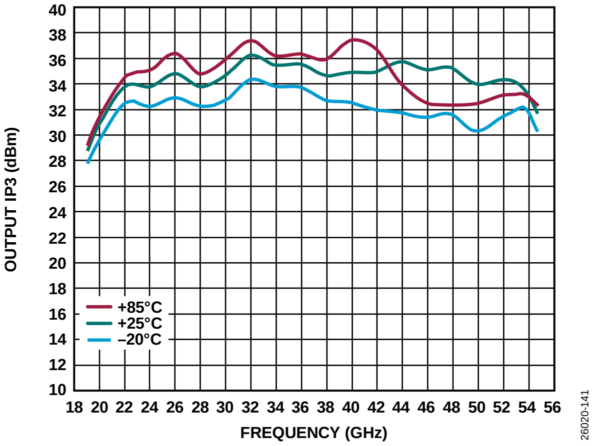


Figure 40. Output IP3 vs. Frequency at +25°C, +85°C and −20°C, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 750 mA

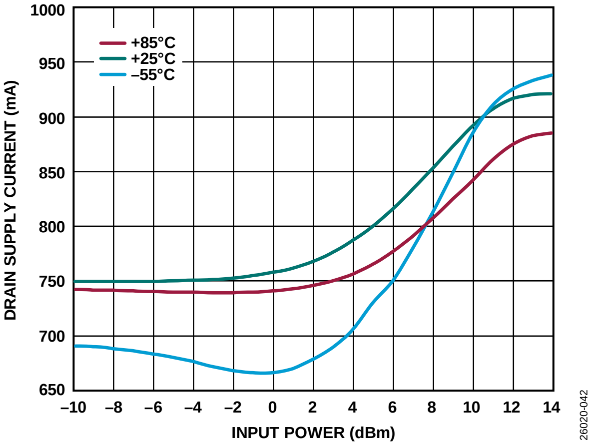


Figure 43. Drain Supply Current vs. Input Power at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 750 mA

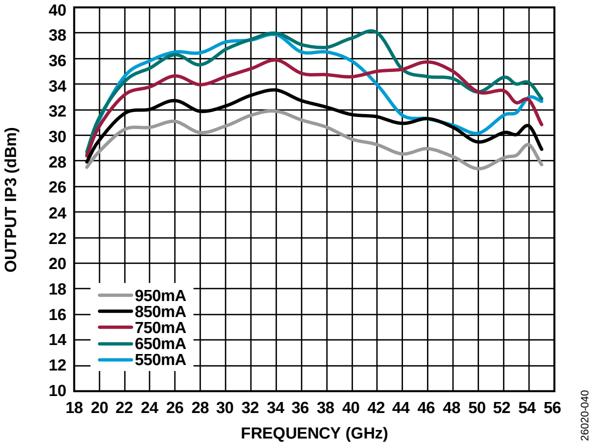


Figure 41. Output IP3 vs. Frequency for Various I_{DQ} Currents, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V

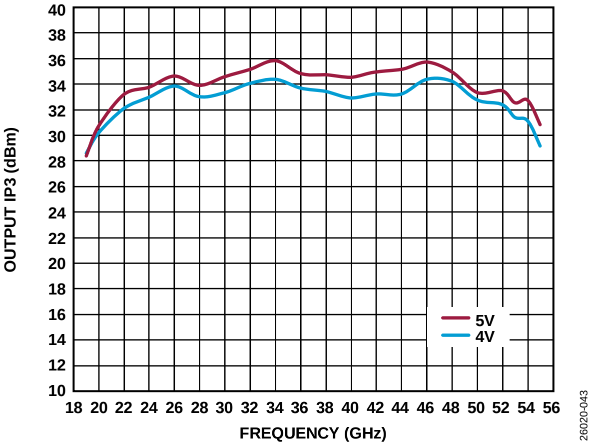


Figure 44. Output IP3 vs. Frequency for Various Supply Voltages, P_{OUT} per Tone = 14 dBm, I_{DQ} = 750 mA

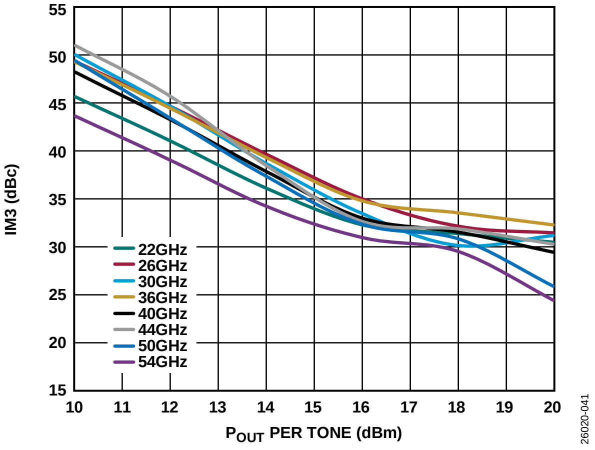


Figure 42. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone, V_{DD} = 4 V, I_{DQ} = 750 mA

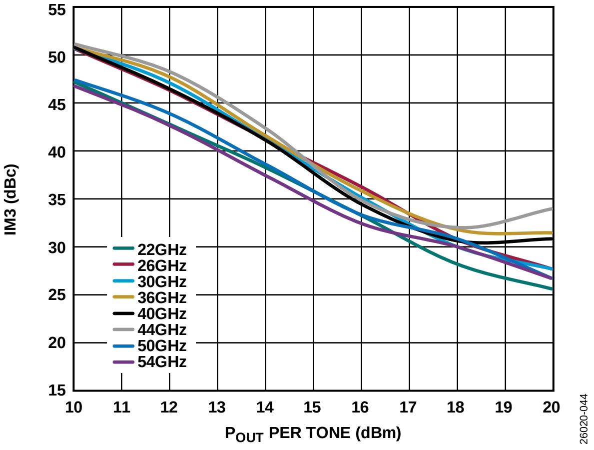


Figure 45. IM3 vs. P_{OUT} per Tone, V_{DD} = 5 V, I_{DQ} = 750 mA

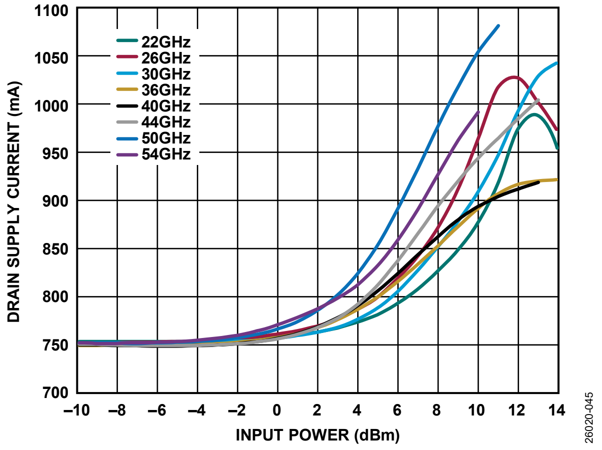


Figure 46. Drain Supply Current vs. Input Power at Various Temperature, 36 GHz, V_{DD} = 5 V, I_{DQ} = 750 mA

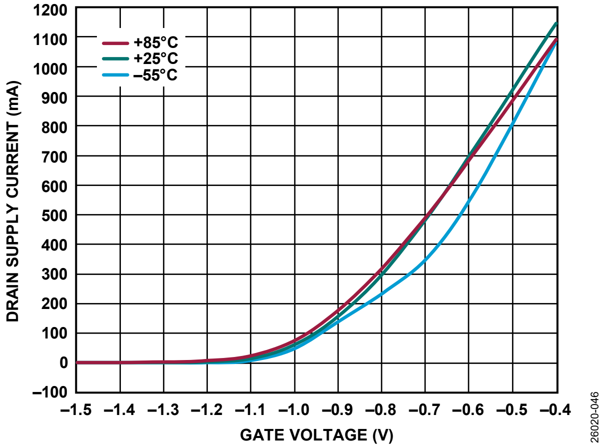


Figure 47. Drain Supply Current vs. Gate Voltage at Various Temperature

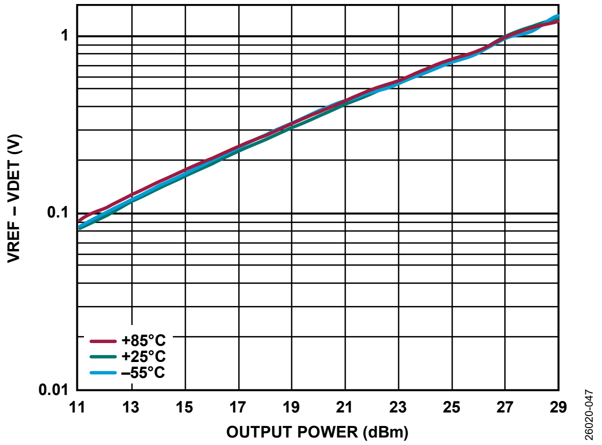


Figure 48. Detector Voltage (VREF – VDET) vs. Output Power for Various Temperatures at 36 GHz

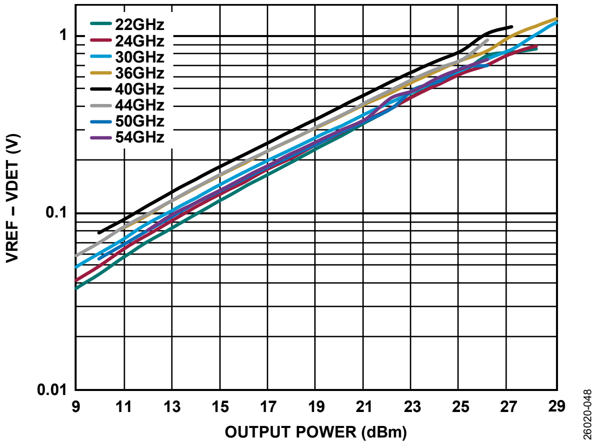


Figure 49. Detector Voltage (VREF – VDET) vs. Output Power for Various Frequencies

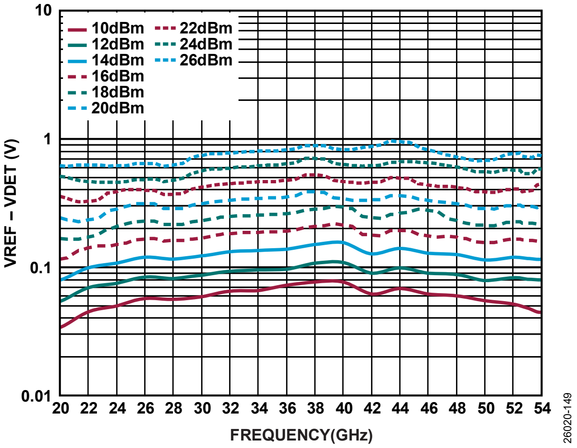


Figure 50. Detector Voltage (VREF – VDET) vs. Frequency for Various Output Powers

LOWER BIAS OPERATION

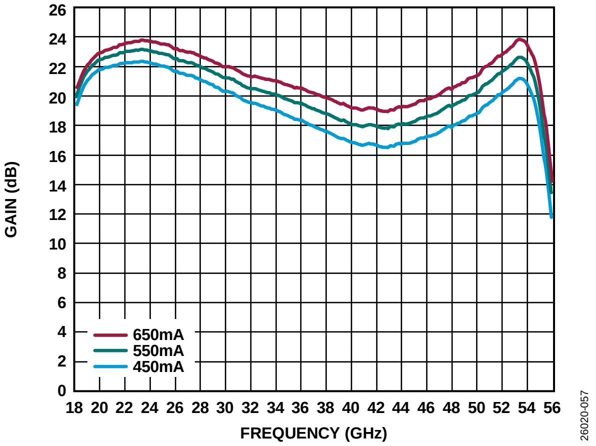


Figure 51. Gain vs. Frequency for Various I_{DQ} Currents, V_{DD} = 3 V

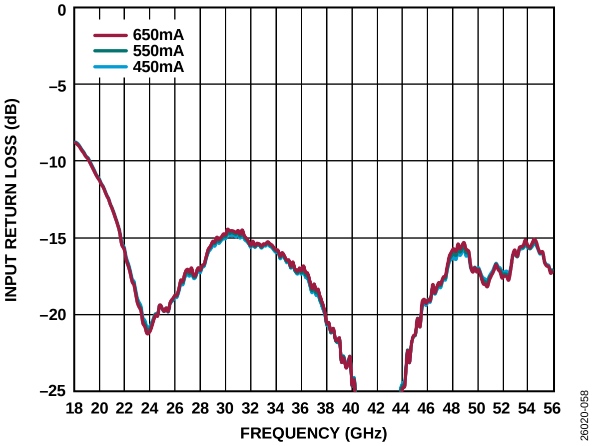


Figure 52. Input Return Loss vs. Frequency for Various I_{DQ} Currents, V_{DD} = 3 V

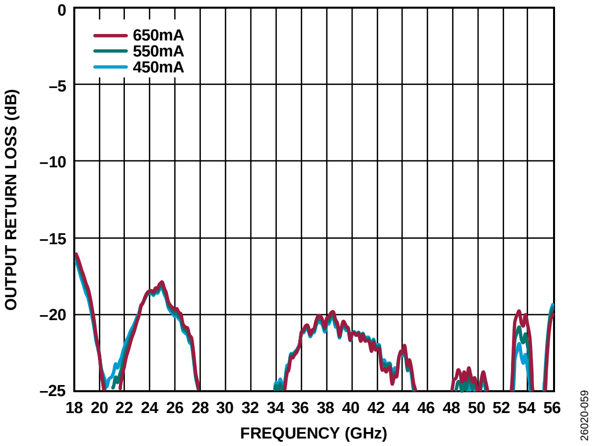


Figure 53. Output Return Loss vs. Frequency for Various I_{DQ} Currents, V_{DD} = 3 V

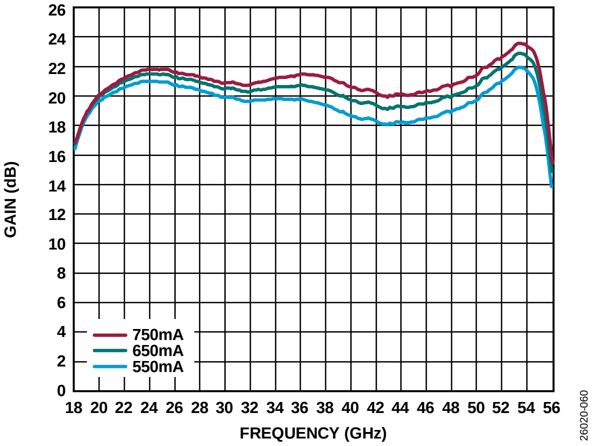


Figure 54. Gain vs. Frequency for Various I_{DQ} Currents, V_{DD} = 4 V

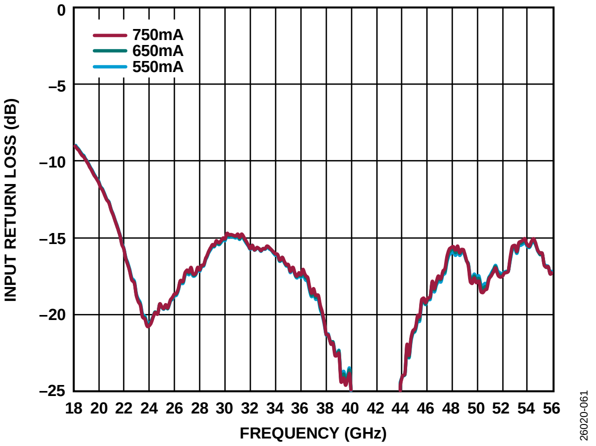


Figure 55. Input Return Loss vs. Frequency for Various I_{DQ} Currents, V_{DD} = 4 V

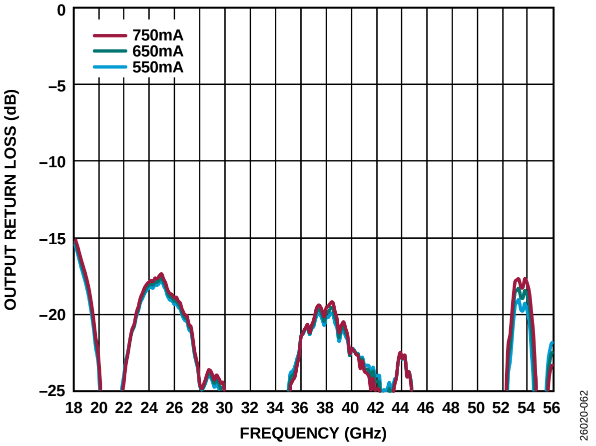


Figure 56. Output Return Loss vs. Frequency for Various I_{DQ} Currents, V_{DD} = 4 V

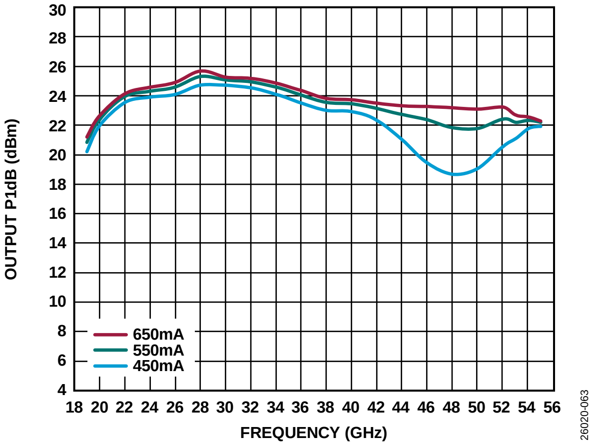


Figure 57. Output P1dB vs. Frequency for Various I_{DQ} Currents, V_{DD} = 3 V

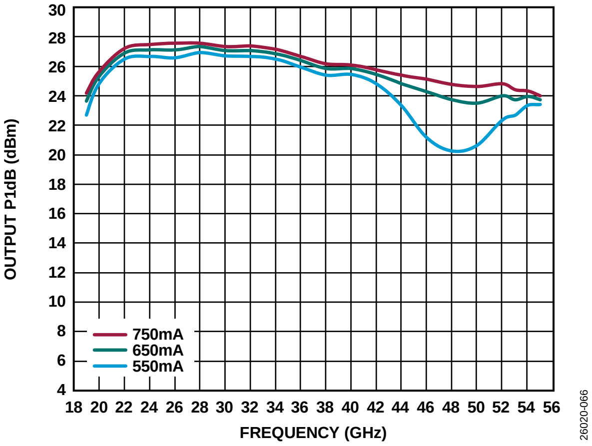


Figure 60. Output P1dB vs. Frequency for Various I_{DQ} Currents, V_{DD} = 4 V

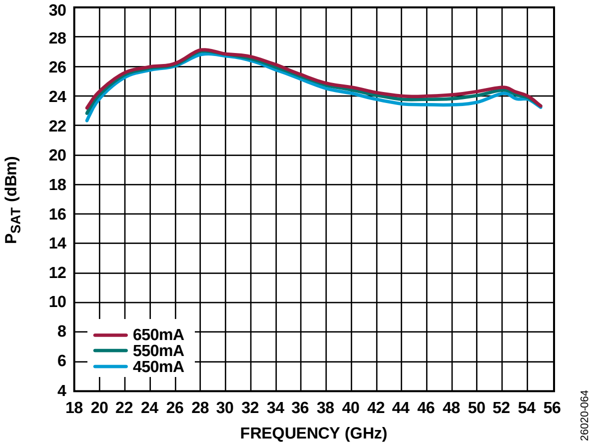


Figure 58. P_{SAT} vs. Frequency for Various I_{DQ} Currents, V_{DD} = 3 V

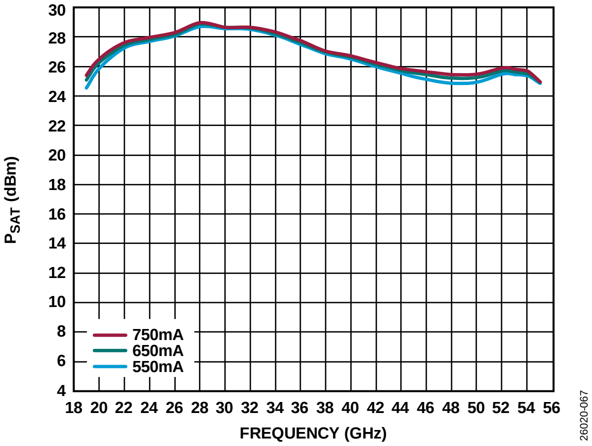


Figure 61. P_{SAT} vs. Frequency for Various I_{DQ} Currents, V_{DD} = 4 V

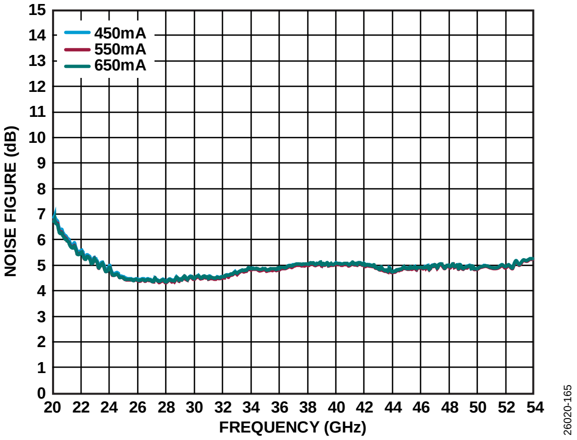


Figure 59. Noise Figure vs. Frequency for Various I_{DQ} Currents, V_{DD} = 3 V

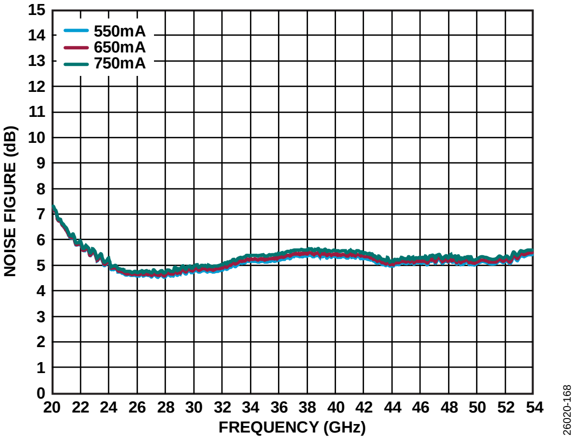


Figure 62. Noise Figure vs. Frequency for Various I_{DQ} Currents, V_{DD} = 4 V

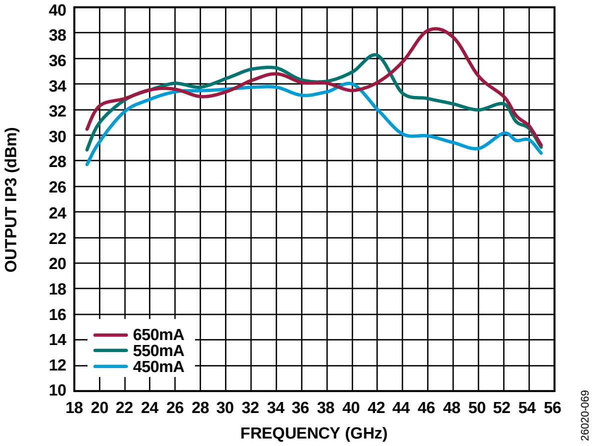


Figure 63. Output IP3 vs. Frequency for Various I_{DQ} Currents, P_{OUT} per Tone = 14 dBm, V_{DD} = 3 V

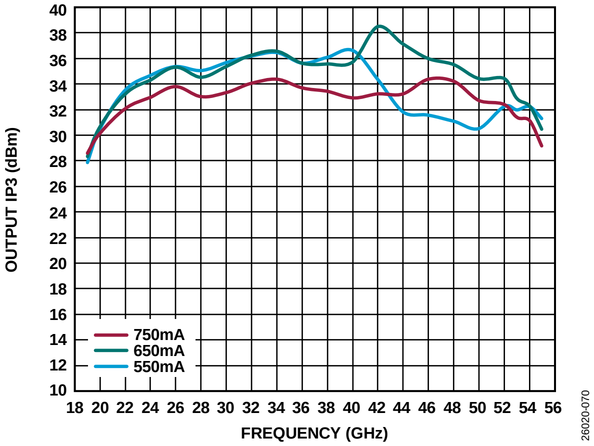


Figure 64. Output IP3 vs. Frequency for Various I_{DQ} Currents, P_{OUT} per Tone = 14 dBm, V_{DD} = 4 V

THEORY OF OPERATION

The architecture of the ADPA7009CHIP, a medium power amplifier, is shown in Figure 65. The ADPA7009CHIP uses a cascaded, four-stage amplifier operating in quadrature between two 90° hybrids.

The input signal is divided evenly in two. Each path is amplified through four independent gain stages. The amplified signals are then combined at the output. This balanced amplifier approach forms an amplifier with a combined gain of 19.5 dB and a P_{SAT} value of 29 dBm. The gate pins are internally connected and can be biased from either north or south of the circuit.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output (see Figure 65).

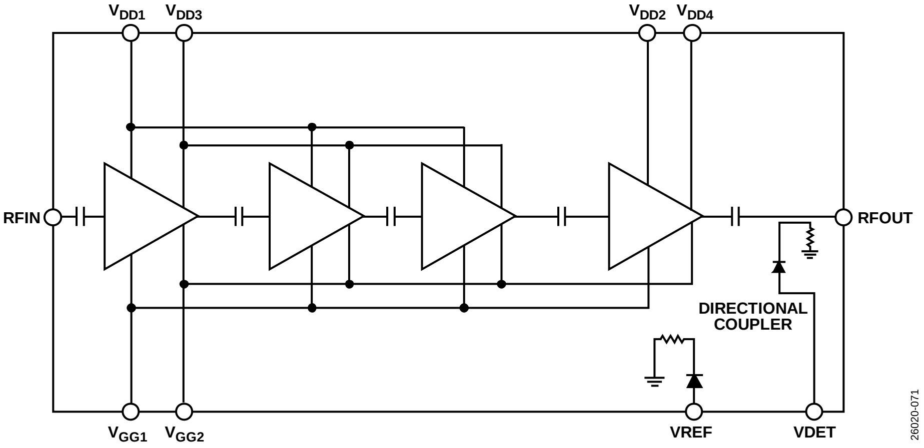


Figure 65. ADPA7009CHIP Architecture

APPLICATIONS INFORMATION

The ADPA7009CHIP is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for all primary and alternate V_{GGx} and V_{DDx} pads. V_{GG1} and V_{GG2} are the gate bias pads for the amplifier. V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4} are the drain bias pads for the amplifier.

All measurements for this device were taken using the primary application circuit (see Figure 66) and were configured as shown in the assembly diagram (see Figure 79).

The recommended bias sequence during power-up is as follows:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, V_{GG1} and V_{GG2}, to −1.5 V.
3. Set all the drain bias voltages, V_{DDx}, to 5 V.
4. Increase the gate bias voltages, V_{GG1} and V_{GG2}, to achieve an I_{DQ} of 750 mA.
5. Apply the RF signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the primary gate bias voltages, V_{GG1} and V_{GG2}, to −1.5 V to achieve I_{DQ} = 0 mA (approximately).
3. Decrease all the drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

The V_{DD} = 5 V and I_{DQ} = 750 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the ADPA7009CHIP at different bias conditions may provide performance that differs from what is shown in Table 1 to Table 4. Biasing the ADPA7009CHIP for higher drain current typically results in higher P1dB and gain at the expense of increased power consumption (see Table 9).

TYPICAL APPLICATION CIRCUIT

Figure 66 shows the primary application circuit. Figure 67 shows the alternate typical application circuit.

Table 9. Power Selection Table[1, 2]

I_{DQ} (mA)	Gain (dB)	P1dB (dBm)	Output IP3 (dBm)	P_{DISS} (W) at P_{SAT}	V_{GGx} (V)
650	20.33	27.57	37.07	3.25	−0.68
750	21.02	27.93	34.83	3.75	−0.63
850	21.52	28.17	32.69	4.25	−0.59
950	22.02	28.34	31.19	4.75	−0.54

[1] Data taken at the following nominal bias conditions: V_{DD} = 5 V, T_A = 25°C, and frequency = 36 GHz.
[2] Adjust V_{GGx} from −1.5 V to 0 V to achieve the desired drain current.

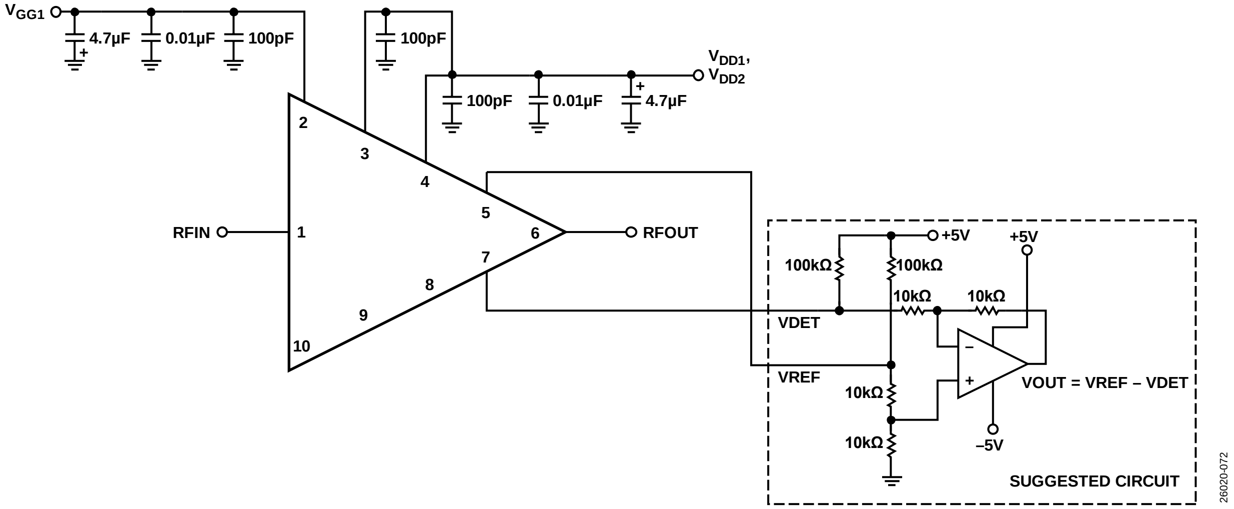


Figure 66. Primary Application Circuit

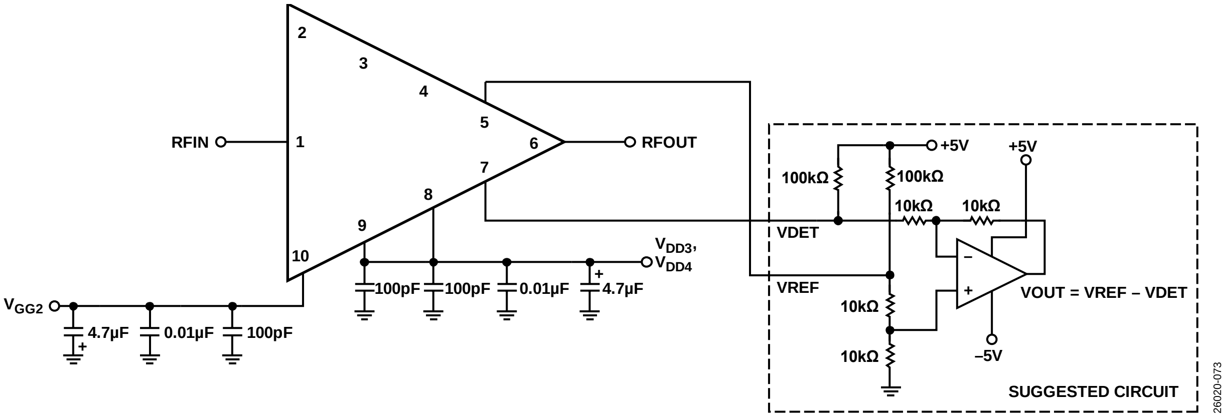


Figure 67. Alternate Application Circuit

BIASING THE ADPA7009CHIP WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirements for enhancement mode and depletion mode amplifiers such as the ADPA7009CHIP. The controller provides constant drain current biasing over temperature and device to device variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self-protection in the event of a short circuit, an internal charge pump that generates the negative voltage needed on the gate of the ADPA7008CHIP, and the option to use an external negative voltage source. The HMC980LP4E is also available in die form as the HMC980-Die.

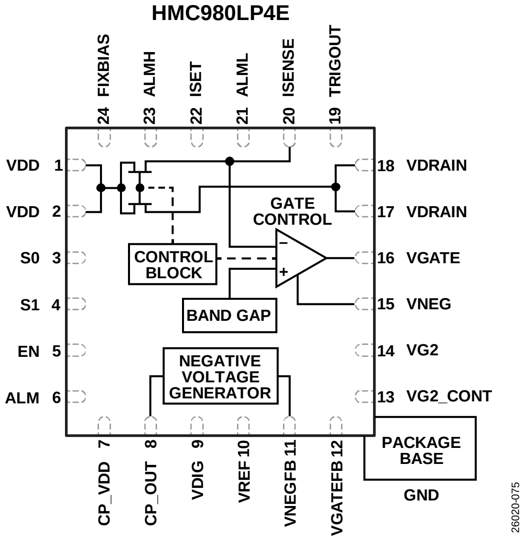


Figure 68. HMC980LP4E Active Bias Control

APPLICATION CIRCUIT SETUP

Figure 69 shows an application circuit using the HMC980LP4E to control the ADPA7009CHIP. When using an external negative supply for VNEG, refer to the application circuit shown in Figure 70.

In the application circuit shown in Figure 69, the ADPA7009CHIP drain voltage, V_{DRAIN}, and drain current, I_{DRAIN}, are set by the following equations:

$$V_{DD} = V_{DRAIN} + (I_{DRAIN} \times 0.85\ \Omega) \tag{1}$$

$$V_{DD} = 5\ \text{V} + (0.85\ \text{A} \times 0.85\ \Omega) = 5.72\ \text{V}$$

where:
V_{DD} and V_{DRAIN} are in volts.
I_{DRAIN} is in amperes.

$$R10 = (150\ \Omega \times \text{A}) \div (I_{DRAIN}) \tag{2}$$

$$R10 = (150\ \Omega \times \text{A}) \div (0.85\ \text{A}) = 176\ \Omega$$

where:
$R10$ is in ohms.
I_{DRAIN} is in amperes.

LIMITING VGATE FOR THE ADPA7009CHIP V_{GGx} ABSOLUTE MAXIMUM RATING REQUIREMENT

When using the HMC980LP4E to control the ADPA7009CHIP, the minimum voltages for VNEG and VGATE must be −1.5 V to keep the voltages within the absolute maximum rating limit for the V_{GGx} pad of the ADPA7009CHIP. To set the minimum voltages, set R15 and R16 to the values shown in Figure 69 and Figure 70. Refer to the AN-1363 Application Note for more information and calculations for R15 and R16.

The HMC980LP4E application circuits for biasing figures in the AN-1363 are two examples of how the HMC980LP4E is used as an active bias controller. Both application circuits within the AN-1363 show the R5 and R7 resistors, which are analogous to the R15 and R16 resistor shown in Figure 69 and Figure 70.

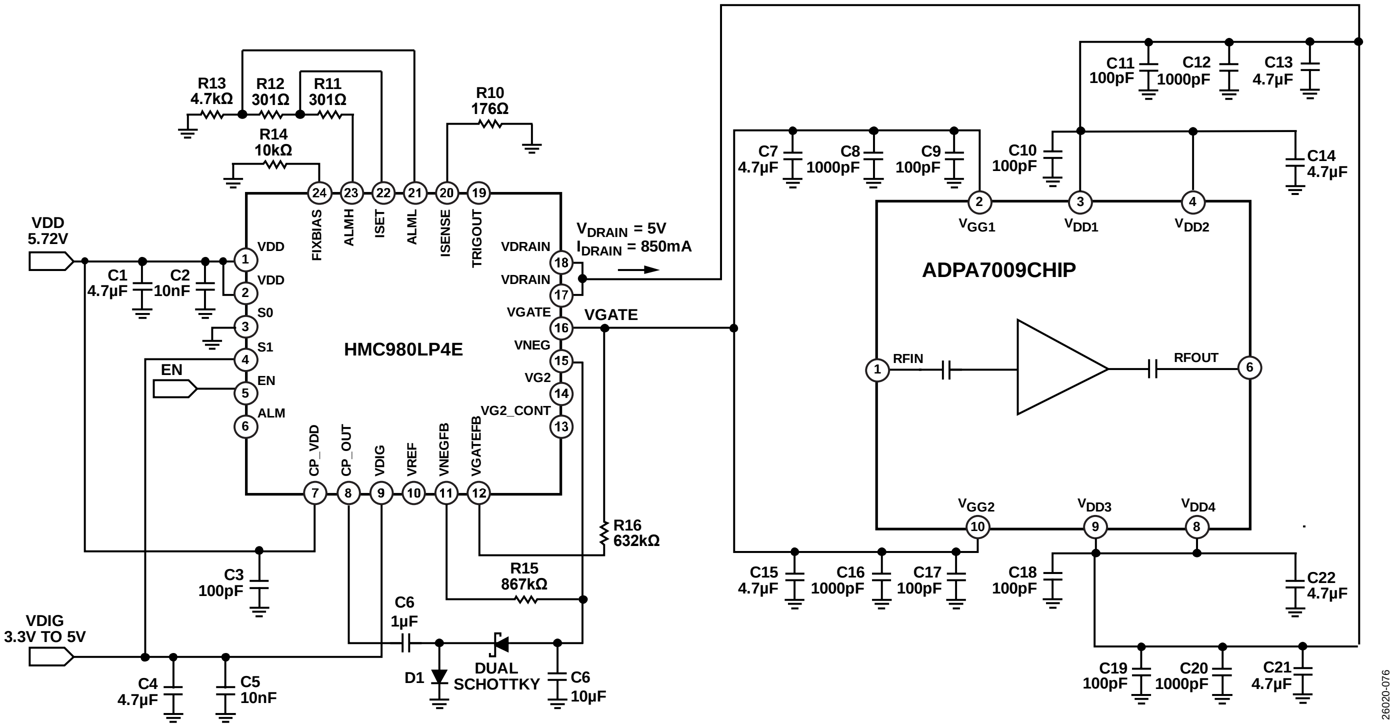


Figure 69. Application Circuit Using the HMC980LP4E with the ADPA7009CHIP (Internal Negative Voltage Source)

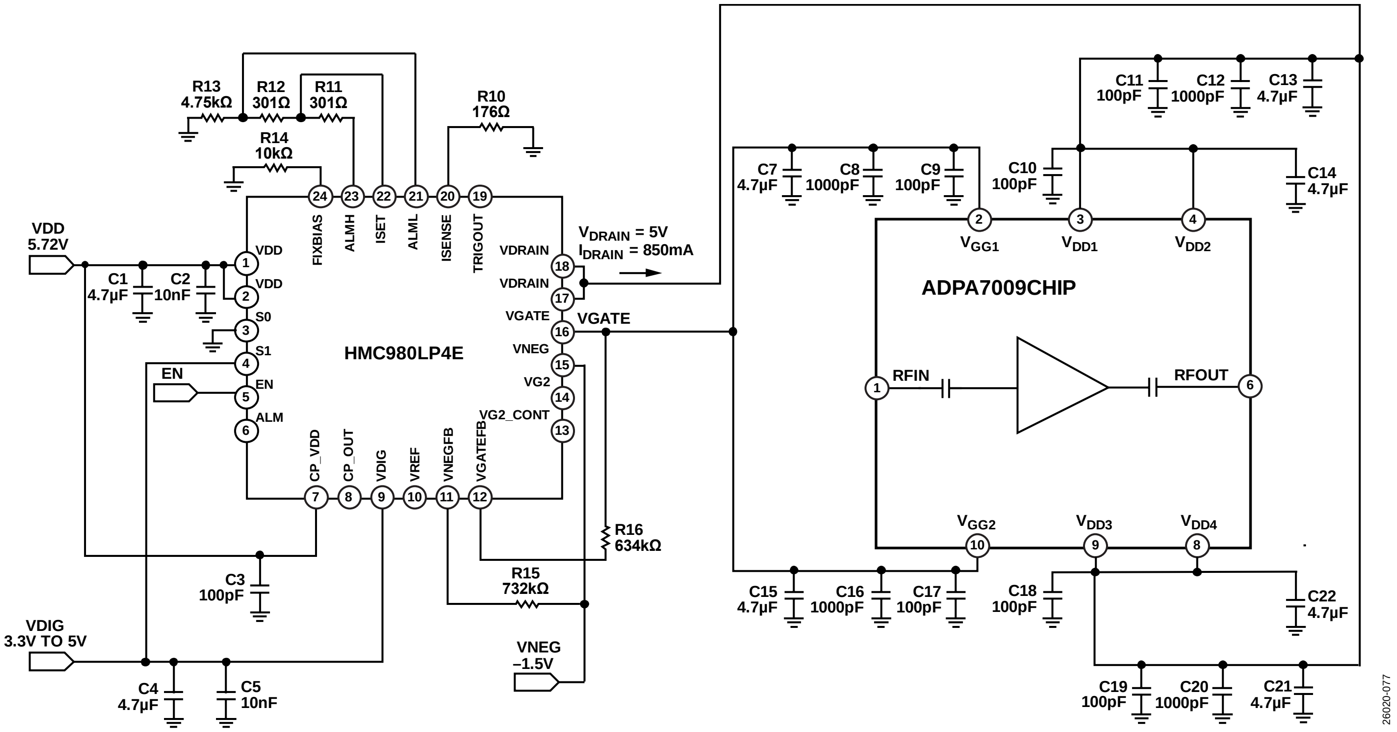


Figure 70. Application Circuit Using the HMC980LP4E with the ADPA7009CHIP (External Negative Voltage Source)

HMC980LP4E BIAS SEQUENCE

The dc supply sequence described in this section is required to prevent damage to the HMC980LP4E when using the device to control the ADPA7009CHIP.

Power-Up Sequence

The power-up sequence for the HMC980LP4E is as follows:

1. Set VDIG = 3.3 V.
2. Set S0 = 3.3 V.
3. Set VDD = 5.72 V.
4. Set VNEG = −1.5 V (this step is unnecessary if using an internally generated voltage).
5. Set EN = 3.3 V (the transition from 0 V to 3.3 V turns on VGATE and VDRAIN).

Power-Down Sequence

The power-down sequence for the HMC980LP4E is as follows:

1. Set EN = 0 V (the transition from 3.3 V to 0 V turns off V_{DRAIN} and V_{GATE}).
2. Set VNEG = 0 V (this step is unnecessary if using and internally generated voltage).
3. Set VDD = 0 V.
4. Set S0 = 0 V.
5. Set VDIG = 0 V.

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7009CHIP on or off by applying 3.3 V or 0 V, respectively, to the EN pad. At EN = +3.3 V, V_{GATE} drops to −1.5 V, and V_{DRAIN} turns on at +5 V. VGATE then rises until I_{DRAIN} = 850 mA, and the closed control loop regulates I_{DRAIN} at 850 mA. When EN = 0 V, VDRAIN is set to −1.5 V, and VDRAIN is set to 0 V.

CONSTANT DRAIN CURRENT BIASING vs. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses closed-loop feedback to continuously adjust VGATE to maintain a constant drain current bias over dc supply variation, temperature, and device to device variation. In addition, constant drain current bias is the optimum method for reducing time in calibration procedures and for maintaining consistent performance over time. By comparing the constant drain current bias with a constant gate voltage bias where the current is driven to increase when RF power is applied, a slightly lower output P1dB is seen with a constant drain current bias. This output P1dB is shown in Figure 78, where the RF performance is slightly lower than the constant gate voltage bias operation due to a lower drain current at the high input powers as the device reaches 1 dB compression.

To increase the output P1dB performance for the constant drain current bias toward the constant gate voltage bias performance, increase the set current toward the I_{DD} value this performance reaches under the RF drive in the constant gate voltage bias condition, as shown in Figure 78. The limit of increasing I_{DQ} under the constant drain current operation is set by the thermal limitations found in Table 5 with the maximum power dissipation specification. As the I_{DD} increase continues, the actual output P1dB does not continue to increase indefinitely and the power dissipation increases. Therefore, when using constant drain current biasing, take the trade-off between the power dissipation and the output P1dB performance into consideration.

CONSTANT I_{DD} OPERATION

T_A = 25°C, V_{DD} = 5 V, I_{DD} = 850 mA for nominal operation, unless otherwise noted. Figure 71 to Figure 78 are biased with the HMC980LP4E active bias controller. See the Biasing the ADPA7009CHIP with the HMC980LP4E section for biasing details.

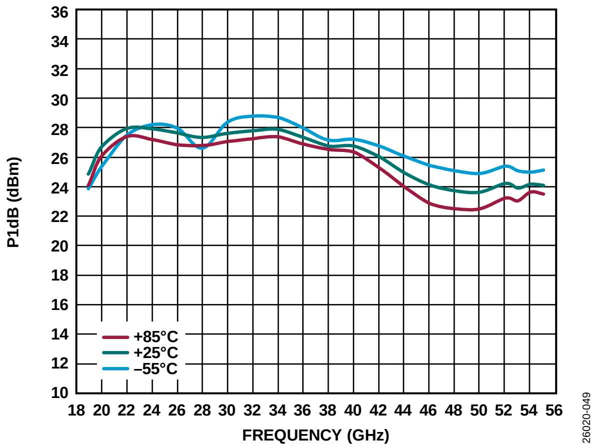


Figure 71. P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

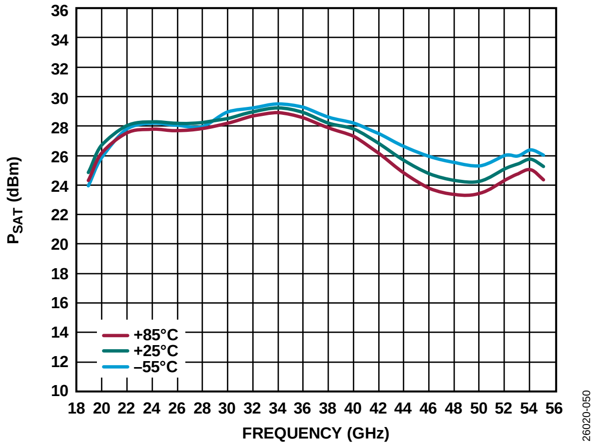


Figure 72. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

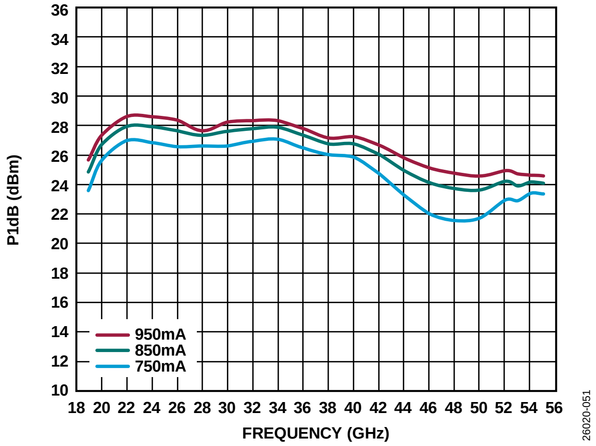


Figure 73. P1dB vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

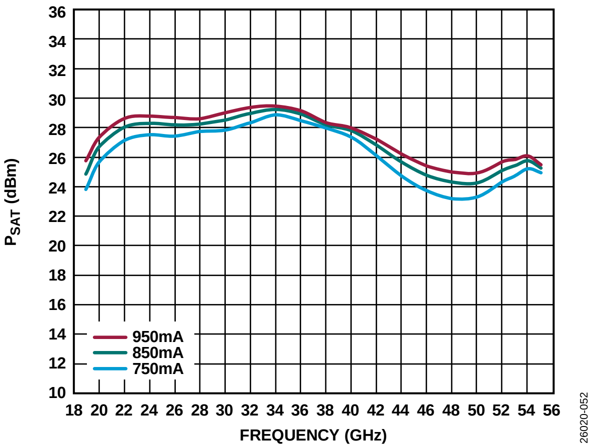


Figure 74. P_{SAT} vs. Frequency for Various Drain Currents, V_{DD} = 5 V, Data Measured with Constant I_{DD}

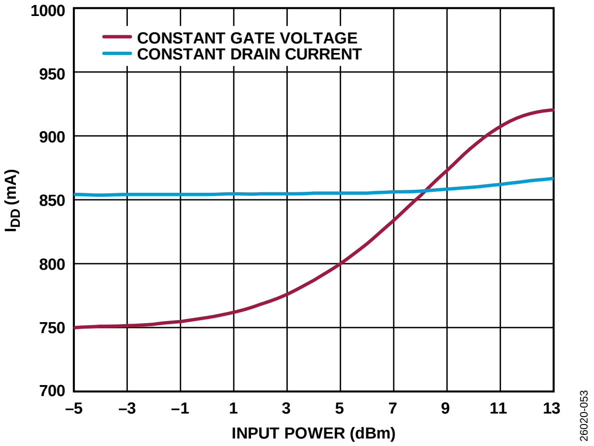


Figure 75. I_{DD} vs. Input Power, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 850 mA) and Constant Gate Voltage Bias (V_{GGx} ≈ −0.63 V)

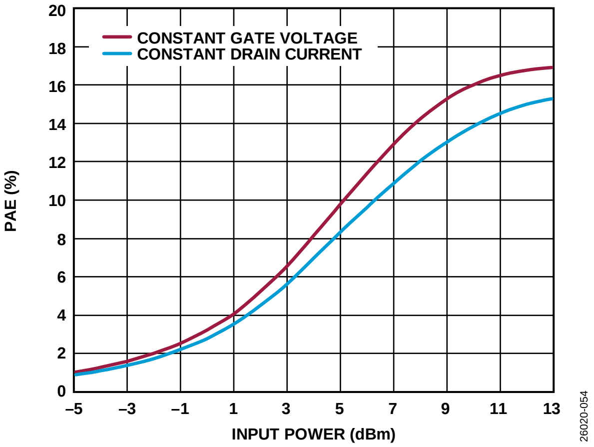


Figure 76. PAE vs. Input Power, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 850 mA) and Constant Gate Voltage Bias (V_{GGx} ≈ −0.63 V)

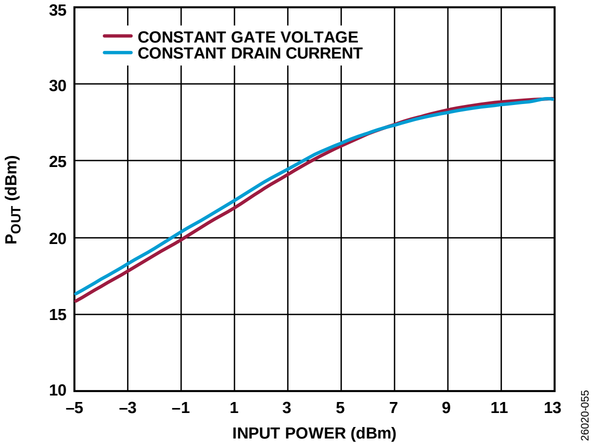


Figure 77. P_{OUT} vs. Input Power, $V_{DD} = 5$ V, Frequency = 36 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 850 mA) and Constant Gate Voltage Bias ($V_{GGx} \approx -0.63$ V)

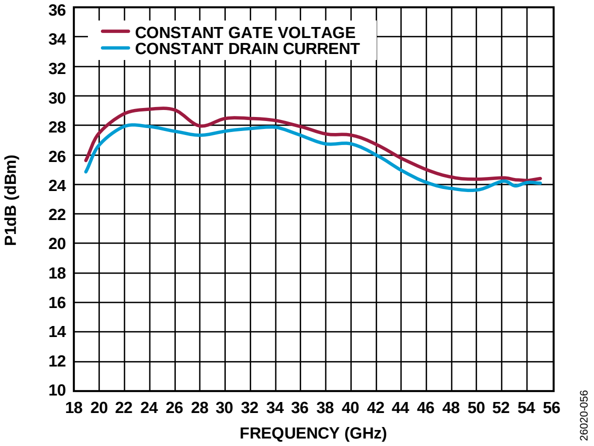


Figure 78. P1dB vs. Frequency, $V_{DD} = 5$ V, Constant Drain Current Bias (I_{DRAIN} Setpoint = 850 mA) and Constant Gate Voltage Bias ($V_{GGx} \approx -0.63$ V)

ASSEMBLY DIAGRAM

Figure 79 shows the assembly diagram for the ADPA7009CHIP.

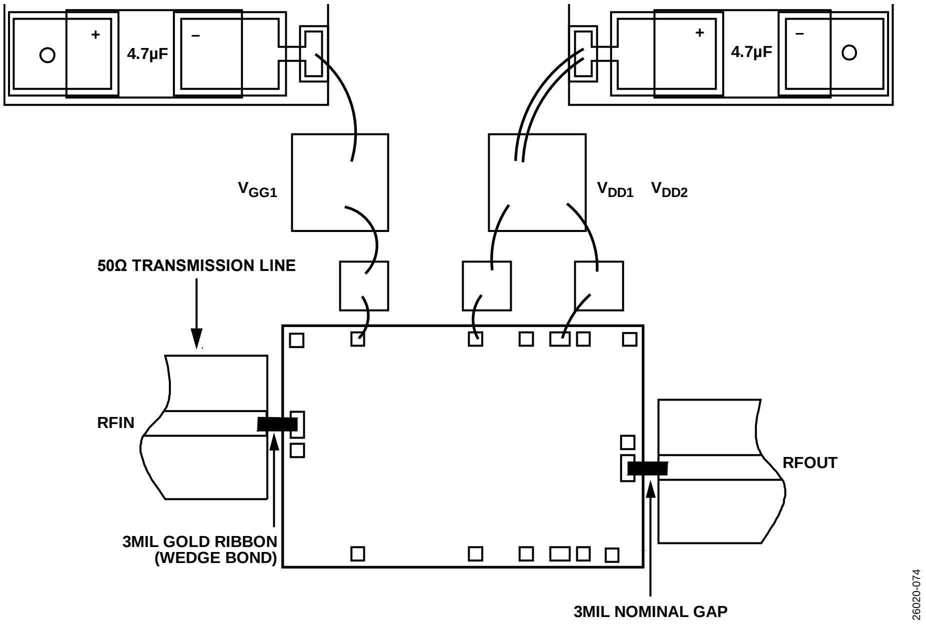


Figure 79. Assembly Diagram with Bias Control on North Side of Die

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Place the microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

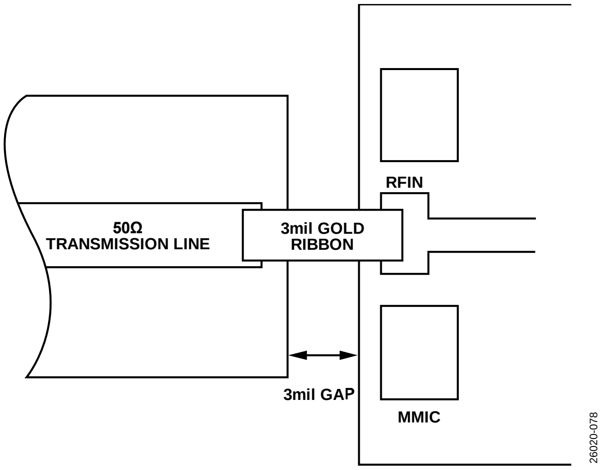


Figure 80. High Frequency Input Wideband Matching

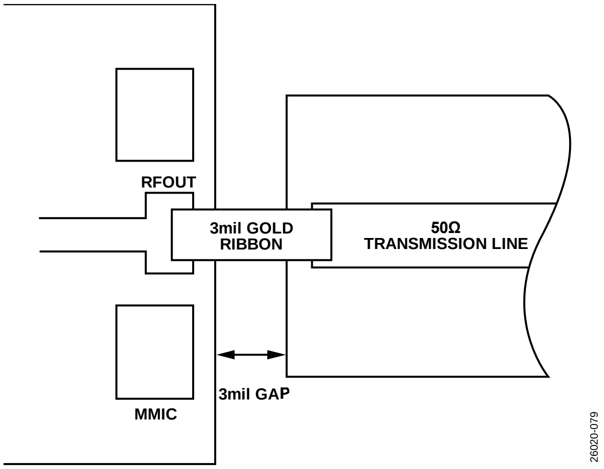


Figure 81. High Frequency Output Wideband Matching

HANDLING PRECAUTIONS

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle- or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chips using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The surface of the chip has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

MOUNTING

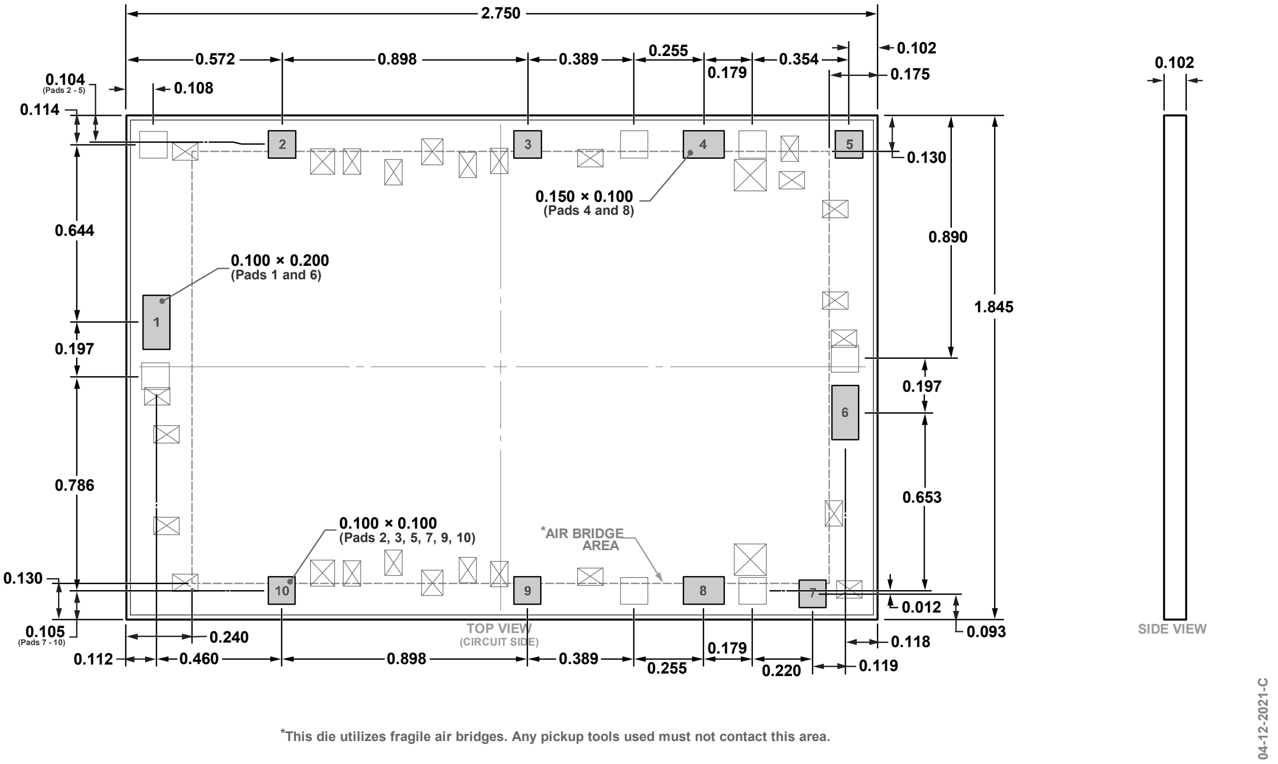
Before the epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

WIRE BONDING

RF bonds made with 0.076 mm × 0.0127 mm (3 mil × 0. 5 mil) gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. Thermosonically bonded dc bonds of 0.025 mm (1mil) diameter are recommended. Create ball bonds with a force of 40 g to 50 g, and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply the minimum amount of ultrasonic energy (depending on the process and package being used) to achieve reliable bonds. Keep all bonds as short as possible, less than 0.31 mm (12.2 mil).

Alternatively, use short RF bonds that are ≤3 mm and made with two 1 mm wires.

OUTLINE DIMENSIONS



*This die utilizes fragile air bridges. Any pickup tools used must not contact this area.

Figure 82. 10-Pad Bare Die [CHIP]
(C-10-13)
Dimensions shown in millimeter

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADPA7009CHIP	−55°C to +85°C	10-Pad Bare Die [CHIP]	C-10-13
ADPA7009C-KIT	−55°C to +85°C	10-Pad Bare Die [CHIP]	C-10-13

[1] The ADPA7009CHIP and ADPA7009C-KIT are RoHS compliant parts.
[2] Die inspected to meet MIL-STD-883 Method 2010, Condition B.

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- ✓ Shortage Management
- ✓ Alternative Solution
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