A31315

3D Magnetic Position Sensor IC

FEATURES AND BENEFITS

- 3D magnetic sensor enables flexible mechanical integration for contactless linear and rotary position applications
- Configurable signal path processing and on-chip angle calculation for accurate 360° and short stroke (<360°) rotary applications
- Multiple programmable linearization options for maximum measurement accuracy:
  - □ Piecewise-linear and binning modes
  - □ Up to 33-point fixed position
  - □ Up to 22-point programmable positions
- Ratiometric Analog, PWM, or SENT (SAE J2716) output formats
- Integrated IC diagnostics for high reliability
- Developed in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications
- Supports operation in harsh conditions, required for automotive and industrial applications
  - □ AEC-Q100 Grade 0 qualified
  - □ –40°C to 150°C temperature range
  - □ 4.5 to 5.5 V supply operating range
  - □ Over- and reverse-voltage protection
- Multiple package options available:
  - □ Single die surface mount (SOIC-8)
  - □ Dual (full redundant) stacked die surface mount (TSSOP-14)

APPLICATIONS

- Contact-less linear and rotary position sensor
- Throttle, valve, and cylinder position sensor
- Pedal position sensor
- Transmission position (fork/clutch, shifter, park lock)

DESCRIPTION

The A31315 3DMAG™ position sensor is designed for on-axis and off-axis rotary as well as linear stroke position measurement in automotive, industrial, and consumer applications.

This sensor integrates vertical and planar Hall-effect elements with precision temperature-compensating circuitry to detect two out of three magnetic field components (X, Y, and Z). Using configurable signal processing, linearization, and angle calculation allows the A31315 to accurately resolve the absolute rotary (full 360° and short-stroke <360°) or linear position of a moving magnetic target.

The A31315 features ratiometric analog, PWM, or SENT (SAE J2716) interface options to output the angle between the two factory-selected axes or the field from a single axis. In addition, the SENT interface provides the option to output the field measurement from both channels.

On-chip EEPROM technology, capable of supporting up to 100 write cycles, is integrated for flexible programming of configuration and calibration parameters and includes 92 bits provided for customer device identification purposes.

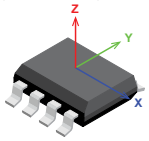
The A31315 contains on-chip diagnostic features required for high reliability automotive applications, including monitors of both internal and external fault conditions.

Developed in accordance with ISO 26262 as a hardware safety element out of context (SEooC) with ASIL B (single die) and ASIL D (dual die) capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

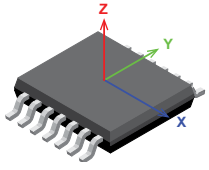
The A31315 is available as a single die in the SOIC-8 package and stacked dual die in the TSSOP-14 package for applications that require full redundancy.

PACKAGES

Single die SOIC-8
(OL suffix)



Dual die TSSOP-14
(LU suffix)



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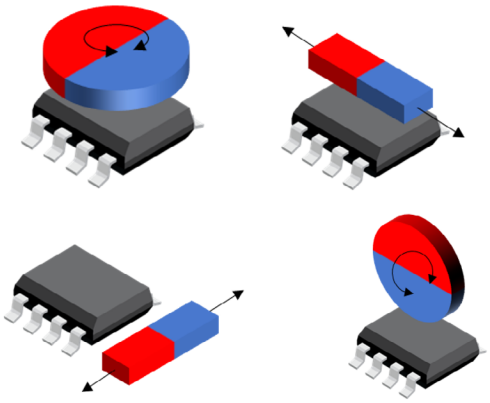
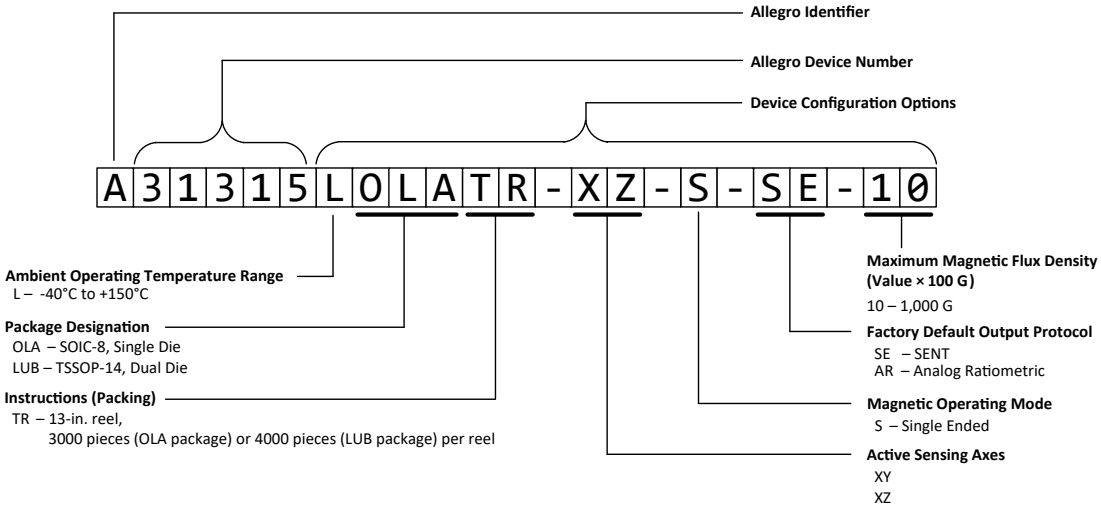


SELECTION GUIDE [1]

Part Number	Die Configuration and Package	Output Interface	Channel A	Channel B	Maximum Field (G)	Packing
A31315LOLATR-XZ-S-SE-10	Single Die SOIC-8	SENT (PWM) [2]	X	Z	1000	3,000 pieces per 13-in reel
A31315LOLATR-XY-S-SE-10			X	Y	1000	
A31315LOLATR-XZ-S-AR-10		Analog Ratiometric	X	Z	1000	
A31315LOLATR-XY-S-AR-10			X	Y	1000	
A31315LLUBTR-XZ-S-SE-10	Dual Stacked Die TSSOP-14	SENT (PWM) [2]	X	Z	1000	4,000 pieces per 13-in reel
A31315LLUBTR-XY-S-SE-10			X	Y	1000	
A31315LLUBTR-XZ-S-AR-10		Analog Ratiometric	X	Z	1000	
A31315LLUBTR-XY-S-AR-10			X	Y	1000	

[1] Contact Allegro for other axis and field range trim options.
[2] SENT interface is enabled by default. PWM is selectable through customer accessible registers.

Part Number Guide



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	$V_{CC(absmax)}$	Supply is clamped with 20 V limit to GND	18	V
Reverse Supply Voltage	$V_{RCC(absmax)}$	Supply is clamped with –20 V limit to GND	–18	V
Forward V_{OUT}-V_{CC} Voltage	$V_{OUT-CC(absmax)}$	V_{OUT} is clamped with 20 V limit to V_{CC}; Note: There is no reverse V_{OUT}-V_{CC} clamp	18	V
Forward Output Voltage	$V_{OUT(absmax)}$	Output is clamped with 20 V limit to GND	18	V
Reverse Output Voltage	$V_{ROUT(absmax)}$	Output is clamped with –10 V limit to GND	–6	V
Forward Supply Current	I_{CC}		30	mA
Reverse Supply Current	I_{RCC}		–30	mA
Output Current Limit	$I_{OUT(SOURCE)}$	VOUT shorted to GND	30	mA
	$I_{OUT(SINK)}$	VCC shorted to VOUT	–30	mA
Extended Operating Ambient Temperature	$T_{A(EXT)}$	Device will work within this temperature range, but performance is not specified	–45 to 165	°C
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{stg}		–65 to 175	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\Theta JA}$	SOIC-8	125	°C/W
		TSSOP-14	214	°C/W

*Additional thermal information available on the Allegro website.

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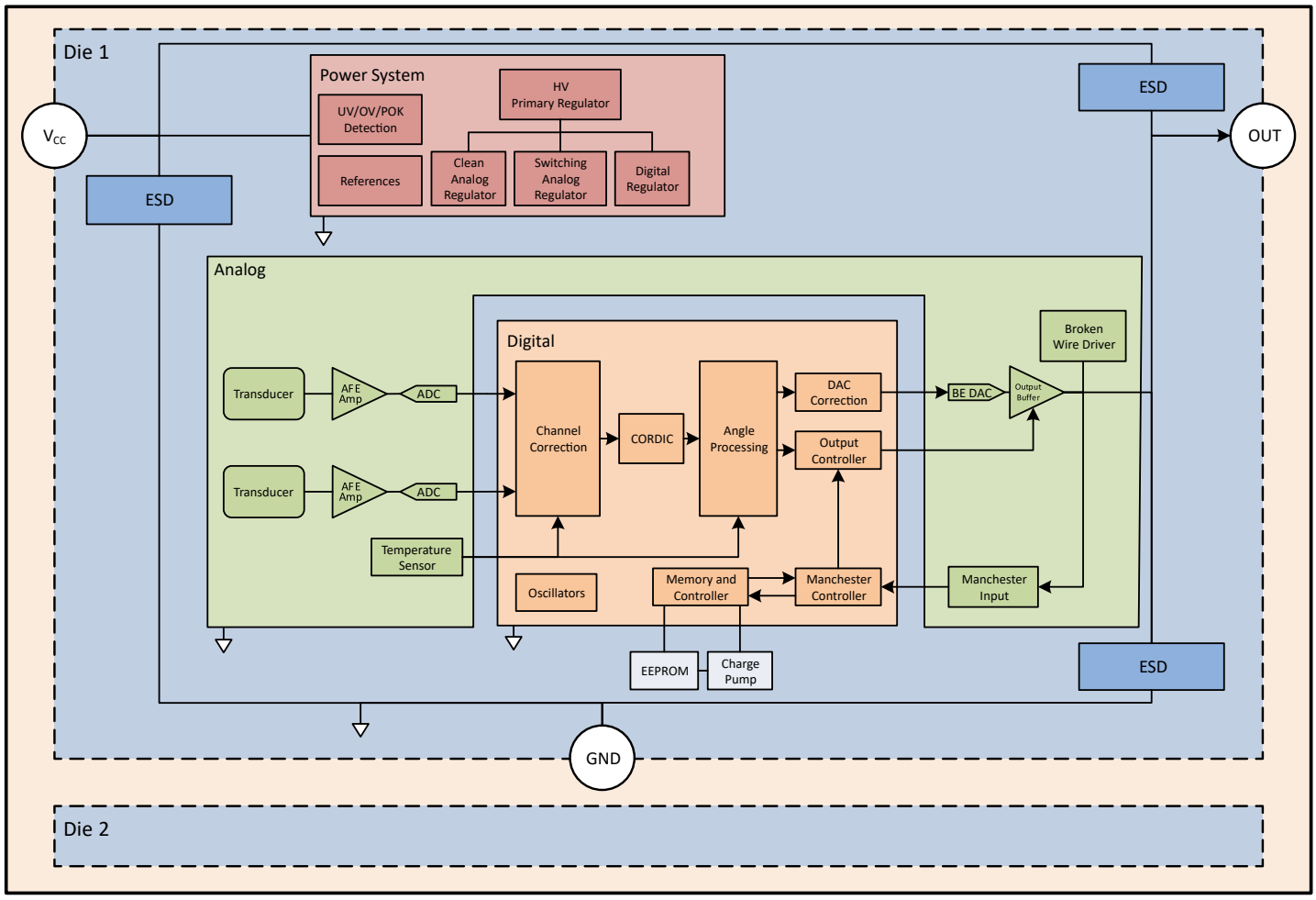

Figure 1: Functional Block Diagram

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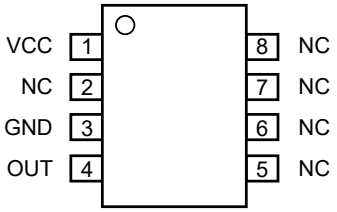
PINOUT DIAGRAMS AND TERMINAL LISTS

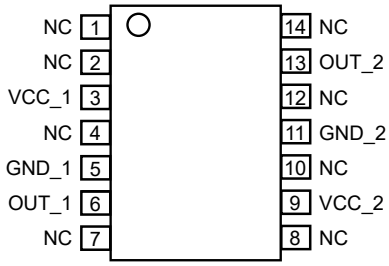


8-Pin SOIC Pinout Diagram

8-Pin SOIC Terminal List

Number	Name	Function
1	VCC	Supply voltage
2	NC	Not connected [1]
3	GND	Ground
4	OUT	Device output
5-8	NC	Not connected [1]

[1] Connect to GND for optimal ESD performance.



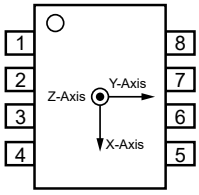
14-Pin TSSOP Pinout Diagram

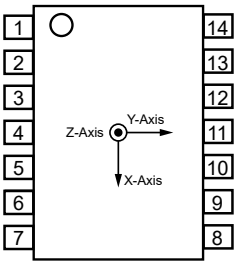
14-Pin TSSOP Terminal List

Number	Name	Die	Function
1-2	NC	1	Not connected [1]
3	VCC_1	1	Supply voltage
4	NC	1	Not connected [1]
5	GND_1	1	Ground
6	OUT_1	1	Device Output
7	NC	1	Not connected [1]
8	NC	2	Not connected [1]
9	VCC_2	2	Supply voltage
10	NC	2	Not connected [1]
11	GND_2	2	Ground
12	NC	2	Not connected [1]
13	OUT_2	2	Device Output
14	NC	2	Not connected [1]

[1] Connect to GND for optimal ESD performance.

AXIS DEFINITIONS





Note: Arrows show the default polarity of each axis. Polarity can be changed with internal settings.

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APPLICATION CIRCUIT

Digital Output Modes

When using the A31315 in digital output modes, either SENT or PWM, both push-pull and open-drain output drive modes are selectable. Regardless of the selected drive style, a pull-up resistor is still recommended in order to provide a known diagnostic state in the event of a line break or device tri-state event. The figure below shows a typical application circuit for the A31315 when using a digital interface. It should be noted that the capacitance value shown assumes the total capacitance of passive component and capacitance due to harness connections.

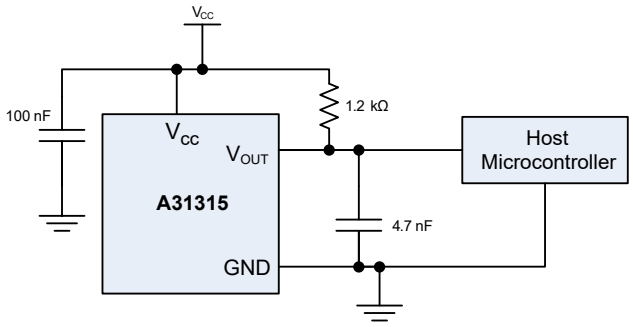

Figure 2: A31315 Typical Application Circuit for Digital Output Modes (SENT / PWM)

Analog Output

When using the analog mode of the A31315, capacitance is required for stability of the output. A load resistor, either to GND or V_{CC} is recommended, as with the digital interface to provide a known diagnostic state in the event of a line break or device tri-state event. For additional filtering and lower noise, a series resistor can be placed prior to the capacitance to create a low-pass filter. However, caution should be taken, as this will also reduce the operating output voltage based on the ratio of the filter resistor and the load resistance. Additionally, the A31315's analog output mode is ratiometric with V_{CC}; for this reason, the host controller monitoring the output voltage should be connected to the same voltage supply as the A31315. A typical application circuit is shown below for using the A31315 as an analog interface.

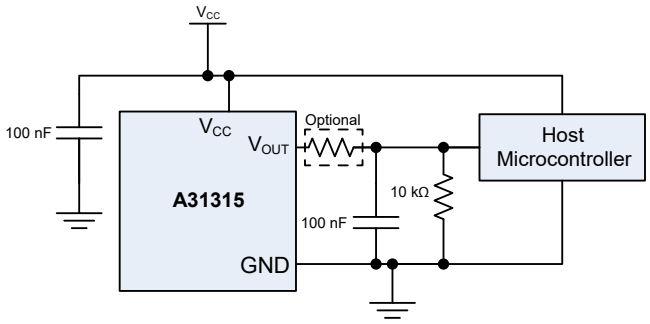

Figure 3: A31315 Typical Application Circuit for Analog Output Modes

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OPERATING CHARACTERISTICS

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL REQUIREMENTS						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Buffer Capacitor	C_{SUP}		10	100	600	nF
Supply Current	I_{CC}	Each die	5.0	8.5	10.0	mA
DEVICE REQUIREMENTS						
Ambient Operating Temperature	T_A		–40	–	150	°C
Number of EEPROM Writes [1]	N_{EEPROM}	T_A = 25°C	–	–	100	writes
MAGNETIC REQUIREMENTS [2]						
Magnetic Flux Density	$\|B_{IN}\|$	For xxx-10 parts, devices tested at $\|B_{IN}\|$ = 300 G, operation below this value is characterized, but not specified	–	±300	±1000	G

[1] EEPROM writes are not supported at temperatures above 85°C.
[2] Magnetic flux density values are based on target device sensitivity. Values here do not account for temperature or lifetime drift. To avoid saturation in application, Allegro recommends a 10% margin below the maximum field.

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PERFORMANCE CHARACTERISTICS: Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
DEVICE SPECIFICATIONS							
Undervoltage Detection Threshold	$V_{UVD\ (LOW,\ FALL)}$	V_{CC} falling, UVD_SEL = 0		3.6	–	4.1	V
	$V_{UVD\ (LOW,\ RISE)}$	V_{CC} rising, UVD_SEL = 0		3.7	–	4.2	V
	$V_{UVD\ (HIGH,\ FALL)}$	V_{CC} falling, UVD_SEL = 1		4.1	–	4.4	V
	$V_{UVD\ (HIGH,\ RISE)}$	V_{CC} rising, UVD_SEL = 1		4.2	–	4.5	V
Overvoltage Detection Threshold	$V_{OVD\ (LOW,\ FALL)}$	V_{CC} falling, OVD_SEL = 1		5.6	–	6.0	V
	$V_{OVD\ (LOW,\ RISE)}$	V_{CC} rising, OVD_SEL = 1		5.65	–	6.05	V
	$V_{OVD\ (HIGH,\ FALL)}$	V_{CC} falling, OVD_SEL = 0		8.4	–	10.2	V
	$V_{OVD\ (HIGH,\ RISE)}$	V_{CC} rising, OVD_SEL = 0		8.6	–	10.4	V
Power-On Reset Voltage	$V_{POR(FALL)}$	V_{CC} falling		2.6	–	2.9	V
	$V_{POR(RISE)}$	V_{CC} rising		2.8	–	3.1	V
Power-On Time	t_{PO}	Time from $V_{CC} > V_{CC(MIN)}$ until unfiltered output is settled		–	1.0	1.7	ms
Oscillator Frequency	f_{OSC}			7.36	8.00	8.64	MHz
ABSOLUTE ANGLE SPECIFICATIONS [1]							
Angle Error (XY)	$ERR_{ANG(XY)}$	$T_A = 25°C$ [2]		–1.0	–	1.0	degrees
		$–40 \leq T_A \leq 150°C$		–1.2	–	1.2	degrees
		After AEC-Q100 Grade 0 Qual Stress, $T_A = –40°C$, 25°C, 150°C		–	±0.65	–	degrees
Angle Error (XZ)	$ERR_{ANG(XZ)}$	$T_A = 25°C$ [2]		–1.0	–	1.0	degrees
		$–40 \leq T_A \leq 150°C$		–1.2	–	1.2	degrees
		After AEC-Q100 Grade 0 Qual Stress, $T_A = –40°C$, 25°C, 150°C		–	±0.93	–	degrees
Input-Referred Angle Noise	$N_{ANG(IN)}$	$\|B_{IN}\|$ = ± 300 G input field	BW_SEL = 0	–	0.0291	–	$degree_{RMS}$
			BW_SEL = 1	–	0.0291	–	$degree_{RMS}$
			BW_SEL = 2	–	0.0326	–	$degree_{RMS}$
			BW_SEL = 3	–	0.0381	–	$degree_{RMS}$
			BW_SEL = 4	–	0.0468	–	$degree_{RMS}$
			BW_SEL = 5	–	0.0575	–	$degree_{RMS}$
			BW_SEL = 6	–	0.0673	–	$degree_{RMS}$
ANGLE DRIFT SPECIFICATIONS [1]							
Angle Drift (XY)	$DRIFT_{Ang,Temp(XY)}$	Change in angle relative to $T_A = 25°C$ [2]		–1.2	–	1.2	degrees
	$DRIFT_{Ang,Life(XY)}$	Change in angle relative to pre-stress conditions [4]		–1.3	±0.40	1.3	degrees
Angle Drift (XZ)	$DRIFT_{Ang,Temp(XZ)}$	Change in angle relative to $T_A = 25°C$ [2]		–1.2	–	1.2	degrees
	$DRIFT_{Ang,Life(XZ)}$	Change in angle relative to pre-stress conditions [4]		–1.33	±0.91	1.33	degrees

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PERFORMANCE CHARACTERISTICS (continued): Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ABSOLUTE CHANNEL SPECIFICATIONS [1]						
Default Channel Sensitivity	$SENS_{Target}$	Selection Guide Part Number: XXX-10	–	32.125	–	LSB / G
Channel Sensitivity Error (X,Y)	$ERR_{Sens(X,Y)}$	T_A = 25°C [2]	–1.5	–	1.5	%
		–40 ≤ T_A ≤ 150°C	–3	–	3	%
Channel Sensitivity Error (Z)	$ERR_{Sens(Z)}$	T_A = 25°C [2]	–1.5	–	1.5	%
		–40 ≤ T_A ≤ 150°C	–4	–	4	%
Channel Offset Error (X,Y)	$ERR_{Off(X,Y)}$	T_A = 25°C [2]	–1.5	–	1.5	G
		–40 ≤ T_A ≤ 150°C	–4	–	4	G
Channel Offset Error (Z)	$ERR_{Off(Z)}$	T_A = 25°C [2]	–1.5	–	1.5	G
		–40 ≤ T_A ≤ 150°C	–1.5	–	1.5	G
Channel Linearity Error (X,Y)	$ERR_{Lin(X,Y)}$	100 G ≤ B_{IN} ≤ 1000 G	–0.3	–	0.3	%
Channel Linearity Error (Z)	$ERR_{Lin(Z)}$	100 G ≤ B_{IN} ≤ 1000 G	–0.3	–	0.3	%
Input-Referred Channel Noise (X,Y)	$N_{CHAN(X,Y)}$	T_A = 25°C	–	5.245	–	mG (RMS/√Hz)
		–40 ≤ T_A ≤ 150°C	–	7.821	–	mG (RMS/√Hz)
Input-Referred Channel Noise (Z)	$N_{CHAN(Z)}$	T_A = 25°C	–	2.083	–	mG (RMS/√Hz)
		–40 ≤ T_A ≤ 150°C	–	3.104	–	mG (RMS/√Hz)
CHANNEL DRIFT SPECIFICATIONS [1]						
Channel Sensitivity Error Drift (X,Y)	$DRIFT_{Sens,Temp(X,Y)}$	Change in sensitivity relative to T_A = 25°C [2]	–2	–	2	%
	$DRIFT_{Sens,Life(X,Y)}$	Change in sensitivity relative to pre-stress conditions [4]	–2.50	±1.3	2.50	%
Channel Sensitivity Error Drift (Z)	$DRIFT_{Sens,Temp(Z)}$	Change in sensitivity relative to T_A = 25°C [2]	–3	–	3	%
	$DRIFT_{Sens,Life(Z)}$	Change in sensitivity relative to pre-stress conditions [4]	–3.50	±2.5	3.50	%
Channel Offset Drift (X,Y)	$DRIFT_{Off,Temp(X,Y)}$	Change in offset relative to T_A = 25°C [2]	–3.5	–	3.5	G
	$DRIFT_{Off,Life(X,Y)}$	Change in offset relative to pre-stress conditions [4]	–0.90	±0.25	0.90	G
Channel Offset Drift (Z)	$DRIFT_{Off,Temp(Z)}$	Change in offset relative to T_A = 25°C [2]	–1.5	–	1.5	G
	$DRIFT_{Off,Life(Z)}$	Change in offset relative to pre-stress conditions [4]	–0.60	±0.5	0.60	G

[1] As measured through digital interface with factory trim. Values do not include DAC or account for customer trim registers.
[2] 25°C measurements taken after 48-72 hour wait at 40-55% relative humidity.
[3] Parameter not measured at final test. Determined by design and characterization.
[4] Min and Max values based on worst case drift seen during Q100 qual.

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INTERFACE CHARACTERISTICS: Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Broken Wire Response Time	t_{BW}	Time after V_{CC} – GND = 0.2 V, either V_{CC} or GND wire broken, C_L = 100 nF, C_{SUP} = 100 nF	–	–	500	µs
High-Z Leakage	$I_{leak(Hi-Z)}$	Device in High-Z mode, output shorted to GND or VCC	–10	–	10	µA
Filter Step Response Time	t_{RESP}	bw_sel = 5, time to 90% response to step	–	396	450	µs
Angle Update Rate	t_{UPDATE}	Valid for all bandwidth settings	14.72	16	17.28	µs
MANCHESTER INTERFACE SPECIFICATIONS						
Manchester Input Thresholds [3]	$V_{trig(H)}$	V_{OUT} rising, DIG_COMM_INPUT_HIGH = 0	1.800	1.980	2.160	V
		V_{OUT} rising, DIG_COMM_INPUT_HIGH = 1	2.185	2.365	2.540	V
	$V_{trig(L)}$	V_{OUT} falling, DIG_COMM_INPUT_LOW = 0	0.830	0.990	1.155	V
		V_{OUT} falling, DIG_COMM_INPUT_LOW = 1	1.385	1.640	1.905	V
	$V_{trig(hys)}$	DIG_COMM_INPUT_HIGH = 0, DIG_COMM_INPUT_LOW = 0	0.815	0.985	1.150	V
		DIG_COMM_INPUT_HIGH = 0, DIG_COMM_INPUT_LOW = 1	0.160	0.335	0.525	V
		DIG_COMM_INPUT_HIGH = 1, DIG_COMM_INPUT_LOW = 0	1.155	1.380	1.605	V
		DIG_COMM_INPUT_HIGH = 1, DIG_COMM_INPUT_LOW = 1	0.495	0.725	0.995	V
Manchester Communication Speed [3]	f_{MAN}	Manchester input bit rate (from host to sensor)	4.0	–	100	kbps
		Manchester output bit rate with 100 nF load (device responds at the input bit rate)	4.0	–	8 [1]	kbps
SENT INTERFACE SPECIFICATIONS						
SENT Tick Time	t_{TICK}	Valid for all SENT Modes, DIG_OUT_DATA_RATE = 0	2.76	3	3.24	µs
		Valid for all SENT Modes, range of selectable tick times [2]	0.5	–	10	µs
SENT Tick Time Tolerance	TOL_{TICK}	Valid for all selectable tick times	–8	–	8	%
SENT Output Resolution	RES_{SENT}	Based on sent_data_sel	12	–	16	bits
SENT Output Saturation Voltage	$V_{SAT(LOW)}$	Output current = –4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.55	V
SENT Output Load Capacitance	C_L		–	4.7	5.7	nF
SENT Output Load Resistance	$R_{L(PULLUP)}$	Output Current ≥ –10 mA	1.2	–	–	kΩ
SENT Output Low Voltage [3]	V_{OL}	Low state voltage with 0.52 mA DC load current	–	–	0.5	V
SENT Output High Voltage [3]	V_{OH}	High state voltage with 0.1 mA DC load current	4.1	–	–	V
SENT Ground Current [3]	I_{GND}	Average current through (signal) ground line over one message	–	–	50	mA
SENT Supply Ripple Current [3]	$I_{SUP-RIPPLE}$	Peak-to-peak variation in supply current consumption over one message at frequencies up to f_C = 30 kHz	–	–	9.0	mA
SENT Fall Time [3]	t_{FALL}	From V_{OUT} = 3.8 V to V_{OUT} = 1.1 V, $I_{GND} \leq$ 20 mA, 3 µs tick time	–	–	6.5	µs
		From V_{OUT} = 3.8 V to V_{OUT} = 1.1 V, 20 mA ≤ $I_{GND} \leq$ 50 mA, 3 µs tick time	–	–	5.0	µs
SENT Rise Time [3]	t_{RISE}	From V_{OUT} = 1.1 V to V_{OUT} = 3.8 V, 3 µs tick time	–	–	18	µs
SENT Edge Jitter [3]	Δt_{FALL}	Edge to edge jitter with static environment for any pulse prior, 3 µs tick time	–	–	0.1	µs
SENT Nibble Jitter [3]	Δt_{NIBBLE}	Variation of maximum nibble time compared to the expected time derived from the calibration pulse, 3 µs tick time	–	–	0.3	µs

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INTERFACE CHARACTERISTICS (continued): Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
PWM INTERFACE SPECIFICATION							
PWM Carrier Frequency	f_{PWM}	See Table 10		125	–	16000	Hz
PWM Carrier Frequency Tolerance	$TOL(f_{PWM})$			–8	–	8	%
PWM Resolution	RES_{PWM}	Based on f_{PWM}		8	–	15	bit
PWM Jitter	PWM_{JIT}	$f_{PWM} \geq 2$ kHz; see Table 10 for LSB definition		–1	–	1	LSB
		$f_{PWM} < 2$ kHz; see Table 10 for LSB definition		–3	–	3	LSB
PWM Duty Cycle	D_{PWM}			2	–	98	%
PWM Saturation Voltage	$V_{SAT(LOW)}$	$R_{PULLUP} \geq 1.2$ kΩ		–	–	0.35	V
PWM Load Capacitance	C_L			–	–	4.7	nF
PWM Load Resistance	$R_{L(PULLUP)}$			1.2	–	–	kΩ
ANALOG INTERFACE SPECIFICATION							
DAC DNL [3]	DNL	V_{CC} = 5 V		–0.022	–	0.022	$\%V_{CC}$
DAC INL [3]	INL	V_{CC} = 5 V		–0.098	–	0.098	$\%V_{CC}$
DAC Ratiometry	RAT	V_{OUT} = 8 to 92 $\%V_{CC}$		–0.2	–	0.2	%
DAC Gain Error	$Gain_{DAC}$	V_{CC} = 5 V		–0.2	–	0.2	%
DAC Offset Error	Off_{DAC}	V_{CC} = 5 V, T_A = 25°C		–3	–	3	mV
		V_{CC} = 5 V		–8	–	8	mV
DAC Noise [3]	N_{DAC}	V_{CC} = 5 V, BW = 12 kHz, outputting fixed DAC code		–	0.37	–	mV_{RMS}
Analog Resolution	RES_{DAC}			–	12	–	bits
Step Size	$STEP_{DAC}$	Step size of DAC		0.01391	0.01465	0.01538	$\%V_{CC}$
Saturation Voltage	$V_{SAT(HIGH)}$	R_L = 4.7 kΩ		93	–	–	$\%V_{CC}$
	$V_{SAT(LOW)}$	R_L = 4.7 kΩ		–	–	7	$\%V_{CC}$
	$V_{SAT(HIGH)}$	R_L = 10 kΩ		95	–	–	$\%V_{CC}$
	$V_{SAT(LOW)}$	R_L = 10 kΩ		–	–	5	$\%V_{CC}$
Operating Voltage Range	V_{OH}	R_L = 4.7 kΩ, linearity error < 0.1 %		92	–	–	$\%V_{CC}$
	V_{OL}	R_L = 4.7 kΩ, linearity error < 0.1 %		–	–	8	$\%V_{CC}$
	V_{OH}	R_L = 10 kΩ, linearity error < 0.1 %		94	–	–	$\%V_{CC}$
	V_{OL}	R_L = 10 kΩ, linearity error < 0.1 %		–	–	6	$\%V_{CC}$
Diagnostic Voltage ranges	$V_{SATDIAG(HIGH)}$	V_{CC} = 5 V	R_L = 3.3 kΩ	94	98	100	$\%V_{CC}$
			R_L = 5 kΩ	96	98	100	$\%V_{CC}$
			R_L = 10 kΩ	97	98	100	$\%V_{CC}$
	$V_{SATDIAG(LOW)}$	V_{CC} = 5 V	R_L = 3.3 kΩ	0	2	6	$\%V_{CC}$
			R_L = 5 kΩ	0	2	4	$\%V_{CC}$
			R_L = 10 kΩ	0	2	3	$\%V_{CC}$

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INTERFACE CHARACTERISTICS (continued): Valid for all electrical and device requirements ranges and $|B_{IN}| \geq 300$ G, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ANALOG INTERFACE SPECIFICATION							
Analog Low Operating Range	$V_{LIMOUT(L)}$	V_{CC} = 5 V	ANA_RANGE_SEL = 0	0.000	0.000	0.014	V
			ANA_RANGE_SEL = 1	0.186	0.200	0.214	V
			ANA_RANGE_SEL = 2	0.236	0.250	0.264	V
			ANA_RANGE_SEL = 3	0.286	0.300	0.314	V
			ANA_RANGE_SEL = 4	0.336	0.350	0.364	V
			ANA_RANGE_SEL = 5	0.386	0.400	0.414	V
			ANA_RANGE_SEL = 6	0.486	0.500	0.514	V
			ANA_RANGE_SEL = 7	0.736	0.750	0.764	V
Analog High Operating Range	$V_{LIMOUT(H)}$	V_{CC} = 5 V	ANA_RANGE_SEL = 0	4.986	5	5	V
			ANA_RANGE_SEL = 1	4.786	4.8	4.814	V
			ANA_RANGE_SEL = 2	4.736	4.75	4.764	V
			ANA_RANGE_SEL = 3	4.686	4.7	4.714	V
			ANA_RANGE_SEL = 4	4.636	4.65	4.664	V
			ANA_RANGE_SEL = 5	4.586	4.6	4.614	V
			ANA_RANGE_SEL = 6	4.486	4.5	4.514	V
			ANA_RANGE_SEL = 7	4.236	4.25	4.264	V
Load Capacitance [3]	C_L	ANA_CAP_SEL = 0		10	–	150	nF
		ANA_CAP_SEL = 2, recommended for $C_L \geq$ 100 nF		50	–	480	nF
		ANA_CAP_SEL = 4, recommended for $C_L \geq$ 400 nF		300	–	600	nF
Load Resistance	R_L	Pull-up to VCC or pull-down to GND		4.23	–	–	kΩ
Analog Response Time [3]	t_{RESP}	Sensor output with 100 nF load 1482 Hz bandwidth, time from 90% input change to 90% output change		–	–	600	µs

[1] Based on receiver design.
[2] Tick times under 0.5 µs are available, but not guaranteed.
[3] Parameter not measured at final test. Determined by design and characterization.

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FUNCTIONAL DESCRIPTION

The A31315 contains two independent signal paths. Each channel has dedicated polarity, sensitivity and offset correction that is available to the customer for end-of-line calibration. This allows the A31315 to be used in both rotary and linear position applications in any mounting orientation relative to the sensing magnet, and to provide high accuracy and matching as the device and magnetic system changes over temperature.

The A31315 features an internal CORDIC calculation of angle from factory-selected pair of detection axes (X, Y, and Z). The CORDIC calculation effective accuracy is 16 bits. Optionally, the A31315 can function as a 1-D sensor by bypassing the CORDIC calculation. See Equation 12 for exact implementation. This mode is also resolved at a 16-bit resolution.

Equation 1:

$$\theta = \text{atan2}(\sin(\theta), \cos(\theta))$$

The output angle value is available in SENT, PWM, or analog output options. Alternatively, the two factory-selected channels of the X, Y, and Z channels are available to output in SENT. Along with the magnetic data, the SENT option provides access to additional device information such as temperature, error flag information, and customer identification register data. End-of-line angle calibration options are available in customer space to allow the device to be used in a wide number of contactless sensing applications.

Typical Application Information

The A31315 has a high level of customer programmability to be used in a number of applications for either on- or off-axis rotary angle or linear position sensing. For on-axis rotary sensing, the on-chip ATAN2 provides an angle output that, combined with the configurable update rate, allows magnetic angular sensing at a wide range of system bandwidth requirements. To help account for errors associated with off-axis mounting of the sensor, the individual channel sensitivity and offset correction can be used to match the signals input to the ATAN2.

The A31315 can be used for slide-by applications where a one-dimensional position change of a target is to be measured. The angle output from the A31315 is related to the linear position of the magnetic target. With the available linearization on the A31315, stroke lengths greater than the length of the magnet can be realized.

Temperature Output

The A31315 temperature sensor output that is used for temperature compensation within the device can be read from primary register temperature_16b, or in SENT in the extended data nibbles or SCN serial message.

Table 1: Temperature Output Options

Temperature Reporting Method	Code Range	Temperature Range	Step Size	Conversion
Read of Register (temperature_16b)	–32,768 … 32,767	–231.0 … 281.0°C	1/8°C	$T_A\,[°C] = \frac{\text{signed 16-bit temperature code}}{128} + 25$
SENT Serial or Extended Nibble	1 … 4088	–230.9 … 280.0 °C	1/8°C	$T_A\,[°C] = \frac{\text{unsigned 12-bit temperature code} - 2048}{8} + 25$
SENT 8-BIT Temperature Data	1 … 255	–229.0… 279.0 °C	2°C	$T_A\,[°C] = (\text{unsigned 8-bit temperature code} - 128) \times 2 + 25$

SENT temperature sensor output corresponds to SAEJ2716 APRIL2016, chapter E.2.2.3, with the following function representation:

SENT Serial or Extended Nibble:
X_1 = –230.875°C = 42.275 K
Y_1 = 1

X_2 = +280.000°C = 553.150 K
Y_2 = 4088

SENT 8-Bit Data:
X_1 = –229.0 °C = 44.150 K
Y_1 = 1

X_2 = +279.000°C = 552.150 K
Y_2 = 255

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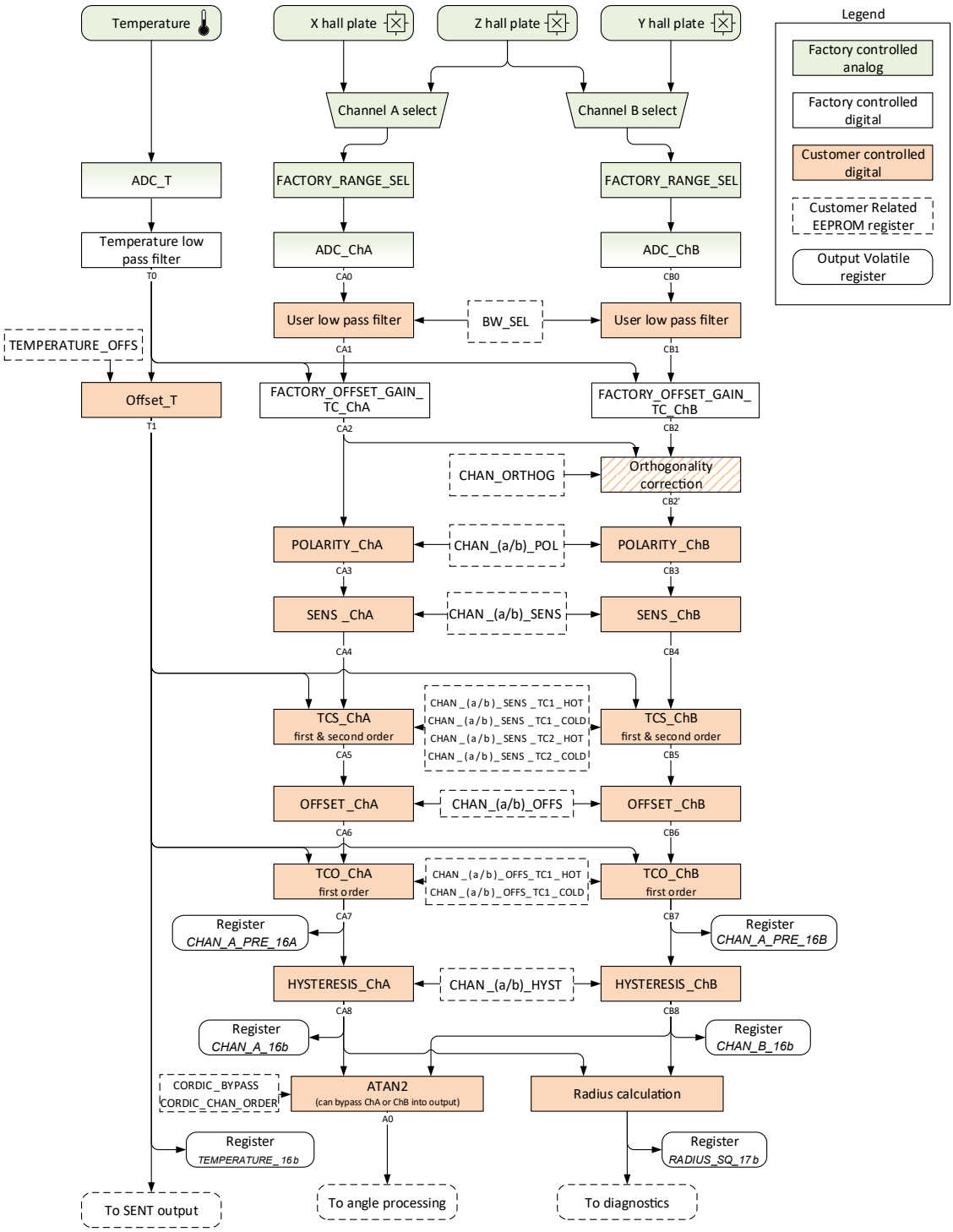

Figure 4: 1D Signal Path Processing Flow

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Signal Path

The A31315 signal path contains two main sections. The first is two 1-D signal paths each reflecting the magnetic field in one direction as specified in the selection guide. The second section uses a CORDIC calculation to determine an angle from the 1-D signals. Both sections provide customer-accessible trim registers for end-of-line calibrations.

1-D Signal Path

FACTORY CHANNEL A / CHANNEL B INPUT SELECTION

Selects the input to Channel A and Channel B. This is programmed at factory level. Use the selection guide to determine which axes are used.

FACTORY RANGE SELECTION

Factory range selection sets the analog pre-amplifier. The A31315 front end settings are configured for a limited field range. To determine the field range, consult the selection guide.

CUSTOMER-CONTROLLABLE DATA PATH

Customer-trimmable registers allow for final test trimming in application. The equations in the following sections explain in detail the available customer trims.

NOTE: If customer registers are used to trim the signal path, performance parameters may not be guaranteed. The customer must take care in changing these components and assumes liability for device performance deviations that come about from the changes applied.

Customer Trimming

LOW-PASS FILTER

The user low-pass filter allows noise reduction without data update rate change using a combination of a CIC and IIR filter. The IIR filter is a third-order low-pass filter. The input of this filter is noted in Figure 4 above as CA0 for Channel A and CB0 for Channel B. Both channels are filtered at the same rate; there is no independent filter settings for each channel.

Equation 2:

$$CA_1 = LPF(CA_0)$$
$$CB_1 = LPF(CB_0)$$

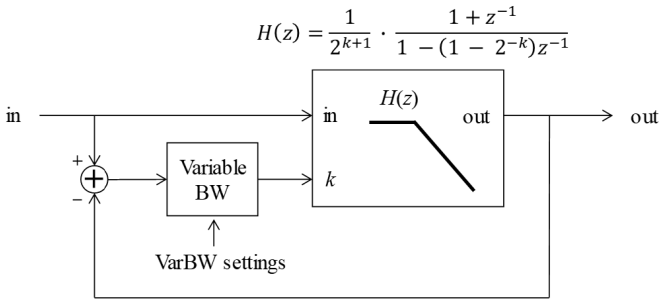

Figure 5: Low-Pass Filter

Table 2: Selection of Customer Low-Pass Filter, EEPROM Parameter BW_SEL

BW_SEL	3 dB Frequency (Hz)	90% Settling (ms)
0	329.1	1.666
1	465.8	1.172
2	556	0.9925
3	700	0.763
4	1000	0.554
5	1482	0.396
6	2024	0.249
7	Adaptive	0.135

The adaptive filter has a selectable minimum and maximum bandwidth for increased customization. The minimum and maximum bandwidths are selected via the BW_ADAPT_MIN and BW_ADAPT_MAX registers respectively. The table below shows the corresponding bandwidths for each register. BW_ADAPT_MIN is by default set to code 0, and BW_ADAPT_MAX is by default set to code 7.

Table 3: BW_ADAPT_(MIN/MAX) Frequencies

BW_ADAPT_(MIN/MAX) (LSB)	Frequency (Hz)
0	38.9
1	77.8
2	156.3
3	314.8
4	638.7
5	1308.6
6	2672.1
7	4734.2

The overall filter response is given below.

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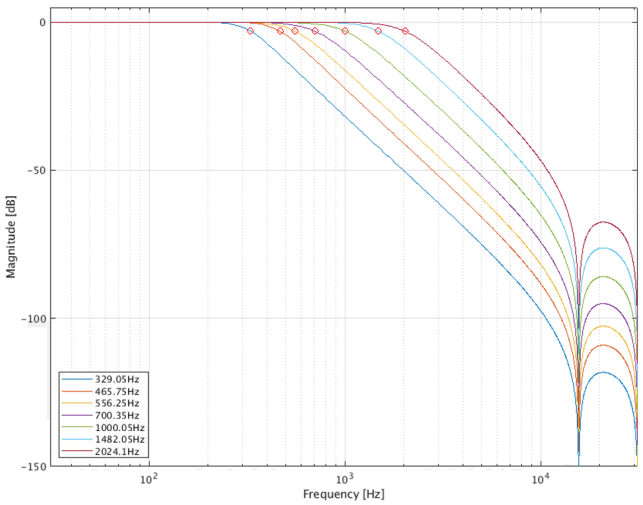

Figure 6: Overall IIR filter Response Depending on the Selected Bandwidth

SENSOR OUTPUT DURING LOW-PASS FILTER INITIALIZATION

After startup, the low-pass filter takes some time to settle. It may be undesirable for the output values to show this settling behavior. For this reason, the parameter POWER_ON_DELAY allows suppressing the sensor output for a configurable amount of time. If desired, the time that the output is suppressed should be set to a value compatible with the filter settling time. It is the user's responsibility to do this. The value is not automatically chosen by the sensor to be compatible with the filter bandwidth setting.

For analog output, if the IIR output is suppressed in this manner the output will be forced to maximum value if ANA_INIT_SEL = 1 or to minimum value if ANA_INIT_SEL = 0.

For SENT output:

- If SENT_ENCODING_SEL = 1 and SENT_DATA_SEL = 0, 4, 7, or 15, an initialization code selected by parameter SENT_INIT_SEL will be transferred for the configured amount of time.
- In other cases, the data will be sent out with SCN[0] = 1 for the configured filter initialization time.

For PWM output, the POR error code for POR will be sent out for the time selected by POWER_ON_DELAY. This error code is represented by the values shown in Table 34. The error may be superseded by errors of higher priority as per Table 34.

The POWER_ON_DELAY options are given in Table 4.

Table 4: Selection of output during low-pass filter startup, EEPROM Parameter POWER_ON_DELAY

POWER_ON_DELAY	Analog Fixed Output Duration (ms)	SENT Additional initialize / POR time (ms)	PWM POR state duration (ms)
0	0.5	0.5	0.5
1	1.0	1.0	1.0
2	1.5	1.5	1.5
3	2.0	2.0	2.0
4	2.5	2.5	2.5
5	3.0	3.0	3.0
6	4.0	4.0	4.0
7	0.25	none	0.25

FACTORY CORRECTION

The A31315 devices are factory-trimmed for the channels and field ranges noted in the selection guide. The trim provides a flat TC to all parameters and accuracy to the datasheet specifications for channel and angle.

Equation 3:

$$CA_2 = Factory_{Correction}\,(CA_1)$$

$$CB_2 = Factory_{Correction}\,(CB_1)$$

ORTHOGONALITY CORRECTION

A factory-trimmed orthogonality correction is implemented. This works by modeling the orthogonality error as a cross-sensitivity from Channel A into Channel B prior to CORDIC calculation.

Equation 4:

$$CB_2' = CB_2 + Phase_{Corr} \times CA_2$$

For information on how to adapt the orthogonality correction, contact Allegro MicroSystems.

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POLARITY, OFFSET, SENSITIVITY, AND TEMPERATURE CALIBRATION

Polarity bits are provided for each channel to invert the direction of sensitivity of either or both axes. Polarity change is the first operation performed in the customer trim path. Because of this, it should be set first to ensure the offset programmed has the proper sign.

The offset and sensitivity parameters can be used to help provide a linear output when using the device in any off-axis orientation. The angle output will be linear for well-matched input sensing vectors. When mounting off axis, one dimension often has an offset and amplitude variation relative to the other. Using CHAN_X_OFFS and CHAN_X_SENS registers can correct this system-level mismatch, effectively providing a simple two parameter linearization method.

The offset and sensitivity temperature compensation parameters can be used to stabilize the sensor output over temperature. First- and second-order corrections, separated per channel, and separated for temperatures above and below 25°C, are provided for post-mounting offset and gain calibration.

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POLARITY CORRECTION

Equation 5:

$$CA_3 = \begin{cases} CA_2 & \text{for} \quad CHAN_A_POL = 0 \\ -CA_2 & \text{for} \quad CHAN_A_POL = 1 \end{cases}$$

$$CB_3 = \begin{cases} CB_2 & \text{for} \quad CHAN_B_POL = 0 \\ -CB_2 & \text{for} \quad CHAN_B_POL = 1 \end{cases}$$

SENSITIVITY ADJUSTMENT

Equation 6:

$CA_4 = CA_3 \times CHAN_A_SENS$
$CB_4 = CB_3 \times CHAN_B_SENS$

The range for CHAN_X_SENS is [0 … 7.9995], with a resolution of 2^{-11} = 4.88e-04. The default value is 2048, resulting in a gain of 1.

SENSITIVITY CORRECTION OVER TEMPERATURE

Equation 7:

$$CA_5 = \begin{cases} CA_4 \times (1 + CHAN_A_SENS_TC1_COLD \times (T_0 - 25°C) + CHAN_A_SENS_TC2_COLD \times (T_0 - 25°C)^4) & \text{Temperature} < 25°C \\ CA_4 \times (1 + CHAN_A_SENS_TC1_HOT \times (T_0 - 25°C) + CHAN_A_SENS_TC2_HOT \times (T_0 - 25°C)^2) & \text{Temperature} \geq 25°C \end{cases}$$

$$CB_5 = \begin{cases} CB_4 \times (1 + CHAN_B_SENS_TC1_COLD \times (T_0 - 25°C) + CHAN_B_SENS_TC2_COLD \times (T_0 - 25°C)^2) & \text{Temperature} < 25°C \\ CB_4 \times (1 + CHAN_B_SENS_TC1_HOT \times (T_0 - 25°C) + CHAN_B_SENS_TC2_HOT \times (T_0 - 25°C)^2) & \text{Temperature} \geq 25°C \end{cases}$$

The range for CHAN_X_SENS_TC1_COLD is [-2^{-7} … ($2^{-7} - 2^{-17}$)] = –0.0078 … +0.0078 with a resolution of 2^{-17} = 7.63e–06.
The range for CHAN_X_SENS_TC1_HOT is [-2^{-8} … ($2^{-8} - 2^{-18}$)] = –0.0039 … +0.0039 with a resolution of 2^{-18} = 3.81e–06.
The range for CHAN_X_SENS_TC2_COLD is [-2^{-16} … ($2^{-16} - 2^{-25}$)] = –1.53e–05… +1.52e–05 with a resolution of 2^{-25} = 2.98e–08.
The range for CHAN_X_SENS_TC2_HOT is [-2^{-14} … ($2^{-14} - 2^{-23}$)] = –6.10e–05… +6.09e–05 with a resolution of 2^{-23} = 1.19e–07.

CUSTOMER OFFSET CORRECTION

Equation 8:

$CA_6 = CA_5 + CHAN_A_OFFS$
$CB_6 = CB_5 + CHAN_B_OFFS$

The range for CHAN_B_OFFS is –32768 … +32764 LSB with a resolution of 4 LSB.

CUSTOMER OFFSET CORRECTION OVER TEMPERATURE

Equation 9:

$$CA_7 = \begin{cases} CA_6 + CHAN_A_OFFS_TC1_COLD \times (T_0 - 25°C) & \text{Temperature} < 25°C \\ CA_6 + CHAN_A_OFFS_TC1_HOT \times (T_0 - 25°C) & \text{Temperature} \geq 25°C \end{cases}$$

$$CB_7 = \begin{cases} CB_6 + CHAN_B_OFFS_TC1_COLD \times (T_0 - 25°C) & \text{Temperature} < 25°C \\ CB_6 + CHAN_B_OFFS_TC1_HOT \times (T_0 - 25°C) & \text{Temperature} \geq 25°C \end{cases}$$

The range for CHAN_X_OFFS_TC1_COLD is [–256 … +255.875] LSB/K with a resolution of 2^{-3} = 0.125 LSB/K.
The range for CHAN_X_OFFS_TC1_HOT is [–128 … +127.9375] LSB/K with a resolution of 2^{-4} = 0.0625 LSB/K.

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HYSTERESIS FILTER

Equation 10:

$$CA_8 = \text{HYSTERESIS_FILTER}(CA_7)$$
$$CB_8 = \text{HYSTERESIS_FILTER}(CB_7)$$

The hysteresis block limits change in the sensor output to remove noise from the channels. The hysteresis block can be disabled by setting the hysteresis window width to zero. The hysteresis block input as measured by the sensor is at the head of the hysteresis window. As long as the hysteresis input (CA_7 / CB_7) advances in the same direction of rotation, the hysteresis output (CA_8 / CB_8) will be unchanged, minimizing latency. If the hysteresis input (CA_7 / CB_7) reverses direction, the hysteresis output is held static until the input data exits the hysteresis window in either direction. If the exit is in the opposite direction of movement as to where the head was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. On sensor reset, the first value change is accepted as initial direction. The behavior of the hysteresis block is shown in Figure 7.

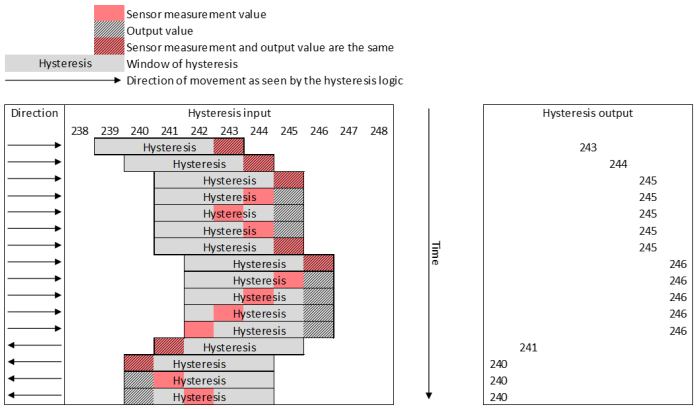

Figure 7: Input and Output Example of Hysteresis Block

The range for CHAN_X_HYST is [0 … 1023] LSB with a resolution of 1 LSB.

DIRECT OUTPUT REGISTER

The Channel A and Channel B data can be read directly through the digital interface for customer trimming and in-application debugging purposes.

Equation 11:

$$\text{CHAN_A_16B}[15:0] = CA_8$$
$$\text{CHAN_B_16B}[15:0] = CB_8$$

ATAN INPUT SELECTION

In order to provide the angle output from the 3D Hall elements, the two-input function atan2 is used. It is internally implemented using the CORDIC algorithm. The sine and cosine inputs to the ATAN2 are user-selectable based on the EEPROM parameter CORDIC_SEL. The CORDIC algorithm will calculate the arctangent to provide the angle between the two input vectors. This angle is related to the linear position in slide-by long stroke applications. A bypass option is provided to route channel A or channel B directly to the next processing steps. This allows using the A31315 as a 1-D sensor. When bypassing the ATAN2 calculation, the most negative 1-D value (–32768) becomes an angle of 0° (value 0), a zero value of the 1-D channel becomes 180° (value 32768), and the most positive value of the 1-D channel becomes 359.99° (value 65535).

Equation 12:

$$A_0 = \begin{cases} \text{atan2}(CA_8, CB_8) & CORDIC_BYPASS = 0,\ CORDIC_CHAN_ORDER = 0 \\ \text{atan2}(CB_8, CA_8) & CORDIC_BYPASS = 0,\ CORDIC_CHAN_ORDER = 1 \\ CA_8 + 32768 & CORDIC_BYPASS = 1,\ CORDIC_CHAN_ORDER = 0 \\ CB_8 + 32768 & CORDIC_BYPASS = 1,\ CORDIC_CHAN_ORDER = 1 \end{cases}$$

Note: in the equation above, atan2(0,1) = 0°, atan2(1,0) = +90°, atan2(0,–1) = +180°, and atan2(–1,0) = +270°. This follows from the function definition of θ = atan2(sin(θ), cos(θ)).

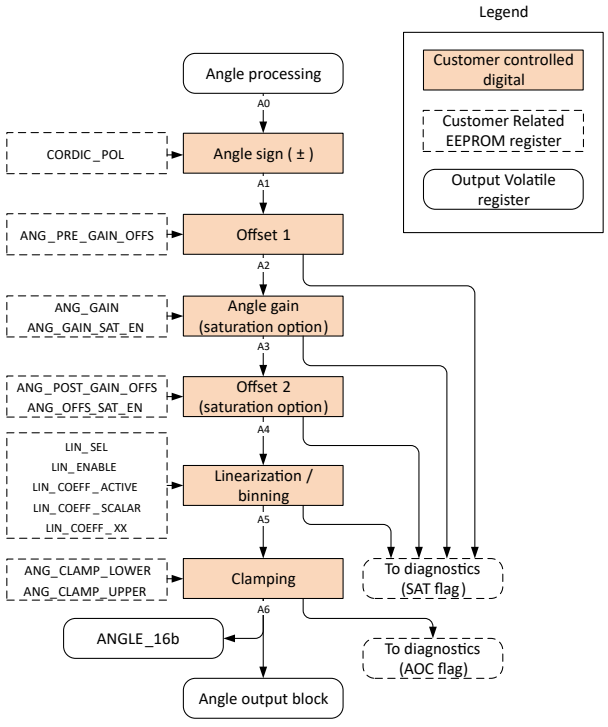

Figure 8: Angle Signal Path Processing Flow

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ANGLE SIGN (ROTATION DIRECTION)

The A31315 has a bit in EEPROM (CORDIC_POL) designating the polarity of the angle reading of the device. Since angle value is calculated from the channel values, which can be polarity inverted earlier in the signal path, care must be taken to ensure the positive direction of rotation is as desired. Since each channel polarity, CORDIC input selection, and angle sign bit affects angle rotation, the equation below is provided as a quick reference for defining angle rotation.

Equation 13:

$$A_1 = \begin{cases} A_0 & \text{for } CORDIC_POL = 0 \\ 360° - A_0 & \text{for } CORDIC_POL = 1 \end{cases}$$

PRE-GAIN ANGLE OFFSET CORRECTION

The A31315 contains a programmable zero angle point allowing the electrical zero angle to be adjusted from the magnetic angle to match mechanical orientations. This is provided in the form of an angle offset correction at the output of the CORDIC angle calculation. This offset is a full-scale offset with a range of 0 to 360 degrees following Equation 14.

Equation 14:

$A_2 = \text{mod}(A_1 + \text{ANG_PRE_GAIN_OFFS}, 360°)$

The output of the pre-gain offset correction block, A_2 is always allowed to roll over from maximum output to minimum output as needed. It is possible to compare the output angle of this block to programmed limits using the parameters ANG_THRESH_LOW and ANG_THRESH_HIGH, if ANG_THRESH_EN = 1. These limits do not saturate the A_2 angle but can only be used to cause a saturation flag.

The range for ANG_PRE_GAIN_OFFS is [0 … 359.989013671875]° with a resolution of $360 / 2^{15} = 0.010986328125°$.

The range for ANG_THRESH_LOW is [0 … 358.59375]° with a resolution of $360 / 2^8 = 1.40625°$.

The range for ANG_THRESH_HIGH is [0 … 358.59375]° with a resolution of $360 / 2^8 = 1.40625°$.

See section “Saturation Flag (SAT)” regarding the possible diagnostics for this block.

ANGLE GAIN CORRECTION

Following the initial angle offset correction, there is an angle gain block. This gain correction, defined by the EEPROM parameter ANG_GAIN, allows inputs to be scaled to any desired output range. This can be to increase inputs for short stroke rotary applications or slide by linear applications to provide the desired output range, or to reduce the inputs if a reduced range is desired for a full output range.

The range for ANG_GAIN is [0 … 63.9990234375] with a resolution of $2^{-10} = 0.0009765625$. Setting the gain to zero results in a zero output of the block and has no practical use.

If the gain is set to a value larger than 1.0×, some input values would result in an output angle larger than 360°. In this case, the output of the angle gain block, A_3, can either saturate to max code or roll over, depending on the preference set by the EEPROM parameter ANG_GAIN_SAT_EN.

If ANG_GAIN_SAT_EN = 0, the output will roll over from 360° to restart from 0°.

If ANG_GAIN_SAT_EN = 1 (saturation after gain enabled), and gain is set to >1, the output will saturate to 360° instead of rolling over. After that, there will be a point where the sensor output jumps from 360° to 0°. This point, measured in pre-gain angle A_2, is user-configurable using the parameter ANG_SAT_ROLLOVER. This is displayed in Figure 9.

The range for ANG_SAT_ROLLOVER is [0 … 358.59375]° with a step size of $360° / 2^8 = 1.40625°$.

In most applications, it will be safest to put the output discontinuity of the chip as far away as possible from the range that is being gained up. This is achieved by setting ANG_SAT_ROLLOVER = 180° + (180°) / ANG_GAIN. For example, with ANG_GAIN set to 4×, the recommended value for ANG_SAT_ROLLOVER would be 225°. This is equal to a register value of ANG_SAT_ROLLOVER = round($2^8 \times (225° / 360°)$) = 160. The value for ANG_SAT_ROLLOVER must be larger than 360° / ANG_GAIN, otherwise the signal path will always saturate to 0 degrees.

The behavior is summarized by the following equations:

Equation 15:

If ANG_GAIN_SAT_EN = 0:

$A_3 = \text{mod}(A_2 \times \text{ANG_GAIN}, 360)$

Equation 16:

If ANG_GAIN_SAT_EN = 1:

$$A_3 = \begin{cases} \text{ANG_GAIN} \times A_2 & \text{for } A_2 < \left(\frac{360°}{\text{ANG_GAIN}}\right) \\ 359.9945° & \text{for } \left(\frac{360°}{\text{ANG_GAIN}}\right) \le A_2 \le \text{ANG_SAT_ROLLOVER} \\ 0° & \text{for } A_2 > \text{ANG_SAT_ROLLOVER} \end{cases}$$

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As an example, the output function for a setting of ANG_GAIN = 4×, ANG_GAIN_SAT_EN = 1, and ANG_SAT_ROLLOVER = 225° is given in the figure below:

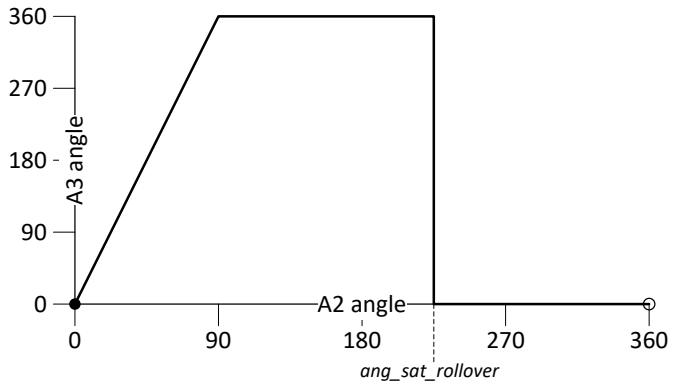

Figure 9: Angle gain behavior over full rotation with gain = 4 and output clamping enabled

As a second example, the output function for a setting of ANG_GAIN = 3× and ANG_GAIN_SAT_EN = 0 is given below:

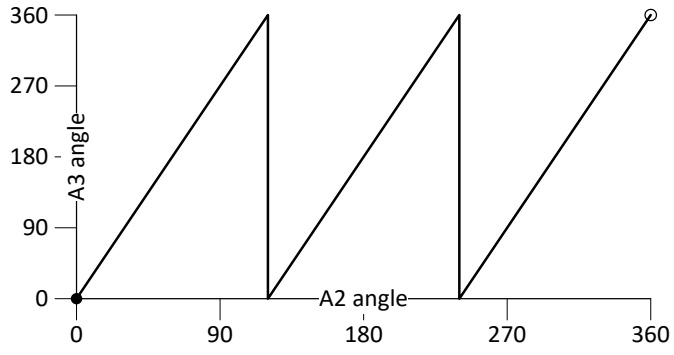

Figure 10: Angle gain behavior over full rotation with gain = 3 and ANG_GAIN_SAT_EN = 0

By default, ANG_GAIN_SAT_EN = 1, and ANG_SAT_ROLLOVER = 0. See chapter “Saturation Flag (SAT)” regarding the possible diagnostics for this block.

POST GAIN ANGLE OFFSET CORRECTION

After the Gain Block, there is an additional offset correction block to allow full flexibility of angle programming. The user can optionally saturate the output of the Post Gain Angle Offset block or allow to rollover using the EEPROM parameter ANG_OFFS_SAT_EN.

Equation 17:

$$A_4 = \begin{cases} \mathrm{mod}(A_3 + ANG_POST_GAIN_OFFS, 360) & \text{for } ANG_OFFS_SAT_EN = 0 \\ \min(\max(A_3 + ANG_POST_GAIN_OFFS, 0), 359.9945) & \text{for } ANG_OFFS_SAT_EN = 1 \end{cases}$$

The range for ANG_POST_GAIN_OFFS is [-360 … 359.9890137] ° with a step size of 720° / 2^{16} = 0.010986328125°.

By default ANG_OFFS_SAT_EN = 1. See chapter “Saturation Flag (SAT)” regarding the possible diagnostics for this block.

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LINEARIZATION AND BINNING

The A31315 contains two different means of using the linearization parameters. These options are a segmented linearization and a discretized output option called binning mode. Each of these options allow for the use of up to 33 fixed points to quantize the angle output or the ability to apply the segment endpoints at configurable sensed angle locations.

See section “Saturation Flag (SAT)” regarding the possible diagnostics for this block.

LINEARIZATION / BINNING MODE SELECTION

The preferred mode is selected by the EEPROM parameter LIN_SEL, as shown in Table 5 and depicted in Figure 11.

Table 5: Linearization / binning mode selection

LIN_SEL Code	Output Transfer Function Option
0	Fixed Segment Linearization
1	Fixed Segment Binning Mode
2	Variable Segment Linearization Mode
3	Variable Segment Binning Mode

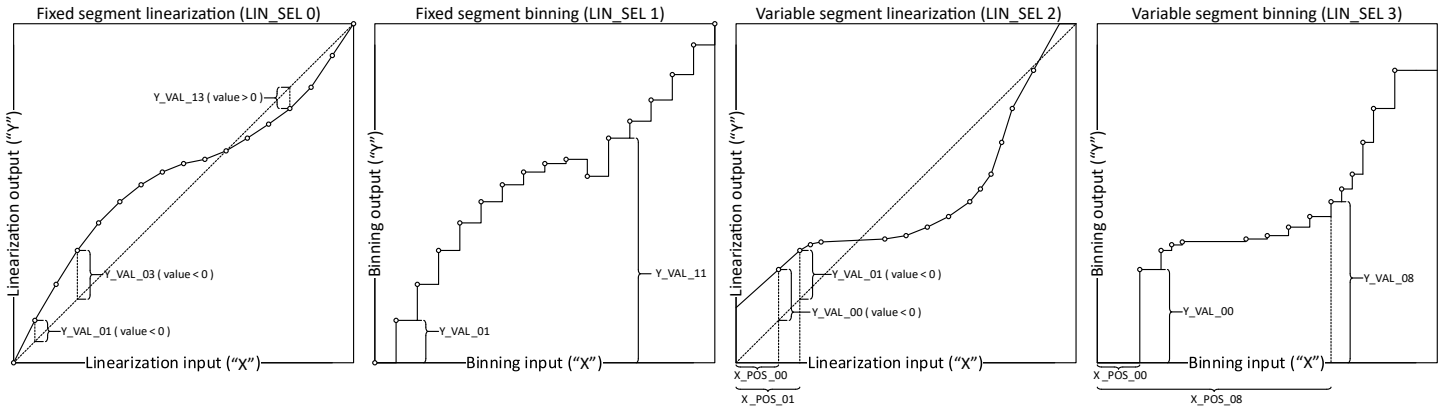

Figure 11: Linearization and Binning Modes

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FIXED SEGMENT LINEARIZATION (LIN_SEL 0)

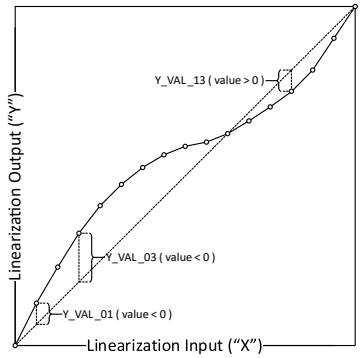

Figure 12: Fixed-Segment Linearization

In fixed-segment linearization mode, between 2 and 33 output correction points are equidistantly positioned between 0° and 360° input. The correction codes Y_VAL_XX are in signed 13-bit format and represent a correction using the format in the table below:

Table 6: Y_VAL_XX range depending on LIN_COEFF_SCALAR setting

LIN_COEFF_ SCALAR	Range (°)	Value for code –4096 (°)	Value for code +4095 (°)	Step size (°)
0	±45	+45	–44.99	$90/2^{13} \approx 0.011$
1	±90	+90	–89.98	$180/2^{13} \approx 0.022$
2	±180	+180	–179.96	$360/2^{13} \approx 0.044$
3	±360	+360	–359.91	$720/2^{13} \approx 0.088$

Most applications will have monotonically rising outputs. However, the sensor can support rising and falling outputs if needed.

If the result of the linearization is outside the 0-360° range, the value will be clipped to 0° or 360°. No overflow will happen in the linearization block. This means that for rotary applications, the 0° correction value and the 360° correction value must both be set to 0. Correction for 0- and 360-degree output values can be obtained with a combination of the offset and gain registers described in the previous section.

FIXED SEGMENT BINNING (LIN_SEL 1)

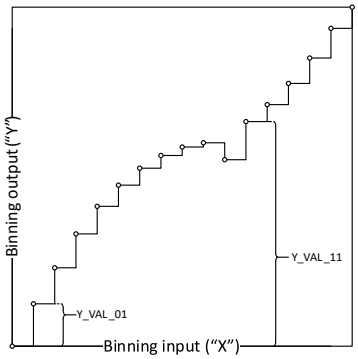

Figure 13: Fixed-Segment Binning

In fixed-segment binning mode, between 2 and 33 bins are equidistantly positioned between 0° and 360° input. The binning output codes Y_VAL_XX are in unsigned 13-bit format and represent an output value of 0° (Y_VAL_XX = 0) and 359.96° (Y_VAL_XX = 8191). Any value is mapped to the bin with a lower value than the input. The parameter LIN_COEFF_SCALAR has no meaning in binning mode. The Y_VAL_XX values do not need to be in any special order.

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VARIABLE SEGMENT LINEARIZATION (LIN_SEL 2)

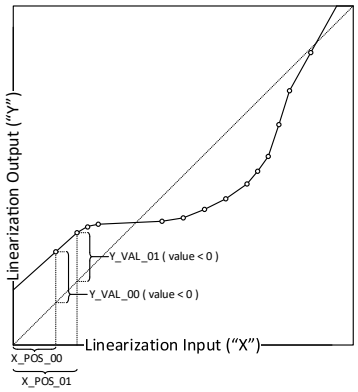

Figure 14: Variable Segment Linearization

In variable-segment linearization mode, between 2 and 22 output correction points are positioned at user-selected positions. The correction codes Y_VAL_XX are in signed 13-bit format and represent a correction using the format in the table below:

Table 7: Y_VAL_XX range depending on LIN_COEFF_SCALAR setting

LIN_COEFF_ SCALAR	Range (°)	Value for code –4096 (°)	Value for code +4095 (°)	Step size (°)
0	±45	+45	–44.99	$90/2^{13} \approx 0.011$
1	±90	+90	–89.98	$180/2^{13} \approx 0.022$
2	±180	+180	–179.96	$360/2^{13} \approx 0.044$
3	±360	+360	–359.91	$720/2^{13} \approx 0.088$

The position codes X_POS_XX are in unsigned 6-bit format and represent positions of 0° (X_POS_XX = 0) to 354.375° (X_POS_XX = 63). The X values must be placed in a rising manner, so that the value of X_POS(n+1) ≥ X_POS(n).

As with fixed segment linearization, if the result of the linearization is outside the 0-360° range, the value will be clipped to 0° or 360°. No overflow will happen in the linearization block. This means that for rotary applications, the 0° correction value and the 360° correction value must both be set to 0.

For input values below the angle defined by the X_POS_00 value, the linearization function will extrapolate the slope set by the first two defined points. For input angles above the angle defined by the last X_POS_XX value, the linearization function will extrapolate the slope set by the last two defined points. The extrapolating behavior is shown in Figure 14 for both low and high input values.

VARIABLE SEGMENT BINNING (LIN_SEL 3)

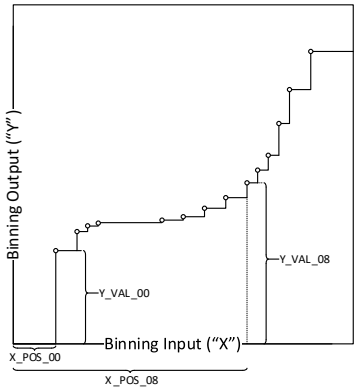

Figure 15: Variable Segment Binning

In variable-segment binning mode, between 2 and 21 bins are positioned at user-selected points between 0° and 360° input. The binning output codes Y_VAL_XX are in unsigned 13-bit format and represent an output value of 0° (Y_VAL_XX = 0) and 359.96° (Y_VAL_XX = 8191). Any value is mapped to the bin as an input angle below that of the input, i.e., the bin that the output ends up in is the bin whose X value is to the left of the measured angle. The parameter LIN_COEFF_SCALAR has no meaning in binning mode.

The position codes X_POS_XX are in unsigned 6-bit format and represent positions between 0° (X_POS_XX = 0) and 354.375° (X_POS_XX = 63). The X values must be placed in a rising manner, so that the value of X_POS_(n+1) ≥ X_POS_(n).

If X_POS_00 does not define a bin at position 0°, a bin with X_POS = 0°, Y_VAL = 0° will be automatically assumed.

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LINEARIZATION/BINNING PARAMETER STORAGE

The individual linearization/binning parameters are stored in the EEPROM parameters LIN_COEFF_00 … LIN_COEFF_32. Depending on the linearization/binning configuration, the contents of these memory locations have different meanings. All modes and EEPROM field contents are listed in Table 13. Parameters that are not used for linearization may be used otherwise. The parameters LIN_COEFF_17 … LIN_COEFF_31 can be sent out through the SENT enhanced serial message for certain constants (see Table 21). If they are used in this manner, the parameter COEFF_ACTIVE must be set in such a way that these two usages do not interfere (see Table 14).

Table 8: Linearization/Binning parameter storage

EEPROM Coefficient	Fixed position linearization (LIN_SEL 0)	Fixed position binning (LIN_SEL 1)	Variable segment linearization (LIN_SEL 2)	Variable segment binning (LIN_SEL 3)	SENT EMSG
	12 11 10 9 8 7 6 5 4 3 2 1 0	12 11 10 9 8 7 6 5 4 3 2 1 0	12 11 10 9 8 7 6 5 4 3 2 1 0	12 11 10 9 8 7 6 5 4 3 2 1 0	
LIN_COEFF_00	Y_VAL_00 (signed 13 bit)	Y_VAL_00 (unsigned 13 bit)	X_POS_01 (uns. 6 bit) X_POS_00 (uns. 6 bit)	X_POS_01 (uns. 6 bit) X_POS_00 (uns. 6 bit)	
LIN_COEFF_01	Y_VAL_01 (signed 13 bit)	Y_VAL_01 (unsigned 13 bit)	X_POS_03 (uns. 6 bit) X_POS_02 (uns. 6 bit)	X_POS_03 (uns. 6 bit) X_POS_02 (uns. 6 bit)	
LIN_COEFF_02	Y_VAL_02 (signed 13 bit)	Y_VAL_02 (unsigned 13 bit)	X_POS_05 (uns. 6 bit) X_POS_04 (uns. 6 bit)	X_POS_05 (uns. 6 bit) X_POS_04 (uns. 6 bit)	
LIN_COEFF_03	Y_VAL_03 (signed 13 bit)	Y_VAL_03 (unsigned 13 bit)	X_POS_07 (uns. 6 bit) X_POS_06 (uns. 6 bit)	X_POS_07 (uns. 6 bit) X_POS_06 (uns. 6 bit)	
LIN_COEFF_04	Y_VAL_04 (signed 13 bit)	Y_VAL_04 (unsigned 13 bit)	X_POS_09 (uns. 6 bit) X_POS_08 (uns. 6 bit)	X_POS_09 (uns. 6 bit) X_POS_08 (uns. 6 bit)	
LIN_COEFF_05	Y_VAL_05 (signed 13 bit)	Y_VAL_05 (unsigned 13 bit)	X_POS_11 (uns. 6 bit) X_POS_10 (uns. 6 bit)	X_POS_11 (uns. 6 bit) X_POS_10 (uns. 6 bit)	
LIN_COEFF_06	Y_VAL_06 (signed 13 bit)	Y_VAL_06 (unsigned 13 bit)	X_POS_13 (uns. 6 bit) X_POS_12 (uns. 6 bit)	X_POS_13 (uns. 6 bit) X_POS_12 (uns. 6 bit)	
LIN_COEFF_07	Y_VAL_07 (signed 13 bit)	Y_VAL_07 (unsigned 13 bit)	X_POS_15 (uns. 6 bit) X_POS_14 (uns. 6 bit)	X_POS_15 (uns. 6 bit) X_POS_14 (uns. 6 bit)	
LIN_COEFF_08	Y_VAL_08 (signed 13 bit)	Y_VAL_08 (unsigned 13 bit)	X_POS_17 (uns. 6 bit) X_POS_16 (uns. 6 bit)	X_POS_17 (uns. 6 bit) X_POS_16 (uns. 6 bit)	
LIN_COEFF_09	Y_VAL_09 (signed 13 bit)	Y_VAL_09 (unsigned 13 bit)	X_POS_19 (uns. 6 bit) X_POS_18 (uns. 6 bit)	X_POS_19 (uns. 6 bit) X_POS_18 (uns. 6 bit)	
LIN_COEFF_10	Y_VAL_10 (signed 13 bit)	Y_VAL_10 (unsigned 13 bit)	X_POS_21 (uns. 6 bit) X_POS_20 (uns. 6 bit)	X_POS_20 (uns. 6 bit)	
LIN_COEFF_11	Y_VAL_11 (signed 13 bit)	Y_VAL_11 (unsigned 13 bit)	Y_VAL_00 (signed 13 bit)	Y_VAL_00 (unsigned 13 bit)	
LIN_COEFF_12	Y_VAL_12 (signed 13 bit)	Y_VAL_12 (unsigned 13 bit)	Y_VAL_01 (signed 13 bit)	Y_VAL_01 (unsigned 13 bit)	
LIN_COEFF_13	Y_VAL_13 (signed 13 bit)	Y_VAL_13 (unsigned 13 bit)	Y_VAL_02 (signed 13 bit)	Y_VAL_02 (unsigned 13 bit)	
LIN_COEFF_14	Y_VAL_14 (signed 13 bit)	Y_VAL_14 (unsigned 13 bit)	Y_VAL_03 (signed 13 bit)	Y_VAL_03 (unsigned 13 bit)	
LIN_COEFF_15	Y_VAL_15 (signed 13 bit)	Y_VAL_15 (unsigned 13 bit)	Y_VAL_04 (signed 13 bit)	Y_VAL_04 (unsigned 13 bit)	
LIN_COEFF_16	Y_VAL_16 (signed 13 bit)	Y_VAL_16 (unsigned 13 bit)	Y_VAL_05 (signed 13 bit)	Y_VAL_05 (unsigned 13 bit)	
LIN_COEFF_17	Y_VAL_17 (signed 13 bit)	Y_VAL_17 (unsigned 13 bit)	Y_VAL_06 (signed 13 bit)	Y_VAL_06 (unsigned 13 bit)	$03
LIN_COEFF_18	Y_VAL_18 (signed 13 bit)	Y_VAL_18 (unsigned 13 bit)	Y_VAL_07 (signed 13 bit)	Y_VAL_07 (unsigned 13 bit)	$05
LIN_COEFF_19	Y_VAL_19 (signed 13 bit)	Y_VAL_19 (unsigned 13 bit)	Y_VAL_08 (signed 13 bit)	Y_VAL_08 (unsigned 13 bit)	$06
LIN_COEFF_20	Y_VAL_20 (signed 13 bit)	Y_VAL_20 (unsigned 13 bit)	Y_VAL_09 (signed 13 bit)	Y_VAL_09 (unsigned 13 bit)	$07
LIN_COEFF_21	Y_VAL_21 (signed 13 bit)	Y_VAL_21 (unsigned 13 bit)	Y_VAL_10 (signed 13 bit)	Y_VAL_10 (unsigned 13 bit)	$08
LIN_COEFF_22	Y_VAL_22 (signed 13 bit)	Y_VAL_22 (unsigned 13 bit)	Y_VAL_11 (signed 13 bit)	Y_VAL_11 (unsigned 13 bit)	$09
LIN_COEFF_23	Y_VAL_23 (signed 13 bit)	Y_VAL_23 (unsigned 13 bit)	Y_VAL_12 (signed 13 bit)	Y_VAL_12 (unsigned 13 bit)	$0A
LIN_COEFF_24	Y_VAL_24 (signed 13 bit)	Y_VAL_24 (unsigned 13 bit)	Y_VAL_13 (signed 13 bit)	Y_VAL_13 (unsigned 13 bit)	$90
LIN_COEFF_25	Y_VAL_25 (signed 13 bit)	Y_VAL_25 (unsigned 13 bit)	Y_VAL_14 (signed 13 bit)	Y_VAL_14 (unsigned 13 bit)	$91
LIN_COEFF_26	Y_VAL_26 (signed 13 bit)	Y_VAL_26 (unsigned 13 bit)	Y_VAL_15 (signed 13 bit)	Y_VAL_15 (unsigned 13 bit)	$92
LIN_COEFF_27	Y_VAL_27 (signed 13 bit)	Y_VAL_27 (unsigned 13 bit)	Y_VAL_16 (signed 13 bit)	Y_VAL_16 (unsigned 13 bit)	$93
LIN_COEFF_28	Y_VAL_28 (signed 13 bit)	Y_VAL_28 (unsigned 13 bit)	Y_VAL_17 (signed 13 bit)	Y_VAL_17 (unsigned 13 bit)	$94
LIN_COEFF_29	Y_VAL_29 (signed 13 bit)	Y_VAL_29 (unsigned 13 bit)	Y_VAL_18 (signed 13 bit)	Y_VAL_18 (unsigned 13 bit)	$95
LIN_COEFF_30	Y_VAL_30 (signed 13 bit)	Y_VAL_30 (unsigned 13 bit)	Y_VAL_19 (signed 13 bit)	Y_VAL_19 (unsigned 13 bit)	$96
LIN_COEFF_31	Y_VAL_31 (signed 13 bit)	Y_VAL_31 (unsigned 13 bit)	Y_VAL_20 (signed 13 bit)	Y_VAL_20 (unsigned 13 bit)	$97
LIN_COEFF_32	Y_VAL_32 (signed 13 bit)	Y_VAL_32 (unsigned 13 bit)	Y_VAL_21 (signed 13 bit)		

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NUMBER OF LINEARIZATION / BINNING POINTS

All modes have a configurable number of activated linearization/ binning points. The number of active points is selected with the parameter LIN_COEFF_ACTIVE:

Table 9: Linearization / binning mode parameters used depending on coeff_active

LIN_COEFF_ ACTIVE	Number of Active Coefficients			
	LIN_SEL 0 fixed segment linearization	LIN_SEL 1 fixed segment binning	LIN_SEL 2 variable segment linearization	LIN_SEL 3 variable segment binning
0	33	32	2	1 [1]
1	17	16	2	2 [2]
2	9	8	3	3 [2]
3	5	4	4	4 [2]
4	3	2	5	5 [2]
5	2	1 [1]	6	6 [2]
6	2	1 [1]	7	7 [2]
7	2	1 [1]	8	8 [2]
8	2	1 [1]	9	9 [2]
9	2	1 [1]	10	10 [2]
10	2	1 [1]	11	11 [2]
11	2	1 [1]	12	12 [2]
12	2	1 [1]	13	13 [2]
13	2	1 [1]	14	14 [2]
14	2	1 [1]	15	15 [2]
15	2	1 [1]	16	16 [2]
16	2	1 [1]	17	17 [2]
17	2	1 [1]	18	18 [2]
18	2	1 [1]	19	19 [2]
19	2	1 [1]	20	20 [2]
20	2	1 [1]	21	21 [2]
21...31	2	1 [1]	22	21 [2]

[1] Single coefficient settings for binning mode serve no practical purpose. The output will always be equal to the set value.
[2] In LIN_SEL = 3, if X_POS_00 does not define a bin at position 0°, a bin with X_POS = 0°, Y_VAL = 0° will be automatically assumed.

BINNING MODE HYSTERESIS

To prevent chattering around the transition threshold between the bins, the A31315 contains internal hysteresis control in binning mode. The BIN_HYST parameter will establish the hysteresis in codes below the threshold, which the input into the binning block must pass before changing to the lower bin. This prevents expected noise and drift from changing the desired output bin for the designated output range. The binning hysteresis is controlled using the parameter BIN_HYST. The default value of BIN_HYST = 0 results in no hysteresis being applied.

The range for BIN_HYST is [0… 11.162109375]° with a step size of 11.25° / 2^7 = 0.087890625°.

Output Clamps

The A31315 contains a digital clamp feature that can clamp the digital output range of the device. These high and low clamps are both programmable to the entire output range of the device. If the input to the clamp block exceeds the upper clamp value, the output is set to the upper clamp value. Similarly, if the input to the clamp block is less than the lower clamp value, the output is set to the lower clamp value.

If high and low clamp value are equal, the output will equal the clamp value. This can be practical for testing purposes.

If the low clamp value is set to a higher value than the high clamp value, the output will equal the low clamp number—this configuration has no practical use.

Equation 18:

$$A_6 = \max(\text{ANG_CLAMP_LOWER}, \min(\text{ANG_CLAMP_UPPER}, A_5))$$

The range for ANG_CLAMP_UPPER is [0 … 65535] LSB with a step size of 1 LSB.

The range for ANG_CLAMP_LOWER is [0 … 65535] LSB with a step size of 1 LSB.

There is an error flag associated with this setting, which asserts when the angle is outside of the clamp range. By default, this flag is masked to allow the clamps to function properly, but if desired this mask can be cleared to use the clamps to set an internal error when the angle exceeds the clamp range.

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OUTPUT PROTOCOLS

Analog Output Mode

The A31315 features an analog output, proportional to the digital angle. Angles are mapped between a minimum and maximum output voltage which can be configured by the EEPROM parameter ANA_RANGE_SEL. The output voltage will increase linearly between the min/max settings when a linearly increasing magnetic angle is detected. Voltage values beyond the upper or lower limits represent diagnostic regions. Output voltages within these two regions will only occur if the device detects an abnormal operating condition or internal error (any unmasked error conditions). These diagnostic regions are entered by the device going into a high-impedance state, defined high state, or defined low state. If the device goes into high-impedance state, the output must be pulled to a rail by an external pull-up or pull-down resistor in order to be detectable.

PWM Output Mode

PWM involves converting the output value to a series of constant-frequency binary pulses, with the percentage of the high portion of the pulse varied in direct proportion to the digital angle.

The PWM output mode (DIG_OUT_SEL = 0) is configured by setting the carrier frequency and diagnostic reporting options in EEPROM. The slew rate of the edges may be adjusted using the EEPROM parameter DIG_OUT_PULL_LIM and DIG_OUT_DRIVE_SEL. See Digital output pin drive strength options for more information.

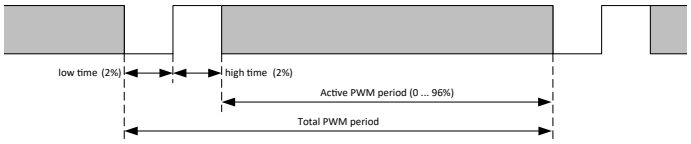

Figure 16: PWM Frame Format

Table 10: PWM Carrier Frequency, EEPROM Parameter DIG_OUT_DATA_RATE

EEPROM Code	PWM Frequency (Hz)	Output Resolution (bit)
0 or 16 (X0000)	125	15
1 or 17 (X0001)	167	15
2 or 18 (X0010)	250	14
3 or 19 (X0011)	333	14
4 or 20 (X0100)	500	13
5 or 21 (X0101)	667	13
6 or 22 (X0110)	800	13
7 or 23 (X0111)	1000	12
8 or 24 (X1000)	1333	12
9 or 25 (X1001)	1600	12
10 or 26 (X1010)	2000	11
11 or 27 (X1011)	2667	11
12 or 28 (X1100)	4000	10
13 or 29 (X1101)	5333	10
14 or 30 (X1110)	8000	9
15 or 31 (X1111)	16000	8

PWM Sampling Time

The data for the PWM output is sampled at the beginning of each frame, as shown in Figure 17. In the figure, Data 0, 1, 3, 5, 7 and 8 are transmitted. Data 2, 4, 6 and 9 are discarded.

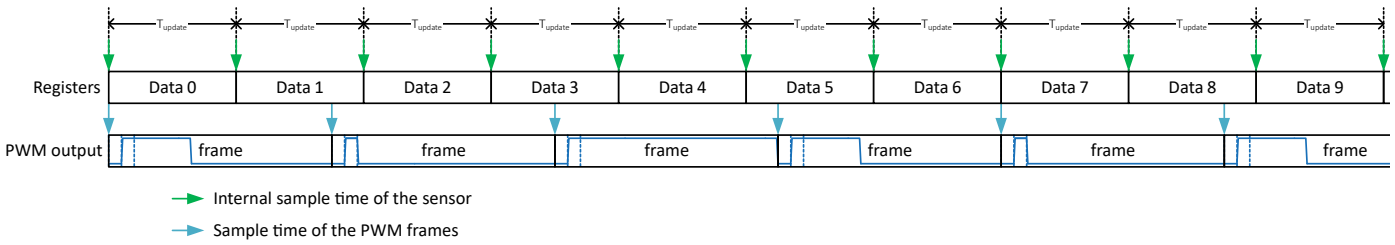

Figure 17: PWM Frame Sampling Timing

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SENT Output Mode

The single-edge nibble transmission (SENT) output mode converts the calculated angle to a binary value mapped to the full-scale output (FSO) range of 0 to 4095, as shown in Figure 18 (for a 12-bit output). This data is inserted into a binary pulse message, referred to as a frame that conforms to the SENT data transmission specification (SAE J2716 APRIL2016). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output mode is configured by setting the following parameters in EEPROM:

- SAE J2716 SENT with enhancement options (DIG_OUT_SEL = 1 (no pause pulse), DIG_OUT_SEL = 2 (pause pulse)).
- Additional configuration parameters in EEPROM.

Message Structure

A SENT message is a series of nibbles. Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval. The low interval is defined as 5 SENT ticks. The high interval contains information and is variable in duration to indicate the data payload of the nibble. The duration of a nibble is denominated in ticks. The period of a tick is set by the DIG_OUT_DATA_RATE parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval. The slew rate of the falling edge may be adjusted using the EEPROM parameter DIG_OUT_PULL_LIM.

The nibbles of a SENT message are arranged in the following required sequence (see Figure 18):

1. Synchronization and Calibration: flags the start of the SENT message.
2. Status and Communication: provides A31315 status.
3. Data: output angle and optional data.
4. CRC (Cyclical Redundancy Check): error checking.
5. Pause Pulse: sets timing relative to a constant message frame length. See chapter SENT output rate for the settings.

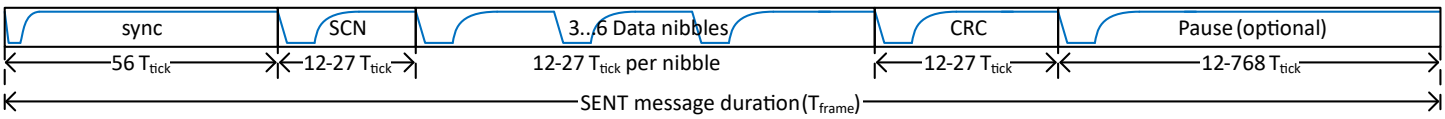

Figure 18: General Format for SENT message

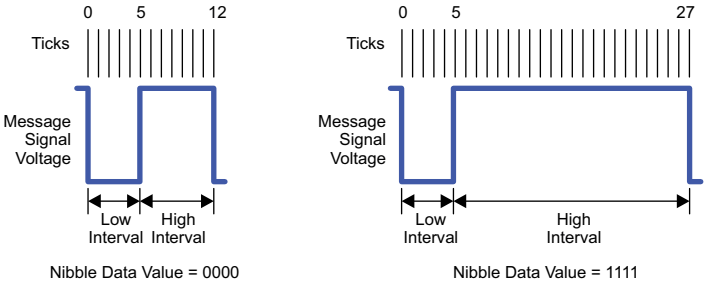

Figure 19: General SENT Nibble Composition

Table 11: SENT Nibble composition and value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0010	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

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SENT Sampling Time

The SENT output data are sampled 33 ticks prior to the start of the SCN nibble. If beginning a new serial message, it is also composed at this time. This is detailed in Figure 20. In the figure, Data 1 and Data 5 are sent out. Others are discarded.

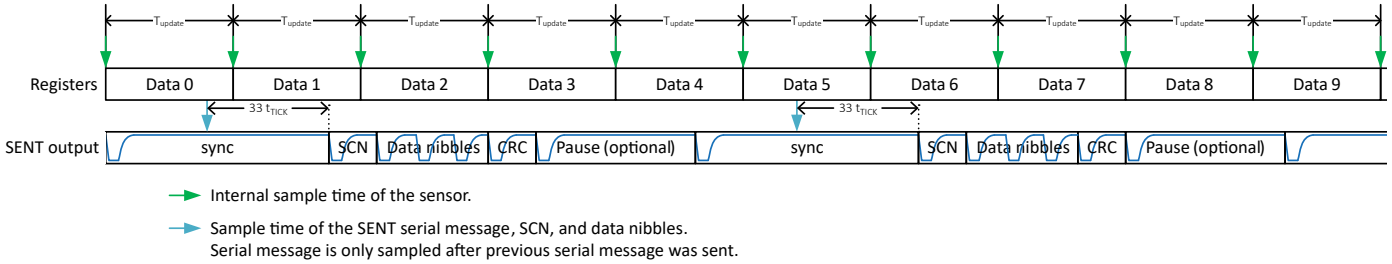

Figure 20: SENT Frame Sample Timing

SENT Output Rate

The SENT output rate depends on the SENT mode. In regular SENT, the frame length is defined by the frame contents. Using SENT-Pause, the frame length is constant. The length of the frames can be selected. There are four options for the frame length settings. Using SENT_FRAME_RATE = 0, the shortest possible pause-pulse that can achieve a fixed frame duration is used, with the calculation shown in the table below. Using the options SENT_FRAME_RATE = 1, 2, or 3, a fixed frame rate, measured in milliseconds rather than ticks, can be selected. Settings are detailed in Table 12.

Table 12: SENT frame duration, depending on SENT_FRAME_RATE

SENT_FRAME_RATE	Frame rate including pause pulse
0	3 data nibbles: frame length 210 t_{tick} 4 data nibbles: frame length 228 t_{tick} 6 data nibbles: frame length 282 t_{tick}
1	0.5 ms
2	1.0 ms
3	2.0 ms

The output behavior for correct frame rate configurations can be seen in Figure 21 below:

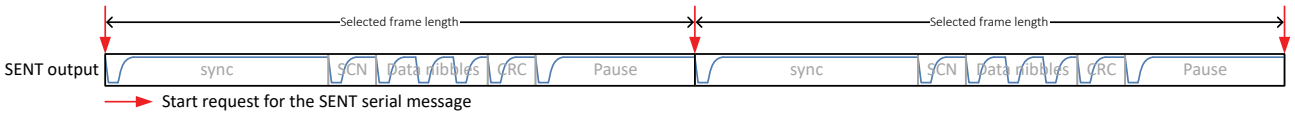

Figure 21: SENT frame start depending on selected frame rate

If the frame rate is configured to be so high that a message is not finished before the intended start of the next one, the start request is discarded. Such a setting is show in Figure 22. This setup is not recommended, as it provides less consistent updates that may vary based on message contents.

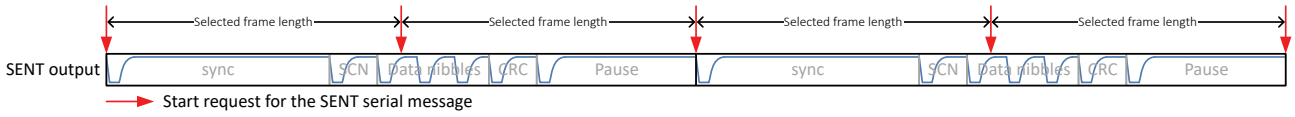

Figure 22: SENT frame start depending on selected frame rate, with SENT_FRAME_RATE defining a too fast frame rate setting

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Optional SENT Slow Serial Output Protocol

SENT output supports an optional mode to transmit additional data. The slow serial mode enables transmission of additional data by encoding information in the Status and Communication (SCN) nibbles. The encoded data is captured over several transmissions and is then decoded to indicate additional serial message data. For more details on the serial message, refer to the SENT SAE J2716 APRIL2016 specification.

The slow serial mode is enabled when the EEPROM parameter SENT_EMSG_DIS = 0. Following a reset, the first message transmitted is 0, following in order of the message ID until message 7, and then repeating. Table 13 and Table 14 identify the data sent with each message ID. The CRC for the Serial Message is derived from the Message ID and data.

Table 13: SCN [3:2] Configuration Control

SENT_EMSG_DIS	SCN Nibble bits [3:2] Contents
0	Serial Message
1	All Zeros

The data in the serial message follows the table below:

Table 14: Serial Message Format in SENT Status and Communication Nibble

received SCN nibble #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SCN[3]	1	1	1	1	1	1	0	0	8-bit ID[7:4]				0	8-bit ID[3:0]				0
SCN[2]	6-bit CRC						12-bit data field											

There are a number of codes available to be sent out in serial mode.

Some codes are based on sensor data, such as the following:

$01: Error and Status Codes

$23: Supplementary data channel #4,1 (Temperature data)

Other codes only send out constants, such as:

$03: Channel 1 / 2 Sensor type

$05: Manufacturer code

$06: Protocol standard revision

$07-0A: Fast Channel 1 Characteristic X1, X2, Y1, Y2

$29~2C: Sensor ID #1~4

$90~97: ASCII character OEM codes MESSAGE ID

Due to EEPROM sharing, the constant values are not compatible with all Linearization modes. The constant values are factory-programmed to EEPROM locations that are shared with for LIN_COEFF_17 through LIN_COEFF_31. If using linearization in parallel with these constants, only LIN_COEFF_00 through LIN_COEFF_16 should be used. This means fixed position linearization and binning can be used with up to 17 points, and variable segment linearization and binning can be used with up to 6 points. See Table 8 for reference. For selecting how many coefficients are used, see Table 9 for the desired COEFF_ACTIVE setting.

If the LIN_COEFF_XX value that is assigned to a constant is changed, the new value will be output instead of the desired constant. For that reason, it is important to take caution when programming linearization coefficients, to ensure desired constant values are not overwritten.

Each message can be activated or deactivated using the SENT_EMSG_SEL EEPROM bits. In this way, if the first constant(s) is(are) not required, their corresponding LIN_COEFF_XX value(s) can be used for linearization. The lowest $xx value used determines how many extra linearization coefficients can be used. If $03 is used, even if no other constants are reported, only 17 or 6 coefficients can be used for fixed or movable point respectively (e.g., if constant $03 and $05 are not reported, up to 19 fixed point coefficients or 8 movable point coefficients can be used).

Using the EEPROM setting SENT_EMSG_ERR_REPEAT = 1, the message-ID $01 is repeated between any other messages. That means that if messages $01, $07, $08, $09, $0A are activated, transmission will be $01-$07-$01-$08-$01-$09-$01-$0A-$01-$07-$01-$08-….

The tables below give the serial output message numbers, the enable bits, the data source, and the byte contents.

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Table 15: SENT Serial Output Message ID Contents for data registers

SENT serial message ID	Enable	Data source	Contents
$01	SENT_EMSG_SEL[0]	error register 0xA3[11:0]	Error and Status Codes
$23	SENT_EMSG_SEL[1]	TEMPERATURE_16B[15:4]	Supplementary data channel #4,1 (Temperature data)

Table 16: SENT Serial Output Message ID Contents for constants

SENT serial message ID	Enable	Data source	Contents
$03	SENT_EMSG_SEL[2]	LIN_COEFF_17[11:0]	Channel 1 / 2 Sensor type
$05	SENT_EMSG_SEL[3]	LIN_COEFF_18[11:0]	Manufacturer code
$06	SENT_EMSG_SEL[4]	LIN_COEFF_19[11:0]	Protocol standard revision
$07	SENT_EMSG_SEL[5]	LIN_COEFF_20[11:0]	Fast Channel 1 Characteristic X1
$08	SENT_EMSG_SEL[6]	LIN_COEFF_21[11:0]	Fast Channel 1 Characteristic X2
$09	SENT_EMSG_SEL[7]	LIN_COEFF_22[11:0]	Fast Channel 1 Characteristic Y1
$0A	SENT_EMSG_SEL[8]	LIN_COEFF_23[11:0]	Fast Channel 1 Characteristic Y2
$29	SENT_EMSG_SEL[9]	0x0 & WAFER_ID[15:8]	Sensor ID #1
$2A	SENT_EMSG_SEL[10]	0x0 & WAFER_ID[7:0]	Sensor ID #2
$2B	SENT_EMSG_SEL[11]	0x0 & WAFER_YPOS[7:0]	Sensor ID #3
$2C	SENT_EMSG_SEL[12]	0x0 & WAFER_XPOS[7:0]	Sensor ID #4
$90	SENT_EMSG_SEL[13]	LIN_COEFF_24[11:0]	ASCII character OEM codes [1]
$91	SENT_EMSG_SEL[14]	LIN_COEFF_25[11:0]	ASCII character OEM codes [1]
$92	SENT_EMSG_SEL[15]	LIN_COEFF_26[11:0]	ASCII character OEM codes [1]
$93	SENT_EMSG_SEL[16]	LIN_COEFF_27[11:0]	ASCII character OEM codes [1]
$94	SENT_EMSG_SEL[17]	LIN_COEFF_28[11:0]	ASCII character OEM codes [1]
$95	SENT_EMSG_SEL[18]	LIN_COEFF_29[11:0]	ASCII character OEM codes [1]
$96	SENT_EMSG_SEL[19]	LIN_COEFF_30[11:0]	ASCII character OEM codes [1]
$97	SENT_EMSG_SEL[20]	LIN_COEFF_31[11:0]	ASCII character OEM codes [1]

[1] Can be used to send two 6-bit ASCII characters in representation according to SAE J2716, APR2016, Table D.9-1.

Data Nibble Format

When transmitting normal operation data, information about the measurement data is embedded in the first three or four data nibbles. Each data nibble consists of 4 bits with values ranging from 0 to 15. In order to present an output with the resolution of 12 or 16 bits, 3 or 4 data nibbles are required. The data nibble containing the MSB of the whole data section is sent first.

Three additional optional data nibbles can be associated with other parameters, by setting the EEPROM parameter: SENT_DATA_SEL as shown in Table 17.

- Counter – Each message frame has a serial number in each Counter nibble.
- Temperature – Temperature data from the A31315 internal temperature sensor.
- Diagnostics – Diagnostic flags can be sent as described in Table 34.
- Inverted nibble 1 – Nibble 1 contents (Data MSB) can be sent in one's complement.

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SENT CRC

The SENT message contains a 4-bit CRC for data validity checks. The CRC polynomial is shown in Equation 18 with an initial seed of 0x5. By default, the CRC only includes the data nibbles of the SENT message with the Synchronization and SCN nibbles being ignored. With the EEPROM parameter SENT_CRC_SEL = 1, the SCN nibble will be included in the CRC calculation.

Equation 19:

$$g(x) = x^4 + x^3 + x^2 + 1$$

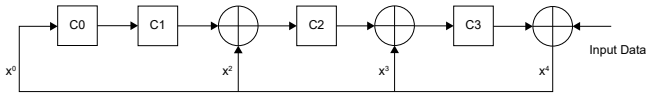

Figure 23: SENT CRC Calculation

SENT Serial Message 6-Bit CRC

The SENT serial message contains a 6-bit CRC, based on the polynomial $x^6 + x^4 + x^3 + 1$.

The CRC checksum can be implemented via a bitwise exclusive OR with a 64-array lookup. The checksum is determined by reading 6-bit groups of the 24-bit message data in sequence, and then calculating the checksum with an extra zero value (augmentation by six 0-bits).

Table 17: SENT Options Bit Contents EEPROM Parameter: SENT_DATA_SEL

SENT Frame	SENT_DATA_SEL	Nibble 1				Nibble 2				Nibble 3				Nibble 4				Nibble 5				Nibble 6			
		3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
H2	0	12 Bit Angle [11:0] [1]												Not Used											
	1	12 Bit Angle [11:0]												8-bit Temperature								4-Bit Message Counter			
	2	12 Bit Angle [11:0]												8-bit DIAG_BYTE (See Table 34)								4-Bit Message Counter			
	3	12 Bit Angle [11:0]												12-Bit Message Counter											
H4	4	12 Bit Angle [11:0] [1]												8-bit Message Counter								Inverted Nibble 1			
	5	12 Bit Angle [11:0]												Ones Complement 12 Bit Angle ~[11:0]											
	6	16-Bit Angle [15:0]																Not Used							
H7	7	16-Bit Angle [15:0] [1]																8-bit Temp[3:0] [1]				8-bit Temp[7:4] [1]			
	8	16-Bit Angle [15:0]																8-bit DIAG_BYTE (See Table 34)							
	9	16-Bit Angle [15:0]																8-bit Message Counter							
	10	12-bit Channel A data												12-bit Channel B data											
	11	ChA	ChB	14-bit Channel A, Channel B (rotates each message)														Not Used							
	12	ChA	ChB	14-bit Channel A, Channel B (rotates each message)														8-bit Temperature							
	13	ChA	ChB	14-bit Channel A, Channel B (rotates each message)														8-bit DIAG_BYTE (See Table 34)							
	14	ChA	ChB	14-bit Channel A, Channel B (rotates each message)														8-Bit Message Counter							
H1	15	12-Bit Angle [11:0] [1]												12-Bit Temp[3:0] [1]				12-Bit Temp[7:4] [1]				12-Bit Temp[11:8] [1]			

[1] This value is subject to modification as per Table 20 based on setting SENT_ENCODING_SEL.

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Table 18: SENT Tick Times, EEPROM Parameter DIG_OUT_DATA_RATE

EEPROM Code	SENT Tick Time (µs)
0 (00000)	3
1 (00001)	0.25
2 (00010)	0.375
3 (00011)	0.5
4 (00100)	0.625
5 (00101)	0.75
6 (00110)	0.875
7 (00111)	1.0
8 (01000)	1.125
9 (01001)	1.25
10 (01010)	1.375
11 (01011)	1.5
12 (01100)	1.625
13 (01101)	1.75
14 (01110)	1.875
15 (01111)	2.0
16 (10000)	2.125
17 (10001)	2.25
18 (10010)	2.375
19 (10011)	2.5
20 (10100)	2.625
21 (10101)	2.75
22(10110)	2.875
23 (10111)	3.0
24 (11000)	3.5
25 (11001)	4.0
26 (11010)	4.5
27 (11011)	5.0
28 (11100)	5.5
29 (11101)	6.0
30 (11110)	7.0
31 (11111)	10.0

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Table 19: SENT Message Frame Definitions

Section	Description
Synchronization and Calibration	
Function	Provide the external controller with a detectable start of the message frame. The large quantity of ticks distinguishes this section for ease of distinction by the external controller.
Syntax	Nibbles: 1 Quantity of ticks: 56 Quantity of bits: 1
Status and Communication	
Function	Provides the external controller with the status of the A31315 and indicates the format and contents of the Data section.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 Quantity of bits: 4 1:0 Device status 3:2 Message serial data protocol
Data	
Function	Provides the external controller with data selected by the SENT_DATA_SEL parameter.
Syntax	Nibbles: 3 to 6 Quantity of ticks: 12 to 27 (each nibble) Quantity of bits: 4 (each nibble)
CRC	
Function	Provides the external controller with cyclic redundancy check (CRC) data for certain error detection routines applied to the Data nibbles to the status information.
Syntax	Nibbles: 1 Quantity of ticks: 12 to 27 Quantity of bits: 4
Pause Pulse	
Function	Additional time can be added at the end of a SENT message frame to ensure all message frames are of appropriate length and correlate to the internal update rate of the device.
Syntax	Nibbles: N/A Quantity of ticks: Varies Quantity of bits: N/A.

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Error Indicators / Specific Messages / Initialization Message in SENT Output Codes

If SENT_DATA_SEL is set to code 0, 4, 7, or 15, it is possible to output specific status information to the SENT data code by EEPROM setting SENT_ENCODING_SEL.

Table 20: SENT error indicators / initialization message, if SENT_ENCODING_SEL = 1 and (SENT_DATA_SEL = 0, 4 , 7 or 15)

n-bit Data Value	12-bit data value	SENT definition	Sensor mapping
Output is High Impedance, or High, or Low, depending on ERR_RESP_SEL			Sensor is in UVD mode (undervoltage detected)
Selectable (see SENT Initialization code selection)	Selectable (see SENT Initialization code selection)	Initialization	Sensor is not in UVD mode, AND Sensor is initializing, no final data available yet
2^n–5	4091	Sensor error indication	Sensor is not in UVD mode, AND Sensor is not initializing, AND any of the errors (UVD | OVD | SAT | AOC) are set
2^n–6	4090	Sensor functionality and processing error indication	Sensor is not in UVD mode, AND Sensor is not initializing, AND none of (OVD | SAT | AOC) are set, AND any of the errors (SLF | SRR | ACF | TSE | POR) are set

SAE J2716 SENT

When DIG_OUT_SEL = 1 the device is configured in free running SENT mode, the SENT output transmits continuously while in normal operating conditions with no extended pause pulse. When DIG_OUT_SEL = 2, the SENT message frame rate is extended with a variable length pause pulse to ensure a constant output rate. The pause pulse is limited to 768 tick times as defined by the SAE J2716 APRIL2016 SENT standard.

SENT Initialization Code Selection

According to the SAE J2716, the output for initialization status must be 0. However, the A31315 permits the user to select other messages instead. The parameter sent_init_sel controls what code is transmitted for initialization, if SENT_ENCODING_SEL = 1 and SENT_DATA_SEL is set to code 0, 4, 7, or 15. This selection does not affect the message counter information, which will always increment each message.

Table 21: SENT initialization code mapping selection when SENT_ENCODING_SEL = 1

SENT_INIT_SEL	n-bit Data Output for Initialization	8-Bit Data Output for Initialization	12-Bit Data Output for Initialization	16-Bit Data Output for Initialization
0	0	0	0	0
1	$2^n - 7$	249	4089	65529
2	$2^n - 4$	252	4092	65532
3	$2^n - 3$	253	4093	65533
4	$2^n - 2$	254	4094	65534
5	$2^n - 1$	255	4095	65535
6	0	0	0	0
7	0	0	0	0

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Digital Output Pin Drive Strength Options

The SENT and PWM output allow configuring the output pin drive strength. This can be done in open-drain and in push-pull mode.

OUTPUT PIN FALL TIME SELECTION

The A31315 allows the user to change the fall time of the open-drain output digital SENT or PWM signal using the EEPROM parameter DIG_OUT_PULL_LIM. This control is viewed as a discrete gradient from Faster to Slower with intermediate steps to provide desired pulse shaping to improve EMC emissions performance. The resulting fall time is heavily dependent on load capacitance. As reference, fall times for certain capacitance values are shown in Table 22.

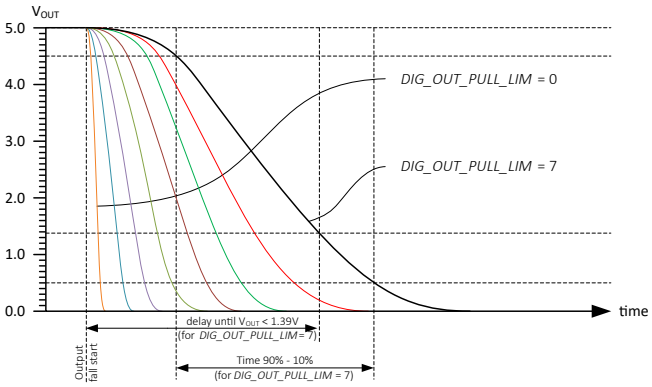

Figure 24: Definition of output fall times and output delay (exemplary plot)

Table 22: Output fall time depending on load capacitor and DIG_OUT_PULL_LIM, with DIG_OUT_DRIVE_SEL = 1

DIG_OUT_PULL_LIM	Time 90% to 10% (µs)	
	Pullup R_L = 5 kΩ	
	C_{load} = 100 pF	C_{load} = 1 nF
0	0.13	0.3
1	0.26	0.44
2	0.39	0.6
3	0.51	0.74
4	1.04	1.35
5	1.82	2.17
6	3.44	3.78
7	5.08	5.32

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PUSH-PULL OUTPUT SETTING FOR SENT AND PWM RISING EDGE

In order to decrease the rise time for digital outputs, it is possible to enable a push-pull output. This is done by setting DIG_OUT_DRIVE_SEL = 0. In such a configuration, a pull-up resistor is not necessary. In this case, a pull-up or pull-down resistor is still recommended as to provide a known voltage state in the event of a broken output line. The table below shows the digital output rise times, depending on the capacitive load. The parameter DIG_OUT_PUSH_LIM determines the push drive strength.

Table 23: Output rise time depending on load capacitor if DIG_OUT_DRIVE_SEL = 0

DIG_OUT_PUSH_LIM	Time 10% to 90% (µs)	
	Pullup R_L = 5 kΩ	
	C_{load} = 100 pF	C_{load} = 1 nF
DIG_OUT_PUSH_LIM_DIS = 1	0.38	0.67
0	0.78	1.45
1	0.82	1.58
2	0.91	1.78
3	1.03	2.06
4	1.17	2.45
5	1.27	3.08
6	1.31	4.21
7	1.32	6.90

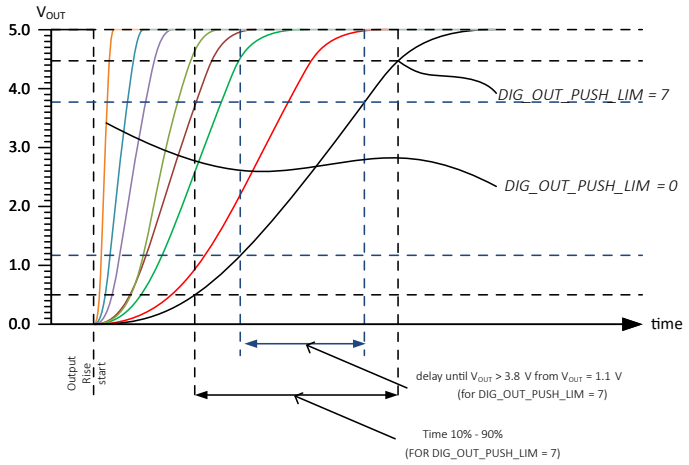

Figure 25: Definition of output rise times and output delay (exemplary plot)

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PROGRAMMING PROTOCOL

The A31315 device generally uses a 3-wire programming interface where V_{CC} can control the program enable signal, data is transmitted on the output pin, and all signals are referenced to ground. This 3-wire interface makes it possible to use multiple devices with shared V_{CC} and ground lines. If V_{CC} can be controlled by the host, this is the preferred method of communication. If V_{CC} cannot be controlled by the host, initiating Manchester communication can be done through the output pin as well. See Physical Layer section for more information.

When performing a write to EEPROM transaction, the A31315 requires a delay of t_w to store the data into the EEPROM. The device will respond with a low-to-high transition on the output pin to indicate the write to EEPROM sequence is complete.

Physical Layer

The serial interface allows an external controller to read and write registers, including EEPROM, in the A31315 using a point-to-point command/acknowledge protocol when using any of the output protocols. The A31315 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is an acknowledge pulse from the A31315 in the form of a low pulse following a successful write. If the command is a read, the A31315 responds by transmitting the requested data in a Read Acknowledge frame. It is the external controller's responsibility to avoid sending a Command Frame which overlaps a Read Acknowledge frame.

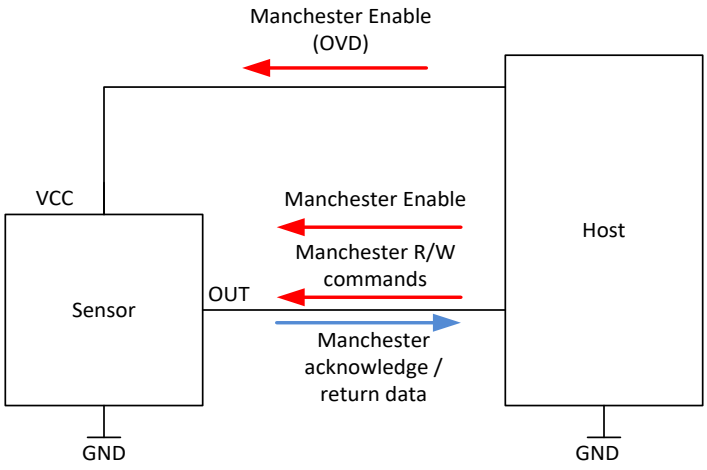

Figure 26: Manchester Communication Block Diagram

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the A31315: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM), and Read. One frame type, Read Acknowledge, is sent by the A31315 in response to a Read command.

Settings Controlling the Manchester Communication

It is possible to limit access to the device by programming certain options. These are detailed below. By default, this is set to 00 to enable all communication methods.

Table 24: MANCH_ACCESS_SEL behavior

MANCH_ ACCESS_SEL	Overvoltage Detection	Trigger	Description
00 (default)	Enabled	Enabled	Communications is enabled by either option.
01	Enabled	Disabled	Communication is enabled only by overvoltage detection.
10	Disabled	Enabled	Communication is enabled only by external trigger on output line.
11	Disabled	Disabled	Communication is locked.

Table 25: ANA_MANCH_LOCK behavior (affects analog output only)

ANA_MANCH_LOCK	Description
0 (default)	Do not demand unlock Code for Analog Output
1	Demand unlock Code for Analog Output

ENTERING MANCHESTER COMMUNICATION MODE THROUGH ANALOG OUTPUT

To enter Manchester communication when using the analog output, the customer must overdrive the Analog output. To prevent the Manchester controller from always listening, a timer after POR exists. The access code must be sent to be able to access the EEPROM, and an incorrect access code leads to the device being locked until the next POR event. In order to ensure the access code is sent correctly, the user should pull the output low during the POR event to ensure the access code is sent correctly. Upon a correct access code receipt by the device, the output will be dependent upon the status of MANCH_EN. If MANCH_EN = 0, the output will remain enabled, and the output may be overdriven to send Manchester commands. If MANCH_EN = 1, the

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output will tristate, to remove the need for overdriving. The start of any Manchester command should begin with holding the output low for 1 µs to ensure reset of the Manchester State machine.

In order to help decrease the likelihood of analog noise being interpreted as Manchester during the operation of the device, there is an EEPROM bit, ANA_MANCH_LOCK. When ANA_MANCH_LOCK = 1, the internal Manchester controller is disabled. This will prevent any unintended interruption from altering EEPROM or affecting the output signal of the device. Performing communication when ANA_MANCH_LOCK = 1 is still possible and detailed in the Manchester unlocking sections below.

Note: ANA_MANCH_LOCK only takes effect when the output mode is Analog.

SERIAL INTERFACE MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 27. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A31315 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 26.

For a Write Access command frame, the data consists of 16 bits. For a Read Request frame, the data bits are omitted. For a Read Acknowledge or Write frame, the data bits are defined as shown in Figure 27, where bit 0 is the LSB.

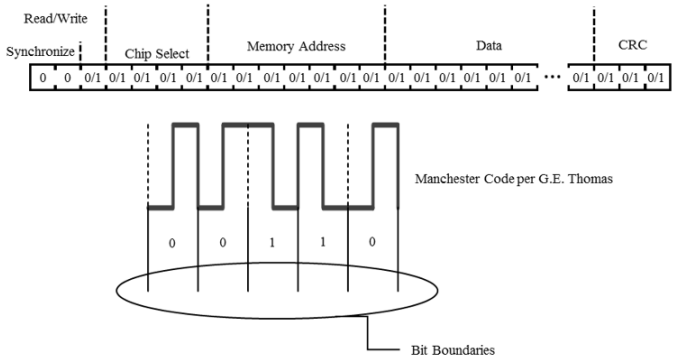

Figure 27: Manchester Bit Stream Definition

Table 26: Manchester Bit Definition (host commands)

Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a Manchester command and communication bit time
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
2	Chip Select		Chip select for up to 2 dies connected in parallel:
		01	[as required] device communication address 0
		10	[as required] device communication address 1
		00 / 11	[as required] Broadcast 00 can be used as default if only one device is connected
8	Address	Any	Register address for read or write
32 (write command) 0 (read command)	Data	Any	32 data bits (write command) 0 bits (read command)
3	CRC	Any	Bits to check the validity of frame.

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During a Read command, the device determines the baud rate from the sync bits and responds with a read response frame using the same baud rate detected. The baud rate during a write command is also automatically detected, but is only used for decoding, as the A31315 does not respond to write commands.

Table 27: Manchester Bit Definition (device response)

Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to announce the beginning of a Manchester interface response
32	Data	Any	Read data
3	CRC	Any	Bits to check the validity of frame.

The device memory contains non-volatile (EEPROM) and volatile registers which are accessible via the serial interface through Manchester communication modes. The memory address space is divided into Factory and Customer areas.

MANCHESTER UNLOCKING – SENT/PWM MODE VIA OVD

1. At any time after POR, create an OVD condition. This sets the OUT in HIGH-Z state since PWM/SENT Output is turned off.
2. Send the correct access code.
3. Device is unlocked.
4. If MANCH_EN bit was set LOW, the OVD condition can be removed and the device returned to PWM/SENT Mode with the device unlocked. OVD is needed for every Manchester Read/Write command.
5. If MANCH_EN bit was set HIGH, the OVD condition can be removed, but the device will remain in communication mode. OVD is not needed for Manchester transactions until MANCH_EN bit is set LOW through a Write Command. This action will lock the device back.

MANCHESTER UNLOCKING – SENT/PWM MODE VIA TRIGGERING PULSES

1. At any time after POR, create the trigger condition by driving the OUT LOW for a specific amount of time depending on the PWM (minimum of 2 full PWM messages) or SENT Mode (minimum of 30 t_{tick}). Then release the line or drive it HIGH to create a 0→1 condition. This is known as the auxiliary interrupt pulse.
2. The device is in communication mode and a 300 µs timeout starts.
3. Write the correct access code before the 300 µs expires. Timing requirements stop once the first sync bit is detected.
4. If the code is wrong, aborted, or it was an incorrect transaction, the part goes back to PWM/SENT mode. Retrying by starting at step 1 is possible.
5. If the code is correct, the device is unlocked and MANCH_EN bit is set to 1. The output is disabled, and the device remains unlocked until MANCH_EN is written to 0 through a Manchester Write.

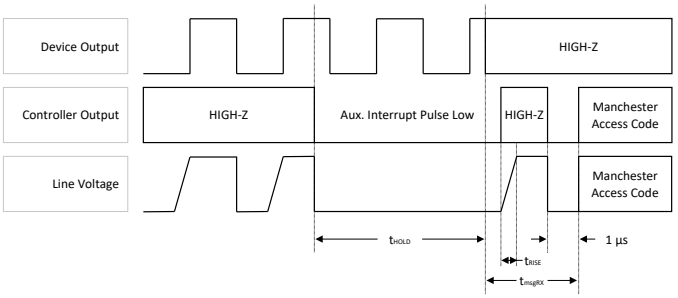

Figure 28: Auxiliary Interrupt Pulse Waveform for PWM Output

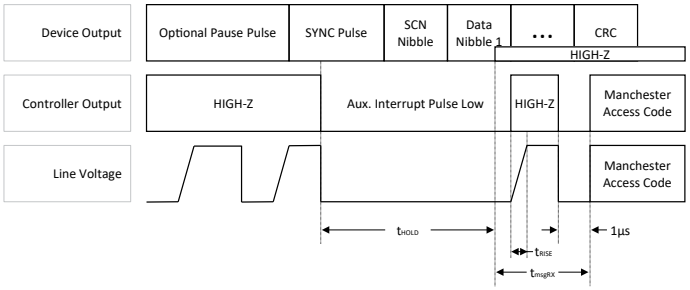

Figure 29: Auxiliary Interrupt Pulse Waveform for SENT Output

Table 28: Auxiliary Interrupt Timing

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Access Code Timeout	t_{msgRX}		–	–	300	µs
Interrupt Pulse Hold Time	t_{HOLD}	SENT	30	–	–	ticks
		PWM	2 × PWM Period [1]	–	–	µs

[1] The minimum hold time for the Auxiliary interrupt when the output is set for PWM is double the PWM period. If the PWM frequency increases as a result of a diagnostic condition, the hold time is double the new PWM period at the diagnosis frequency.

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MANCHESTER UNLOCKING – ANALOG MODE VIA OVD IF (ANA_LOCK = 1'b1) AND (ANA_MANCH_LOCK = 1'b1)

1. After POR and all the shadow registers have been loaded, there is a 40 ms timeout to unlock the device. If this timer expires before fully unlocking the device, the only way to try again is through a POR event.
2. Apart from the 40 ms timer, there is a maximum number of 3 unlock attempts. If three unlocking attempts fail, then the part cannot be unlocked until next POR.
3. Before generating the OVD event, it is recommended to start overdriving the OUT LOW.
4. Before the 40 ms expires, generate the OVD condition and write the unlock code. After the second sync pulse is recognized, the 40 ms timer is paused.
5. If the unlock code is incorrect or the transaction aborted, go back to step 2. The 40 ms timer is resumed and it will count as a failed attempt.
6. If the unlock code is correct, there is a 1 ms timeout to write the correct access code with MANCH_EN = 1. After the second sync pulse is recognized, the 40 ms timer is paused and the 1 ms is stopped.
7. If the access code is incorrect or the transaction aborted, go back to step 2. The 40 ms timer is resumed and it will count as a fail attempt.
8. If the access code is correct, the device will be unlocked until next POR.

MANCHESTER UNLOCKING – ANALOG MODE VIA OVD IF (ANA_LOCK = 1'b1) AND (ANA_MANCH_LOCK = 1'b0)

1. After POR and ALL the shadow registers have been loaded, there is a 40 ms timeout to unlock the device. If this timer expires before fully unlocking the device, the only way to try again is through a POR event.
2. Apart from the 40 ms timer, there is a maximum number of unlocking tries, which is 3. If three unlocking attempts fail, then the part cannot be unlocked until next POR.
3. Before generating the OVD event, it is recommended to start overdriving the OUT LOW.
4. Before the 40 ms expires, generate the OVD condition and write the correct access code with MANCH_EN = 1. After the second sync pulse is recognized, the 40 ms timer is paused.
5. If the access code is incorrect or the transaction aborted, go back to step 2. The 40 ms timer is resumed and it will count as a fail attempt.
6. If the access code is correct, the device will be unlocked until next POR.

MANCHESTER UNLOCKING – ANALOG MODE WITHOUT OVD IF (ANA_LOCK = 1'b0) AND (ANA_MANCH_LOCK = 1'b1)

1. After POR and ALL the shadow registers have been loaded, there is a 40 ms timeout to unlock the device. If this timer expires before fully unlocking the device, the only way to try again is through a POR event.
2. Apart from the 40 ms timer, there is a maximum number of unlocking tries, which is 3. If three unlocking attempts fail, then the part cannot be unlocked until next POR.
3. Every time a Manchester command is driven, the OUT must be overdriven LOW for 500 µs prior to it to reset the internal state machine.
4. Before the 40 ms expires, write the unlock code. After the second sync pulse is recognized, the 40 ms timer is paused.
5. If the unlock code is incorrect or the transaction aborted, go back to step 2. The 40 ms timer is resumed and it will count as a fail attempt.
6. If the unlock code is correct, there is a 1 ms timeout to send the correct access code. After the second sync pulse is recognized, the 40 ms timer is paused and the 1ms is stopped.
7. If the access code is incorrect or the transaction aborted, go back to step 2. The 40 ms timer is resumed and it will count as a fail attempt.
8. If the access code is correct, the device will be unlocked until next POR.

MANCHESTER UNLOCKING – ANALOG MODE WITHOUT OVD (ANA_LOCK = 1'B0) AND (ANA_MANCH_LOCK = 1'B0)

1. After POR and ALL the shadow registers have been loaded, there is a 40 ms timeout to unlock the device. If this timer expires before fully unlocking the device, the only way to try again is through a POR event.
2. Apart from the 40 ms timer, there is a maximum number of unlocking tries, which is 3. If three unlocking attempts fail, then the part cannot be unlocked until next POR.
3. Every time a Manchester command is driven, the OUT must be overdriven LOW for 500 µs prior to it to reset the internal state machine.
4. Before the 40 ms expires, write the correct access code. After

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the second sync pulse is recognized, the 40 ms timer is paused.

5. If the factory/customer code is incorrect or the transaction aborted, go back to step 2. The 40 ms timer is resumed and it will count as a fail attempt.
6. If the factory/customer code is correct, the device will be unlocked until next POR.

The access codes contain 32 bits, the 31 MSBs are constants, while the LSB can be used to select MANCH_EN for Manchester communications. MANCH_EN mode will keep the device output (SENT, PWM, or Analog) disabled so the pin shared for Manchester communications can be used without needing to use the modes of initiating Manchester. To leave MANCH_EN mode, the volatile bit, MANCH_EN, can be reset via a POR condition or a write to the register.

To send the access codes shown in Table 29, the customer writes to the access register to send the full 32-bit access code.

When the customer access code is received, factory registers are readable, but not writeable.

Table 29: Unlock Code and Customer Access Codes

Command	Write address	Write data
Unlock	0x86	0x414C5333
Customer access code (Read access to factory) MANCH_EN = 1	0x86	0xC2D8E67B
Customer access code (Read access to factory) MANCH_EN = 0	0x86	0xC2D8E67A

Manchester Communication CRC

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the following polynomial and the calculation is represented graphically in Figure 30. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111.

$$g(x) = x^3 + x + 1$$

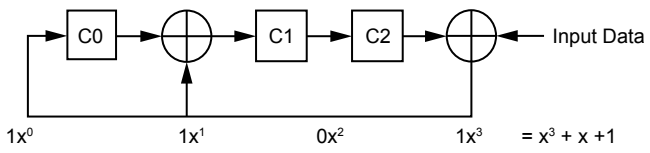

Figure 30: Manchester CRC Implementation

EEPROM Lock

There are 3 different lock modes available in the A31315: EELOCK, WRLOCK, and FLOCK. Each of these are separate from access lock which requires a customer unlock code to control. EELOCK locks the EEPROM from external write access, while still allowing writes to shadow and volatile registers. The entirety of memory can still be read in this mode allowing for a level of customer lock, while maintaining debug support. WRLOCK prevents any write both EEPROM and volatile registers. Factory read support is maintained. This is not recommended for any output mode. The FLOCK mode locks out both reads and writes to EEPROM and all registers. This prevents any access by either customer or factory, removing available support options from the factory.

NOTE: When any of the EEPROM lock options are set, non-destructive factory debug support is limited.

Table 30: Serial Communication Lockout Modes

MEM_LOCK_SEL [3:0]	Lock Mode	Description
4'b0011	EELOCK	EEPROM Lock: Prevents writes to EEPROM but all volatile registers including shadow can be written. All registers and EEPROM can be read normally.
4'b0110	WRLOCK	Write Lock: Prevents writing anything to either EEPROM or registers. Factory debug support is still available
4'b1100	FLOCK	Full Lock: Prevents writing and reading to any register in the device.

EEPROM Margin Checking

The A31315 contains a test mode, EEPROM Margining, to check the logic levels of the EEPROM bits. The EEPROM margining is accessible with customer access. The EEPROM margining is selectable to check all logic 1, logic 0, or both. The results of the test are reported back in EEPROM registers.

Note: A fail of the margin test does not force the output to a diagnostic state.

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Table 31: Error Registers

Address	NAME	Access	Bit													
			31...13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xA3	ERROR	RO	0	OFE	SPE	EUE	OVD	UVD	ESE	POR	SRR	SLF	SAT	TSE	AOC	ACF

Error Flag Registers

The different error flags available in the A31315 are stored in the primary memory space of register 0xA4. If the error conditions are removed, all the non-critical error flags are cleared on a read of this register, or after being sent out through the output protocols. The register contents can be seen in Table 36.

Analog Check Failure (ACF)

To ensure proper operation of the internal regulators, a voltage check is done on the different reference sources for the analog and digital circuitry, as well as for the Hall element drivers. If any of these voltages deviate to where the accuracy of the part will be in question, the ACF flag will be set and the device will go into a state as defined in Table 34. If the voltages are detected to recover, a read of the device register or reporting through the output modes will clear the error flag so normal operation can resume. The ACF flag can be disabled by setting ACF_MASK bit in EEPROM.

Angle Outside Clamp (AOC)

If the upper and lower clamps are set within the operating range of the device, the AOC flag can be set as shown in Table 34 to indicate the signal reaching this clamp value. If the signal moves back within the range defined ANG_CLAMP_HIGH and ANG_CLAMP_LOW as described in the Output Clamps section, the AOC flag can be removed by a read of the device register or through reporting in the applicable output protocol. If the flag is not desired, the EEPROM bit AOC_MASK can be set. The AOC error is updated with every angle update. However, the error may be suppressed for up to 16 t_{update} based on the FAULT_FILT EEPROM setting.

Temperature Error (TSE)

The TSE flag is set if the temperature sensor output saturates high, which indicates the junction temperature is greater than 175.138°C or less than –54.963°C. If any of these conditions occur, the TSE flag will be set, and the device will go into a state as defined in Table 34. If the temperature is detected to recover, a read of the device register or reporting through the output modes will clear the error flag so normal operation can resume. The TSE flag can be disabled by setting TSE_MASK bit in EEPROM.

Saturation Flag (SAT)

The Saturation Flag is provided to warn the user in case the magnetic signal is outside of the detectable range of the signal path. A saturation can occur:

- In the ADC and filters, which would indicate a front-end gain too large for the detected field, or
- A digital signal path saturation, which would indicate a gain setting too large.

If either of these conditions occur, the SAT flag will be set as defined in Table 34. If the saturation condition is removed, the error flag can be cleared by a read of the device register or through reporting in the applicable output protocol.

Overall, the SAT flag is constructed as follows:

- SAT can be caused by SAT_LIN, SAT_FILT, and SAT_COR. All reporting options of the SAT error can be masked by setting SAT_MASK = 1.
  - □ SAT_LIN is linearization saturation and can be disabled independently by setting SAT_LIN_MASK = 1. This mask is set by default, as it is often a desired functionality of the signal path.
  - □ SAT_FILT is saturation in the ADC or low-pass filter.
  - □ SAT_COR is saturation in the remaining data path and can be disabled independently by setting SAT_COR_MASK = 1. This mask is set by default, as it is often a desired functionality of the signal path. Possible causes are:
    - ◦ factory 1-D trim saturation.
    - ◦ customer 1-D trim saturation.
    - ◦ Output value of Pre-gain Angle Offset Correction is outside ANG_THRESH_LOW / ANG_THRESH_HIGH limits. This saturation check can be enabled/disabled individually by setting ANG_THRESH_EN = 1/0.
    - ◦ saturation of angle after Angle Gain Correction. This saturation feature (not just the flag) can be enabled/disabled by setting ANG_GAIN_SAT_EN = 1/0.
    - ◦ saturation of angle after Post Gain Angle Offset Correction. This saturation feature (not just the flag) can be enabled/disabled by setting ANG_OFFS_SAT_EN = 1/0.

The SAT error is updated with every angle update. However, the error can be suppressed for a number of t_{update} based on the fault_filt EEPROM setting, to a maximum of 16 t_{update}.

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Oscillator Frequency Error (OFE)

The A31315 contains a low frequency oscillator to act as a watchdog of the main oscillator. If these two oscillators deviate beyond comparison threshold (20%), the device will go into a state as defined in Table 34. This error is considered critical and cannot be cleared by any action besides a device reset (POR). To mask OFE errors, the OFE_MASK bit can be set. It is not recommended to set this bit for normal operation but is provided for debugging purposes. The OFE error detection starts every 10 t_{update}.

Signal Processing Logic Failure (SLF)

To help check the main signal path logic in the device during operation, a set of known inputs will periodically be run through key parts of the data path and compared to known outputs. This allows the user to have confidence in the accuracy of the digital signal path without need for running the LBIST which interrupts the device operation. Additionally, a watchdog checks that the output angle is updated at the expected delay after the input signals are available. In case of unexpected test outputs, or missed watchdog timer, the SLF flag will be set as shown in Table 34. If the error condition is removed, the error flag can be cleared by a read of the device register or by reporting through the output modes so normal operation can resume. The SLF error is determined every 10 t_{update}.

Signal Radius Out of Range (SRR)

The A31315 has an internal check on the two dimensions that are used to calculate angle (called sine and cosine) by calculating the radius and comparing to user defined diagnostic boundaries. These boundaries are set by the MAGNETIC_THRESH_MIN and MAGNETIC_THRESH_MAX EEPROM parameters. The condition for no error is calculated by the equation below:

Equation 20:

$$\begin{aligned} &\text{MAGNETIC_THRESH_MIN}^2 \\ &\quad < \text{RADIUS_SQ_17B} \\ &\quad < \text{MAGNETIC_THRESH_MAX}^2 \end{aligned}$$

with

$$\text{RADIUS_SQ_17B} = \left(\frac{\text{CHAN_A_16B}}{128} \right)^2 + \left(\frac{\text{CHAN_B_16B}}{128} \right)^2$$

The brackets [x] denote the floor function, which rounds x down to the nearest integer. The current value of RADIUS_SQ_17B can be read directly from the appropriate register.

The SRR check helps ensure the accuracy of the ATAN2 by the assumption the magnitude of the two dimensions will remain constant over the complete rotation. This is only true in rotary applications. In the event the magnetic field is outside of the threshold boundaries MAGNETIC_THRESH_MIN and MAGNETIC_THRESH_MAX, the SRR flag will be set as shown in Table 34. If the error condition is removed, the error flag can be cleared by a read of the device register or reporting through the output modes so normal operation can resume. Individual checks of the minimum or maximum threshold can be enabled or disabled individually by setting the MAGNETIC_THRESH_MIN_EN and MAGNETIC_THRESH_MAX_EN bits respectively. The SRR flag can be disabled by setting SRR_MASK bit in EEPROM. The SRR error is updated with every angle update. However, the error can be suppressed for up to 8 t_{update} based on the FAULT_FILT EEPROM setting.

Power-On Reset (POR)

To indicate a Power-On Reset event occurred, the POR error flag will be set on startup. In the event of a reset, the filters and signal path will need time to settle and this error flag is set to help indicate this state in the event the reset was unintentional. This flag is reported as shown in Table 34. Once the first angle update is available, a read of the device register, or reporting through the output modes will clear the POR flag so normal operation can resume. The POR flag can be disabled by setting the POR_MASK bit in EEPROM.

If the part is in SENT or PWM mode, the first output message (SENT) or first output cycle (PWM) will report the POR error, unless POR is masked.

POR error may be prolonged in PWM mode to suppress filter initialization showing on the output. Refer to Sensor Output During Low-Pass Filter Initialization section for more information.

EEPROM Multiple Bit Error (EUE) and EEPROM Single Bit Error (ESE)

The A31315 contains EEPROM with error checking and correction codes, ECC, that provide correction of any single EEPROM bit error without affecting device performance. The ECC also detects a multiple bit EEPROM error and triggers an internal fault signal at which point the device will go into a state as defined in Table 34. An EEPROM multi-bit error is considered critical and cannot be cleared by any action besides a device reset (POR). The EEPROM single bit error flag is cleared after a read, or once reported by the output protocol. A single bit error will not affect the device output as it is immediately corrected but it may indicate deteriorating performance of the EEPROM and should be monitored. The ESE flag can be disabled by setting the ESE_

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MASK bit in EEPROM. The EUE flag cannot be disabled. The EUE and ESE flags can only be set during an EEPROM read, which occurs only at POR during normal operation.

Shadow Parity Error (SPE)

Upon power up of the A31315, the EEPROM parameters are loaded into fast access shadow registers for use in operation. These registers have a simple parity structure to ensure proper loading of the EEPROM parameters. If a parity error is detected, the SPE error flag is set and the device will go into a state as defined in Table 34. This error is considered critical and cannot be cleared by any action besides a device reset (POR). The SPE flag can be disabled by setting the SPE_MASK bit in EEPROM. The parity error is detected every 10 t_{update}.

Undervoltage Detection (UVD)

The A31315 contains circuitry to detect a condition when the supply voltage drops below the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{UVD(RISE)} - V_{UVD(FALL)}$. As an example, initially V_{CC} and OUT are within the normal operating range. If V_{CC} drops below $V_{UVD(FALL)}$, OUT is forced to a state as defined in Table 34. When V_{CC} returns above $V_{UVD(RISE)}$, OUT returns to its normal operating state after a read of the device register or once the error is reported through the output mode. If V_{CC} drops below the internal reset level, $V_{POR(FALL)}$, the output is forced to a high impedance state. When V_{CC} returns above the rising reset level, $V_{POR(RISE)}$, the output responds with the POR flag if enabled.

Undervoltage Detection is set to one of two configurable thresholds based on the EEPROM parameter UVD_SEL as shown in Table 32 and Figure 31.

Table 32: uvd_sel settings for V_{UVD}

uvd_sel	$V_{UVD(RISE)}$	$V_{UVD(FALL)}$
0	$V_{UVD(LOW, RISE)}$	$V_{UVD(LOW, FALL)}$
1	$V_{UVD(HIGH, RISE)}$	$V_{UVD(HIGH, FALL)}$

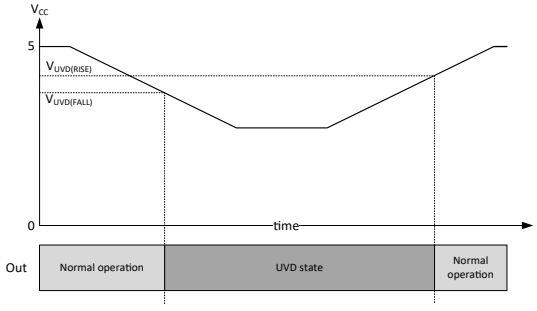

Figure 31: V_{CC} Low Threshold Levels

Overvoltage Detection (OVD)

The A31315 contains circuitry to detect a condition when the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{OVD(RISE)} - V_{OVD(FALL)}$. As an example, Initially, V_{CC} and OUT are within the normal operating range. If V_{CC} rises above $V_{OVD(RISE)}$, OUT is forced to a state as defined in Table 34. When V_{CC} returns below $V_{OVD(FALL)}$, OUT returns to its normal operating state after a read of the device register or reporting through the output mode. If the device is in SENT/PWM or Analog output modes, and the EEPROM lock options are not set, the device will enter programming mode and the output will always be forced to a high impedance state when V_{CC} increases above $V_{OVD(RISE)}$. The overvoltage detection is only enabled if the EEPROM lock options are set, otherwise the device will be in programming mode (Manchester Communication on the OUT Pin).

Overvoltage Detection is set to one of two configurable thresholds based on the EEPROM parameter OVD_SEL as shown in Figure 32 and Table 33.

Table 33: ovd_sel settings for V_{OVD}

ovd_sel	$V_{OVD(RISE)}$	$V_{UVD(FALL)}$
0	$V_{OVD(HIGH, RISE)}$	$V_{OVD(HIGH, FALL)}$
1	$V_{OVD(LOW, RISE)}$	$V_{OVD(LOW, FALL)}$

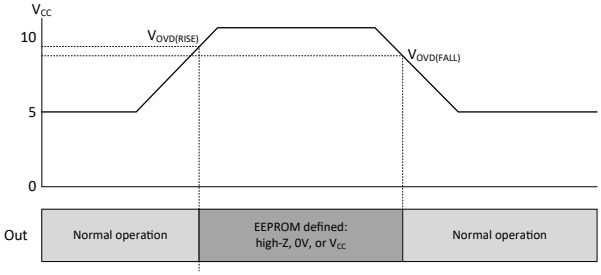

Figure 32: OVD Threshold Levels

SENT Output Error Reporting

In SENT mode, there are four ways to report error flags: the SCN status bits [1:0], the slow serial message, the extended data options that include a rotating report of the error registers, or by entering a High-Z state. When any error flag is set, these status bits will be set until a clear condition occurs. The clear condition can be a Manchester read of the err register, or a SENT message that contains the SCN bit set. The SENT message will clear the error flag from the err register. If either of the SCN status bits are set, the data from that SENT frame should not be trusted as there

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was an error between the last frame transmission and the current frame. These bits are constructed as follows:

SCN[0] = SLF | SRR | ACF | TSE | POR (see Sensor Output During Low-Pass Filter Initialization section for information on POR bit setting during filter initialization).

SCN[1] = UVD | OVD | SAT | AOC.

The serial message requires successive SENT messages to be received. The Error flags that are sent in this method are taken from an internal register which is not cleared during normal conditions to allow normal operation for other interfaces. Once the error bits are sent out from the slow serial message, the register will be cleared.

The third reporting method is through the optional extended diagnostic nibbles in SENT_DATA_SEL options 2, 8, or 13. This method sends the error flags in every SENT message. The error flags for this method are taken from an internal copy of the error registers to allow the error register to be cleared separately. The bits are sent out as shown in Table 34. Note that overvoltage and undervoltage are reported through the same bit.

If the specific error flags are not desired to be transmitted, the EEPROM parameter DIG_OUT_ERR_RESP_SEL can be set to put the output in a high-impedance state when an error condition occurs. If the error condition is removed, the output will return to normal operation. This option will prevent the device from transmitting any data through the SENT mode, but Manchester communication is still possible.

PWM Output Error Reporting

When in PWM output mode, the error flags are reported by sending out a specific diagnostic message format. The format consists of reducing the carrier frequency to half of the configured setting and sending a specific duty cycle as defined in Table 34. In the event of more than one error occurring, the higher priority message will be sent. If two error conditions occur and clear at the same time, only one error flag will be seen. Table 34 is listed in descending order in terms of priority.

If the specific error flags are not desired to be transmitted, the EEPROM parameter DIG_OUT_ERR_RESP_SEL can be set to put the output in a high-impedance state when an error condition occurs. If the error condition is removed, the output will return to normal operation. Either option prevents the device from transmitting any data through the PWM mode, but Manchester communications are still possible. If using the half frequency error reporting with the trigger pulse Manchester method, the trigger must cover two full periods at the new frequency.

Analog Output Error Reporting

To prevent the device from transmitting an angle reading through the analog output when an error condition is present, the output will go to a high-impedance state, drive high, or drive low, depending on the EEPROM programming. If the sensor is programmed for high-Z error state, the output will go to the rail as defined by the resistive load, which can be a pull-down to ground, or a pull-up to a specific voltage. In order to ensure the output can reach the rail when a transient error occurs, the high-impedance state will be held for the number of angle updates defined by the EEPROM parameter ERR_RESP_SEL.

Broken Wire Detection

The A31315 contains circuitry to detect a condition when the ground or supply connection is disconnected. If the GND connection is broken, the output will be at $V_{SAT(DIAG, HIGH)}$. If the V_{CC} connection is broken, the output will be at $V_{SAT(DIAG, LOW)}$.

Logic Built-In Self-Test (LBIST)

It is possible to test the logic of the sensor using a built-in self-test. This self-test runs quasi-random signals though a scan chain connection of the digital logic. A checksum is calculated by the sensor and compared to a known good checksum value.

The user can start the self-test by unlocking the part (see Programming Protocol section) and writing 1 to the BIST_START. The self-test typically takes 200 ms to complete. No communication is possible while LBIST is running.

After LBIST is done:

- LBIST_STATUS will be set to 1 regardless of the test result.
- LBIST_RESULT will be set to 1 if the test was successful.
- The checksum can be read out be reading LBIST_RESULT_SIGNATURE. This is not necessary to judge the test result. The correct checksum is 0x6C56C9EF.

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Table 34: Device Error Flag Responses

Error Flag	ERR Register (Bit)	Meaning	Analog / PWM Error Priority	SENT Response DIG_OUT_ERR_RESP_SEL = 0	PWM Response DIG_OUT_ERR_RESP_SEL = 0	SENT/PWM Response DIG_OUT_ERR_RESP_SEL = 1	Analog Response
OFE	ERR[12]	Oscillator Frequency Error	1 (highest)	High Impedance	High Impedance	High Impedance	High
EUE	ERR[10]	EEPROM Multiple Bit Error	2	High Impedance	High Impedance	High Impedance	High
SPE	ERR[11]	Shadow Parity Error	3	High Impedance	High Impedance	High Impedance	High
SLF	ERR[4]	Signal Processing Logic Failure	5	SCN[0] = 1 DIAG_BYTE[0] = 1	½ Frequency 10% Duty Cycle	High Impedance [*4]	High Impedance, or High, or Low, depending on ERR_RESP_SEL
SRR	ERR[5]	Signal Radius Out of Range	6	SCN[0] = 1 DIAG_BYTE[1] = 1	½ Frequency 20% Duty Cycle	High Impedance [*4]	High Impedance, or High, or Low, depending on ERR_RESP_SEL
ACF	ERR[0]	Voltage Check Failure	7	SCN[0] = 1 DIAG_BYTE[2] = 1	½ Frequency 30% Duty Cycle	High Impedance [*4]	High Impedance, or High, or Low, depending on ERR_RESP_SEL
TSE	ERR[2]	Temperature Error	8	SCN[0] = 1 DIAG_BYTE[3] = 1	½ Frequency 40% Duty Cycle	High Impedance [*4]	High Impedance, or High, or Low, depending on ERR_RESP_SEL
POR	ERR[6]	Power-On Reset	9	SCN[0] = 1 [*6] DIAG_BYTE[4] = 1	½ Frequency 50% Duty Cycle [*6]	High Impedance [*4]	None
UVD	ERR[8]	Undervoltage Detection	10	High Impedance, or High, or Low, depending on err_resp_sel and SENT reset [*2] and SCN[1] = 1 [*3] and DIAG_BYTE[5] = 1 [*5]	High Impedance, or High, or Low, depending on ERR_RESP_SEL and ½ Frequency 60% Duty Cycle [*3]	Same as with DIG_OUT_ERR_RESP_SEL = 0	High Impedance, or High, or Low, depending on ERR_RESP_SEL
OVD [*1]	ERR[9]	Overvoltage Detection	11	SCN[1] = 1 DIAG_BYTE[5] = 1	½ Frequency 70% Duty Cycle	High Impedance [*4]	High Impedance, or High, or Low, depending on ERR_RESP_SEL
SAT	ERR[3]	Saturation Flag	12	SCN[1] = 1 DIAG_BYTE[6] = 1	½ Frequency 80% Duty Cycle	High Impedance [*4]	High Impedance, or High, or Low, depending on ERR_RESP_SEL

Continued on next page...

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Table 34: Device Error Flag Responses (continued)

Error Flag	ERR Register (Bit)	Meaning	Analog / PWM Error Priority	SENT Response DIG_OUT_ERR_RESP_SEL = 0	PWM Response DIG_OUT_ERR_RESP_SEL = 0	SENT/PWM Response DIG_OUT_ERR_RESP_SEL = 1	Analog Response
AOC	ERR[1]	Angle Outside Clamp	13	SCN[1] = 1 DIAG_BYTE[7] = 1	½ Frequency 90% Duty Cycle	High Impedance [*4]	High Impedance, or High, or Low, depending on ERR_RESP_SEL
ESE	ERR[7]	EEPROM Single Bit Error	14 (lowest)	None	None	High Impedance [*4]	None

[*1] OVD will cause the device to go High Impedance if MANCH_ACCESS_SEL = 2'b0X in SENT/PWM output modes.
[*2] SENT interface will restart after coming out of the UVD reporting, starting with message counter = 0 (if enabled) and the first serial message (if enabled).
[*3] At the first frame and potentially further frames transmitted after UVD condition is released, depending on ERR_HOLD_SEL setting.
[*4] Errors reported by a high Impedance response will not be communicated through a SENT packet. Additionally, the High-Z state will interrupt enhanced serial messages requiring the host controller to re-sync on the next message.
[*5] At the first frame after UVD condition is released.
[*6] POR status on PWM output, and SCN[0] = 1 status can also be caused by filter initialization reporting. See Sensor output during low-pass filter initialization.

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DIAGNOSTIC SETTING AND CLEARING

Diagnostic bits are set internally as soon as an error is detected and are sent out whenever the protocol allows it.

In PWM, this occurs at the start of the next PWM cycle.

In SENT, this occurs at the creation of the next SENT frame.

For SENT serial messages, this occurs at the creation of the next serial message.

In Analog, this is done directly.

In SENT, PWM, and analog output mode, the errors are cleared when they no longer occur.

For PWM and SENT, it is ensured that they are sent out at least once.

MEMORY ACCESS

The A31315 uses a primary-only memory structure to allow fast communication. The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing a write to the shadow addresses, or by reprogramming the corresponding EEPROM fields. Use of Shadow Memory is substantially faster than accessing EEPROM. In situations where many parameters need to be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and will return 0 when read. Shadow registers do not contain the ECC bits. All EEPROM and Shadow locations may be read after customer unlock. Requiring the access code in Analog Output mode helps to prevent unwanted device operation due to potential noise toggling the output around the Manchester thresholds. The customer is able to read Wafer ID and Die position information without factory access code.

The device does not answer Manchester reads commands from registers that do not exist or that only contain “write-only” bits.

Shadow Memory Read and Write Transactions

Shadow memory Read and Write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM addresses, one must address to the Shadow addresses, which are located at an offset of 0x40 above the EEPROM.

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Table 35: Register Description – Volatile

Volatile Address (hex)	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Volatile Address (hex)
0x83																			EE_MARGIN_LOOP	EE_MARGIN_TEST_ADDR						EE_MARGIN_TEST_ADDR_EN	EE_MARGIN_RESULT	EE_MARGIN_STATUS		EE_MARGIN_MIN_DIS	EE_MARGIN_MAX_DIS	EE_MARGIN_START	0x83
0x85																											LBIST_RESULT	LBIST_STATUS					0x85
0x86																															MEMORY_ACCESS		0x86
0xA0																									MANCH_EN							LBIST_START	0xA0
0xA1	LBIST_RESULT_SIGNATURE																																0xA1
0xA2																																SOFTWARE_RESET	0xA2
0xA3																				OFE	SPE	EUE	OVD	UVD	ESE	POR	SRR	SLF	SAT	TSE	AOC	ACF	0xA3
0xA7	TEMPERATURE_16B																ANGLE_16B																0xA7
0xA8	CHAN_B_16B																CHAN_A_16B																0xA8
0xA9	CHAN_B_PRE_16B																CHAN_A_PRE_16B																0xA9
0xAA																RADIUS_SQ_17B																	0xAA

The table above shows the location of all useful volatile registers. Most volatile registers are read only and meant to provide information about the device's internal functions.

Other unmarked registers may contain data used for internal purposes, only registers useful for external interfacing are shown. When writing to volatile registers, all unlabeled bits should be set to 0.

Volatile 0x83

EE_MARGIN_LOOP (BITS 13) R/W (READ AND WRITE)

If set, the margin testing will continuously test the register in EE_MARGIN_TEST_ADDR.

EE_MARGIN_TEST_ADDR (BITS 12:7) R/W

If the margin testing fails, this register contains the address of the register that failed. If multiple registers fail, this contains the address of the most recent failed register (highest register). If EE_MARGIN_TEST_ADDR_EN is set to 1, this address can be written to and used as the starting address for margin testing.

EE_MARGIN_TEST_ADDR_EN (BIT 6) R/W

Determines if a custom starting address is used, or the default starting address is used.

- If EE_MARGIN_TEST_ADDR_EN = 0, Margin testing begins at address 0.
- If EE_MARGIN_TEST_ADDR_EN = 1 Margin testing begins at the address contained in EE_MARGIN_TEST_ADDR.

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EE_MARGIN_RESULT (BIT 5) RO (READ ONLY)

Indicates which limit the margin failed. When the margin testing fails, this bit is set based on the fail condition.

- If EE_MARGIN_RESULT = 0, Lower margin failed
- If EE_MARGIN_RESULT = 1, Upper margin failed

EE_MARGIN_STATUS (BITS 4:3) RO

Indicates the current status of margin testing.

- If EE_MARGIN_STATUS = 00, Test has not been run
- If EE_MARGIN_STATUS = 01, Test has passed
- If EE_MARGIN_STATUS = 10, Test has failed
- If EE_MARGIN_STATUS = 11, Test is currently running

EE_MARGIN_MIN_DIS (BIT 2) R/W

Determines if the low margin testing will be performed or skipped.

- If EE_MARGIN_MIN_DIS = 0, Lower margin testing will be performed when margin testing is run.
- If EE_MARGIN_MIN_DIS = 1, Lower margin testing will not be performed when margin testing is run.

EE_MARGIN_MAX_DIS (BIT 1) R/W

Determines if the high margin testing will be performed or skipped.

- If EE_MARGIN_MAX_DIS = 0, Upper margin testing will be performed when margin testing is run.
- If EE_MARGIN_MAX_DIS = 1, Upper margin testing will not be performed when margin testing is run.

EE_MARGIN_START (BIT 0) R/W

Write to 1 to begin the margin testing. This bit self-clears when the margin testing finishes. If cleared during testing, the test will end prematurely.

Volatile 0x85

LBIST_RESULT (BIT 5) RO

Indicates whether LBIST has passed or failed when run.

- If LBIST_RESULT = 0, LBIST test failed
- If LBIST_RESULT = 1, LBIST test passed

LBIST_STATUS (BIT 4) RO

Indicates when BIST test is finished.

- If LBIST_STATUS = 0, BIST is not finished or not started
- If LBIST_STATUS = 1, BIST has finished and LBIST_RESULT contains valid results.

Volatile 0x86

MEMORY_ACCESS (BIT 1) RO

Set to 1 when access code is successfully sent.

Volatile 0xA0

MANCH_EN (BIT 7) R/W

Disables the current device output and forces Manchester interface to be active.

- If MANCH_EN = 0, Device is in normal operation mode and will output based on EEPROM settings
- If MANCH_EN = 1, Device output is in High-Z mode, and Manchester is active and waiting for commands.

Volatile 0xA1

LBIST_START (BITS 32:0) RO

Contains the calculated LBIST signature. This is internally compared against the expected value to determine if there are any internal logic failures.

Volatile 0xA3

OFE (BIT: 12) RO

Indicates when the oscillator frequency error has occurred. This bit will NOT be asserted if the flag is masked.

SPE (BIT: 11) RO

Indicates when the shadow parity error has occurred. This bit will NOT be asserted if the flag is masked.

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EUE (BIT: 10) RO

Indicates when the EEPROM uncorrectable error has occurred. This bit will NOT be asserted if the flag is masked.

OVD (BIT: 9) RO

Indicates when the OVD error has occurred. This bit will NOT be asserted if the flag is masked.

UVD (BIT: 8) RO

Indicates when the UVD error has occurred. This bit will NOT be asserted if the flag is masked.

ESE (BIT: 7) RO

Indicates when the EEPROM single bit error has occurred. This bit will NOT be asserted if the flag is masked.

POR (BIT: 6) RO

Indicates when a power-on reset has occurred. This bit will NOT be asserted if the flag is masked.

SRR (BIT: 5) RO

Indicates when the signal radius is out of range. This bit will NOT be asserted if the flag is masked.

SLF (BIT: 4) RO

Indicates when an error is detected in the signal path logic. This bit will NOT be asserted if the flag is masked.

SAT (BIT: 3) RO

Indicates when saturation occurs within the signal path. This bit will NOT be asserted if the flag is masked.

TSE (BIT: 2) RO

Indicates when the temperature sensor is either in error or out of range. This bit will NOT be asserted if the flag is masked.

AOC (BIT: 1) RO

Indicates when the angle is outside of the clamped region. This bit will NOT be asserted if the flag is masked.

ACF (BIT: 0) RO

Indicates when a failure has occurred on the internal analog checks. This bit will NOT be asserted if the flag is masked.

Volatile 0xA7

TEMPERATURE_16B (BITS: 31:16) RO

Contains the digital readout of the temperature sensor. This value is provided in 2's complement. Conversion to degrees can be done with the following equation:

$$\text{Temperature [°C]} = (\text{TEMPERATURE_16B}) / 128 + 25$$

ANGLE_16B (BITS: 15:0) RO

The calculated angle after all trimming and compensation.

Volatile 0xA8

CHAN_B_16B (BITS: 31:16) RO

Final output of channel B after customer trimmed compensation. This value is directly input to the CORDIC calculation.

CHAN_A_16B (BITS: 15:0) RO

Final output of channel A after customer trimmed compensation. This value is directly input to the CORDIC calculation.

Volatile 0xA9

CHAN_B_PRE_16B (BITS: 31:16) RO

Customer-trimmed output of channel B before the hysteresis filter.

CHAN_A_PRE_16B (BITS: 15:0) RO

Customer-trimmed output of channel A before the hysteresis filter.

Volatile 0xAA

RADIUS_SQ_17B (BITS: 16:0) RO

The squared radius as calculated internally. This value is used to determine if the signal radius is out of range.

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Table 36: Register Description – EEPROM & Shadow

EEPROM Address (hex)	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	EEPROM Address (hex)	Shadow Address (hex)
0x05	ECC		ANA_INIT_SEL	DIG_OUT_DRIVE_SEL	CHAN_B_HYSTERESIS										CHAN_A_HYSTERESIS										ANA_CAP_SEL			0x05	0x45
0x15	ECC											SPARE_0X15			CHAN_ORTHOG											CHAN_B_DIS	CHAN_A_DIS	0x15	0x55
0x16	ECC										ANG_THRESH_HIGH								ANG_THRESH_LOW								ANG_THRESH_EN	0x16	0x56
0x17	ECC												CHAN_A_POL	CHAN_A_OFFS														0x17	0x57
0x18	ECC			CHAN_A_OFFS_TC1_HOT												CHAN_A_OFFS_TC1_COLD												0x18	0x58
0x19	ECC													CHAN_A_SENS														0x19	0x59
0x1A	ECC					CHAN_A_SENS_TC1_HOT										CHAN_A_SENS_TC1_COLD													0x1A	0x5A
0x1B	ECC							CHAN_A_SENS_TC2_HOT										CHAN_A_SENS_TC2_COLD										0x1B	0x5B
0x1C	ECC												CHAN_B_POL	CHAN_B_OFFS														0x1C	0x5C
0x1D	ECC			CHAN_B_OFFS_TC1_HOT												CHAN_B_OFFS_TC1_COLD												0x1D	0x5D
0x1E	ECC													CHAN_B_SENS														0x1E	0x5E
0x1F	ECC					CHAN_B_SENS_TC1_HOT										CHAN_B_SENS_TC1_COLD													0x1F	0x5F
0x20	ECC		TEMPERATURE_OFFS					CHAN_B_SENS_TC2_HOT										CHAN_B_SENS_TC2_COLD										0x20	0x60
0x21	ECC	LIN_COEFF_0														SPARE_0X21		LIN_COEFF_ACTIVE					LIN_COEFF_SCALAR		LIN_SEL	LIN_ENABLE	0x21	0x61
–	ECC	–														–												–	–
0x31	ECC	LIN_COEFF_32														LIN_COEFF_31												0x31	0x71
0x32	ECC									ANG_PRE_GAIN_OFFS														CORDIC_BYPASS	CORDIC_CHAN_ORDER	CORDIC_POL	0x32	0x72
0x33	ECC				BIN_HYST							ANG_GAIN																0x33	0x73
0x34	ECC	ANG_SAT_ROLLOVER								ANG_GAIN_SAT_EN	ANG_POST_GAIN_OFFS																ANG_OFFS_SAT_EN	0x34	0x74
0x35	ECC									MAGNETIC_THRESH_MAX								MAGNETIC_THRESH_MAX_EN	MAGNETIC_THRESH_MIN							MAGNETIC_THRESH_MIN_EN	0x35	0x75
0x36	ECC											ANG_CLAMP_LOWER																0x36	0x76
0x37	ECC		BW_ADAPT_MAX			BW_ADAPT_MIN			BW_SEL			ANG_CLAMP_UPPER																0x37	0x77
0x38	ECC						POWER_ON_DELAY			BW_ADAPT_DELAY											BW_ADAPT_EXP			BW_ADAPT_FRAC				0x78

Continued on next page...

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Table 36: Register Description – EEPROM and Shadow (continued)

EEPROM Address (hex)	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	EEPROM Address (hex)	Shadow Address (hex)
0x39	ECC			SENT_FRAME_RATE		SENT_INIT_SEL			SENT_ENCODING_SEL	SENT_CRC_SEL	SENT_EMSG_DIS	DIG_OUT_PULL_LIM_DIS	DIG_OUT_PULL_LIM			DIG_OUT_DATA_RATE						SENT_DATA_SEL				DIG_COMM_ID	DIG_OUT_SEL		0x39	0x79
0x3A	ECC					SENT_EMSG_ERR_REPEAT	SENT_EMSG_SEL																					0x3A	0x7A
0x3B	ECC	ENHANCED_SETTINGS_UNLOCK	SPARE_0X3B	DIG_OUT_PUSH_LIM				DIG_OUT_PUSH_LIM_SEL	SAT_COR_MASK	SAT_LIN_MASK	ACF_FAULT_FILT	FAULT_FILT				OVD_MASK	UVD_MASK	SPE_MASK	ESE_MASK	POR_MASK	SRR_MASK	SLF_MASK	OFE_MASK	SAT_MASK	TSE_MASK	AOC_MASK	ACF_MASK	0x3B	0x7B
0x3C	ECC	ANA_MANCH_LOCK	MEM_LOCK_SEL				MANCH_ACCESS_SEL		TEST_MODE_DIS	OVD_SEL	UVD_SEL	SPARE_0X3C				ANA_RANGE_SEL		ANA_BW_SEL	DIG_OUT_ERR_RESP_SEL	ERR_RESP_SEL			ERR_HOLD_SEL		ANA_LOCK	DIG_COMM_INPUT_HIGH	DIG_COMM_INPUT_LOW	0x3C	0x7C
0x3D	ECC	SPARE_0X3D																										0x3D	0x7D
0x3E	ECC	SPARE_0X3E																										0x3E	0x7E
0x3F	ECC	SPARE_0X3F																										0x3F	0x7F

The table above shows the location of all customer-accessible EEPROM registers. Additionally, Shadow registers are mirrored in volatile space to allow quick access to the values during operating. All Shadow registers are located at an address 0x40 higher than the EEPROM register of which it is a copy. The Shadow registers are written with copies of the data from EEPROM at power up, and when an EEPROM write is performed. Values that are manually written to Shadow take effect immediately, and last until they are reset either by a changing the Shadow register itself, changing the EEPROM register, or power cycling the device. This allows quick testing of parameters with no risk of permanently changing the device performance. It also reduces the number of EEPROM writes required during testing which can improve test time, as EEPROM writes take longer than Shadow writes.

For all EEPROM and Shadow registers the first 6 most significant bits [31:26] are dedicated to ECC bits. These are used for internal testing to allow the device to correct single bit disturbances and detect double bit disturbances when copying EEPROM into Shadow. When performing an EEPROM/Shadow write there is no need to manually calculate the ECC bits. The ECC bits are ignored and replaced with the internally calculated values. During an EEPROM/Shadow read, the ECC bits will be transmitted along with the rest of the register data and may be ignored.

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EEPROM 0x05 / Shadow 0x45

ANA_INIT_SEL (BIT 24)

Selects the analog output value directly following power up, after EEPROM is loaded into Shadow.

- If ANA_INIT_SEL = 0, the analog output drives LOW until the first data from the internal filtering is available.
- If ANA_INIT_SEL = 1, the analog output drives HIGH until the first data from the internal filtering is available.

DIG_OUT_DRIVE_SEL (BIT 23)

Selects the digital output driver mode.

- If DIG_OUT_DRIVE_SEL = 0 the digital output driver functions as a push-pull output.
- If DIG_OUT_DRIVE_SEL = 1 the digital output driver functions as an open-drain output.

CHAN_B_HYST (BITS 22:13)

Selects the amount of hysteresis present on channel B of the 1-D signal path. This value directly selects the number of LSBs of hysteresis applied to each channel at a 1:1 ratio.

CHAN_A_HYST (BITS 12:3)

Selects the amount of hysteresis present on channel A of the 1-D signal path. This value directly selects the number of LSBs of hysteresis applied to each channel at a 1:1 ratio.

ANA_CAP_SEL (BITS 2:0)

This should be selected based on the capacitive load connected to the analog output. This setting has no impact on digital interfaces.

EEPROM 0x15 / Shadow 0x55

EEPROM 0x15 can be factory-accessible or customer-accessible based on the bit ENHANCED_SETTINGS_UNLOCK. When ENHANCED_SETTINGS_UNLOCK = 0, EEPROM 0x15 is considered Factory space and cannot be written to at customer level. This can be used to prevent accidental changes to this value.

SPARE_0X15 (BITS 15:11)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.

CHAN_ORTHOG (BITS 10:2)

CHAN_ORTHOG determines the phase correction that is applied to channel B for the purposes of removing orthogonality error.

CHAN_B_DIS (BIT 1)

Disables channel B when set.

- If CHAN_B_DIS = 0, Channel B operates normally.
- If CHAN_B_DIS = 1, Channel B is disabled.

CHAN_A_DIS (BIT 0)

Disabled channel A when set.

- If CHAN_A_DIS = 0, Channel A operates normally.
- If CHAN_A_DIS = 1, Channel A is disabled.

EEPROM 0x16 / Shadow 0x56

ANG_THRESH_HIGH (BITS 16:9)

Sets a high angle saturation point before gain is applied to the angle. A diagnostic flag will trigger if the angle recorded is above the programmed value. ANG_THRESH_HIGH can be set between 0 and 360 degrees with 1.41-degree steps. Since the value into the comparison is rolled over to 0-360, an ANG_THRESH_HIGH value of 0 will always result in an error flag, and an ANG_THRESH_HIGH value of 255 will never result in an error flag.

ANG_THRESH_LOW (BITS 8:1)

Sets a low angle saturation point before gain is applied to the channel. A diagnostic flag will trigger if the angle recorded is below the programmed value. ANG_THRESH_LOW can be set between 0 and 360 degrees with 1.41 degree steps. Since the value into the comparison is rolled over to 0-360, an ANG_THRESH_LOW value of 0 will never result in an error flag, and an ANG_THRESH_LOW value of 255 will always result in an error flag.

ANG_THRESH_LOW/HIGH	Degrees
0	0
x	x × 1.41
255	360

ANG_THRESH_EN (BIT 0)

Enables the pre-gain saturation check.

- ANG_THRESH_EN = 0, Angle threshold check is disabled.
- ANG_THRESH_EN = 1, Angle value prior to gain block is checked against the programmed thresholds ANG_THRESH_(LOW/HIGH) to set the thresholds ANG_THRESH_(LOW/HIGH) diagnostic flag.

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EEPROM 0x17 / Shadow 0x57

CHAN_A_POL (BIT 14)

Changes the polarity of channel A when set.

- CHAN_A_POL = 0, Channel A follows axis definition.
- CHAN_A_POL = 1, Channel A polarity is inverted.

CHAN_A_OFFS (BITS 13:0)

Customer offset trim at room temperature for channel A.

EEPROM 0x18 / Shadow 0x58

CHAN_A_OFFS_TC1_HOT (BITS 23:12)

Customer 1st order offset trim for room to hot slope of channel A.

CHAN_A_OFFS_TC1_COLD (BITS 11:0)

Customer 1st order offset trim for room to cold slope of channel A.

EEPROM 0x19 / Shadow 0x59

CHAN_A_SENS (BITS 13:0)

Customer sensitivity trim at room temperature for channel A.

EEPROM 0x1A / Shadow 0x5A

CHAN_A_SENS_TC1_HOT (BITS 21:11)

Customer 1st order sensitivity trim for room to hot slope of channel A.

CHAN_A_SENS_TC1_COLD (BITS 10:0)

Customer 1st order sensitivity trim for room to cold slope of channel A.

EEPROM 0x1B / Shadow 0x5B

CHAN_A_SENS_TC2_HOT (BITS 19:10)

Customer 2nd order sensitivity trim for room to hot slope of channel A.

CHAN_A_SENS_TC2_COLD (BITS 9:0)

Customer 2nd order sensitivity trim for room to cold slope of channel A.

EEPROM 0x1C / Shadow 0x5C

CHAN_B_POL (BIT 14)

Changes the polarity of channel B when set.

- CHAN_B_POL = 0, Channel B follows axis definition.
- CHAN_B_POL = 1, Channel B polarity is inverted.

CHAN_B_OFFS (BITS 13:0)

Customer offset trim at room temperature for channel B.

EEPROM 0x1D / Shadow 0x5D

CHAN_B_OFFS_TC1_HOT (BITS 23:12)

Customer 1st order offset trim for room to hot slope of channel B.

CHAN_B_OFFS_TC1_COLD (BITS 11:0)

Customer 1st order offset trim for room to cold slope of channel B.

EEPROM 0x1E / Shadow 0x5E

CHAN_B_SENS (BITS 13:0)

Customer sensitivity trim at room temperature for channel B.

EEPROM 0x1F / Shadow 0x5F

CHAN_B_SENS_TC1_HOT (BITS 19:10)

Customer 1st order sensitivity trim for room to hot slope of channel B.

CHAN_B_SENS_TC1_COLD (BITS 9:0)

Customer 1st order sensitivity trim for room to cold slope of channel B.

EEPROM 0x20 / Shadow 0x60

TEMPERATURE_OFFS (BITS 24:20)

Customer temperature offset trim. Value is added to the temperature reported, represented in 2's complement format, step size is 0.5°C/LSB.

CHAN_B_SENS_TC2_HOT (BITS 21:11)

Customer 2nd order sensitivity trim for room to hot slope of channel B.

CHAN_B_SENS_TC2_COLD (BITS 10:0)

Customer 2nd order sensitivity trim for room to cold slope of channel B.

EEPROM 0x21 / Shadow 0x61

LIN_COEFF_0 (BITS 25:13)

Linearization coefficient number 0. Functionality is based on linearization mode and scalar. See Linearization section for details.

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SPARE_0X21 (BITS 12:10)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.

LIN_COEFF_ACTIVE (BITS 9:5)

Determines the number of active linearization coefficients. See Linearization section for details.

LIN_COEFF_SCALAR (BITS 4:3)

Determines what scalar quantity is applied to the LIN_COEFF_X values. See Linearization section for details.

LIN_SEL (BITS 2:1)

Determines what function the linearization block performs on the signal path.

LIN_ENABLE (BIT 0)

Enables the linearization block when set.

- If LIN_ENABLE = 0, linearization is disabled, and all related registers have no effect on device operation.
- If LIN_ENABLE = 1, linearization is enabled, and functions based on the linearization settings.

EEPROM 0x22 / Shadow 0x62

LIN_COEFF_2 (BITS 25:13)

Linearization coefficient number 2. Functionality is based on linearization mode and scalar. See Linearization section for details.

LIN_COEFF_1 (BITS 12:0)

Linearization coefficient number 1. Functionality is based on linearization mode and scalar. See Linearization section for details.

EEPROM 0x23 – 0x31 / Shadow 0x63 – 0x71

LIN_COEFF_XX (BITS 25:13 & BITS 12:0)

The remaining linearization coefficients are stored in EEPROM registers 0x23 through 0x31. They follow the same pattern as EEPROM 0x22 with the higher coefficient value stored in bits 25:13 of the register, and the lower coefficient value stored in bits 12:0.

EEPROM 0x32 / Shadow 0x72

ANG_PRE_GAIN_OFFS (BITS 17:3)

The 2's complement value that is added to the digital angle prior to the gain stage of the short stroke block.

CORDIC_BYPASS (BIT 2)

Bypasses the CORDIC angle calculation when set. The value that is passed through is based on the CORDIC_CHAN_ORDER bit.

- If CORDIC_BYPASS = 0, device performs CORDIC angle calculation based on channel A and channel B data.
- If CORDIC_BYPASS = 1, no CORDIC calculation is performed, and the device passes through channel A or B directly through the rest of the signal path.

CORDIC_CHAN_ORDER (BIT 1)

Determines the order of inputs to the CORDIC calculation or determines which channel to pass when CORDIC_BYPASS = 1.

CORDIC_BYPASS	CORDIC_CHAN_ORDER	Output of CORDIC
0	0	atan2(chanA, chanB)
0	1	atan2(chanB, chanA)
1	0	chanA+32768
1	1	chanB+32768

CORDIC_POL (BIT 0)

Inverts the polarity of the output of the CORDIC when set.

EEPROM 0x33 / Shadow 0x73

BIN_HYST (BITS 22:16)

Determines the amount of hysteresis for each bin when using binning mode of linearization.

ANG_GAIN (BITS 15:0)

Determines the amount of that is applied to the signal within the short stroke block.

EEPROM 0x34 / Shadow 0x74

ANG_SAT_ROLLOVER (BITS 25:18)

Determines the saturation rollover point for the post gain signal value.

ANG_GAIN_SAT_EN (BIT 17)

Determines the signal functionality in cases where the digital value exceeds the value set by the ANG_SAT_ROLLOVER.

- If ANG_GAIN_SAT_EN = 0, the angle will rollover back to 0.
- If ANG_GAIN_SAT_EN = 1, the angle will saturate high or low based on the pre gain angle and ANG_SAT_ROLLOVER.

ANG_POST_GAIN_OFFS (BITS 16:1)

Offset value added to the digital signal after the gain of the short stroke block.

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ANG_OFFS_SAT_EN (BIT 0)

Enables the post gain saturation feature when set.

- If ANG_OFFS_SAT_EN = 0 device will output the value after gain and offset, ignoring ANG_SAT_ROLLOVER.
- If ANG_OFFS_SAT_EN = 1 the device will either rollover or saturate the signal at the ANG_SAT_ROLLOVER based on the ANG_GAIN_SAT_EN bit.

EEPROM 0x35 / Shadow 0x75

MAGNETIC_THRESH_MAX (BITS 17:10)

Sets the maximum magnetic magnitude threshold. All values above this set value will trigger an error flag.

MAGNETIC_THRESH_MAX_EN (BIT 9)

Enables the maximum magnetic threshold checking when enabled.

- If MAGNETIC_THRESH_MAX_EN = 0, MAGNETIC_THRESH_MAX is ignored.
- If MAGNETIC_THRESH_MAX_EN = 1, magnetic magnitude is compared against MAGNETIC_THRESH_MAX and will trigger a flag if condition fails.

MAGNETIC_THRESH_MIN (BITS 8:1)

Sets the minimum magnetic magnitude threshold. All values below this set value will trigger an error flag.

MAGNETIC_THRESH_MIN_EN (BIT 0)

Enables the minimum magnetic threshold checking when enabled.

- If MAGNETIC_THRESH_MIN_EN = 0, MAGNETIC_THRESH_MIN is ignored.
- If MAGNETIC_THRESH_MIN_EN = 1, magnetic magnitude is compared against MAGNETIC_THRESH_MIN and will trigger a flag if condition fails.

EEPROM 0x36 / Shadow 0x76

CLAMP_LOWER (BITS 15:0)

Sets the low clamp value for the output of the digital signal path. All signals below this value will be limited to this value.

EEPROM 0x37 / Shadow 0x77

BW_ADAPT_MAX (BITS 24:22)

Sets the maximum bandwidth of the adaptive filter.

BW_ADAPT_MIN (BITS 21:19)

Sets the minimum bandwidth of the adaptive filter.

BW_SEL (BITS 18:16)

Determines which bandwidth settings to use for internal filtering.

BW_SEL	Bandwidth (Hz)
0	329.1
1	465.8
2	556
3	700
4	1000
5	1482
6	2024
7	Adaptive

CLAMP_LOWER (BITS 15:0)

Sets the upper clamp value for the output of the digital signal path. All signals above this value will be limited to this value.

EEPROM 0x38 / Shadow 0x78

POWER_ON_DELAY (BITS 20:18)

Selects the length of time for which the device will output the POR condition before beginning to transmit data. See Sensor Output During Low-Pass Filter Initialization section for more details.

POWER_ON_DELAY	Additional Delay (ms)
0	0.5
1	1.0
2	1.5
3	2.0
4	2.5
5	3.0
6	4.0
7	0.0

BW_ADAPT_DELAY (BITS 17:8)

Number of clock cycles at 8 MHz delay before the adaptive filter bandwidth decreases.

BW_ADAPT_EXP (BITS 7:4)

Exponential gain of the feedforward adaptive filter loop.

BW_ADAPT_FRACT (BITS3:0)

Fractional gain of the feedforward adaptive filter loop.

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EEPROM 0x39 / Shadow 0x79

SENT_FRAME_RATE (BITS 23:22)

Sets the frame rate when using paused SENT.

SENT_FRAME_RATE	Frame Rate including pause pulse
0	3 data nibbles: frame length 210 t_{tick} 4 data nibbles: frame length 228 t_{tick} 6 data nibbles: frame length 282 t_{tick}
1	0.5 ms
2	1.0 ms
3	2.0 ms

SENT_INIT_SEL (BITS 21:19)

Selects which data the SENT interface will transmit during the initialization time. If no initialization time is selected this register does nothing.

SENT_INIT_SEL	n-bit data Output
0	0
1	$2^n - 7$
2	$2^n - 4$
3	$2^n - 3$
4	$2^n - 2$
5	$2^n - 1$
6	0
7	0

SENT_ENCODING_SEL (BIT 18)

Selects SENT data mapping for SENT configurations 0, 4, 7, and 15.

- If SENT_ENCODING_SEL = 0, mapping is disabled, SENT will output the data as it appears in the registers.
- If SENT_ENCODING_SEL = 1, output SENT data is remapped per the table below.

DATA Value	SENT Output
0	1
1 through $2^n - 8$	Unchanged
≥ $2^n - 8$	$2^n - 8$
SCN 1 Error flag	$2^n - 5$
SCN 2 Error flag	$2^n - 6$
Not Valid	0

* n is the number of bits in the data of the SENT packet.

** Not valid refers to the period of time after power up before the SENT interface receives the first valid update from the signal path.

SENT_CRC_SEL (BIT 17)

Includes the SCN nibble in the CRC calculations when set.

SENT_EMSG_DIS (BIT 16)

Disables SENT serial message when set.

DIG_OUT_PULL_LIM_DIS (BIT 15)

Disables slew rate control for digital interfaces when set.

DIG_OUT_PULL_LIM (BITS 14:12)

Selects the slew rate control for digital interfaces.

DIG_OUT_DATA_RATE (BITS 11:7)

Selects the tick time if using SENT interface or the period when using the PWM interface. This register has no effect on analog output devices.

SENT_DATA_SEL (BITS 6:3)

Selects the SENT data configuration.

DIG_COMM_ID (BIT 2)

Sets the device ID for Manchester communication protocol.

DIG_OUT_SEL (1:0)

Selects the output mode for digital interface devices. This register has no effect on analog output devices.

DIG_OUT_SEL	Output Protocol
0	PWM
1	SENT
2	SENT with Pause Pulse
3	PWM

EEPROM 0x3A / Shadow 0x7A

SENT_EMSG_ERR_REPEAT (BIT 21)

Enables SENT EMSG to repeat error message when set.

SENT_EMSG_SEL (BITS 20:0)

Selects which EMSG messages will be sent.

EEPROM 0x3B / Shadow 7B

ENHANCED_SETTINGS_UNLOCK (BIT 25)

Enables write access to register 0x16 when set.

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SPARE_0X3B (BITS 24:23)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.

DIG_OUT_PUSH_LIM (BITS 22:20)

Selects the digital output push driver current limit. Approximate current limits are provided below:

Settings	Current Limit (mA)
DIG_OUT_PUSH_LIM_DIS = 1	20
DIG_OUT_PUSH_LIM = 0	10
DIG_OUT_PUSH_LIM = 1	8.75
DIG_OUT_PUSH_LIM = 2	7.5
DIG_OUT_PUSH_LIM = 3	6.25
DIG_OUT_PUSH_LIM = 4	5
DIG_OUT_PUSH_LIM = 5	3.75
DIG_OUT_PUSH_LIM = 6	2.5
DIG_OUT_PUSH_LIM = 7	1.25

DIG_OUT_PUSH_LIM_DIS (BIT 19)

Disables the digital push driver current limit.

SAT_COR_MASK (BIT 18)

Disables the saturation correction error flag when set. This mask only affects the error flag reporting ability. It does not change the effect of the saturation on the signal path data.

SAT_LIN_MASK (BIT 17)

Disables the saturation linearization error flag when set. This mask only affects the error flag reporting ability. It does not change the effect of the saturation on the signal path data.

ACF_FAULT_FILT (BITS 16:15)

Filters the ACF fault condition, the error condition must be present for the number of cycles shown below before a fault flag is tripped.

ACF_FAULT_FILT	Cycles
0	0
1	2
2	4
3	8

FAULT_FILT (BITS 14:12)

Filters the SAT, AOC, and SRR flags; each error condition must be present for the number of cycles shown below before their respective flag is tripped.

FAULT_FILT	Cycles
0	0
1	2
2	4
3	8
4	16
5-7	0

OVD_MASK (BIT 11)

Disables the overvoltage detection error flag when set.

UVD_MASK (BIT 10)

Disables the undervoltage detection error flag when set.

SPE_MASK (BIT 9)

Disables the signal path error flag when set.

ESE_MASK (BIT 8)

Disables the EEPROM single bit error flag when set.

POR_MASK (BIT 7)

Disables the power-on reset error flag when set.

SRR_MASK (BIT 6)

Disables the signal radius out of range error flag when set.

SLF_MASK (BIT 5)

Disables the signal processing logic failure error flag when set.

OFE_MASK (BIT 4)

Disables the oscillator frequency error flag when set.

SAT_MASK (BIT 3)

Disables the saturation error flag when set.

TSE_MASK (BIT 2)

Disables the temperature sensor error flag when set.

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AOC_MASK (BIT 1)

Disables the angle outside of clamp error flag when set.

ACF_MASK (BIT 0)

Disables the analog check failure error flag when set.

EEPROM 0x3C / Shadow 0x7C

ANA_MANCH_LOCK (BIT 25)

Requires the unlock code for analog output when set.

MEM_LOCK_SEL (BITS 24:21)

Prevents writes to EEPROM memory when set.

MANCH_ACCESS_SEL (BITS 20:19)

Disables Manchester entry triggers.

MANCH_ACCESS_SEL	Manchester Entry Method
00	Manchester enabled by OVD or function pulses
01	Manchester enabled by OVD only
10	Manchester enabled by function pulses only
11	Manchester cannot be enabled

* Note: Setting MANCH_ACCESS_SEL = 11 prevents all further communication.

TEST_MODE_DIS (BIT 18)

Disables internal test modes which affect the device output (Margin testing). In order to perform margin testing with this bit active, it must first be cleared in Shadow before margin testing can be run. This is provided to prevent single bit error in volatile space from causing an invalid output.

OVD_SEL (BIT 17)

Selects which overvoltage value to use when determining if an overvoltage error occurred.

UVD_SEL (BIT 16)

Selects which undervoltage value to use when determining if an under-voltage error occurred.

SPARE_0X3C (BITS 15:13)

Spare bits that can be used as non-volatile storage within the device. This register has no effect on device performance.

ANA_RANGE_SEL (BITS 12:10)

Selects the scaling for the analog output DAC. This value only changes how the DAC is mapped. The spec table should be referenced to determine saturation and linearity limitations based on load circuity.

ANA_RANGE_SEL	DAC Scaling
0	0 - 100%
1	4 - 96%
2	5 - 95%
3	6 - 96%
4	7 - 93%
5	8 - 92%
6	10 - 90%
7	15 - 85%

ANA_BW_SEL (BIT 9)

Selects the filter setting just before data enters the analog driver.

- If ANA_BW_SEL = 0, filter is set to 15 kHz.
- If ANA_BW_SEL = 1, filter is set to 30 kHz.

The analog driver's frequency is below 15 kHz, so this setting does not affect device response times; it only affects noise filtering.

DIG_OUT_ERR_RESP_SEL (BIT 8)

Selects how the digital output responds to error flags.

- If DIG_OUT_ERR_RESP_SEL = 0, response will be 1/2 frequency for PWM and report error flags in diagnostic registers in SENT mode.
- If DIG_OUT_ERR_RESP_SEL = 1, response will be to enter High-Z state for any error flag.

ERR_RESP_SEL (BITS 7:6)

Selects how the analog output responds to error flags.

ERR_RESP_SEL	Analog Output
0	High-Z
1	Force High
2	Force Low
3	High-Z

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ERR_HOLD_SEL (BITS 5:3)

Sets the minimum number of angle updates with no flags set required before the analog output returns to normal operation after entering an error state. Also selects the number of updates the SENT and PWM interface report a UVD error condition for after returning to normal V_{CC} levels.

ERR_HOLD_SEL	Analog Release	Digital UVD Reports
0	0	1
1	1	2
2	2	4
3	4	8
4	8	16
5	16	32
6	32	64
7	64	128

ANA_LOCK (BIT 2)

Device requires an analog event to enable Manchester when set. Otherwise, Manchester is always active.

DIG_COMM_INPUT_HIGH (BIT 1)

Sets the threshold for the rising edge when determining Manchester data input.

DIG_COMM_INPUT_LOW (BIT 0)

Sets the threshold for the falling edge when determining Manchester data input. Also determines the low threshold for overdriving the output to initiate Manchester interface when in digital modes.

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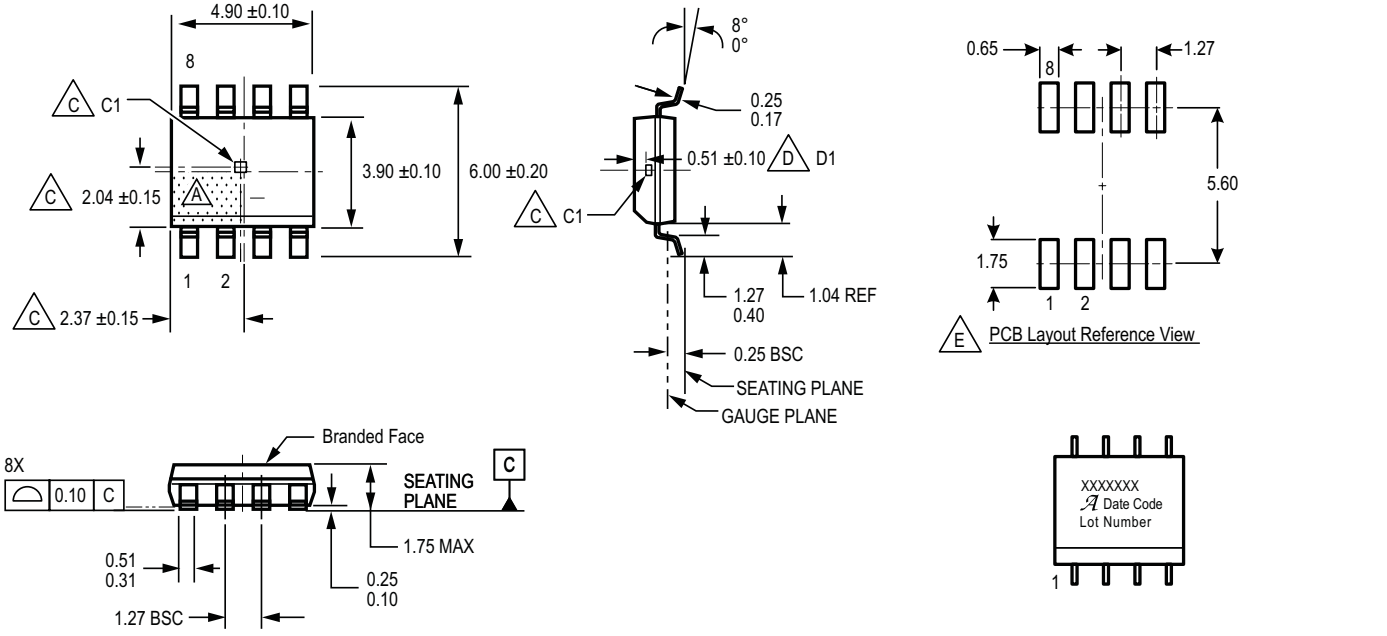
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference MS-012AA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Hall element (C1); not to scale

D Active Area Depth (D1); not to scale

E Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances.

B Standard Branding Reference View

Lines 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 33: Single Die SOIC-8 (OL suffix)

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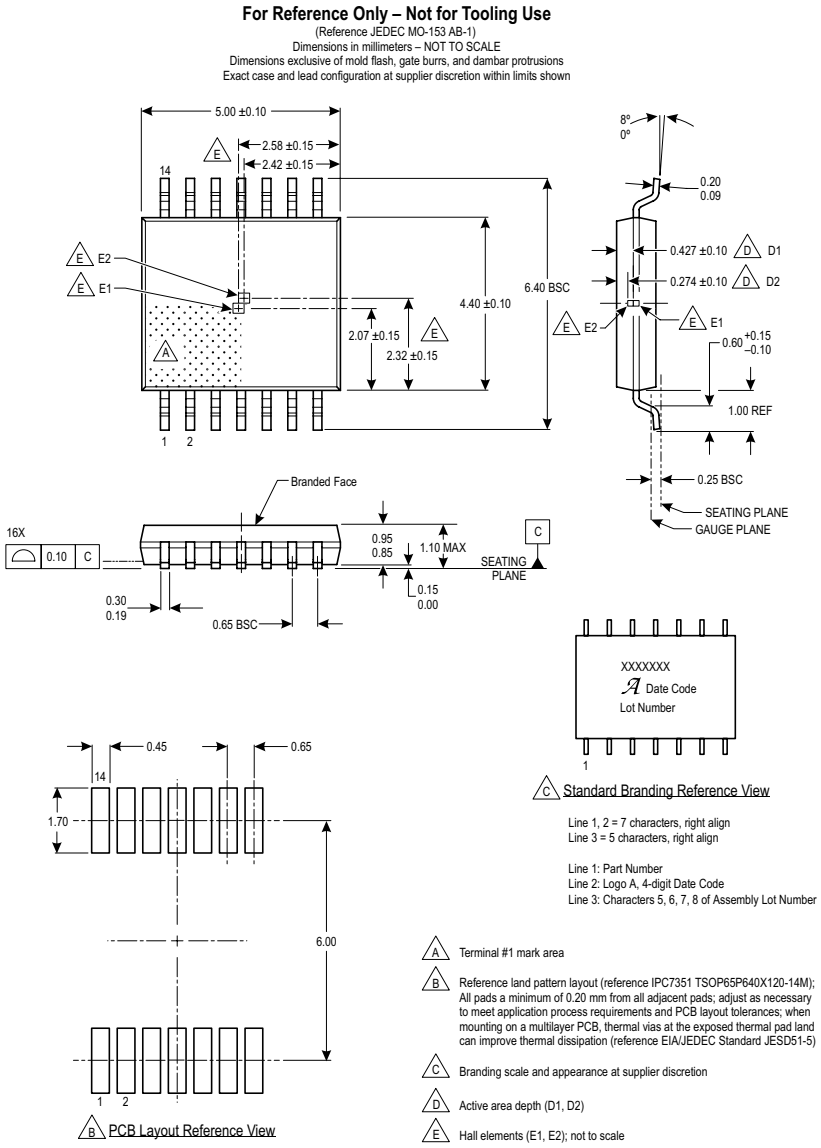

Figure 34: Dual Die TSSOP-14 (LU suffix)

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APPENDIX A: SPECIFICATION DEFINITIONS

Internal Definitions

The following definitions are used to provide a common language for terms used within specification definitions or equations. This is done to remove all ambiguity.

Test Angle (Θ)

This is the representation of the angle being tested. This is the target angle applied to the device and is a stand in for an array of angle between 0-360°.

Mechanical Angle ($Ang_{Mech}(\Theta)$)

This is the physical angle of the element meant to be measured. In many cases, such as on-axis, this is equivalent to the magnetic angle aside from a potential misalignment of the defined zero angle position. However, in some cases, such as off-axis or arc-magnets, this will differ from the magnetic angle due to the system's construction.

Despite the term "mechanical", this is also used to represent the angle created by the Allegro test hardware. This is because there is still a mechanical misalignment between the electrical angle the device sees and the applied angle due to the tolerances of placing the device.

Magnetic Angle ($Ang_{Mag}(\Theta)$)

This is the vector of the applied magnetic flux density seen by the part as defined in relation to the 0 angle of the device package and plane of rotation.

Electrical Angle ($Ang_{Elect}(\Theta)$)

This is the angle measured by the device. Often electrical angle can be used to refer to multiple different locations within the device's signal path. If no specific reference to a location is provided, the default is to assume the electrical angle is referring to the output of the device's digital signal path. The goal of most applications is to align the electrical angle with the mechanical angle.

Misalignment (φ_{Mis})

This is the angular offset between the mechanical angle and magnetic angle. In on-axis applications this is often the only difference between the two angles. For consistent sign values, the misalignment is defined as:

$$\varphi_{Mis} = Ang_{Mech} - Ang_{Mag}$$

Recorded Channel ($Chan_x$)

This is the value of the channel as recorded directly from the device after factory trimming. This is the CHAN_*x*_PRE_*y*B register of the device, where *x* is channel A, B, or C, and *y* denotes the resolution of the channel. In 2oo3 angle calculations, two channels are assigned to represent the sine and cosine components of the magnetic flux over angle. In this documentation, channels will be referred to by these components. Mapping device channels A, B, and C to these sinusoidal notations will be based on package axis definitions and the magnetic rotation plane.

In order to determine which channels are associated with which sinusoidal component, the definition is liked with the ATAN2 function of the device.

$$Ang_{Elect} = ATAN2(Chan_{Sin}, Chan_{Cos})$$

Channel Parameters ($Sens_x$, $Offs_x$, and Pha_x)

The measured channel parameters are defined as the sensitivity offset and phase of each channel provided by the FFT method as shown below. Since only two channels are used to calculate angle, any given angle sweep only provides the data for two channels when using this method. As noted above, these channels are assigned to the device's A, B, or C channels based on package definitions and plane of magnetic rotation.

$$fft(Chan_x) = \frac{1}{N}\sum_{n=0}^{N-1} Re_{(n)} + i \times Im_{(n)}$$

$$Sens_x = \frac{\sqrt{Re_{x(1)}{}^2 + Im_{x(1)}{}^2}}{B_{in}}$$

$$Offs_{LSB(x)} = Re_{x(0)}$$

$$Offs_{Gauss(x)} = \frac{Offs_{LSB(x)}}{Sens_x}$$

$$Pha_x = atan2\left(\frac{Im_{x(1)}}{Re_{x(1)}}\right)$$

where

x is the sine or cosine channel being measured, device channel

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A, B, or C;

B_{in} is the magnitude of the applied magnetic flux density in gauss;

N is the number of recorded samples;

$R_{e(n)}$ is the real portion of the output series for point n; and

$I_{m(n)}$ is the imaginary portion of the output series for point n.

Note: Since the FFT provides values in reference to a cosine function, the Phase_Sin is expected to have a value of –90°.

The generic equation for the channels as a function is provided below:

$$Chan_{Cos} = Sens_{Cos} \times B_{in} \times cos(Ang_{Mag} + Pha_{Cos}) + Offs_{LSB(Cos)}$$

$$Chan_{Sin} = Sens_{Sin} \times B_{in} \times sin(Ang_{Mag} + Pha_{Sin} + 90°) + Offs_{LSB(Sin)}$$

Angle Specifications

3D linear devices that calculate an internal angle are expected to provide specifications on the angle's performance. These specifications are similar to dedicated angle sensors and can be used interchangeably in many cases.

Angle Error

Angle error is the deviation of the reported angle from the applied angle. For this specification, the angle output is recorded at the end of the digital signal path using Manchester or other digital communication. This assumes no angle gain or offset is applied.

$$ERR_{Ang(\Theta)} = Ang_{Elect(\Theta)} - Ang_{Mag(\Theta)}$$

Since many systems, including Allegro's final test system, are only capable of measuring Ang_{Mech}, the following equation is more accurate to actual test conditions.

$$ERR_{Ang(\Theta)} = Ang_{Elect(\Theta)} - Ang_{Mech(\Theta)} - \varphi_{Mis}$$

where φ_{Mis} is measured as:

$\varphi_{Mis} = avg(Ang_{Elect(\Theta)} - Ang_{Mech(\Theta)})$, over a full rotation.

Angle Drift

Angle drift is the deviation of the reported angle over the parameter of interest from the reported angle under initial conditions.

$$DRIFT_{Ang,Temp}(\Theta) = Ang_{Elect}(t,T_A,\Theta) - Ang_{Elect}(t,T_R,\Theta)$$

$$DRIFT_{Ang,Life}(\Theta) = Ang_{Elect}(t,T_A,\Theta) - Ang_{Elect}(t_0,T_A,\Theta)$$

where:

t is any point in time over the operating life of the device, as simulated by qualification stress;

t_0 is a constant representing the point in time the device is installed into the final application;

T_A is the ambient temperature; this can be any value within the operating range of the device; and

T_R is a constant representing room temperature (25°C).

Channel Specifications

Each channel of the 3D linear device is a measurement of the magnetic flux density in the direction of that channel axis. When using a 3D linear device to detect the angle of a rotating magnet in the plane of the two selected channels, the magnetic flux in those directions is a sinusoidal function of magnetic flux magnitude and applied angle. The exact equation is based on how the device calculates angle.

Sensitivity Error

Sensitivity error is the percentage deviation of the channel sensitivity from the specified target sensitivity value.

$$ERR_{Sens(x)} = \frac{(Sens_x - Sens_{Target})}{Sens_{Target}} \times 100\ \%$$

Sensitivity Mismatch

Sensitivity mismatch is the deviation of each channel from the average sensitivity of the two selected channels. Based on which channel is referenced the mismatch may be positive or negative, but the magnitude will always be the same.

$$ERR_{Sens(Mis)} = \frac{Sens_{Sin} - Sens_{Cos}}{(Sens_{Sin} + Sens_{Cos})/2} \times 100\ \%$$

Offset Error

Channel offset provided as an input referred magnetic field value. In order to calculate this value from channel readings, divide the recorded LSB values by the measured sensitivity of the channel.

$$ERR_{Off(x)} = Offs_{Gauss(x)}$$

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Orthogonality Error

Orthogonality error is the degree to which the two selected channels are not orthogonal. Calculated as a difference in the direction of sensitivity error from ideal.

$$ERR_{Orthog} = ERR_{Phase(Cos)} - ERR_{Phase(Sin)}$$

where:

$ERR_{Phase(Cos)} = Pha_{Cos}$

$ERR_{Phase(Sin)} = Pha_{Sin} + 90°$

Linearity Error

Linearity error is the deviation of channel readings over applied magnetic field relative to a perfect line.

$$ERR_{Lin(x)} = \frac{Chan_x - (B_{Applied} \times Sens_x + Offs_{LSB(x)})}{B_{Applied} \times Sens_x + Offs_{LSB(x)}} \times 100\ \%$$

where

$B_{Applied}$ refers specifically to the flux applied in the direction of sensitivity of the channel.

Sensitivity Error Drift

Sensitivity error drift is the deviation of the channel sensitivity in percentage of target value over the parameter of interest from the sensitivity under initial conditions.

$$DRIFT_{Sens,Temp} = ERR_{Sens}(t,T_A) - ERR_{Sens}(t,T_R)$$

$$DRIFT_{Sens,Life} = ERR_{Sens}(t,T_A) - ERR_{Sens}(t_0,T_A)$$

Sensitivity Mismatch Drift

Sensitivity mismatch drift is the change in percentage of sensitivity mismatch with respect to initial conditions.

$$DRIFT_{Mis,Temp} = ERR_{Sens(Mis)}(t,T_A) - ERR_{Sens(Mis)}(t,T_R)$$

$$DRIFT_{Mis,Life} = ERR_{Sens(Mis)}(t,T_A) - ERR_{Sens(Mis)}(t_0,T_A)$$

Offset Drift

Offset drift is the deviation of channel offset with respect to initial conditions.

$$DRIFT_{Off,Temp} = ERR_{Off}(t,T_A) - ERR_{Off}(t,T_R)$$

$$DRIFT_{Off,Life} = ERR_{Off}(t,T_A) - ERR_{Off}(t_0,T_A)$$

Orthogonality Drift

Orthogonality drift is the deviation of orthogonality with respect to initial conditions.

$$DRIFT_{Orthog,Temp} = ERR_{Orthog}(t,T_A) - ERR_{Orthog}(t,T_R)$$

$$DRIFT_{Orthog,Life} = ERR_{Orthog}(t,T_A) - ERR_{Orthog}(t_0,T_A)$$

where:

t is any point in time over the operating life of the device, as simulated by qualification stress;

t_0 is a constant representing the point in time the device is installed into the final application;

T_A is the ambient temperature; this can be any value within the operating range of the device; and

T_R is a constant representing room temperature (25°C).

Analog Specifications

Devices which contain an analog output will need to specify how accurately this analog interface converts the digital output of the device into an analog signal.

Ratiometry

Analog ratiometric interfaces must specify a ratiometric accuracy, which is provided as a percentage error due to V_{CC} deviating from the target voltage all other specifications are tested at (typically 5 V).

$$RAT = \left(\frac{V_{OUT}(V_{CC})}{V_{cc}} - \frac{V_{OUT}(5\ V)}{5\ V} \right) \times 100\ \%$$

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Revision History

Number	Date	Description
–	March 23, 2020	Initial release
1	April 27, 2020	Updated Hall element tolerances (page 60-61)
2	August 20, 2020	Changed datasheet status from Advance Information to Final. Updated Features and Benefits, Applications, Description (page 1). Updated Selection Guide (page 2). Updated Table of Contents (page 3). Updated Absolute Maximum Ratings (page 4). Updated Operating Characteristics (page 8). Updated Performance Characteristics (pages 9-13). Updated Table 3 (page 16). Updated Functional Description (pages 14-37). Updated Programming Protocol (pages 38-46). Updated Memory Access (pages 50-62). Added temperature_offs description (page 56). Added Appendix A.
3	December 15, 2020	Updated Angle Error (XY) and Angle Error (XZ) test conditions (page 9). Removed Angle Micro Linearity Error (page 9). Updated Absolute Channel and Channel Drift test conditions and footnote 3 (page 10). Added Sent Output Resolution symbol (page 11). Updated SENT Supply Ripple Current test conditions (page 11). Updated footnote 3 (page 13). Updated Functional Description (page 14). Updated Figure 14 (page 15). Removed Factory Trimming section (page 16). Updated Table 4 and Equation 3 (page 17) and added Factory Correction section (page 17). Updated Sensitivity Adjustment section (page 18). Updated equation 15 (page 20) and 16 (page 21). Updated Linearization / Binning Mode Selection section and table headings (page 22-25). Updated equation 17 (page 26). Updated SENT Sampling Time and SENT Output Rate section (page 29). Updated Optional SENT Slow Serial Output Protocol (page 30). Updated SENT CRC section and Table 17 (page 32). Updated Table 19 (page 34). Updated Figure 26 (page 38). Added Auxiliary Interrupt Pulses figures and table (page 40). Updated Equation 19 (page 44). Updated CHAN_B_HYST and CHAN_A_HYST sections (page 55). Updated CHAN_B_SENS_TC2_HOT and CHAN_B_SENS_TC2_COLD bits (page 56). Updated ANG_GAIN_SAT_EN section (page 57). Removed Angle Micro Linearity Error section (page A-2)
4	January 11, 2021	Updated Manchester Input Thresholds maximum value (page 11), PWM Saturation Voltage values (page 12), and Variable Segment Binning (LIN_SEL_3) section (page 25); corrected Table 34 references (pages 44-49).
5	March 4, 2021	Added PCB layout reference drawing to OL-8 package drawing (page 64)
6	March 12, 2021	Added 3DMAG branding (page 1)
7	March 26, 2021	Updated ASIL status (page 1)
8	May 18, 2021	Updated trademarked 3DMAG branding and placement (page 1)
9	September 20, 2022	Updated SENT_ENCODING_SEL table (page 60)
10	July 3, 2024	Added footnote 2 (page 8)
11	March 26, 2025	Updated registers to current standard (uppercase); corrected storage temperature max value (page 4)
12	August 14, 2025	Corrected CHAN_B_SENS_TC1_COLD register name (page 54)

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