# TGA2595

## 27.5 – 31 GHz 9 W GaN Power Amplifier

## Product Description

Qorvo's TGA2595 is a balanced Ka-band power amplifier fabricated on Qorvo's 0.15 um GaN on SiC process. The balanced configuration supports low return loss and improves robustness into non-ideal loads.

Operating from 27.5 to 31 GHz, it achieves 9 W saturated output power, power-added efficiency of 22 % and 30 dB small signal gain. Along with excellent linear characteristics, the TGA2595 is ideally suited to support both commercial and defense related satellite communications.

To simplify system integration, the TGA2595 is fully matched to 50 Ω with integrated DC blocking caps on both I/O ports.

The TGA2595 is 100 % DC and RF tested on-wafer to ensure compliance to electrical specifications.

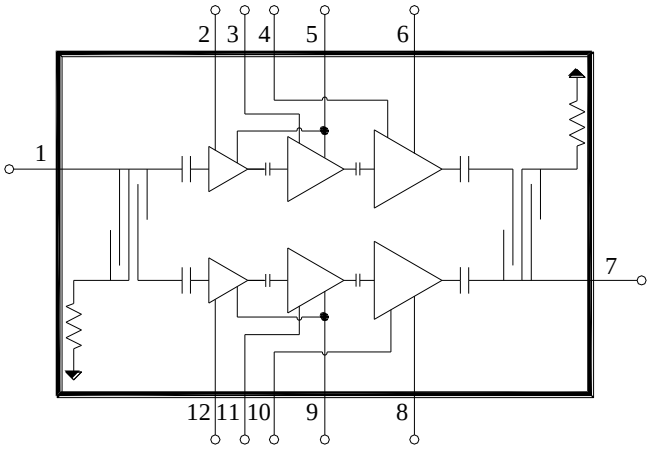
Lead-free and RoHS compliant.


## Product Features

- Frequency Range: 27.5 to 31 GHz
- $P_{OUT}$: 39 dBm ($P_{IN}$ = 22 dBm), CW
- PAE: 22 % ($P_{IN}$ = 22 dBm), CW
- Small Signal Gain: 30 dB
- Return Loss: 20 dB
- IM3 @ 33 dBm/tone: −30 dBc
- IM5 @ 33 dBm/tone: −35 dBc
- Bias: $V_D$ = +20 V, $I_{DQ}$ = 280-560 mA, $V_G$ ≈ −2.5 V Typical
- Chip Dimensions: 3.60 x 3.24 x 0.10 mm

*Performance is typical across frequency. Please reference electrical specification table and data plots for more details.*

## Functional Block Diagram




## Applications

- Satellite Communications

## Ordering Information

| Part No. | Description |
|---|---|
| TGA2595 | 27.5 – 31GHz 9W GaN Power Amplifier |
| TGA2595EVB | Evaluation Board for TGA2595 |

## Absolute Maximum Ratings

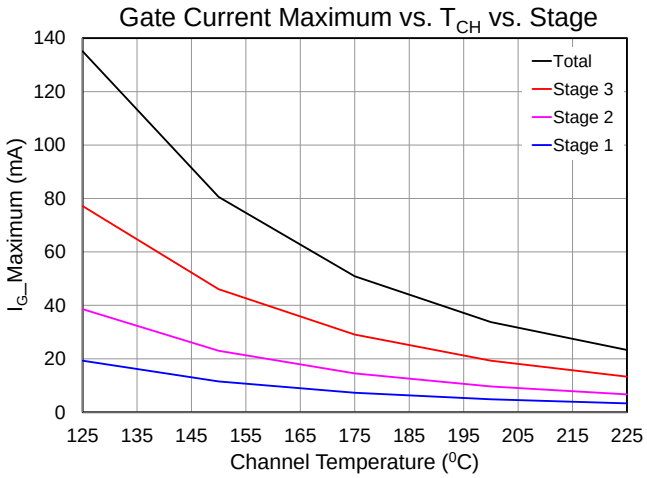
| Parameter | Value / Range |
|---|---|
| Drain Voltage ($V_D$) | 29.5 |
| Gate Voltage Range ($V_G$) | −5 to 0 V |
| Drain Current ($I_D$) | 2.8 A |
| Gate Current ($I_G$) | See chart |
| Power Dissipation ($P_{DISS}$), CW, 85°C | 44 W |
| Input Power ($P_{IN}$), CW, 50 Ω, $V_D$=22 V, $I_{DQ}$=280 mA, 85 °C | 30 dBm |
| Input Power ($P_{IN}$), CW, 10:1 VSWR, $V_D$=22 V , $I_{DQ}$=280 mA, 25 °C | 25 dBm |
| Channel Temperature ($T_{CH}$) | 275 °C |
| Mounting Temperature (30 seconds) | 320 °C |
| Storage Temperature | −40 to 150 °C |

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Drain Voltage ($V_D$) | | +20 | | V |
| Drain Current, Quiescent ($I_{DQ}$) | | 280-560 | | mA |
| Drain Current, RF ($I_{D\_Drive}$) | See charts page 6 | | | mA |
| Gate Voltage Typ. Range ($V_G$) | −2 to −3 | | | V |
| Operating Temp. Range | −40 | +25 | +85 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.




## Electrical Specifications

| Parameter | Conditions (1) (2) | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Operational Frequency Range | | 27.5 | | 31 | GHz |
| Output Power at Saturation, $P_{SAT}$ | $P_{IN}$ = +22 dBm | 37 | 39 | | dBm |
| Power Added Efficiency, PAE | $P_{IN}$ = +22 dBm | | 22 | | % |
| Small Signal Gain, S21 | | 24 | 30 | | dB |
| Input Return Loss, IRL | | | 20 | | dB |
| Output Return Loss, ORL | | | 20 | | dB |
| 3RD Intermodulation Products, IM3 | $P_{OUT/TONE}$ = +33 dBm, $I_{DQ}$ = 325 mA | | −30 | | dBc |
| 5th Intermodulation Products, IM5 | $P_{OUT/TONE}$ = +33 dBm, $I_{DQ}$ = 325 mA | | −35 | | dBc |
| $P_{SAT}$ Temperature Coefficient | $T_{DIFF}$ = +25°C to +85°C; $P_{IN}$ = +22 dBm | | −0.01 | | dBm/°C |
| S21 Temperature Coefficient | $T_{DIFF}$ = −40°C to +85°C | | −0.09 | | dB/°C |

Notes:
1. Test conditions unless otherwise noted: CW, $V_D$ = +20 V, $I_{DQ}$ = 560 mA, $V_G$ = -2.5 V +/- 0.5 V typical , $T_{BASE}$ = +25 °C, $Z_0$ = 50 Ω
2. $T_{BASE}$ is back side of carrier plate

## Thermal and Reliability Information

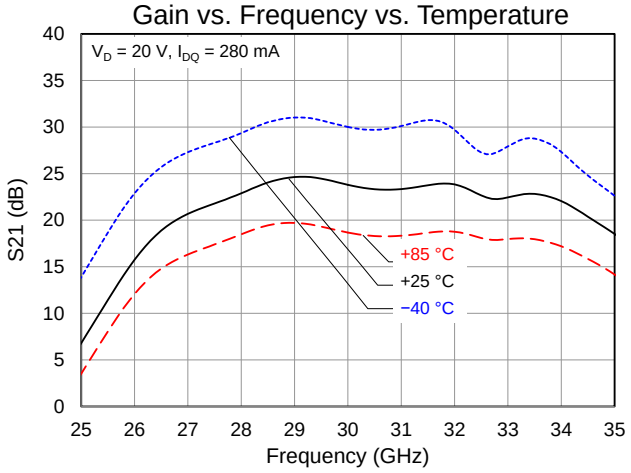
| Parameter | Test Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance ($\theta_{JC}$) | For $I_{DQ}$ = 280 mA:<br>$T_{BASE}$ = 85 °C, $V_D$ = +20 V, $I_{D\_Drive}$ = 1600 mA,<br>$P_{IN}$ = 22 dBm, $P_{OUT}$ = 39 dBm, $P_{DISS}$ = 24 W | 2.83 | ºC/W |
| Channel Temperature ($T_{CH}$) under RF Drive | | 153 | °C |
| Thermal Resistance ($\theta_{JC}$) | For $I_{DQ}$ = 560 mA:<br>$T_{BASE}$ = 85 °C, $V_D$ = +20 V, $I_{D\_Drive}$ = 1780 mA,<br>$P_{IN}$ = 22 dBm , $P_{OUT}$ = 39.5 dBm, $P_{DISS}$ = 26.7 W | 2.82 | ºC/W |
| Channel Temperature ($T_{CH}$) under RF Drive | | 160 | °C |

Notes:
1. Thermal resistance measured to back of carrier plate. MMIC mounted on 20 mils CuMo carrier using 1.5 mil 80/20 AuSn.
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

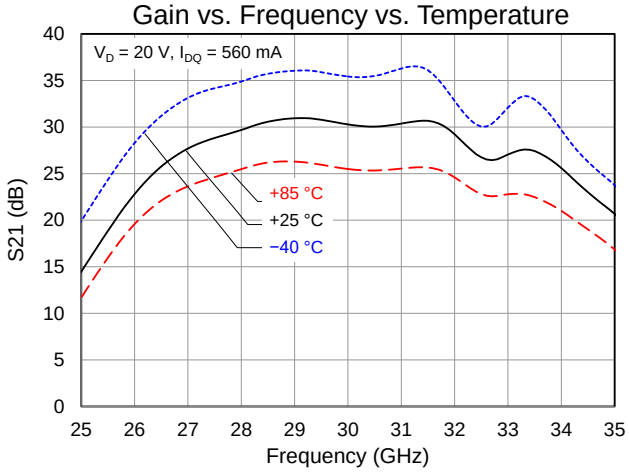
## Typical Performance – Small Signal

Test conditions unless otherwise noted: CW, $V_D$ = +20 V, $I_{DQ}$ = 280 mA and 560mA, $T_{BASE}$ =+25 °C

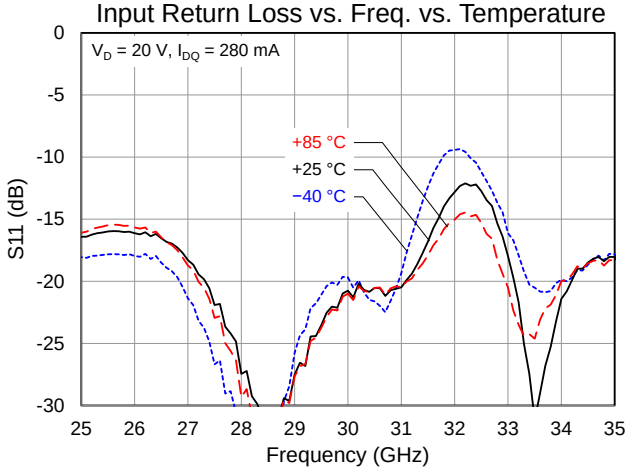
Gain vs. Frequency vs. Temperature



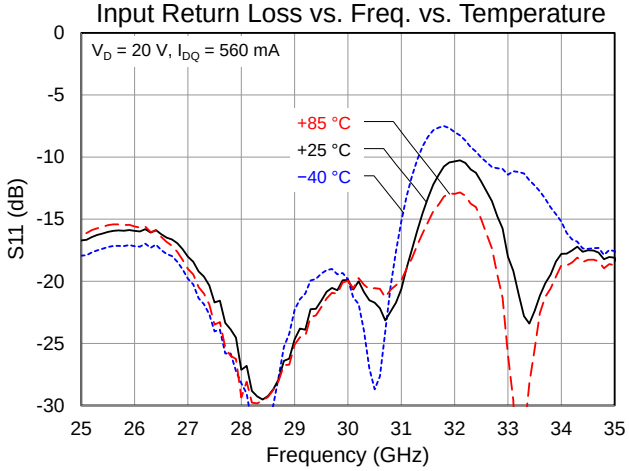

Gain vs. Frequency vs. Temperature



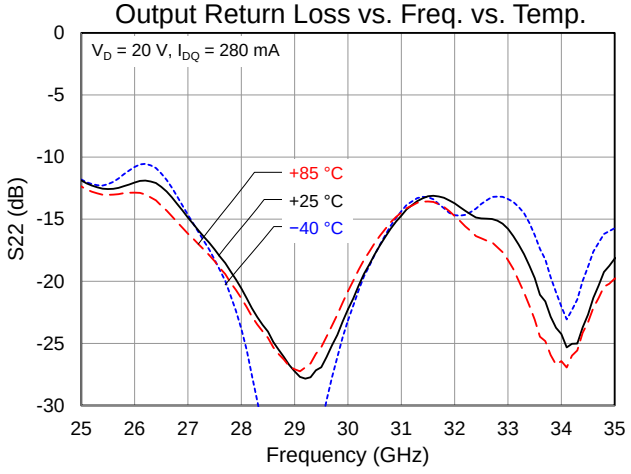

Input Return Loss vs. Freq. vs. Temperature



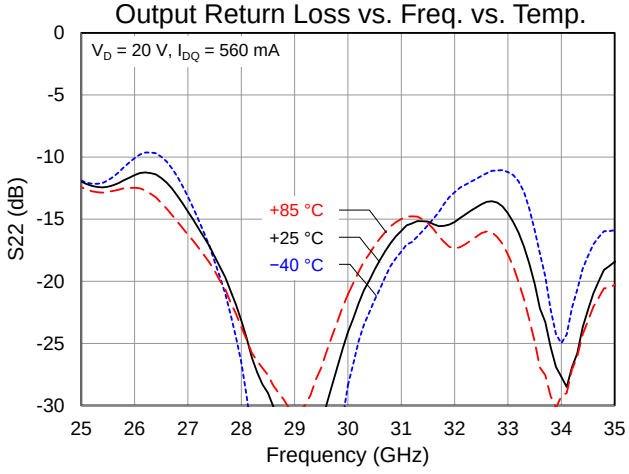

Input Return Loss vs. Freq. vs. Temperature




Output Return Loss vs. Freq. vs. Temp.

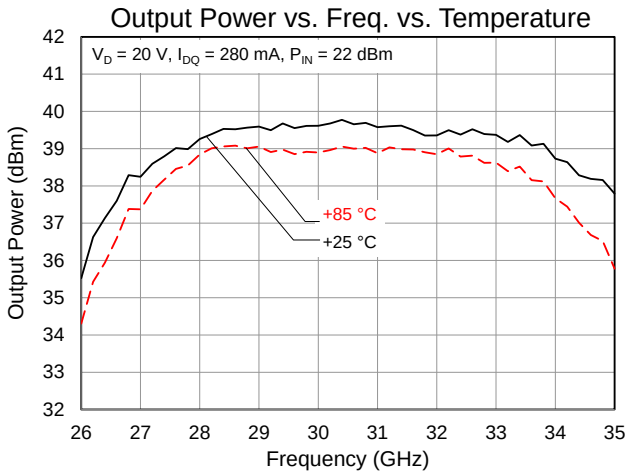


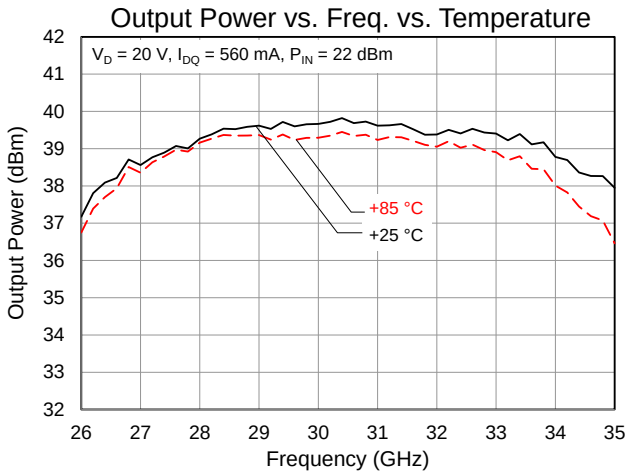

Output Return Loss vs. Freq. vs. Temp.

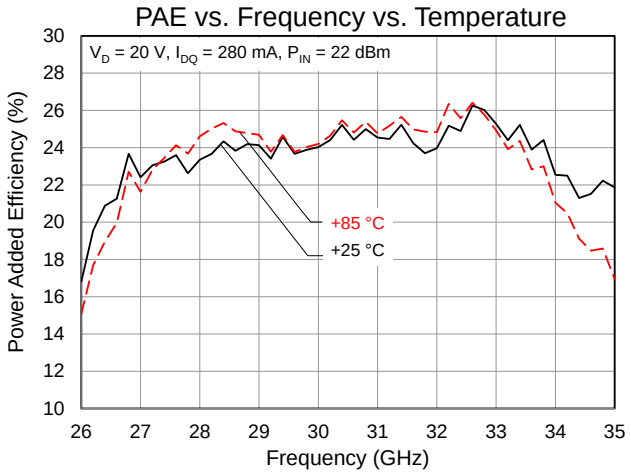


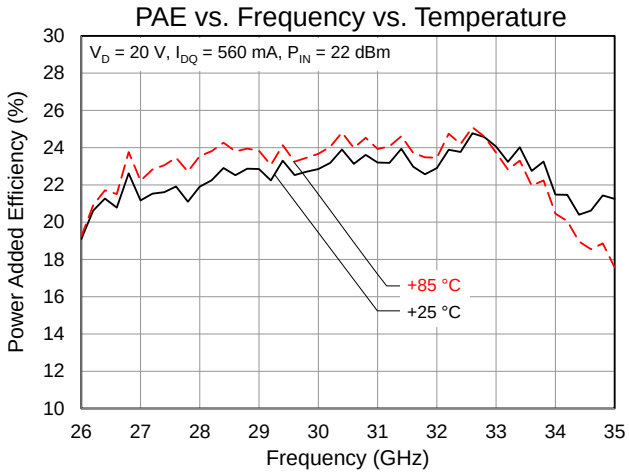
## Typical Performance – Large Signal

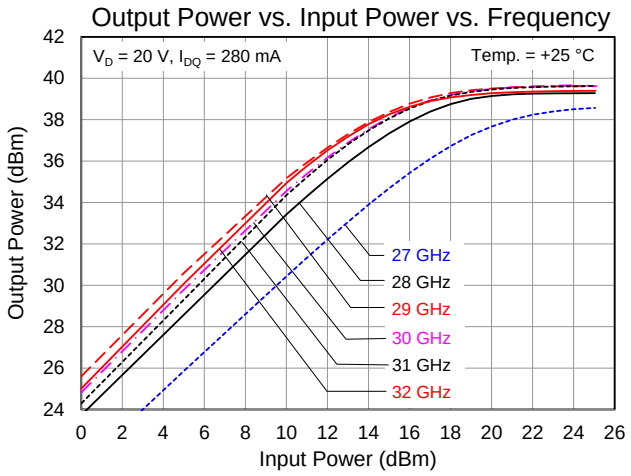
Test conditions unless otherwise noted: CW, $V_D$ = +20 V, $I_{DQ}$ = 280 mA and 560mA, $T_{BASE}$ =+25 °C

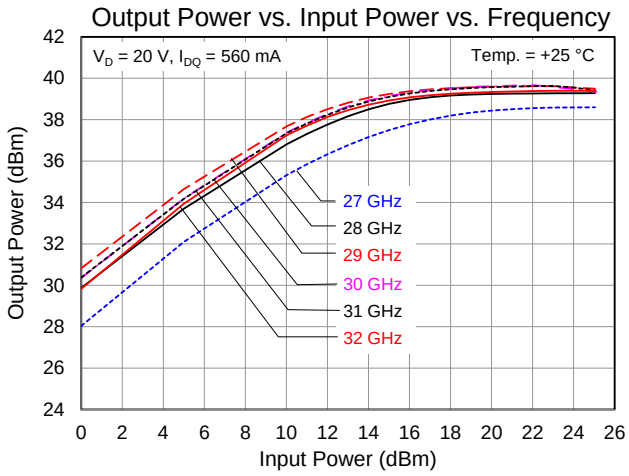


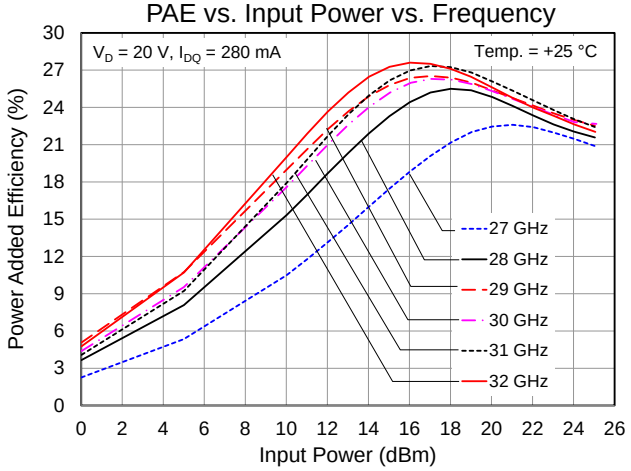



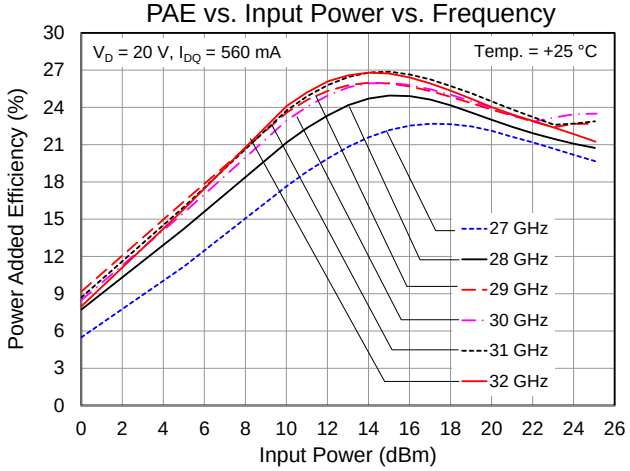
## Typical Performance – Large Signal (cont.)

Test conditions unless otherwise noted: CW, $V_D$ = +20 V, $I_{DQ}$ = 280 mA and 560mA, $T_{BASE}$ =+25 °C

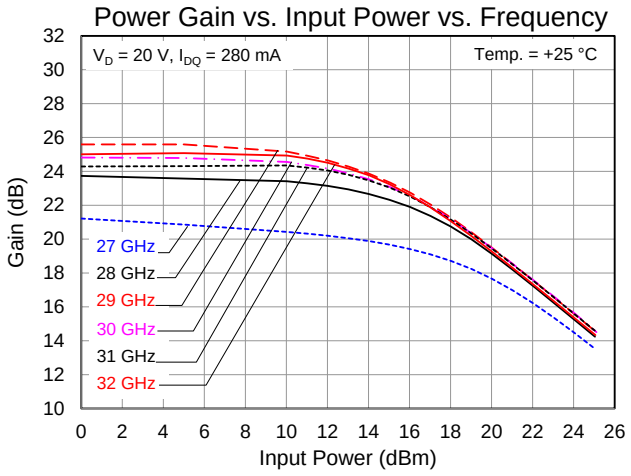
PAE vs. Input Power vs. Frequency



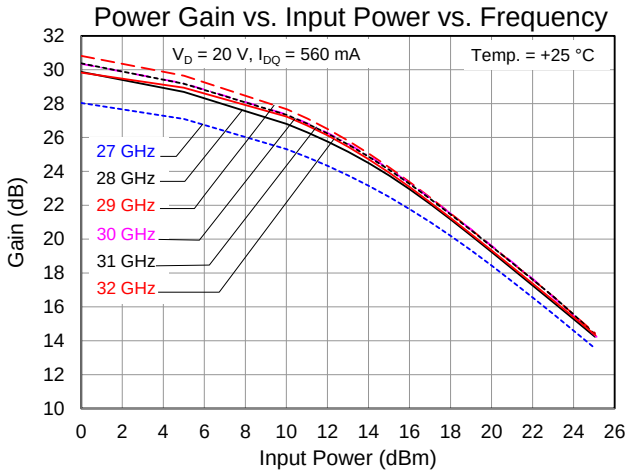

PAE vs. Input Power vs. Frequency



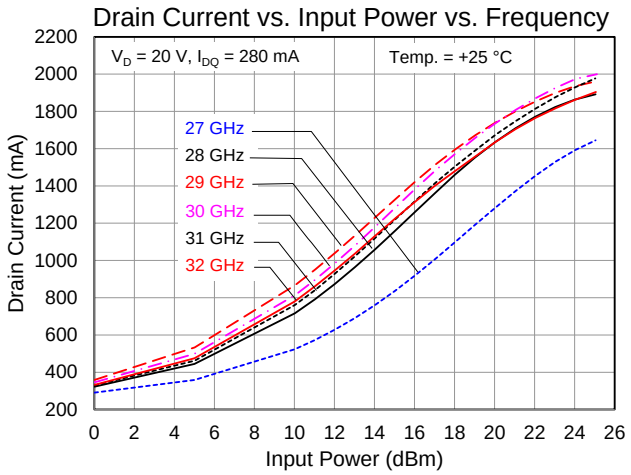

Power Gain vs. Input Power vs. Frequency



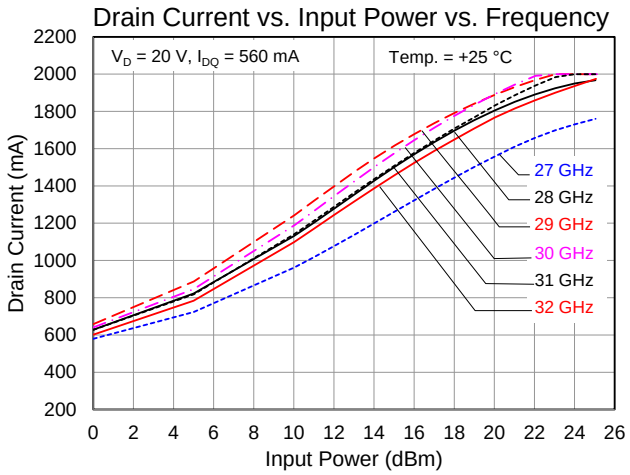

Power Gain vs. Input Power vs. Frequency




Drain Current vs. Input Power vs. Frequency

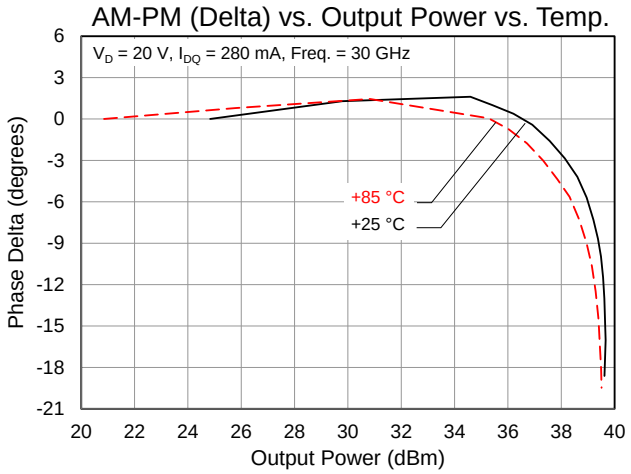


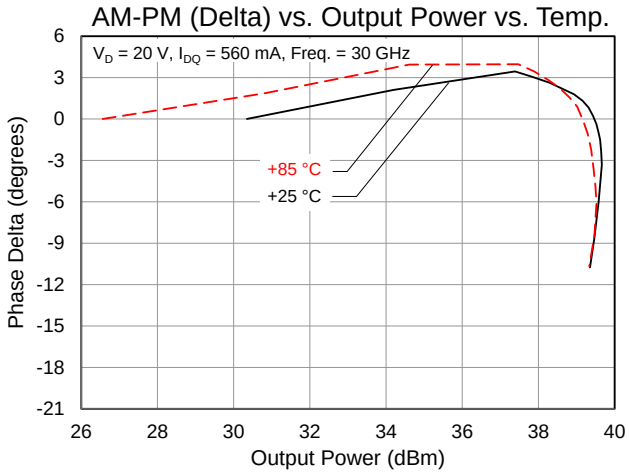

Drain Current vs. Input Power vs. Frequency

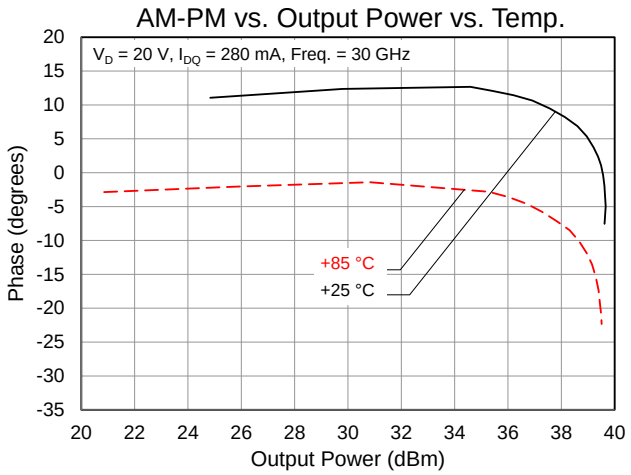


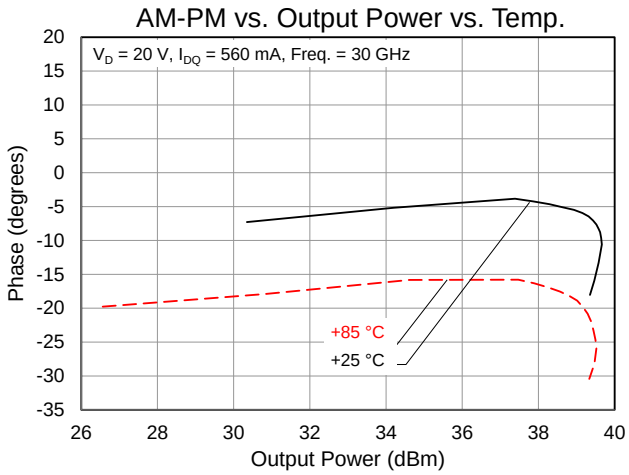
## Typical Performance – Large Signal (Cont.)

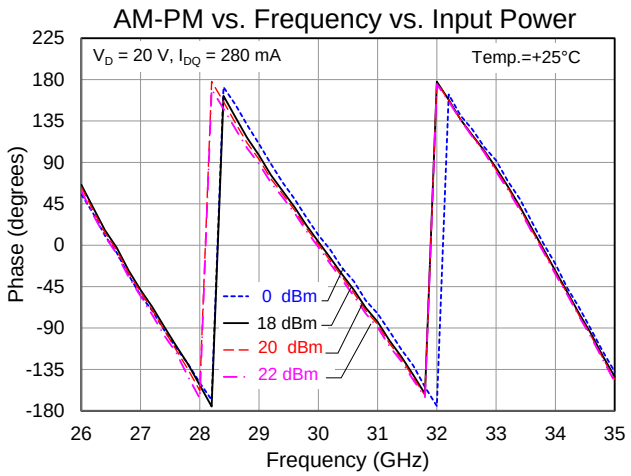
Test conditions unless otherwise noted: CW, $V_D$ = +20 V, $I_{DQ}$ = 280 mA and 560mA, $T_{BASE}$ =+25 °C

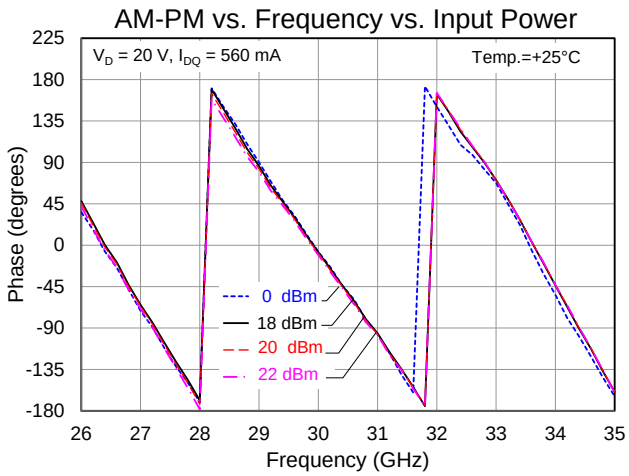


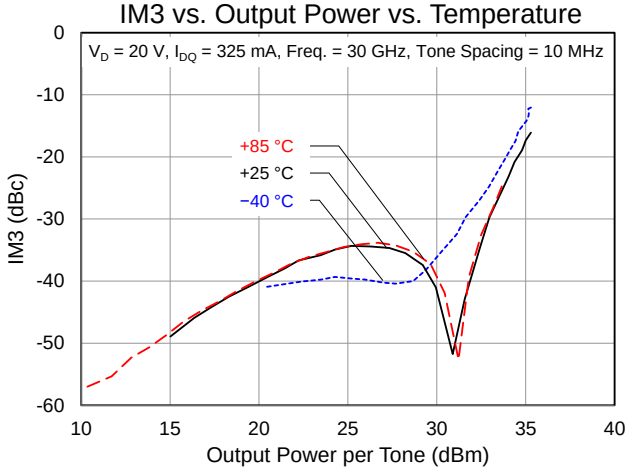



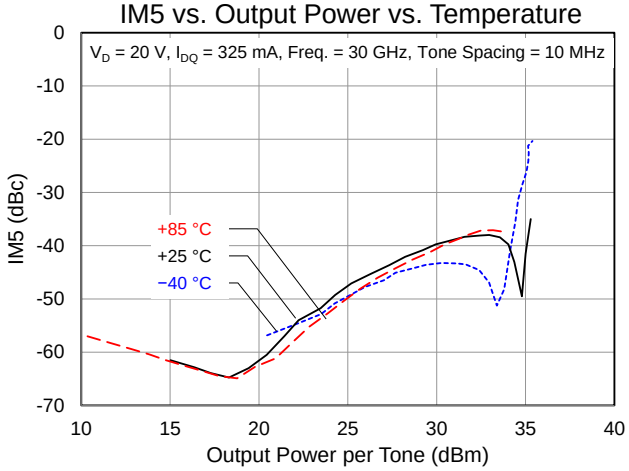
## Typical Performance – Linearity

Test conditions unless otherwise noted: CW, $V_D$ = +20 V, $I_{DQ}$ = 325 mA, $T_{BASE}$ =+25 °C

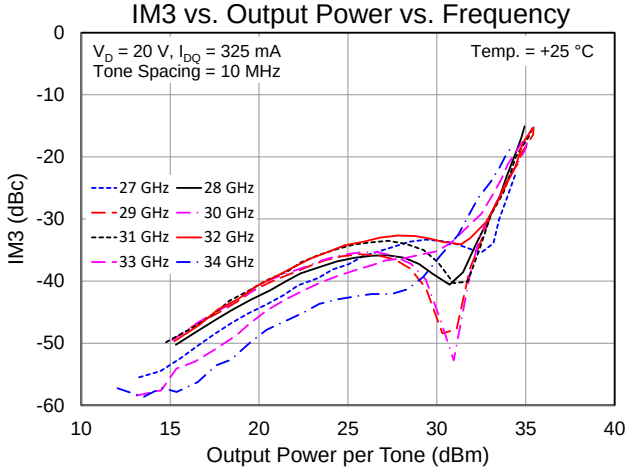
IM3 vs. Output Power vs. Temperature



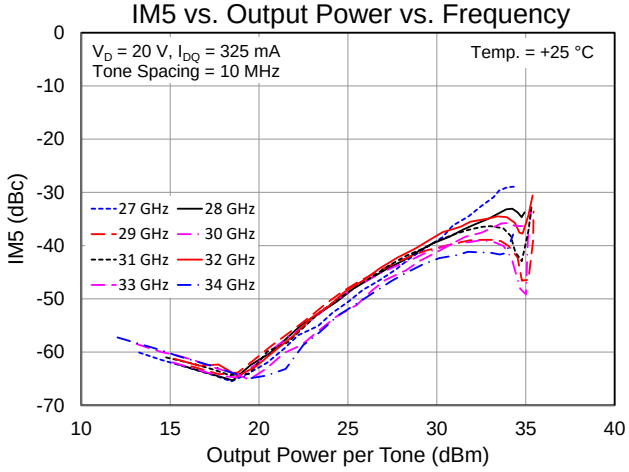

IM5 vs. Output Power vs. Temperature



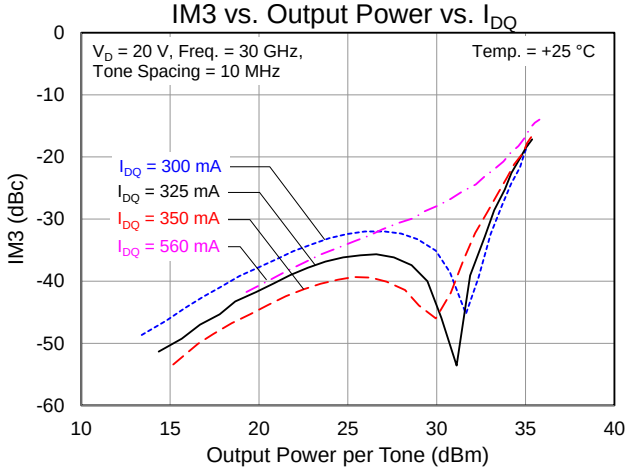

IM3 vs. Output Power vs. Frequency



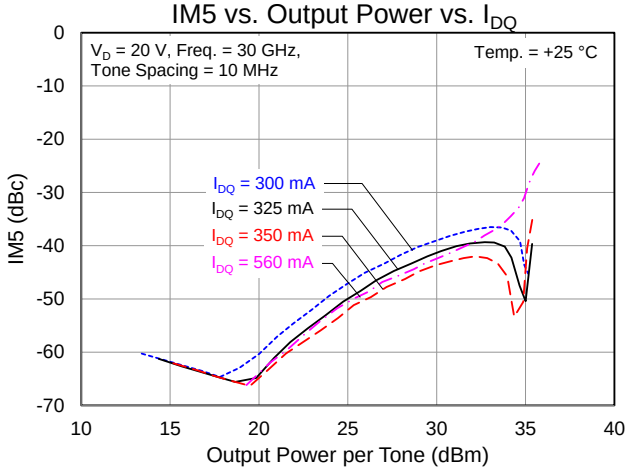

IM5 vs. Output Power vs. Frequency



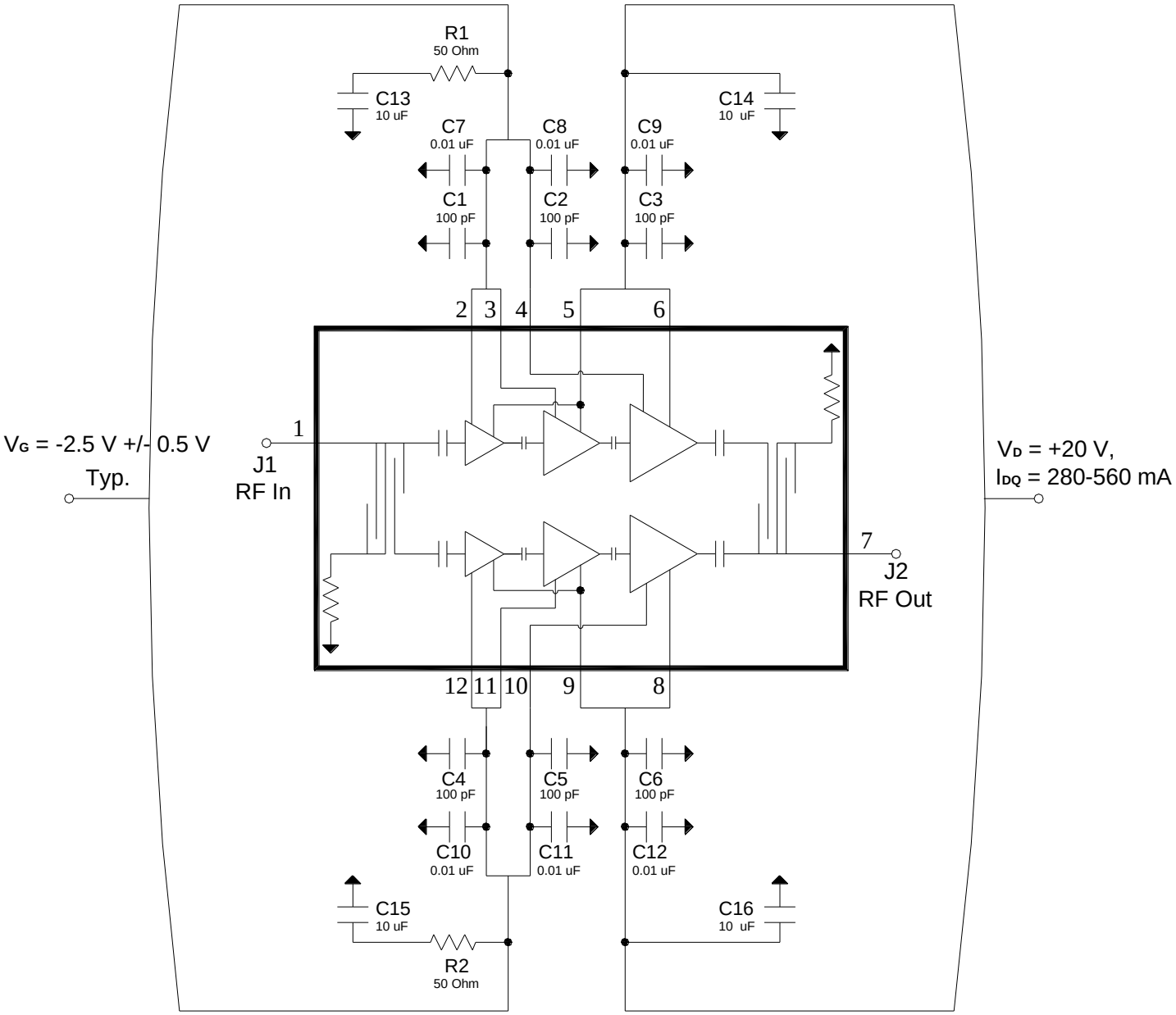

IM3 vs. Output Power vs. $I_{DQ}$




IM5 vs. Output Power vs. $I_{DQ}$



## Application Circuit



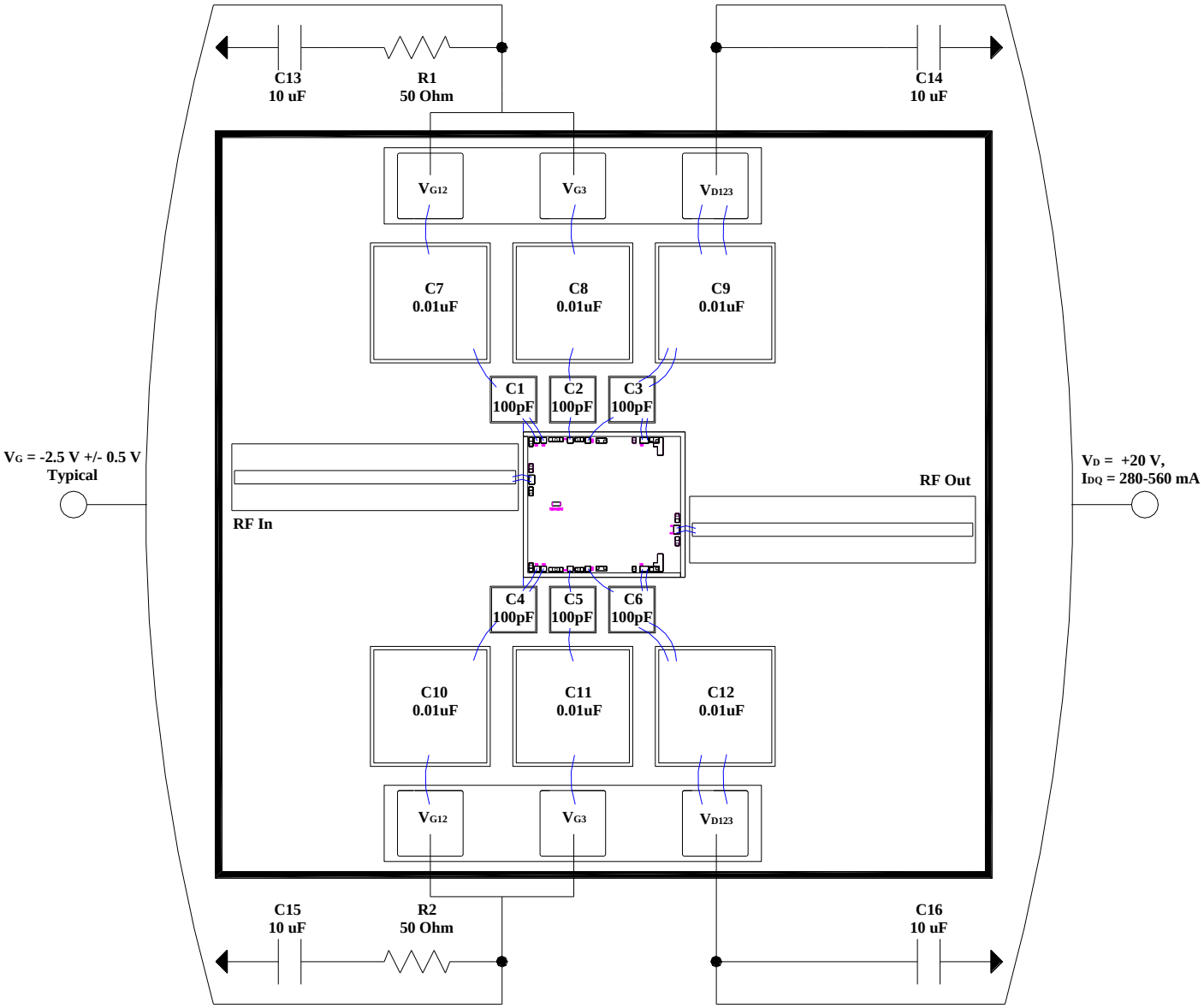

## Bias Up Procedure

| |
|---|
| 1. Set $I_D$ limit to 2.2 A, $I_G$ limit to 10 mA |
| 2. Apply −5 V to $V_G$ (Combine all $V_G$'s together) |
| 3. Apply + 20 V to $V_D$ (Combine all $V_D$'s together) |
| 4. Adjust $V_G$ until $I_{DQ}$ = 280 - 560 mA ($V_G$ ~ -2.5 V +/- Typ.) |
| 5. Apply RF signal |

## Bias Down Procedure

| |
|---|
| 1. Turn off RF signal |
| 2. Reduce $V_G$ to −5 V; ensure $I_{DQ}$ is approx. 0 mA |
| 3. Set $V_D$ to 0 V |
| 4. Turn off $V_D$ supply |
| 5. Turn off $V_G$ supply |

## Assembly Drawing

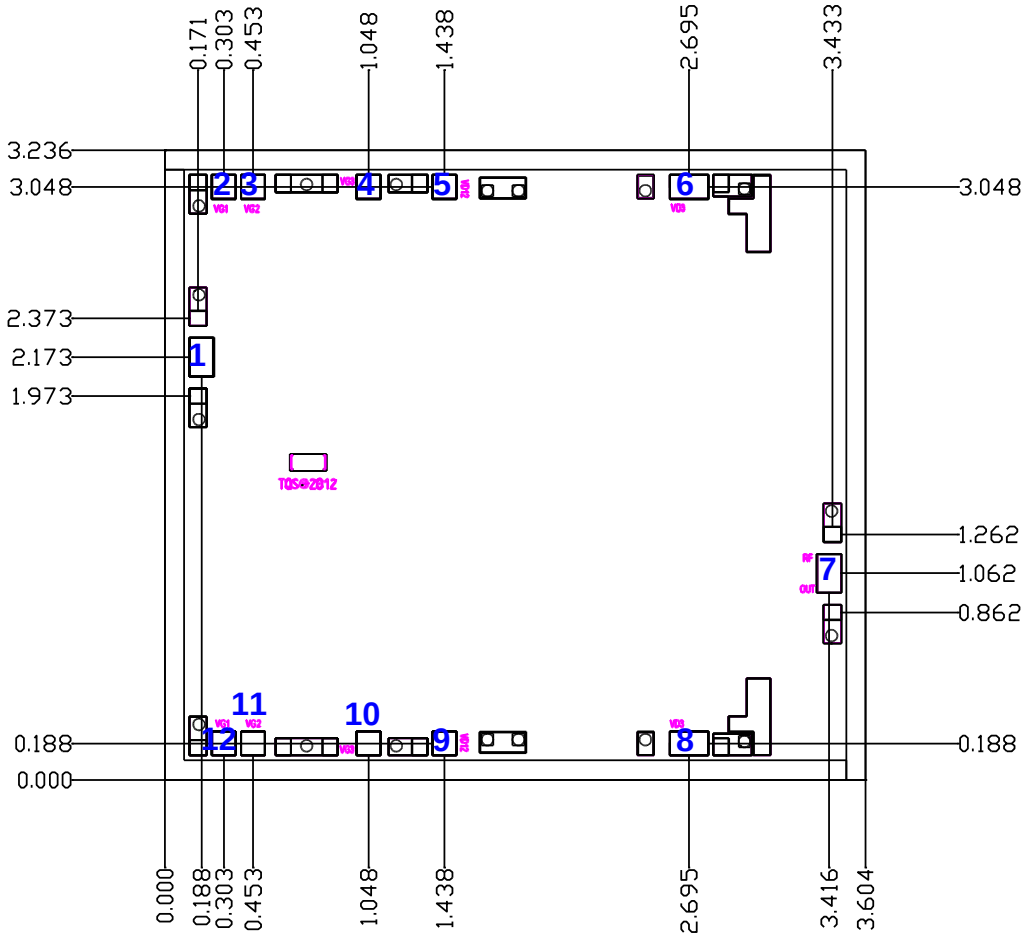



Notes:
Amplifier must be biased from both sides.
Minimize RF wirebond lengths to achieve optimum return loss. Options in order of preference are:

1. Short w = 5mil ribbon bonds
2. Multiple short wedge or chisel bonds
3. Multiple ball bonds

Each set of chip capacitor 100 pF//0.01 uF (total 8 sets) can be replaced by one Presidio chip capacitor MVB3030x103M2H5C1F (RoHS compliant version).

## Mechanical Drawing




Unit: millimeters
Thickness: 0.10
Die x, y size tolerance: ± 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

## Bond Pad Description

| Pad No. | Symbol | Pad Size | Description |
|---|---|---|---|
| 1 | RF In | 0.125 x 0.200 | Input; matched to 50 Ω; DC blocked. |
| 2, 12 | $V_{G1}$ | 0.125 x 0.125 | Gate voltage, $V_{G1}$ top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example. |
| 3, 11 | $V_{G2}$ | 0.125 x 0.125 | Gate voltage, $V_{G2}$ top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example. |
| 4, 10 | $V_{G3}$ | 0.125 x 0.125 | Gate voltage, $V_{G1}$ top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example. |
| 5, 9 | $V_{D12}$ | 0.125 x 0.125 | Drain voltage, $V_{D12}$ top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example. |
| 6, 8 | $V_{D3}$ | 0.200 x 0.125 | Drain voltage, $V_{D3}$ top and bottom. Bias network is required; must be biased from both sides; see Application Circuit on page 9 as an example. |
| 7 | RF Out | 0.125 x 0.200 | Output; matched to 50 Ω; DC blocked. |

## Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

## Handling Precautions

| Parameter | Rating | Standard |
|---|---|---|
| ESD – Human Body Model (HBM) | 1A | ANSI/ESD/JEDEC JS-001 |
| ESD – Charged Device Model (CDM) | C2 | ANSI/ESD/JEDEC JS-002 |

Caution!
ESD-Sensitive Device

## Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

## RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** www.qorvo.com

**Tel:** 1-844-890-8163

**Email:** customer.support@qorvo.com

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