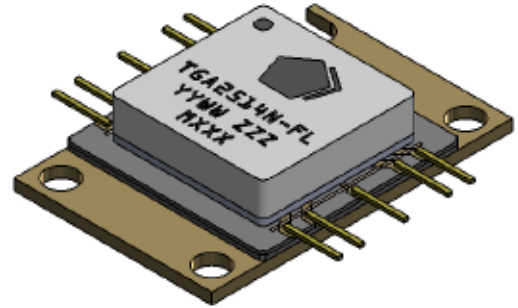


### Product Description

Qorvo’s TGA2514N-FL is a packaged Ku-band power amplifier operating from 13–16 GHz. Fabricated on Qorvo’s production 0.25  $\mu\text{m}$  GaAs pHEMT process (QPHT25), the TGA2514N-FL delivers 6.5 W of saturated output power with 24 dB of small signal gain. Performance is ideal for VSAT transmitters, data links and point to point radios.

To support easy system integration, the TGA2514N-FL is offered in a 10-pin flange-mounted package, offering robust handling and good thermal management. In addition, both RF ports have integrated DC blocking capacitors and are fully matched to 50 ohms.

Lead free and RoHS compliant.

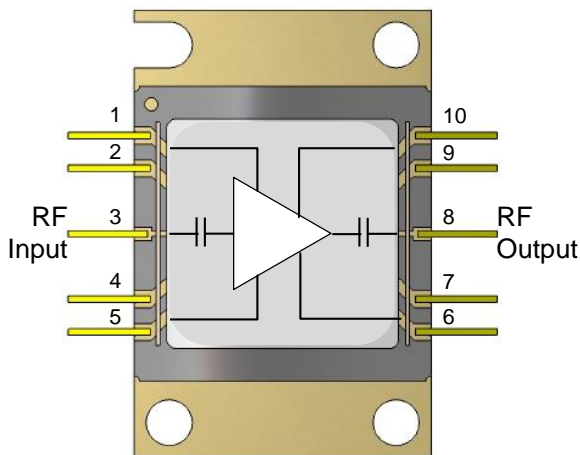


### Product Features

- Frequency Range: 13 – 16 GHz
- Saturated Output Power: 38 dBm
- Small Signal Gain: 24 dB
- Input and Output Return Loss: 14 dB
- Bias Condition (VD/IDQ): 8.0V/2.6 A
- Package Size: 0.448 x 0.682 x 0.120 inches (11.379 x 17.323 x 3.048 mm)

*Performance is typical across frequency. Please reference electrical specification table and data plots for more details*

### Functional Block Diagram



### Applications

- Ku Band VSAT Transmitter
- Point to Point Radio

### Ordering Information

Part No.	Description
TGA2514N-FL	13 – 16 GHz Power Amplifier
1127039	Evaluation Board



# TGA2514N-FL

## 13 – 18 GHz Power Amplifier

### Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage ( $V_D$ )	9.0 V
Drain Current ( $I_D$ )	3.8 A
Gate Voltage Range ( $V_G$ )	-5 to 0 V
Gate Current ( $I_G$ )	-18 to +18 mA
Input Power, CW ( $P_{IN}$ )	21 dBm
Power Dissipation ( $P_{DISS}$ )	33.3 W
Operating Channel Temperature	200 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

### Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage ( $V_G$ )	8.0 V
Gate Voltage ( $V_S$ )	-0.65 V
Drain Current ( $I_{DQ}$ )	2.6 A
Temperature Range	-40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

### Electrical Specifications

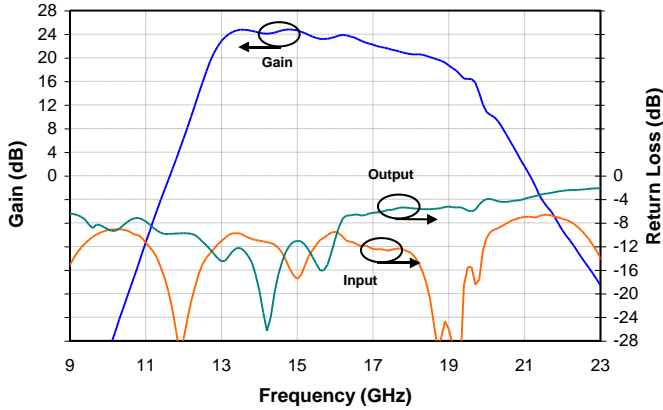
Parameter	Min	Typ	Max	Units
Frequency Range	13		16	GHz
Small Signal Gain		24		dB
Saturated Output Power		38		dBm
Input Return Loss		14		dB
Output Return Loss		14		dB

Test conditions, unless otherwise noted: Temp = 25 °C,  $V_D$  = 8.0 V,  $I_{DQ}$  = 2.6 A

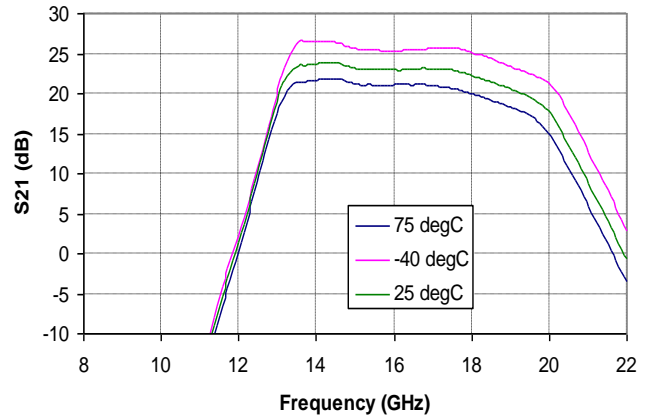
### Typical Performance – Small and Large Signal

Test conditions, unless otherwise noted: Temp = 25 °C,  $V_D = 8.0$  V,  $I_{DQ} = 2.6$  A

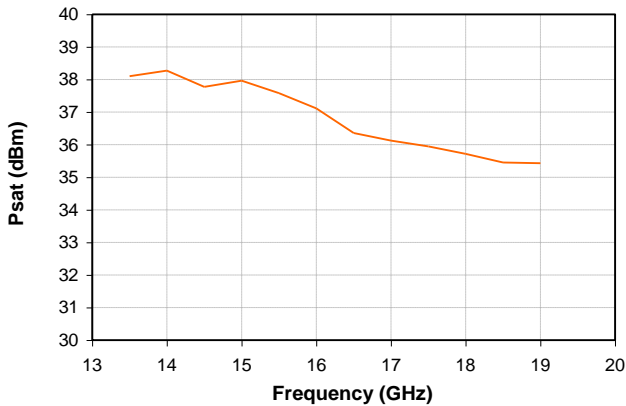
Gain and Return Loss vs. Frequency



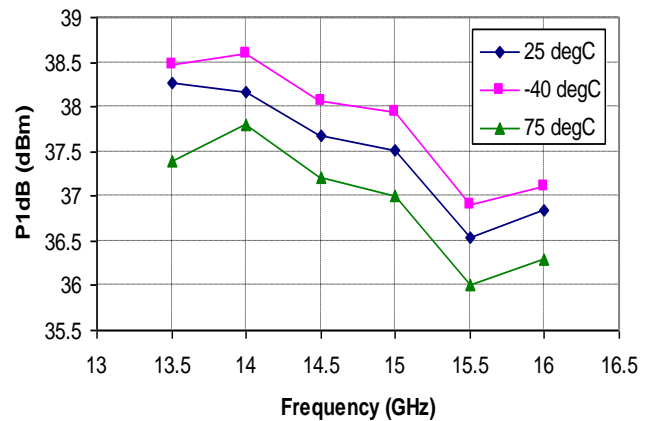
Gain vs. Frequency vs. Temperature



Saturated Output Power vs. Frequency



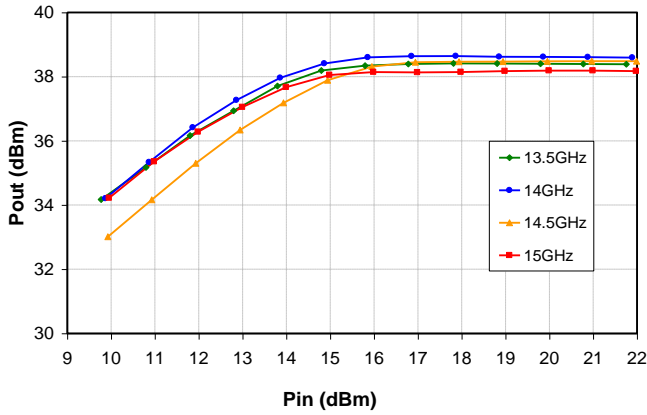
P1dB vs. Frequency vs. Temperature



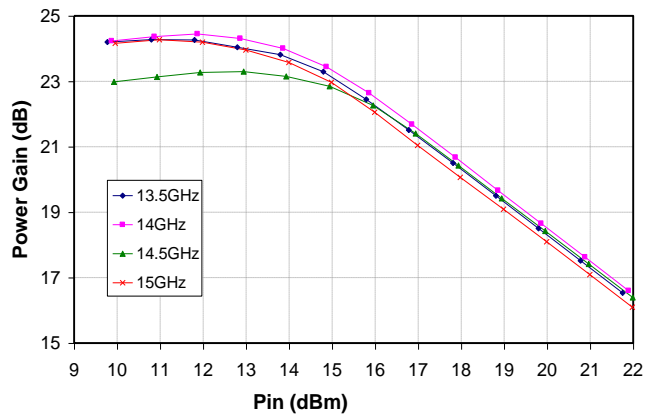
### Typical Performance – Large Signal

Test conditions, unless otherwise noted: Temp = 25 °C,  $V_D = 8.0$  V,  $I_{DQ} = 2.6$  A

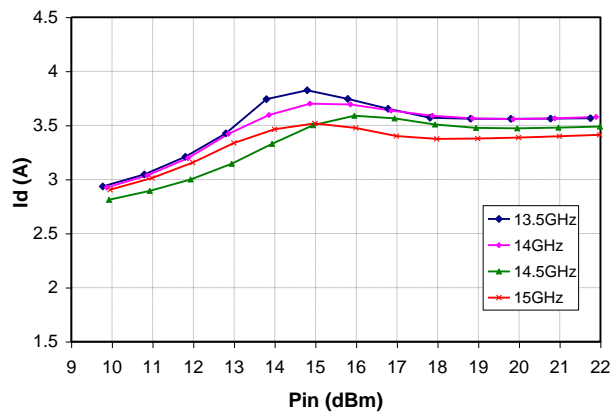
Output Power vs. Input Power vs. Frequency



Gain vs. Input Power vs. Frequency



Drain Current vs. Input Power vs. Frequency



### Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{BASE} = 70\text{ }^{\circ}\text{C}$ , $V_D = 8\text{ V}$ $I_{DQ} = 2.6\text{ A}$ , $P_{DISS} = 20.8\text{ W}$	3.9	$^{\circ}\text{C/W}$
Channel Temperature ( $T_{CH}$ ) <sup>(1)</sup>		151	$^{\circ}\text{C}$
Median Lifetime ( $T_M$ )		9.3E5	Hrs
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{BASE} = 70\text{ }^{\circ}\text{C}$ , $V_D = 8\text{ V}$ $I_{DQ} = 2.6\text{ A}$ , $P_{DISS} = 22.5\text{ W}$ (Under RF Drive)	3.9	$^{\circ}\text{C/W}$
Channel Temperature ( $T_{CH}$ ) <sup>(1)</sup>		158	$^{\circ}\text{C}$
Median Lifetime ( $T_M$ )		5.2E5	Hrs

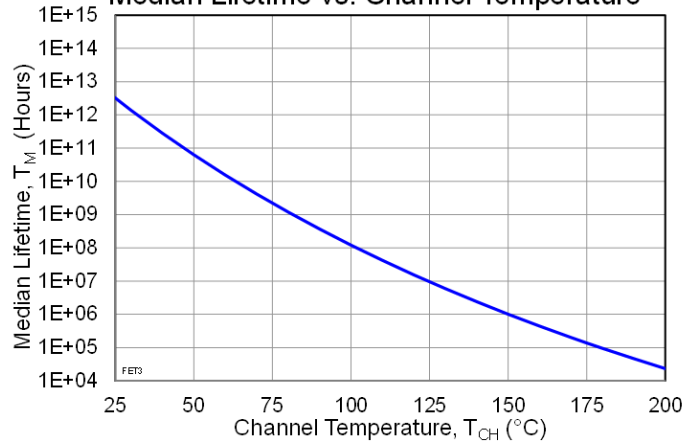
Notes:

1. Thermal resistance is referenced to the back of package ( $70\text{ }^{\circ}\text{C}$ )

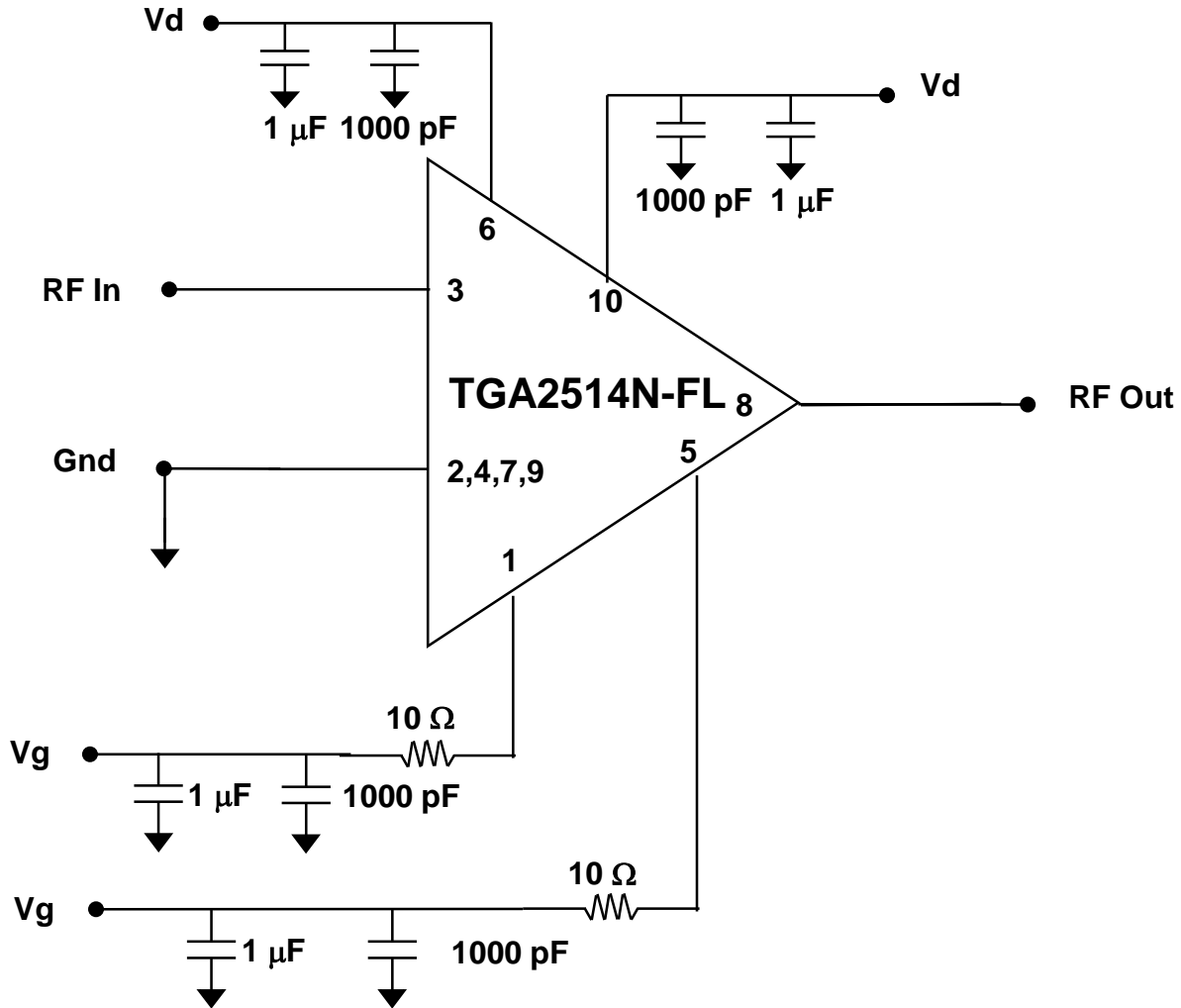
### Median Lifetime

Failure Criterion = 10% reduction in  $I_{D\text{ MAX}}$

Median Lifetime vs. Channel Temperature



## Applications Circuit



Notes:

1.  $V_G$  can be biased from either pin 1 or pin 5.
2.  $V_D$  must be biased from both sides (Pins 6 and 10)

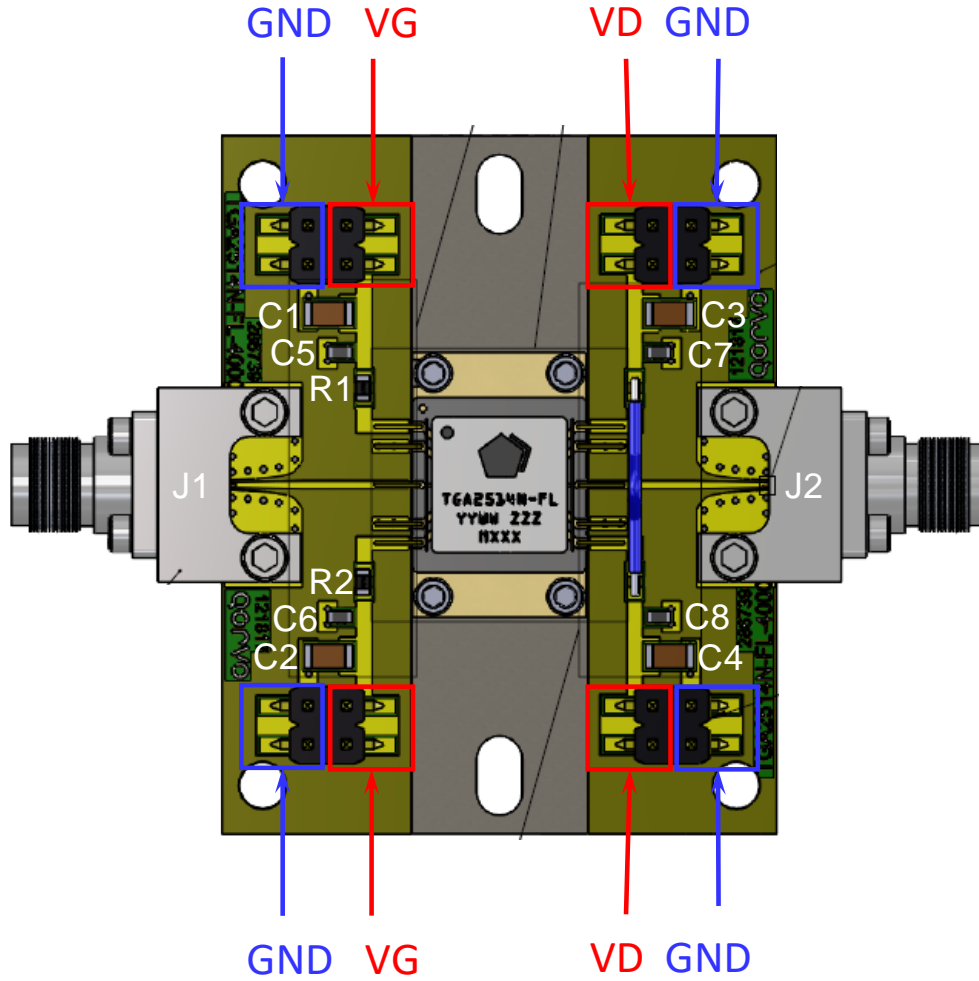
### Bias Up Procedure

1. Set  $I_D$  limit to 3.3 A,  $I_G$  limit to 18 mA
2. Apply  $-1.5\text{ V}$  to  $V_G$
3. Apply  $+8\text{ V}$  to  $V_D$ ; ensure  $I_{DQ}$  is approx. 0 mA
4. Adjust  $V_G$  until  $I_{DQ} = 2.6\text{ A}$  ( $V_G \sim -0.65\text{ V Typ.}$ ).
5. Turn on RF supply

### Bias Down Procedure

1. Turn off RF supply
2. Reduce  $V_G$  to  $-1.5\text{ V}$ ; ensure  $I_{DQ}$  is approx. 0 mA
3. Set  $V_D$  to 0 V
4. Turn off  $V_D$  supply
5. Turn off  $V_G$  supply

**Evaluation Board (EVB) Assembly Drawing**



**PCB NOTES:**

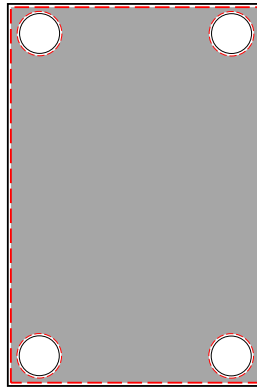
1. RF Layer is 0.010" thick Rogers Corp. RO4350,  $\epsilon_r = 3.38$ . Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

**Bill of Materials**

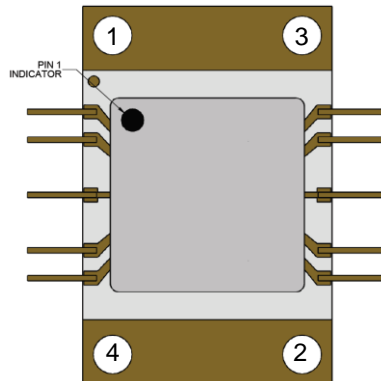
Reference Des.	Value	Description	Manuf.	Part Number
C1, C2, C3, C4	1.0 uF	CAP, 1uF, 5% 50V, X7R, 1206	Various	–
C5, C6, C7, C8	1000 pF	CAP, 1000pF, 5%, 50V, NP0, 0603	Various	–
R1, R2	0 $\Omega$	RES, 0 OHM, 1/10W, 0603	Various	–
J1, J2	2.92 mm	CONNECTOR, FEMALE, ENDLAUNCH	Southwest Microwave	1092-01A-5

### Assembly Notes

- Carefully clean the PC board, mounting surface, and package leads with 90% (or higher) isopropyl alcohol. Allow it to dry fully.
- To improve the thermal and RF performance, Qorvo recommends attaching the amplifier to a heat sink, and apply either a thermal compound (Arctic Silver 5 recommended) or a .004 inch (maximum thickness) indium shim (HeatSpring™ material is recommended) between the heat sink and the package. If using an indium shim, the overall dimensions should be no larger than the package base, with clearance holes for the mounting screws. Cut the indium shim material by whatever means are convenient (razor blade, pre-purchased cut pieces, etc.), using the outline of the package base as a guideline (see the figure below; gray area is the indium shim). The shim can be cut a few mils undersize to allow for tolerance in the placement, but the shim must cover the full area of the base, *especially under the 4 mounting screws*. Cutting the shim too small (covering just the center area of the component base or leaving the corners unsupported) may result in deformation of the package base when the mounting screws are tightened, causing poor thermal conductivity due to bowing of the base, and possible attachment issues with the various components inside the package.



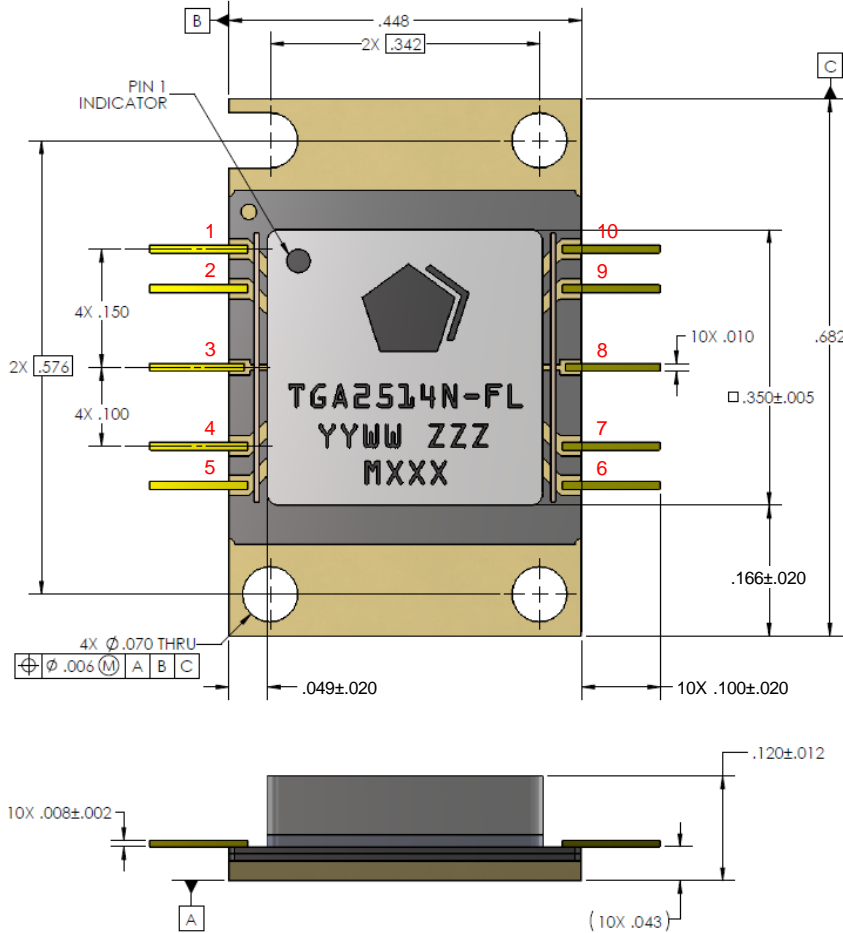
- Use 0-80 screws to attach the component to the next level assembly (heat sink, module, etc.). Use the following tightening pattern:



(There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.)

- The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the TGA2514N-FL. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. Each solder connection should be completed within 2 to 5 seconds. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable.
- The packaged part should not be subjected to conventional SMT automated solder reflow processes.

### Mechanical Information



- NOTES:
1. PACKAGE BASE: CERAMIC ON METAL FLANGE.
  2. PACKAGE LID: PLASTIC.
  3. ALL METALIZED FEATURES ARE GOLD PLATED.
  4. THE PART IS EPOXY SEALED.
  5. PART MARKING:  
 TGA2514N-FL: PART NUMBER  
 YY: PART ASSY YEAR  
 WW: PART ASSY WEEK  
 ZZZ: SERIAL NUMBER  
 MXXX: BATCH ID

THE GENERAL TOLERANCE IS  $\pm .006$  UNLESS OTHERWISE SPECIFIED  
 ALL DIMENSIONS ARE IN INCHES

### Pin Description

Pad No.	Symbol	Description
1,5	$V_G$	Gate Voltage; bias network is required, part can be biased from either pin
2,4,7,9	GND	Ground
3	RF Input	RF Input; 50 $\Omega$ , AC coupled
6,10	$V_D$	Drain Voltage; bias network is required, part must be biased from both pins
8	RF Output	RF Output; 50 $\Omega$ , AC coupled

### Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 0B	JEDEC Standard JESD22 A114
MSL – Moisture Sensitivity Level	N/A	JEDEC standard J-STD-020



Caution!  
ESD-Sensitive Device

### Solderability

The component leads should be manually soldered, and the package should not be subjected to conventional reflow processes. Soldering of the component leads is compatible with the latest version of J-STD-020, lead-free solder, 260 °C. The use of no-clean solder to avoid washing after soldering is recommended.

### RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

### Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: [www.qorvo.com](http://www.qorvo.com)

Tel: 1-844-890-8163

Email: [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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