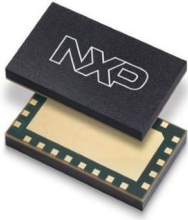


# A5M36TG140

## Airfast Power Amplifier Module

Rev. 2 — 27 November 2024

Product data sheet



## 1 General description

The A5M36TG140 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS and GaN-on-SiC power amplifiers are designed for TDD LTE and 5G systems.

## 2 Features and benefits

- 2-stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude

## 3 Typical performance

Table 1. 3300–3800 MHz — Typical LTE performance

$P_{out} = 9\text{ W Avg.}$ ,  $V_{DC1} = V_{DP1} = 5\text{ Vdc}$ ,  $V_{DC2} = V_{DP2} = 48\text{ Vdc}$ ,  $1 \times 20\text{ MHz LTE}$ , input signal PAR = 8 dB @ 0.01% probability on CCDF.<sup>[1]</sup>

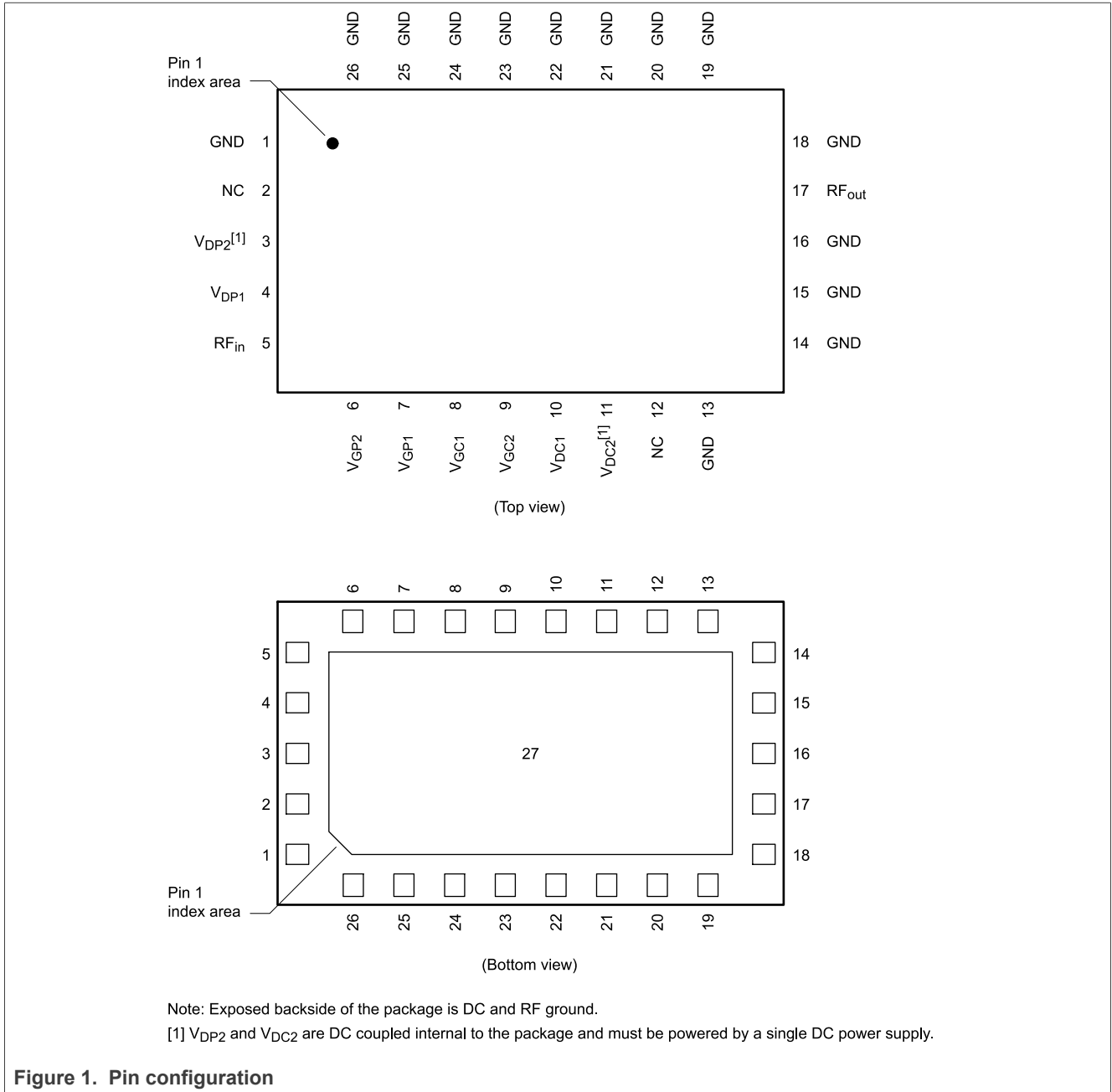
Carrier center frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3310 MHz	30.5	-28.8	42.9
3410 MHz	31.0	-30.1	45.4
3500 MHz	31.3	-31.8	46.2
3600 MHz	31.8	-33.7	46.1
3700 MHz	32.2	-36.0	45.8
3790 MHz	32.3	-34.8	45.4

[1] All data measured with device soldered in NXP reference circuit.



## 4 Pinning information

### 4.1 Pinning

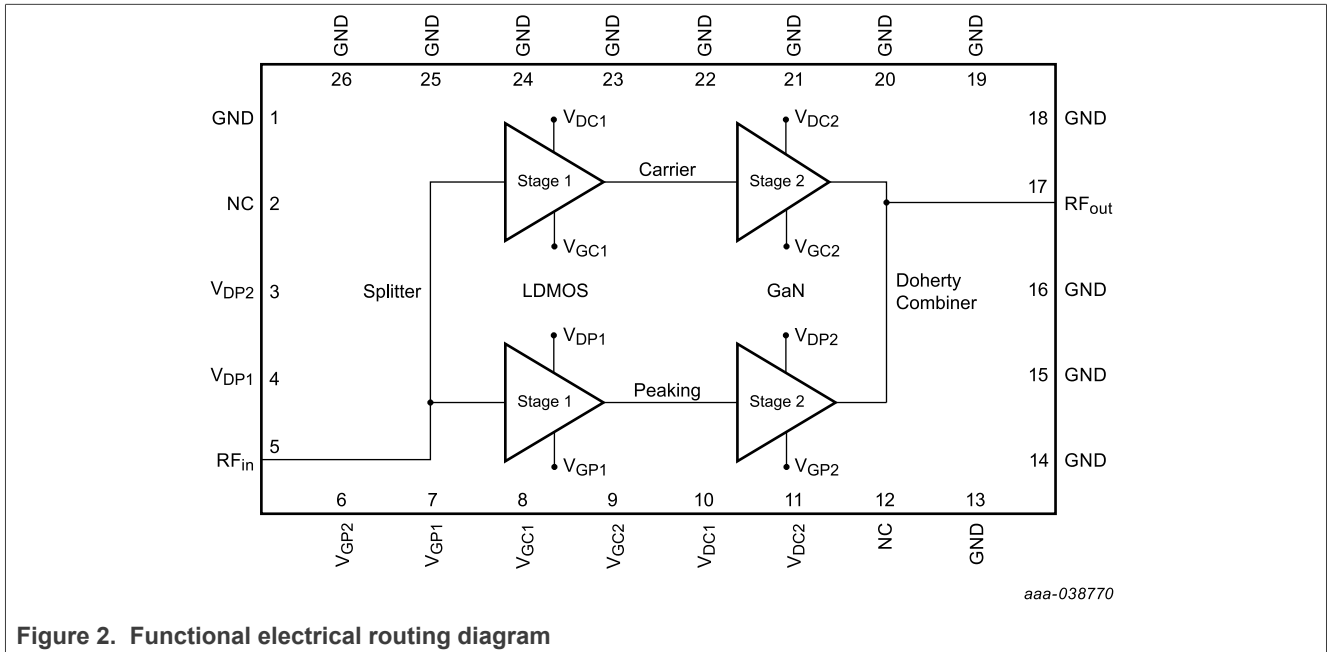


**4.2 Pin description**

**Table 2. Pin description**

Pin number	Pin function	Pin description
1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27	GND	Ground
2, 12	NC	No connection
3	V <sub>DP2</sub>	Peaking drain supply, stage 2
4	V <sub>DP1</sub>	Peaking drain supply, stage 1
5	RF <sub>in</sub>	RF input
6	V <sub>GP2</sub>	Peaking gate supply, stage 2
7	V <sub>GP1</sub>	Peaking gate supply, stage 1
8	V <sub>GC1</sub>	Carrier gate supply, stage 1
9	V <sub>GC2</sub>	Carrier gate supply, stage 2
10	V <sub>DC1</sub>	Carrier drain supply, stage 1
11	V <sub>DC2</sub>	Carrier drain supply, stage 2
17	RF <sub>out</sub>	RF output

**5 Functional electrical routing diagram**



**Figure 2. Functional electrical routing diagram**

**6 Ordering information**

**Table 3. Ordering information**

Device	Tape and reel information	Package
A5M36TG140T2	T2 suffix = 2,000 units, 24 mm tape width, 13-inch reel	10 mm × 6 mm Module

## 7 Product marking

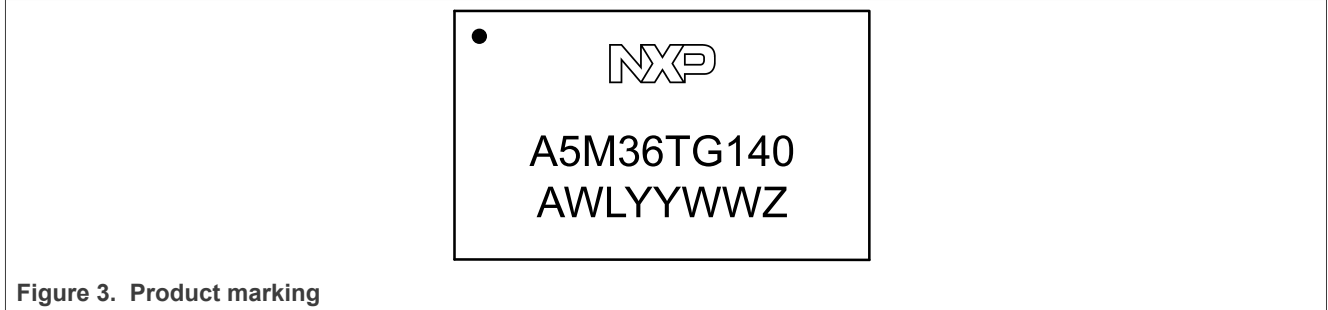


Figure 3. Product marking

Table 4. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

## 8 Limiting values

Table 5. Limiting values

Rating	Symbol	Value	Unit
Gate-bias voltage range	$V_{G1}$ $V_{G2}$	-0.5 to +10 -8, 0	Vdc
Operating voltage range	$V_{DD1}$ $V_{DD2}$	4.75 to 5.25 +38 to +55	Vdc
Maximum forward gate current, $I_G$ (A+B), @ $T_C = 25^\circ\text{C}$	$I_{GMAX}$	8.1	mA
Storage temperature range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Case operating temperature	$T_C$	125	$^\circ\text{C}$
Maximum channel temperature	$T_{CH}$	225	$^\circ\text{C}$
Peak input power (3600 MHz, pulsed CW, 10 $\mu\text{sec}$ (on), 10% duty cycle, $V_{DC1} = V_{DP1} = 5 \text{ Vdc}$ , $V_{DC2} = V_{DP2} = 48 \text{ Vdc}$ )	$P_{in}$	28	dBm

## 9 Lifetime

Table 6. Lifetime

Characteristic	Symbol	Value	Unit
Mean time to failure (Case temperature 125 $^\circ\text{C}$ , 75% duty cycle, 9 W Avg., $V_{DC1} = V_{DP1} = 5 \text{ Vdc}$ , $V_{DC2} = V_{DP2} = 48 \text{ Vdc}$ )	MTTF	> 10	Years

## 10 Thermal characteristics

**Table 7. Thermal characteristics**

Characteristic	Symbol	Value	Unit
Thermal resistance by infrared measurement, active die surface-to-case (Case temperature 125°C, P <sub>D</sub> = 11.0 W)	R <sub>θSC</sub> (IR)	5.6 <sup>[1]</sup>	°C/W
Thermal resistance by finite element analysis, channel-to-case <sup>[2][3]</sup> (Case temperature 125°C, P <sub>D</sub> = 10.8 W)	R <sub>θCHC</sub> (FEA)	9.3 (Typical)	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.

[2] R<sub>θCHC</sub> (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = 10<sup>[A + B/(T + 273)]</sup>, where T is the channel temperature in degrees Celsius, A = -11.6 and B = 9129.

[3] Simulated maximum FEA channel-to-case thermal resistance: 10.7°C/W, P<sub>D</sub> = 9.4 W.

## 11 ESD protection characteristics

**Table 8. ESD protection characteristics**

Test methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

## 12 Moisture sensitivity level

**Table 9. Moisture sensitivity level**

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

## 13 Electrical characteristics

### 13.1 DC characteristics — off characteristics

**Table 10. DC characteristics — off characteristics**

(T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Carrier + peaking stage 2, GaN — off characteristics</b>					
Off-state drain leakage <sup>[1]</sup> (V <sub>DS</sub> = 150 Vdc, V <sub>GS</sub> = -8 Vdc)	I <sub>D(BR)</sub>	—	—	5.0	mAdc
Off-state gate leakage (V <sub>DS</sub> = 48 Vdc, V <sub>GS</sub> = -7 Vdc)	I <sub>GLK</sub>	-4.0	—	—	mAdc

[1] Carrier side and peaking side are tied together for these measurements.

## 13.2 DC characteristics — on characteristics

Table 11. DC characteristics — on characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
<b>Carrier stage 1, LDMOS — on characteristics</b>				
Gate threshold voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DC1} = 120\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.33	$\pm 0.4$	Vdc
Gate quiescent voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DQC1} = 80\ \text{mAdc}$ , measured in functional test)	$V_{GS(Q)}$	1.90	$\pm 0.4$	Vdc
<b>Carrier stage 2, GaN — on characteristics</b>				
Gate threshold voltage <sup>[1]</sup> ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 8.1\ \text{mAdc}$ )	$V_{GS(th)}$	-2.72	$\pm 1.0$	Vdc
Gate quiescent voltage ( $V_{DS} = 48\text{ Vdc}$ , $I_{DQC2} = 10\ \text{mAdc}$ , measured in functional test)	$V_{GS(Q)}$	-2.75	$\pm 1.0$	Vdc
<b>Peaking stage 1, LDMOS — on characteristics</b>				
Gate threshold voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DP1} = 120\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.36	$\pm 0.4$	Vdc
Gate quiescent voltage ( $V_{DS} = 5\text{ Vdc}$ , $I_{DQP1} = 40\ \text{mAdc}$ , measured in functional test)	$V_{GS(Q)}$	1.85	$\pm 0.4$	Vdc
<b>Peaking stage 2, GaN — on characteristics</b>				
Gate threshold voltage <sup>[1]</sup> ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 8.1\ \text{mAdc}$ )	$V_{GS(th)}$	-2.72	$\pm 1.0$	Vdc
Gate quiescent voltage ( $V_{DS} = 48\text{ Vdc}$ , $I_{DQP2} = 0\ \text{mAdc}$ , measured in functional test)	$V_{GS(Q)}$	-3.90	$\pm 1.0$	Vdc

[1] Carrier side and peaking side are tied together for these measurements.

**13.3 Functional tests**

**Table 12. Functional tests — 3400 MHz**

(In NXP Doherty production ATE<sup>[1]</sup> test fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[2]</sup>  $V_{DD1} = 5\text{ Vdc}$ ,  $V_{DD2} = 48\text{ Vdc}$ ,  $I_{DQC1} = 80\text{ mA}$ ,  $I_{DQC2} = 10\text{ mA}$ ,  $I_{DQP1} = 40\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 1.3)^{[3]}$  Vdc,  $P_{out} = 9\text{ W Avg.}$ , 1-tone CW,  $f = 3400\text{ MHz}$ .

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	28.0	30.3	—	dB
Drain efficiency	$\eta_D$	38.0	45.3	—	%
$P_{out}$ @ 3 dB compression point (Pulsed CW, 5% duty cycle)	P3dB	48.0	49.0	—	dBm

- [1] ATE is a socketed test environment.
- [2] Part input and output matched to 50 ohms.
- [3] Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 35\text{ mA}$  current is attained, and then subtract 1.3 V for final  $V_{GP2}$  bias voltage.

**Table 13. Functional tests — 3800 MHz**

(In NXP Doherty production ATE<sup>[1]</sup> test fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[2]</sup>  $V_{DD1} = 5\text{ Vdc}$ ,  $V_{DD2} = 48\text{ Vdc}$ ,  $I_{DQC1} = 80\text{ mA}$ ,  $I_{DQC2} = 10\text{ mA}$ ,  $I_{DQP1} = 40\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 1.3)^{[3]}$  Vdc,  $P_{out} = 9\text{ W Avg.}$ , 1-tone CW,  $f = 3800\text{ MHz}$ .

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	28.0	30.2	—	dB
Drain efficiency	$\eta_D$	35.0	42.4	—	%
$P_{out}$ @ 3 dB compression point (Pulsed CW, 5% duty cycle)	P3dB	47.6	48.6	—	dBm

- [1] ATE is a socketed test environment.
- [2] Part input and output matched to 50 ohms.
- [3] Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 35\text{ mA}$  current is attained, and then subtract 1.3 V for final  $V_{GP2}$  bias voltage.

**13.4 Wideband ruggedness**

**Table 14. Wideband ruggedness**

(In NXP Doherty power amplifier module reference circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[1]</sup>  $I_{DQC1} = 80\text{ mA}$ ,  $I_{DQC2} = 10\text{ mA}$ ,  $I_{DQP1} = 40\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 1.0)^{[2]}$  Vdc,  $f = 3600\text{ MHz}$ , Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Test results
ISBW of 400 MHz at 55 Vdc, 3 dB input overdrive from 9 W Avg. modulated output power	No device degradation

- [1] All data measured in fixture with device soldered in NXP reference circuit.
- [2] Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 35\text{ mA}$  current is attained, and then subtract 1.0 V for final  $V_{GP2}$  bias voltage.

**13.5 Typical performance**

**Table 15. Typical performance**

(In NXP Doherty power amplifier module reference circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[1]</sup>  
 $V_{DD1} = 5\text{ Vdc}$ ,  $V_{DD2} = 48\text{ Vdc}$ ,  $I_{DQC1} = 80\text{ mA}$ ,  $I_{DQC2} = 10\text{ mA}$ ,  $I_{DQP1} = 40\text{ mA}$ ,  $V_{GP2} = (V_{BIAS} - 1.0)$ <sup>[2]</sup> Vdc,  $f = 3600\text{ MHz}$ .

Characteristic	Symbol	Min	Typ	Max	Unit
VBW resonance point, 2-tone, 1 MHz tone spacing (IMD third order intermodulation inflection point)	VBW <sub>res</sub>	—	300	—	MHz
<b>1-carrier 20 MHz LTE, 8 dB input signal PAR</b>					
Gain	G	—	31.8	—	dB
Power added efficiency	PAE	—	46.1	—	%
Adjacent channel power ratio	ACPR	—	-33.7	—	dBc
Adjacent channel power ratio	ALT1	—	-46.9	—	dBc
Adjacent channel power ratio	ALT2	—	-54.1	—	dBc
Gain flatness <sup>[3]</sup>	G <sub>F</sub>	—	1.3	—	dB
<b>Pulsed CW, 10% duty cycle</b>					
P <sub>out</sub> @ 3 dB compression point	P3dB	—	48.3	—	dBm
AM/PM @ P3dB	Φ	—	-24	—	°
Gain variation @ Avg. power over temperature (-40°C to +105°C)	ΔG	—	0.051	—	dB/°C
P3dB variation over temperature (-40°C to +105°C)	ΔP3dB	—	0.007	—	dB/°C

[1] All data measured in fixture with device soldered in NXP reference circuit.  
 [2] Increase V<sub>GP2</sub> (peaking side) until I<sub>DQP2</sub> = 35 mA current is attained, and then subtract 1.0 V for final V<sub>GP2</sub> bias voltage.  
 [3] Gain flatness = Max(G(f<sub>Low</sub> to f<sub>High</sub>)) - Min(G(f<sub>Low</sub> to f<sub>High</sub>)).

## Correct Biasing Sequence

### Turn ON:

#### Bias ON the GaN final stage first

1. Set gate voltage  $V_{GC2}$  and  $V_{GP2}$  to  $-5$  V.
2. Set drain voltage  $V_{DC2}$  and  $V_{DP2}$  to nominal supply voltage ( $+48$  V).
3. Increase  $V_{GP2}$  (peaking side) until  $I_{DQP2} = 35$  mA current is attained, and then subtract  $1.0$  V for final  $V_{GP2}$  bias voltage.
4. Increase  $V_{GC2}$  (carrier side) until  $I_{DQC2}$  current is attained.

#### Bias ON the LDMOS driver stage second

1. Set drain voltage  $V_{DC1}$  and  $V_{DP1}$  to nominal supply voltage ( $+5$  V).
2. Increase  $V_{GC1}$  (carrier side) until  $I_{DQC1}$  current is attained.
3. Increase  $V_{GP1}$  (peaking side) until  $I_{DQP1}$  current is attained.
4. Apply RF input power to desired level.

### Turn OFF:

#### Bias OFF the GaN final stage first

1. Disable RF input power.
2. Adjust gate voltage  $V_{GC2}$  and  $V_{GP2}$  to  $-5$  V.
3. Adjust drain voltage  $V_{DC2}$  and  $V_{DP2}$  to  $0$  V. Allow adequate time for drain voltage to reduce to  $0$  V from external drain capacitors.
4. Disable  $V_{GC2}$  and  $V_{GP2}$ .

#### Bias OFF the LDMOS driver stage second

1. Adjust gate voltage  $V_{GC1}$  and  $V_{GP1}$  to  $0$  V.
2. Adjust drain voltage  $V_{DC1}$  and  $V_{DP1}$  to  $0$  V.

## 14 Component layout and parts list

### 14.1 Component layout

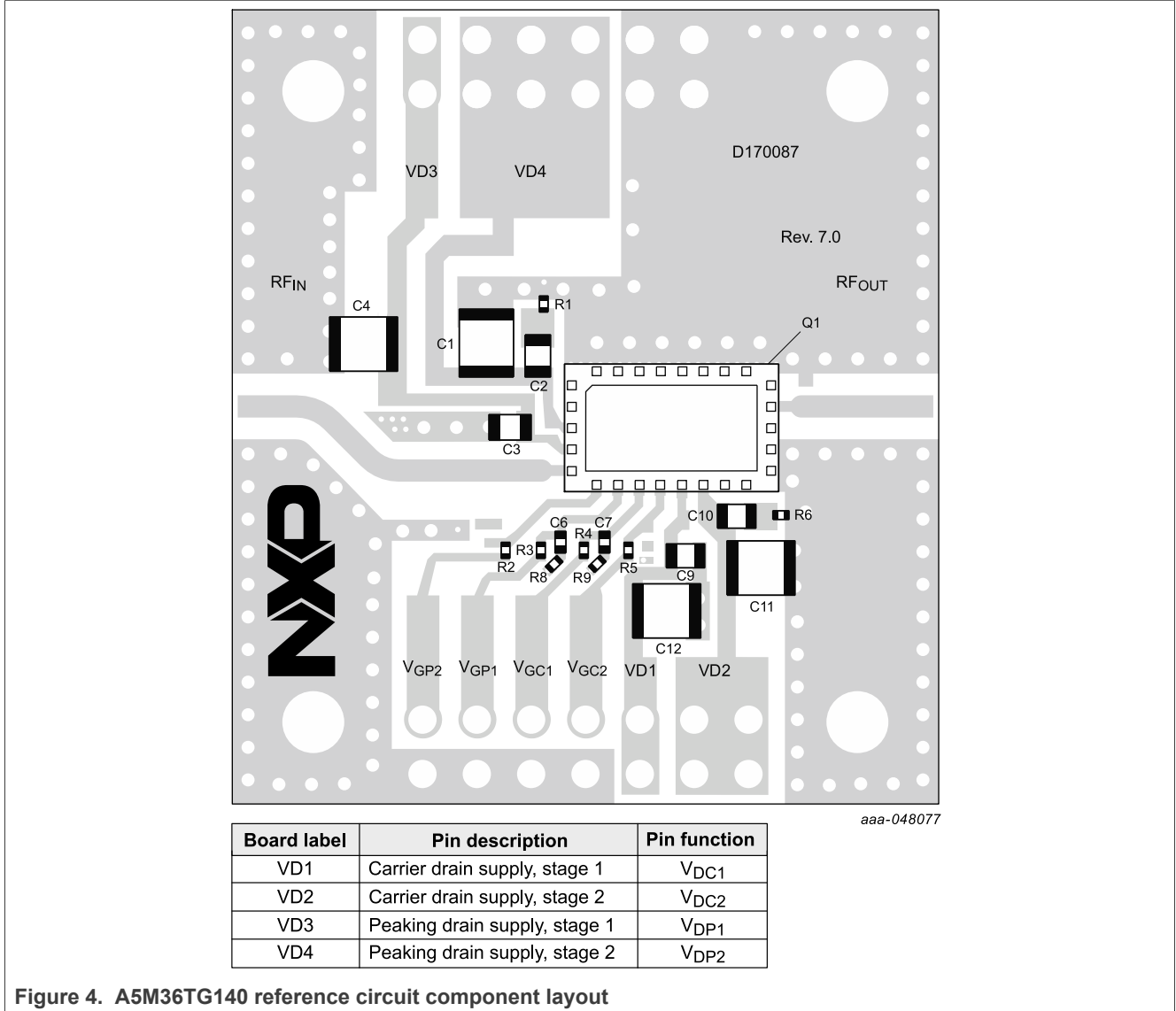


Figure 4. A5M36TG140 reference circuit component layout

## 14.2 Component designations and values

Table 16. A5M36TG140 reference circuit component designations and values

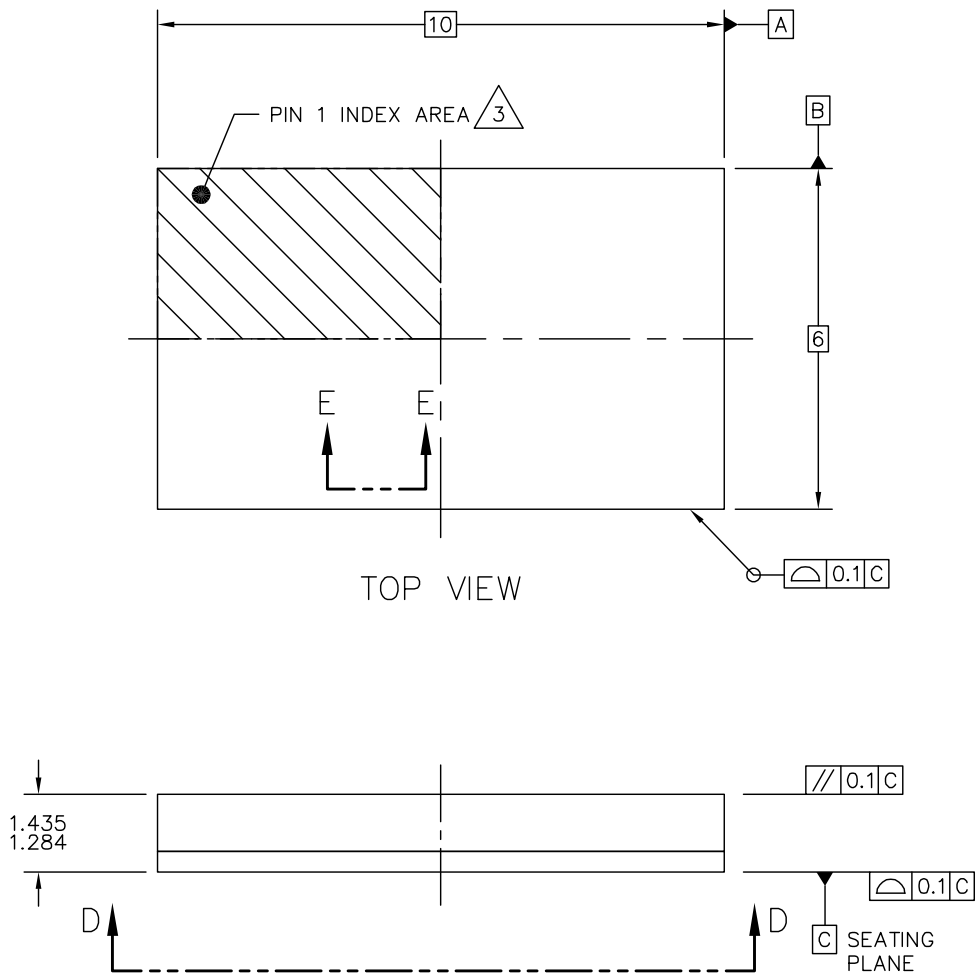
Part	Description	Part number	Manufacturer
C1, C4, C11, C12	10 $\mu$ F chip capacitor	GRM32EC72A106KE05L	Murata
C2, C3, C9, C10	1 $\mu$ F chip capacitor	GRM21BC72A105KE01L	Murata
C6, C7	1000 pF chip capacitor	GRM155R72A102KA01D	Murata
Q1	Power amplifier module	A5M36TG140	NXP
R1, R2, R5, R6, R8, R9	0 $\Omega$ , 1/20 W chip resistor	RC0201JR-070RL	Yageo
R3, R4	10 $\Omega$ , 1/20 W chip resistor	RC0201FR-0710RL	Yageo
PCB	Rogers RO4350B, 0.020, $\epsilon_r = 3.66$	D170087	MTL

Note: Component numbers C5, C8 and R7 are intentionally omitted.

15 Package information

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2



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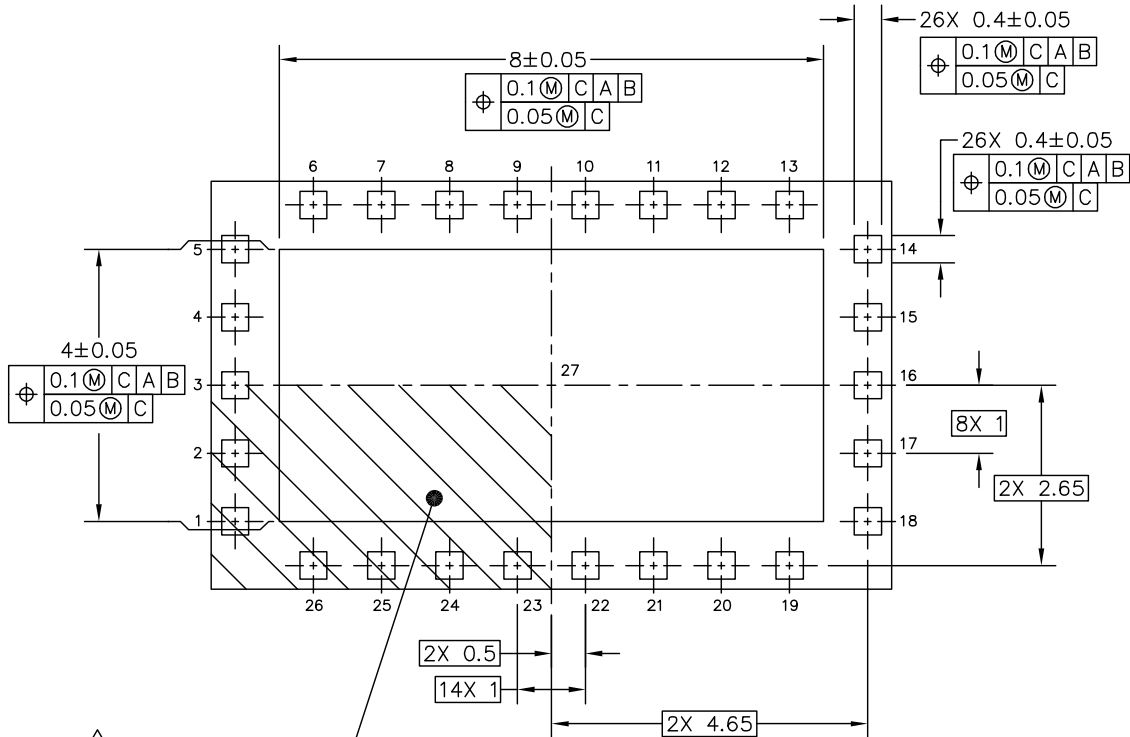
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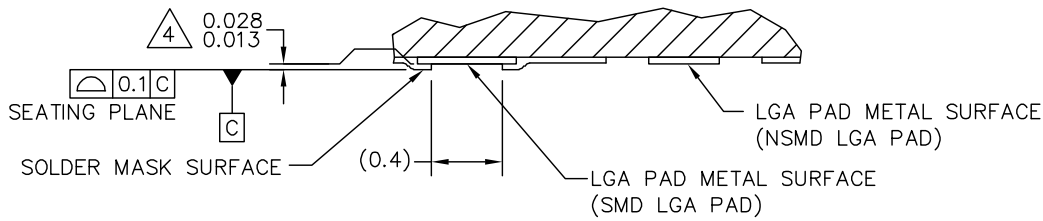
Figure 5. Package outline (10 mm × 6 mm Module) — top view

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2



VIEW D-D  
(BOTTOM VIEW)



SECTION E-E 5

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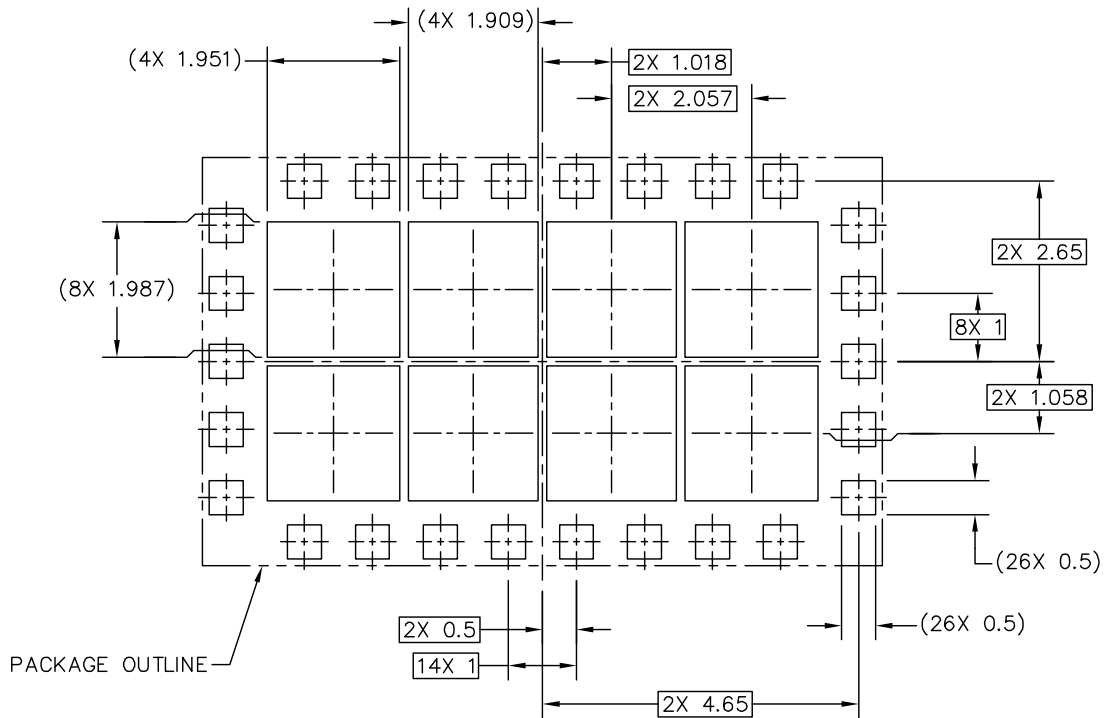
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Figure 6. Package outline (10 mm × 6 mm Module) — bottom view

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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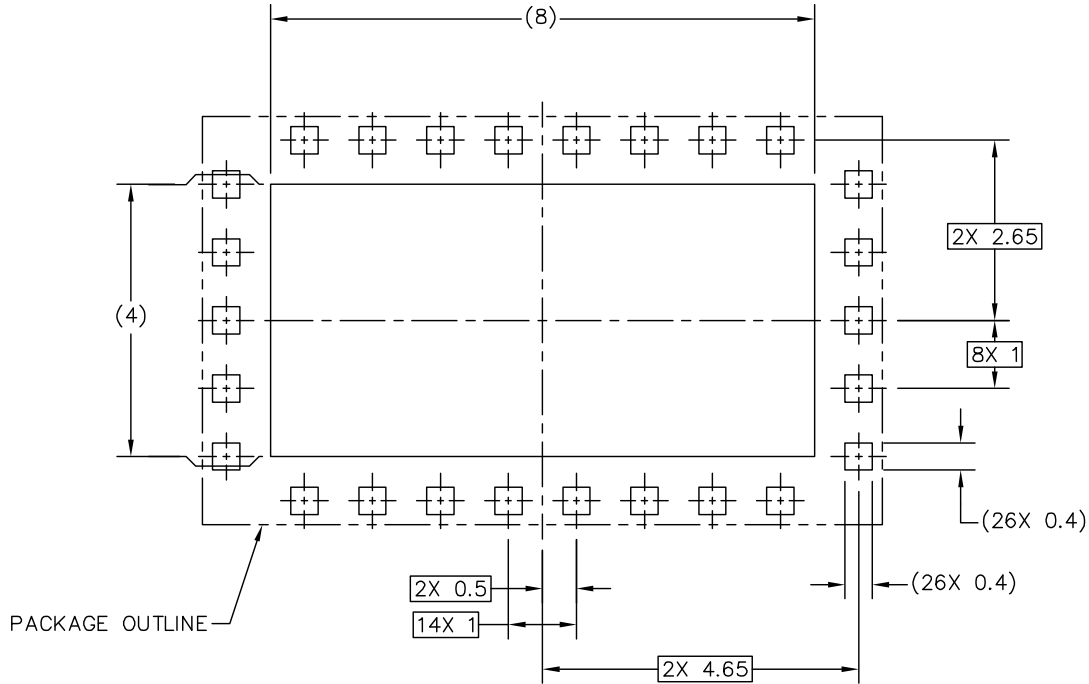
DATE: 26 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01540D	REVISION: 0	PAGE: 3
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Figure 7. Package outline (10 mm × 6 mm Module) — PCB design guidelines: solder mask opening pattern

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

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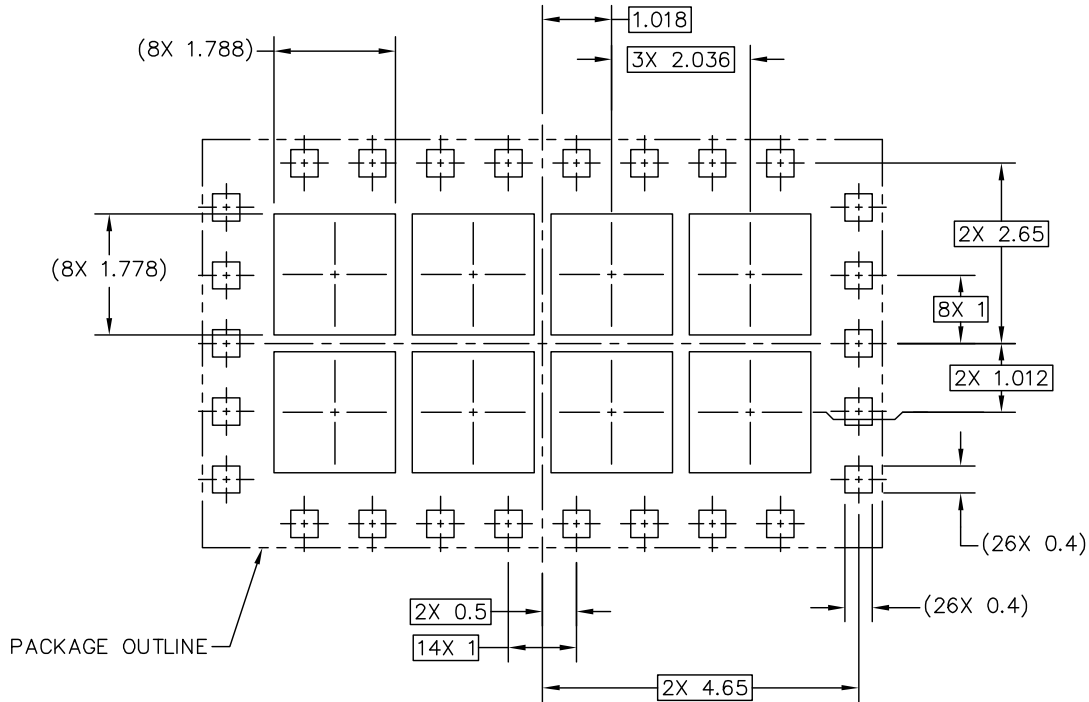
DATE: 26 SEP 2019

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Figure 8. Package outline (10 mm × 6 mm Module) — PCB design guidelines: I/O pads and solderable areas

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 9. Package outline (10 mm × 6 mm Module) — PCB design guidelines: solder paste stencil

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. DIMENSION APPLIES TO ALL LEADS AND FLAG.

5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON-SOLDERMASK DEFINED (NSMD).

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01540D	REVISION: 0	PAGE: 6
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**Figure 10. Package outline (10 mm × 6 mm Module) — notes**

## 16 Product documentation and tools

Refer to the following resources to aid your design process.

### Application notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Development tools

- Printed circuit boards

## 17 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

## 18 Revision history

The following table summarizes revisions to this document.

Table 17. Revision history

Document ID	Release date	Description
A5M36TG140 Rev. 2	27 November 2024	• Tables 12 and 13, Functional Tests, 3400 MHz and 3800 MHz: updated output power test condition, p. 7
A5M36TG140 Rev. 1	13 January 2023	<ul style="list-style-type: none"> <li>• Maximum Ratings table, Maximum Forward Gate Current value: updated to reflect device periphery, p. 4</li> <li>• Thermal Characteristics table, Thermal Resistance Channel-to-Case: updated to include both typical and maximum FEA simulated values, p. 4</li> <li>• Typical Performance table, 1-carrier 20 MHz LTE, ALT2: updated Typ value to reflect test data, p. 6</li> <li>• Typical Performance table, Pulsed CW, 10% Duty Cycle Typ values: updated to reflect test data, p. 6</li> </ul>
A5M36TG140 Rev. 0	28 October 2022	• Initial release of product data sheet

## Legal information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

### Definitions

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