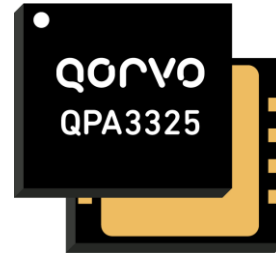
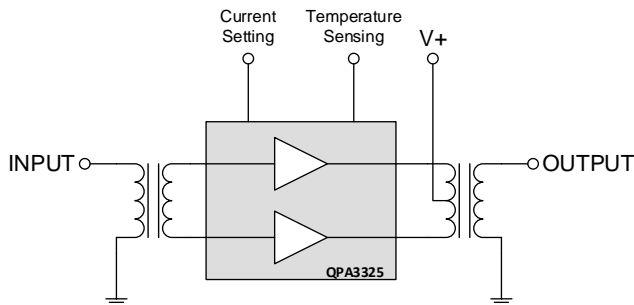


Product Description

The QPA3325 is a Power Doubler amplifier SMD Module. The part employs GaAs pHEMT and GaN HEMT die and is operated from 45MHz to 1218MHz. It provides excellent linearity and superior return loss performance with low noise and optimal reliability. DC current of the device can be externally adjusted for optimum distortion performance versus power consumption over a wide range of output level.

Functional Block Diagram



9 pin, 9.0 mm x 8.0 mm x 1.32 mm package

Product Features

- Excellent Linearity
- Superior Return Loss Performance
- Extremely Low Distortion
- Optimal Reliability
- Low Noise
- Unconditionally Stable Under all Terminations
- Extremely High Output Capability
- 25.0 dB min Gain at 1218 MHz
- 480 mA max at 24 VDC
- Temperature Sensing Feature

Applications

- 45 – 1218 MHz CATV Amplifier Systems

Ordering Information

Part No.	Description
QPA3325SB	Sample bag 5 pcs
QPA3325SR	7" Reel with 100 pcs
QPA3325TR13	13" Reel with 1000 pcs
QPA3325PCBA-410	Fully assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
DC Supply over-voltage (5 minutes)	+30 V
Storage Temperature	-40 to 100 °C
Operating Mounting Base Temperature	-30 to 110 °C
Moisture Sensitivity Level IPC/JEDEC J-STD-20	MSL 3 @ 260 °C
RF Input Voltage (single tone; on Evaluation Board)	75dBmV

Operation of this device outside the parameter ranges given above may cause permanent damage.

Electrical Specifications

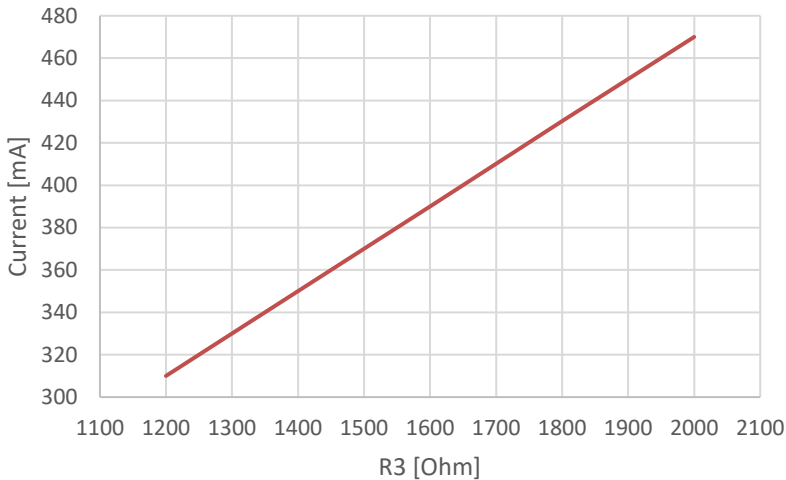
Parameter	Conditions (V+=24V, T _{MB} =30°C, Z _S =Z _L =75Ω, I _{DC} =I _{DC} (typ.))	Min	Typ	Max	Units
Operational Frequency Range	–	45		1218	MHz
Current (I _{DC})	–	–	470	480	mA
Gain (S ₂₁)	f _o = 45 MHz	–	23.7	–	dB
Gain (S ₂₁)	f _o = 1218 MHz	25.0	25.5	26.5	
Gain Slope ^[1]	45 to 1218 MHz	1.0	1.8	3.0	
Gain Flatness	45 to 1218 MHz (Peak to valley)		0.7	1.2	
Thermal Resistance	Junction to Mounting Base		3.9		K/W
Input Return Loss (-S ₁₁)	f _o = 45 to 1218 MHz	18	20	–	dB
Output Return Loss (-S ₂₂)	f _o = 45 to 1218 MHz	18	20	–	dB
Noise Figure	f _o = 50 to 1218 MHz	–	2.5	–	dB
CCN ^[2]	V _O = 57.3dBmV at 1215MHz, 18dB tilt, 190ch J.83/B	48	51		dB
BER ^[3]	256QAM (57 to 1215MHz). TCP ^[4] : 74dBmV		< 1,0E-09		BER

1. The slope is defined as the difference between the gain at the start frequency and the gain at the stop frequency.
2. CCN (Carrier to Composite Noise): The “composite noise” component is the summation of thermal noise and the intermodulation noise (i.e. noise-like intermodulation distortion products) produced by the amplifier. CCN is measured and calculated per ANSI/SCTE 17 2007.
3. Bit Error Rate (BER) before Reed-Solomon error correction
4. Total Composite Power

Current Adjustment

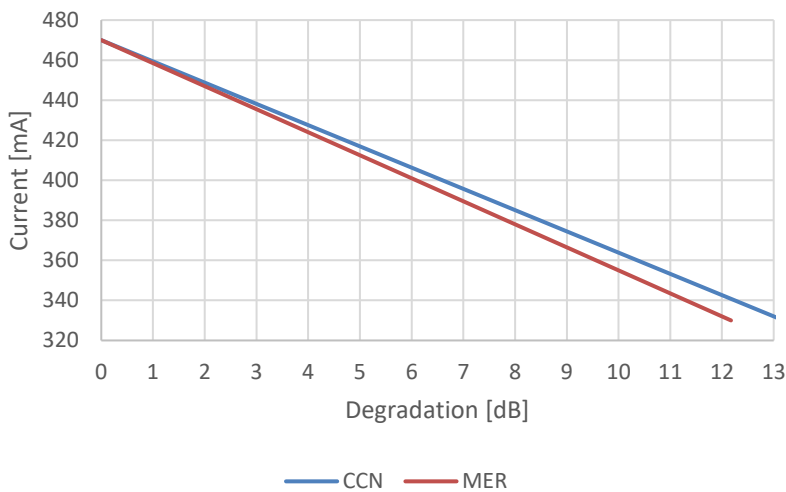
The QPA3325 can be operated over a wide range of current to provide maximum required performance with minimum current consumption. Changing the value of resistor R3 on application circuit allows a variation of the current between 310 mA and 470 mA (typ.). Within the recommended range of current between 330 mA and 470 mA gain (S21) change is less than 0.1 dB (typ.) and noise figure change is less than 0.1 dB (typ.).

Device Current vs. Resistor R3 (typical values)



Device Current [mA] (typical)	R5 [Ω]
470	2000
430	1800
390	1600
370	1500
330	1300
310	1200

Device Current vs. Distortion Degradation (typical values)



Test Condition:

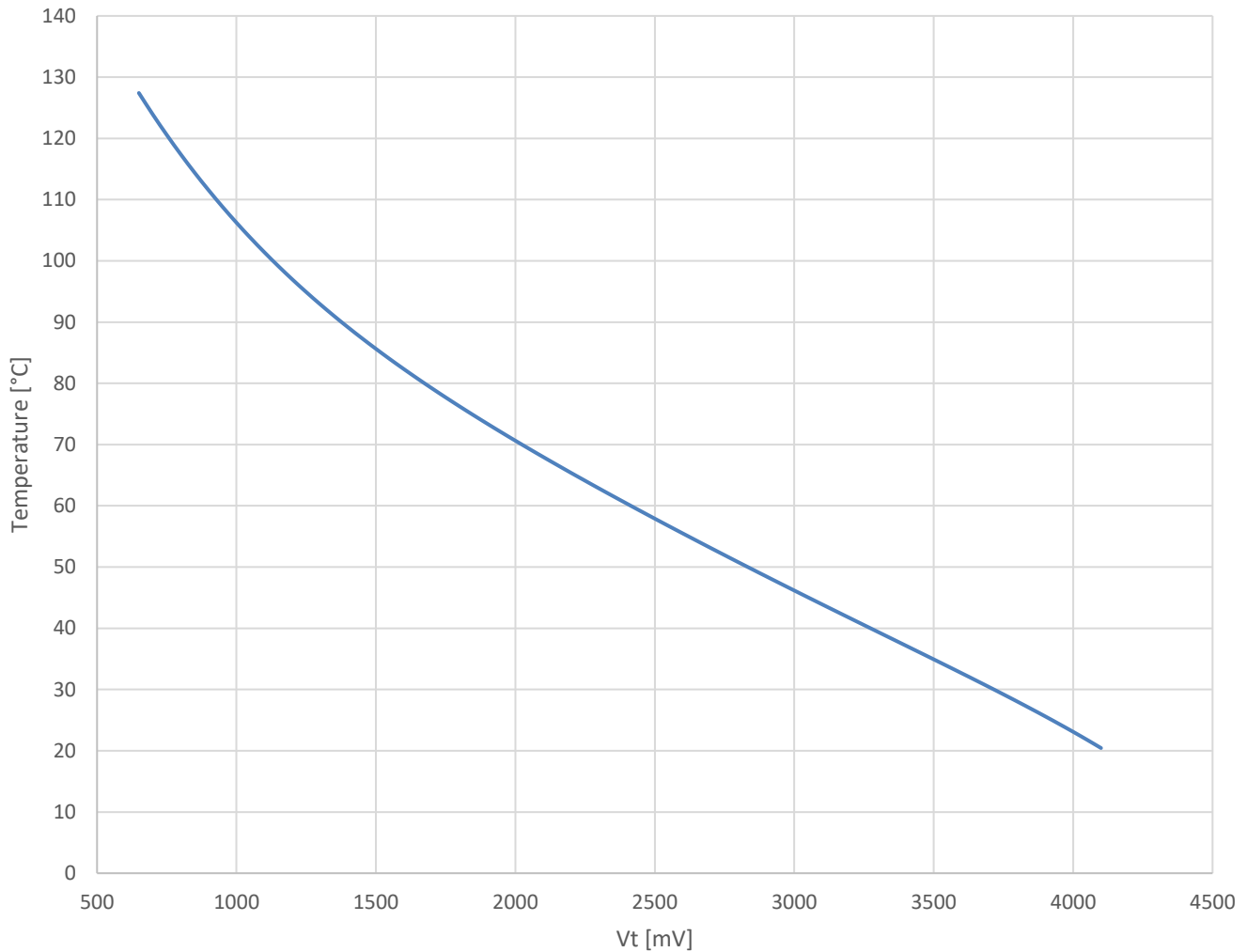
$V_{+} = 24V$, $T_{MB} = 30^{\circ}C$, $Z_S = Z_L = 75 \Omega$

$V_O = 57.35dBmV$ at 1215MHz, 18dB tilt, 190ch J.83/B 256QAM (57 to 1215MHz); TCP: 74dBmV

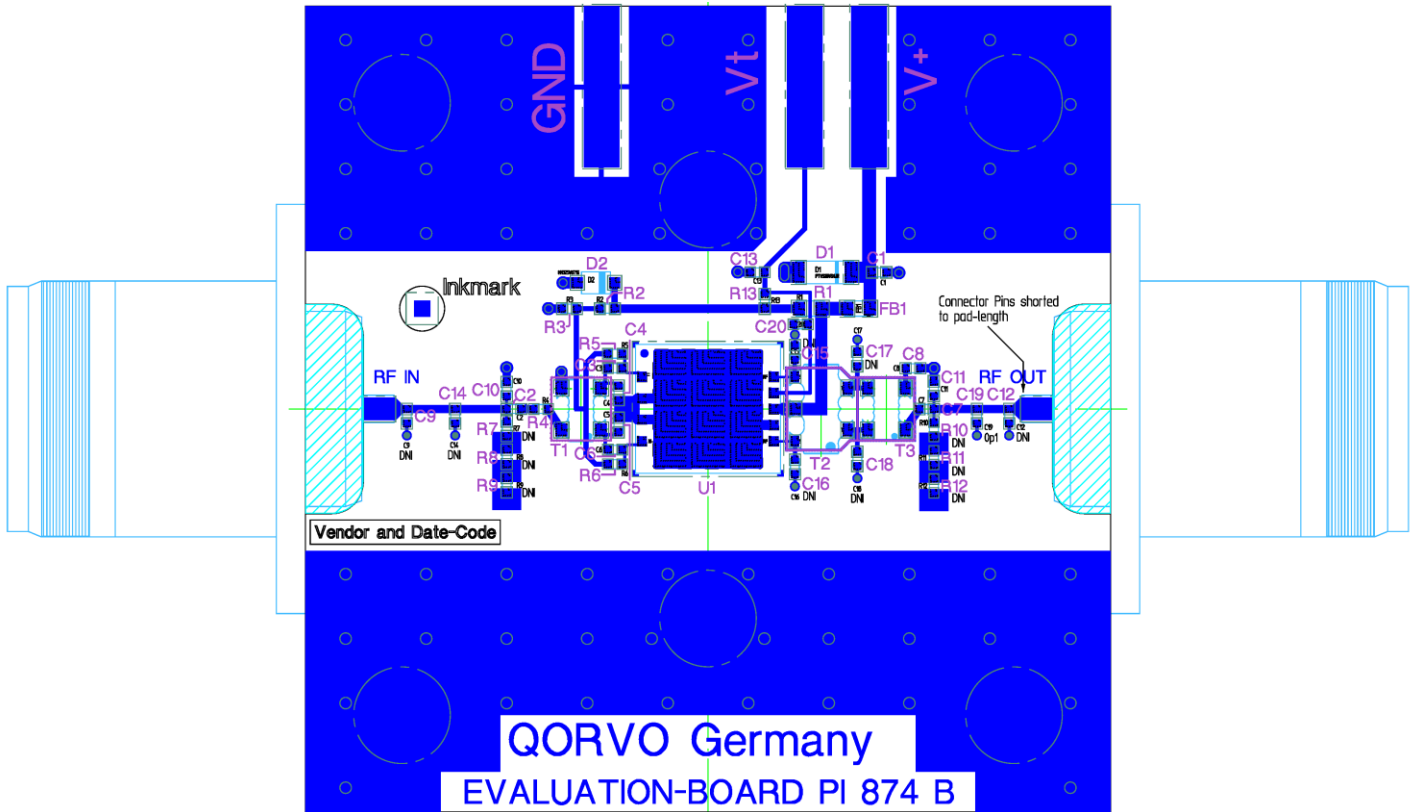
QPA3325 Temperature Sensing Feature

The QPA3325 provides an internal NTC resistor for temperature sensing. This resistor is located right next to the output transistor stage. Within the application circuit the NTC is part of a voltage divider. The output voltage of the voltage divider (V_t) can be correlated to the module backside temperature.

Module Backside Temperature vs. V_t (typical values)



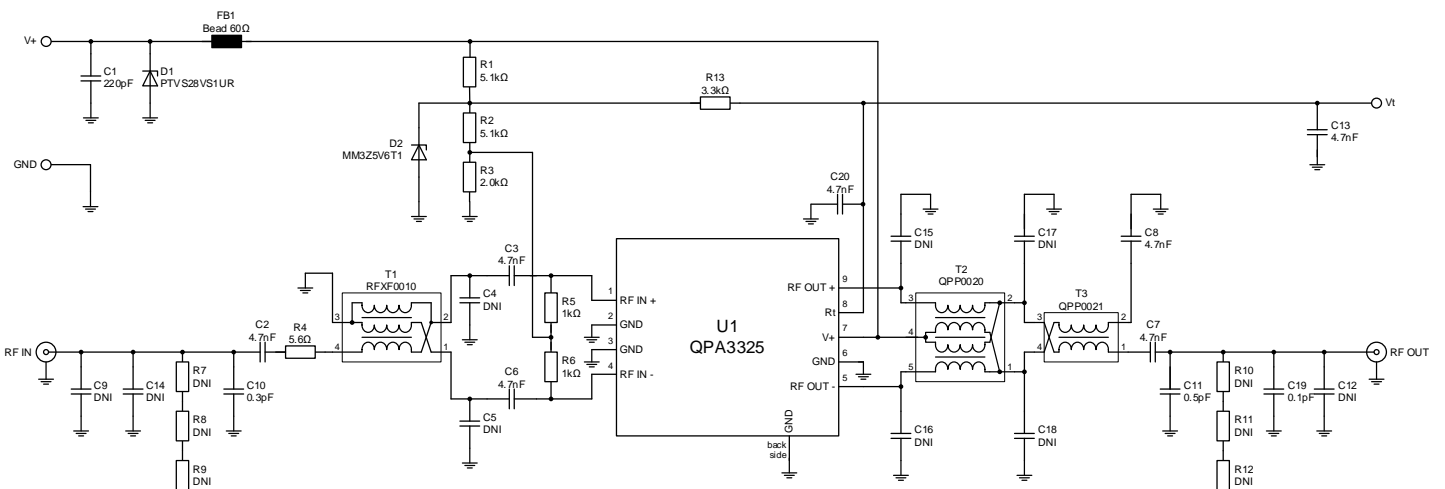
Evaluation Board Assembly Drawing



Evaluation board PCB: FR4, double sided, 1.5mm, 35um Cu

Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. A via drill diameter of 0.4mm and a minimum via wall copper plating thickness of 25um is recommended. Open vias are preferred to allow flux and gases to escape during reflow soldering and therefore to minimize voiding. Underneath this via array a heat sink with thermal grease needs to be placed which is able to dissipate the complete module DC power (up to 11.52Watts). In any case the module backside temperature should not exceed 110 °C.

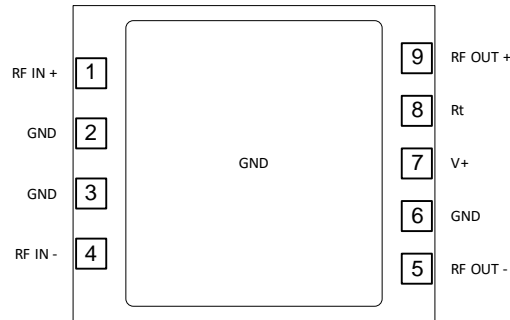
Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)

Reference Des.	Value	Description	Manuf.	Part Number
PCB		PCB QPA3325 – EVB 874A	Qorvo	
C4, C5, C9, C12, C14, C15, C16, C17, C18	DNI	optional to improve matching in application		
C2, C3, C6, C7, C8, C13, C20	4.7 nF	CAP, 0402, 10%, 50V, X7R		
C1	220 pF	CAP, 0402, 10%, 50V, X7R		
C10	0.3 pF	CAP, 0402, ± 0.1 pF, 50V, C0G		
C11	0.5 pF	CAP, 0402, ± 0.1 pF, 50V, C0G		
C19	0.1 pF	CAP, 0402, ± 0.05 pF, 50V, C0G		
R1	5.1 k Ω	RES, 0603, 1%, TK100		
R2	5.1 k Ω	RES, 0402, 1%, TK100		
R3	2.0 k Ω	RES, 0402, 1%, TK100 to set current value see page 5		
R4	5.6 Ω	RES, 0402, 1%, TK200		
R5, R6	1.0 k Ω	RES, 0402, 1%, TK100		
R13	3.3 k Ω	RES, 0402, 1%, TK100		
R7, R8, R9, R10, R11, R12	DNI	optional to improve matching in application		
FB1	60 Ω at 100MHz	Impedance Bead	Murata	BLM18PG600SN1
D1	28 V	Diode, TVS, PTVS28VS1UR, SOD123W	Nexperia	PTVS28VS1UR
D2	5.6 V	Zener Diode MM3Z5V6T1G, SOD-323	ON Semiconductor	MM3Z5V6T1G
T1		Balun	Qorvo	RFXF0010
T2		Transformer	Qorvo	QPP0020
T3		Balun	Qorvo	QPP0021
U1	DUT	QPA3325	Qorvo	QPA3325

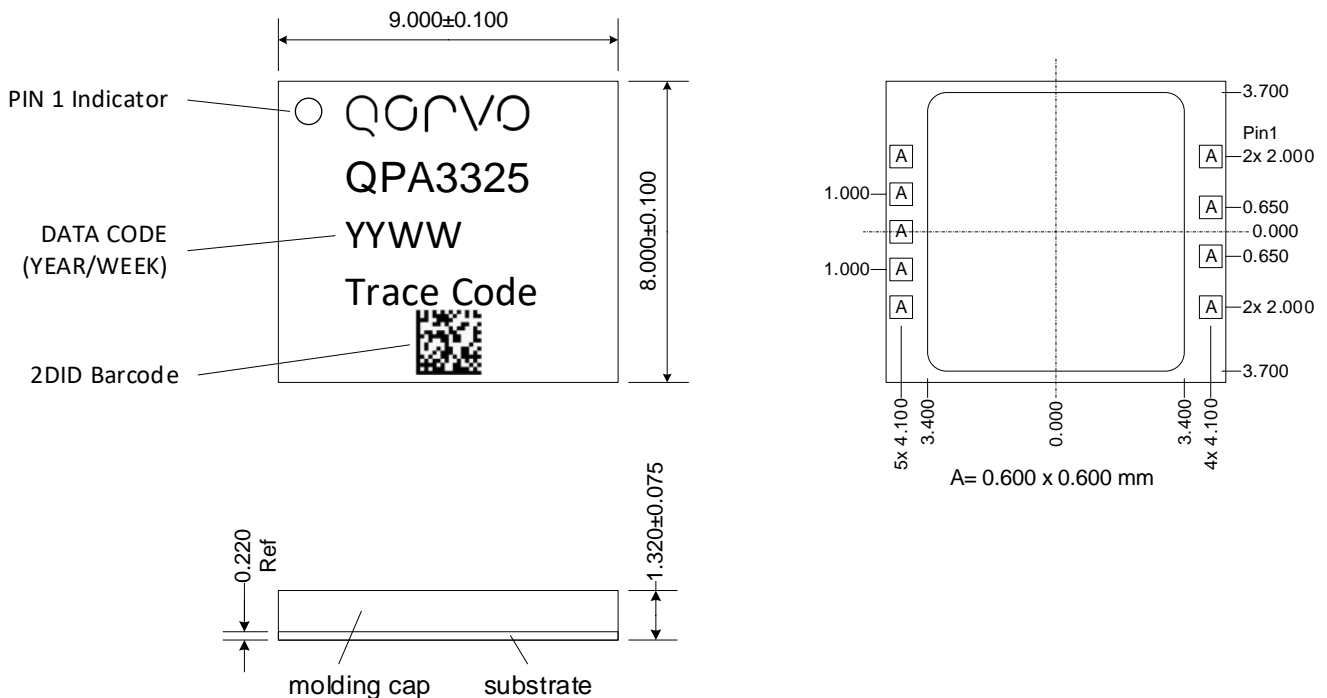
Pin Configuration



Pin Description

Pin No.	Label	Description
1	RF IN (+)	RF AMP Positive Input
2, 3, 6	GND	Ground
4	RF IN (-)	RF AMP Negative Input
5	RF OUT (-)	RF AMP Negative Output
7	V+	Supply Voltage 24V
8	Rt	NTC Output for Temperature Sensing
9	RF OUT (+)	RF AMP Positive Output

Package Outline Drawing (Dimensions in millimeters)



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: ENEPIG

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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