



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

General Description

The MAX2067 high-linearity analog variable-gain amplifier (VGA) is a monolithic SiGe BiCMOS attenuator and amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range (see the *Typical Application Circuit*). The analog attenuator is controlled using an external voltage or through the SPI™-compatible interface using an on-chip 8-bit DAC.

Because each stage has its own RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), or OIP3 (amplifier last). The device's performance features include 22dB amplifier gain (amplifier only), 4dB NF at maximum gain (includes attenuator insertion loss), and a high OIP3 level of +43dBm. Each of these features makes the MAX2067 an ideal VGA for numerous receiver and transmitter applications.

In addition, the MAX2067 operates from a single +5V supply with full performance, or a single +3.3V supply with slightly reduced performance, and has an adjustable bias to trade current consumption for linearity performance. This device is available in a compact 40-pin thin QFN package (6mm x 6mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range (T_C = -40°C to +85°C).

Applications

IF and RF Gain Stages
 Temperature Compensation Circuits
 Cellular Band WCDMA and cdma2000® Base Stations
 GSM 850/GSM 900 EDGE Base Stations
 WiMAX and LTE Base Stations and Customer Premise Equipment
 Fixed Broadband Wireless Access
 Wireless Local Loop
 Military Systems
 Video-on-Demand (VOD) and DOCSIS®-Compliant EDGE QAM Modulation
 Cable Modem Termination Systems (CMTS)
 RFID Handheld and Portal Readers

Features

- ◆ 50MHz to 1000MHz RF Frequency Range
- ◆ Pin-Compatible Family Includes
 - MAX2065 (Analog/Digital VGA)
 - MAX2066 (Digital VGA)
- ◆ +21.9dB (typ) Maximum Gain
- ◆ 0.5dB Gain Flatness Over 100MHz Bandwidth
- ◆ 31dB Gain Range
- ◆ Built-In DAC for Analog Attenuation Control
- ◆ Excellent Linearity (Configured with Amplifier Last)
 - +43dBm OIP3
 - +66dBm OIP2
 - +19dBm Output 1dB Compression Point
 - 70dBc HD2
 - 87dBc HD3
- ◆ 4dB Typical Noise Figure (NF)
- ◆ Single +5V Supply (Optional +3.3V Operation)
- ◆ External Current-Setting Resistors Provide Option for Operating Device in Reduced-Power/Reduced-Performance Mode

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|--------------|----------------|-----------------|
| MAX2067ETL+ | -40°C to +85°C | 40 Thin QFN-EP* |
| MAX2067ETL+T | -40°C to +85°C | 40 Thin QFN-EP* |

+Denotes a lead-free package.

*EP = Exposed pad.

T = Tape and reel.

Pin Configuration appears at end of data sheet.

SPI is a trademark of Motorola, Inc.

cdma2000 is a registered trademark of Telecommunications Industry Association.

DOCSIS and CableLabs are registered trademarks of Cable Television Laboratories, Inc. (CableLabs®).



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|------------------------|---|---|
| VCC_ to GND | -0.3V to +5.5V | RF Input Power (AMP_IN)..... | +18dBm |
| VDD_LOGIC, DATA, $\overline{\text{CS}}$, CLK, VDAC_EN, VREF_SELECT..... | -0.3V to (VCC_ + 0.3V) | Continuous Power Dissipation (Note 1) | 6.5W |
| AMP_IN, AMP_OUT, VREF_IN, ANALOG_VCTRL | -0.3V to (VCC_ + 0.3V) | θ_{JA} (Notes 2, 3)..... | +38°C/W |
| ATTEN_IN, ATTEN_OUT..... | -1.2V to +1.2V | θ_{JC} (Note 3) | +10°C/W |
| RSET to GND..... | -0.3V to +1.2V | Operating Temperature Range (Note 4)..... | $T_{\text{C}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ |
| RF Input Power (ATTEN_IN, ATTEN_OUT)..... | +20dBm | Maximum Junction Temperature | +150°C |
| | | Storage Temperature Range | -65°C to +150°C |
| | | Lead Temperature (soldering, 10s) | +300°C |

Note 1: Based on junction temperature $T_{\text{J}} = T_{\text{C}} + (\theta_{\text{JC}} \times V_{\text{CC}} \times I_{\text{CC}})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a printed-circuit board (PCB). See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Junction temperature $T_{\text{J}} = T_{\text{A}} + (\theta_{\text{JA}} \times V_{\text{CC}} \times I_{\text{CC}})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Note 4: T_{C} is the temperature on the exposed pad of the package. T_{A} is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, high-current (HC) mode, $V_{\text{CC}} = V_{\text{DD}} = +3.0\text{V}$ to $+3.6\text{V}$, $T_{\text{C}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Typical values are at $V_{\text{CC}} = V_{\text{DD}} = +3.3\text{V}$ and $T_{\text{C}} = +25^{\circ}\text{C}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|------------|-----|-----|-----|-------|
| Supply Voltage | V_{CC} | Note 5 | 3.0 | 3.3 | 3.6 | V |
| Supply Current | I_{CC} | | | 60 | 82 | mA |
| LOGIC INPUTS (DATA, $\overline{\text{CS}}$, CLK, VDAC_EN, VREF_SELECT) | | | | | | |
| Input High Voltage | V_{IH} | | | 2 | | V |
| Input Low Voltage | V_{IL} | | | 0.8 | | V |

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, $V_{\text{CC}} = V_{\text{DD}} = +4.75\text{V}$ to $+5.25\text{V}$, $T_{\text{C}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Typical values are at $V_{\text{CC}} = V_{\text{DD}} = +5\text{V}$ and $T_{\text{C}} = +25^{\circ}\text{C}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|------------------------|------|-----|------|---------------|
| Supply Voltage | V_{CC} | | 4.75 | 5 | 5.25 | V |
| Supply Current | I_{CC} | Low-current (LC) mode | | 72 | 92 | mA |
| | | High-current (HC) mode | | 123 | 146 | |
| LOGIC INPUTS (DATA, $\overline{\text{CS}}$, CLK, VDAC_EN, VREF_SELECT) | | | | | | |
| Input High Voltage | V_{IH} | | 3 | | | V |
| Input Low Voltage | V_{IL} | | | | 0.8 | V |
| Input Current Logic-High | I_{IH} | | -1 | | +1 | μA |
| Input Current Logic-Low | I_{IL} | | -1 | | +1 | μA |

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, $V_{CC} = V_{DD} = +3.0V$ to $+3.6V$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = V_{DD} = +3.3V$, HC mode with attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|----------|--|-----|------|------|-------|
| RF Frequency Range | f_{RF} | (Notes 5, 7) | 50 | | 1000 | MHz |
| Small-Signal Gain | G | | | 21.3 | | dB |
| Output Third-Order Intercept Point | OIP3 | $P_{OUT} = 0dBm/$ tone, maximum gain setting | | 38 | | dBm |
| Noise Figure | NF | Maximum gain setting | | 4.3 | | dB |
| Total Attenuation Range | | | | 31 | | dB |

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, $V_{CC} = V_{DD} = +4.75V$ to $+5.25V$, HC mode with attenuator set for maximum gain, $50MHz \leq f_{RF} \leq 1000MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = V_{DD} = +5.0V$, HC mode, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------|---|--------|--------|------|----------------|
| RF Frequency Range | f_{RF} | (Notes 5, 7) | 50 | | 1000 | MHz |
| Small-Signal Gain | G | 200MHz | | 21.9 | | dB |
| | | 350MHz, $T_C = +25^\circ C$ (Note 5) | 20.3 | 21.3 | 22.3 | |
| | | 450MHz | | 20.9 | | |
| | | 750MHz | | 19.4 | | |
| | | 900MHz | | 18.7 | | |
| Gain Variation vs. Temperature | | | | -0.006 | | dB/ $^\circ C$ |
| Gain Flatness vs. Frequency | | Any 100MHz frequency band from 50MHz to 500MHz | | 0.5 | | dB |
| Noise Figure | NF | 200MHz | | 4 | | dB |
| | | 350MHz, $T_C = +25^\circ C$ (Note 5) | | 4.2 | 5.2 | |
| | | 450MHz | | 4.3 | | |
| | | 750MHz | | 4.8 | | |
| | | 900MHz | | 5 | | |
| Total Attenuation Range | | | | 31 | | dB |
| Output Second-Order Intercept Point | OIP2 | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz$, $f_1 + f_2$ | | 66 | | dBm |
| Output Third-Order Intercept Point | OIP3 | $P_{OUT} = 0dBm/$ tone, HC mode, $\Delta f = 1MHz$ | 200MHz | | 43 | dBm |
| | | | 350MHz | | 40.8 | |
| | | | 450MHz | | 39.8 | |
| | | | 750MHz | | 37.3 | |
| | | | 900MHz | | 36.2 | |
| | | $P_{OUT} = 0dBm/$ tone, LC mode, $\Delta f = 1MHz$ | 200MHz | | 40 | |
| | | | 350MHz | | 38.2 | |
| | | | 450MHz | | 37.4 | |
| | | | 750MHz | | 35.5 | |
| | | | 900MHz | | 34.3 | |

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(Typical Application Circuit, $V_{CC} = V_{DD} = +4.75$ to $+5.25V$, HC mode with attenuator set for maximum gain, $50MHz \leq f_{RF} \leq 1000MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = V_{DD} = +5.0V$, HC mode, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|-----------|---|------|-------|------|------------|
| Output -1dB Compression Point | P_{1dB} | 350MHz, $T_C = +25^\circ C$ (Notes 5, 8) | 17 | 18.7 | | dBm |
| Second Harmonic | | $P_{OUT} = +3dBm$, $f_{RF} = 200MHz$, $T_C = +25^\circ C$ (Note 5) | -61 | -70 | | dBc |
| Third Harmonic | | $P_{OUT} = +3dBm$, $f_{RF} = 200MHz$, $T_C = +25^\circ C$ (Note 5) | -74 | -87 | | dBc |
| Attenuator Response Time (Note 9) | | Input from ANALOG_VCTRL | | 1 | | μs |
| | | Input from \overline{CS} rising edge | | 3.2 | | |
| Group Delay | | Maximum gain setting, includes EV kit PCB delays | | 0.8 | | ns |
| Input Return Loss | | 50 Ω source, maximum gain setting | | 30 | | dB |
| Output Return Loss | | 50 Ω load, maximum gain setting | | 16 | | dB |
| ANALOG ATTENUATOR | | | | | | |
| Insertion Loss | | | | 1.2 | | dB |
| Input Second-Order Intercept Point | IIP2 | $P_{RF1} = 0dBm$, $P_{RF2} = 0dBm$, maximum gain setting, $\Delta f = 1MHz$, $f_1 + f_2$ | | 70 | | dBm |
| Input Third-Order Intercept Point | IIP3 | $P_{RF1} = 0dBm$, $P_{RF2} = 0dBm$, maximum gain setting, $\Delta f = 1MHz$ | | 36 | | dBm |
| Attenuation Range | | Analog control input | | 31 | | dB |
| Gain-Control Slope | | Analog control input | | -12.5 | | dB/V |
| Maximum Gain-Control Slope | | Over analog control input range | | -35 | | dB/V |
| Insertion Phase Change | | Over analog control input range | | 18 | | Degrees |
| Group Delay vs. Control Voltage | | Over analog control input range | | -0.25 | | ns |
| Analog Control Input Range | | | 0.25 | | 2.75 | V |
| Analog Control Input Impedance | | | | 80 | | k Ω |
| Input Return Loss | | 50 Ω source, maximum gain setting | | 22 | | dB |
| Output Return Loss | | 50 Ω load, maximum gain setting | | 22 | | dB |
| DAC | | | | | | |
| Number of Bits | | | | 8 | | Bits |
| Output Voltage | | DAC code = 00000000 | | | 0.25 | V |
| | | DAC code = 11111111 | 2.75 | | | |

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(Typical Application Circuit, $V_{CC} = V_{DD} = +4.75$ to $+5.25V$, HC mode with attenuator set for maximum gain, $50MHz \leq f_{RF} \leq 1000MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = V_{DD} = +5.0V$, HC mode, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, unless otherwise noted.) (Note 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|------------|-----|-----|-----|-------|
| SERIAL PERIPHERAL INTERFACE (SPI) | | | | | | |
| Maximum Clock Speed | f _{CLK} | | | 20 | | MHz |
| Data-to-Clock Setup Time | t _{CS} | | | 2 | | ns |
| Data-to-Clock Hold Time | t _{CH} | | | 2.5 | | ns |
| Clock-to- \overline{CS} Setup Time | t _{ES} | | | 3 | | ns |
| \overline{CS} Positive Pulse Width | t _{EW} | | | 7 | | ns |
| \overline{CS} Setup Time | t _{EWS} | | | 3.5 | | ns |
| Clock Pulse Width | t _{CW} | | | 5 | | ns |

Note 5: Guaranteed by design and characterization.

Note 6: All limits include external component losses. Output measurements are performed at RF output port of the *Typical Application Circuit*

Note 7: Operating outside this range is possible, but with degraded performance of some parameters.

Note 8: It is advisable not to continuously operate the VGA RF input above +15dBm.

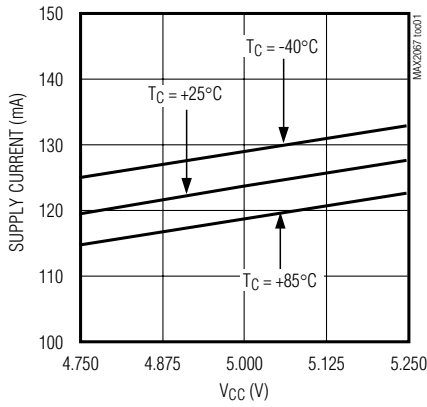
Note 9: Response time includes full attenuation range change with output setting to within $\pm 0.1dB$.

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

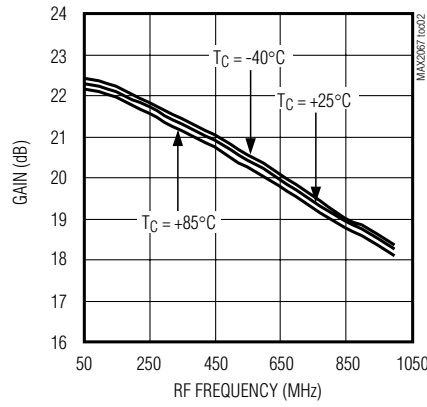
Typical Operating Characteristics

($V_{CC} = V_{DD} = +5.0V$, HC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)

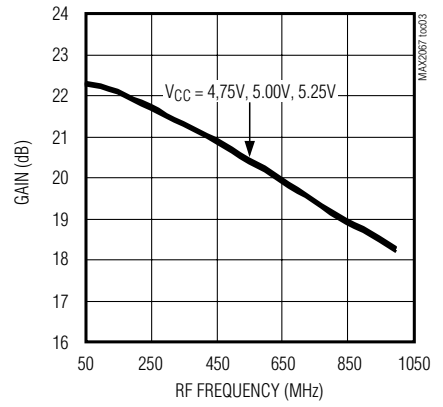
SUPPLY CURRENT vs. SUPPLY VOLTAGE



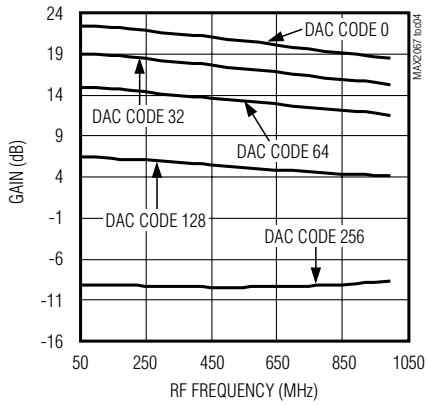
GAIN vs. RF FREQUENCY



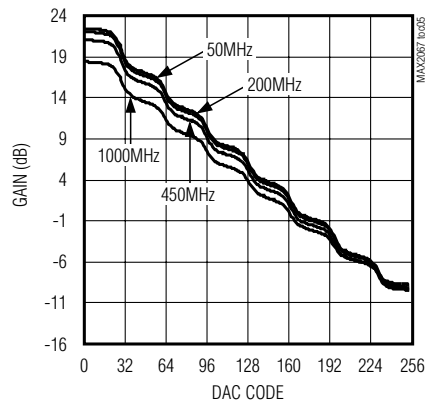
GAIN vs. RF FREQUENCY



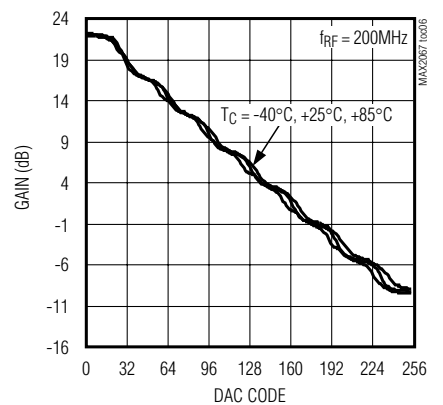
GAIN OVER ATTENUATOR SETTING vs. RF FREQUENCY



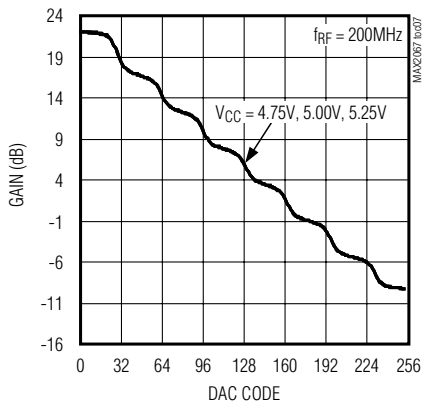
GAIN vs. ATTENUATOR SETTING



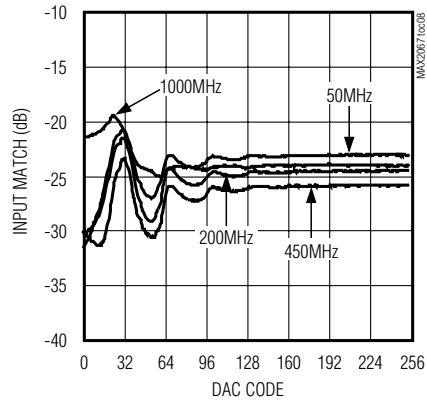
GAIN vs. ATTENUATOR SETTING



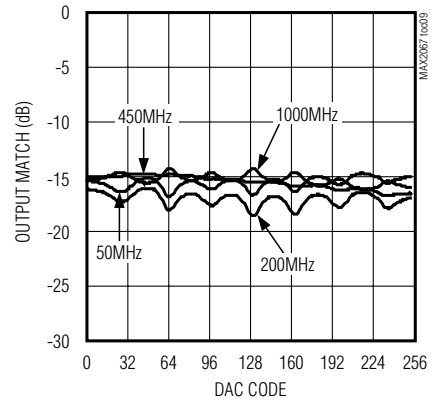
GAIN vs. ATTENUATOR SETTING



INPUT MATCH vs. ATTENUATOR SETTING



OUTPUT MATCH vs. ATTENUATOR SETTING



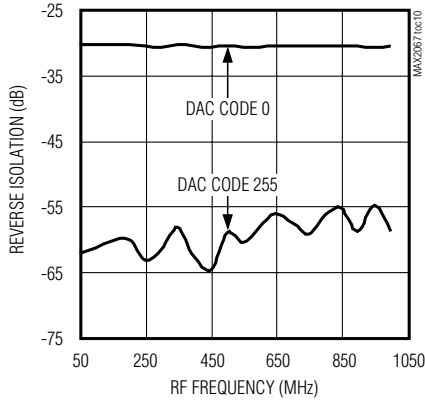
50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

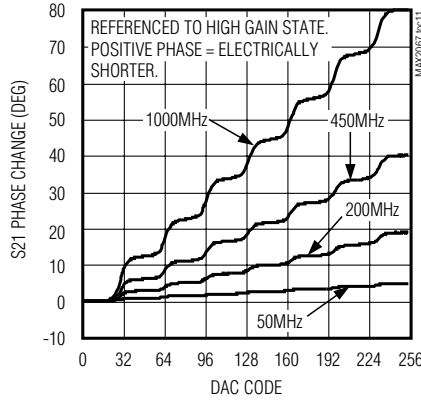
Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +5.0V$, HC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)

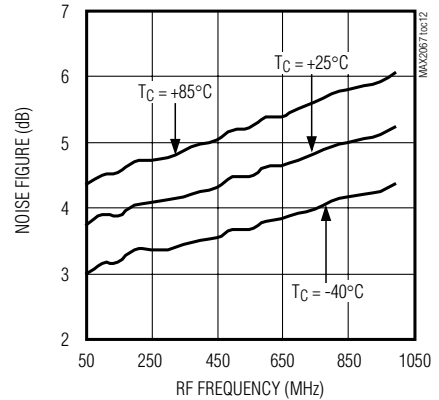
REVERSE ISOLATION OVER ATTENUATOR SETTING vs. RF FREQUENCY



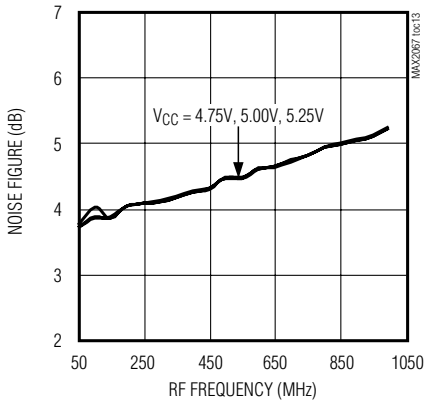
S21 PHASE CHANGE vs. ATTENUATOR SETTING



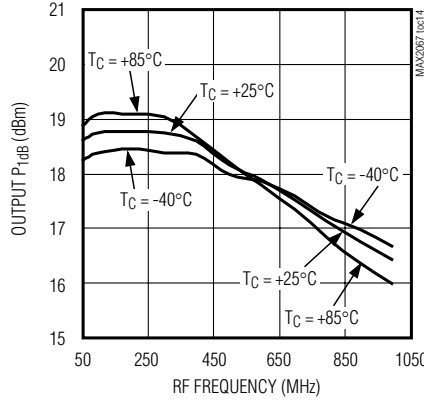
NOISE FIGURE vs. RF FREQUENCY



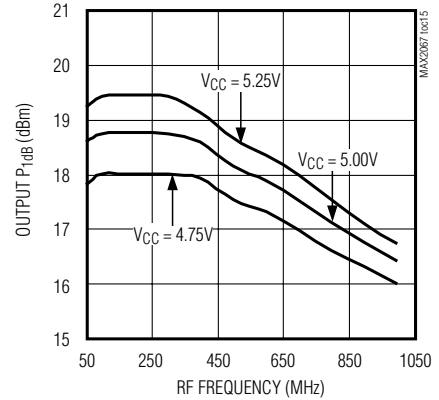
NOISE FIGURE vs. RF FREQUENCY



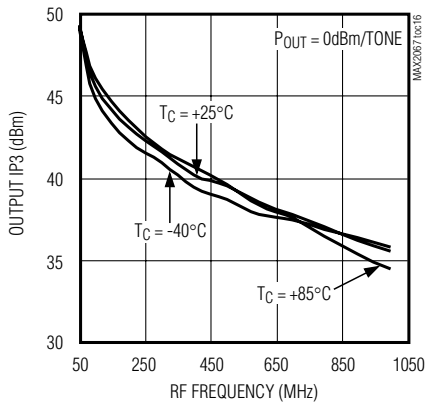
OUTPUT P1dB vs. RF FREQUENCY



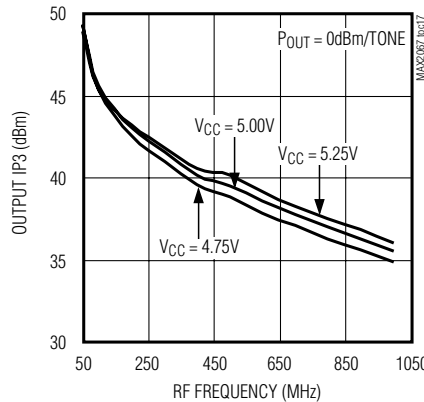
OUTPUT P1dB vs. RF FREQUENCY



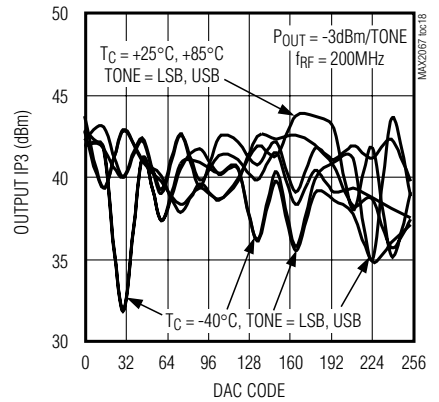
OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. RF FREQUENCY



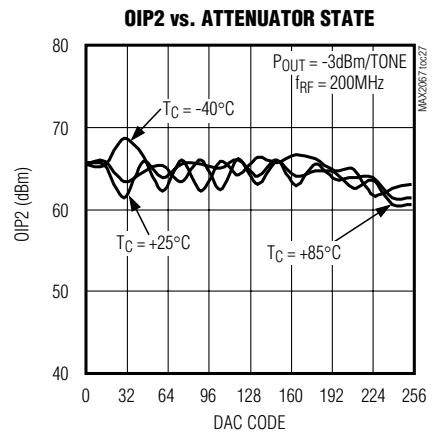
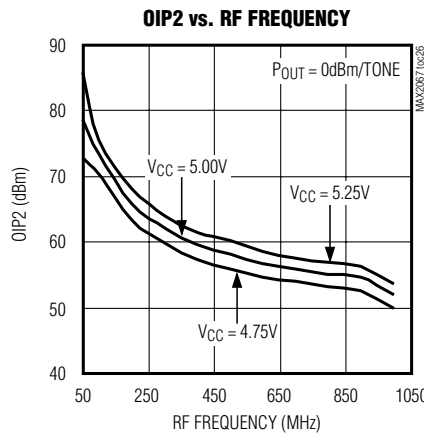
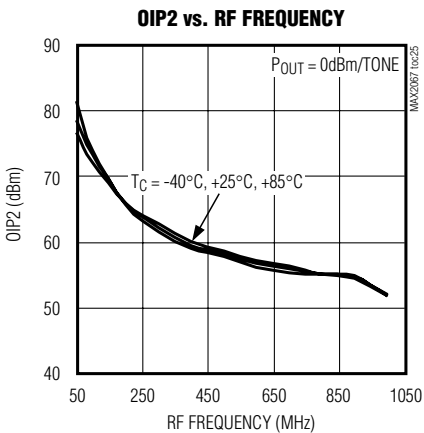
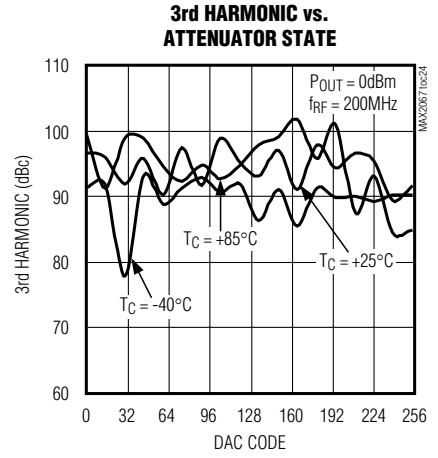
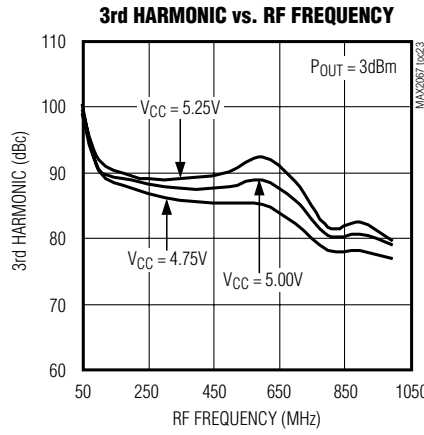
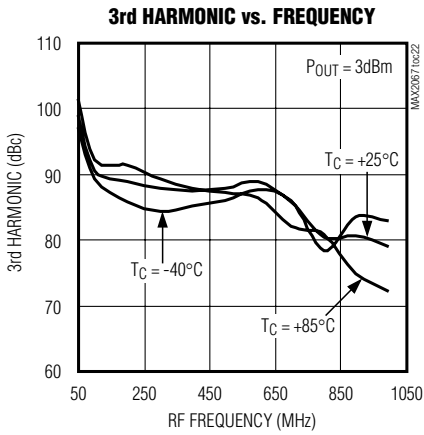
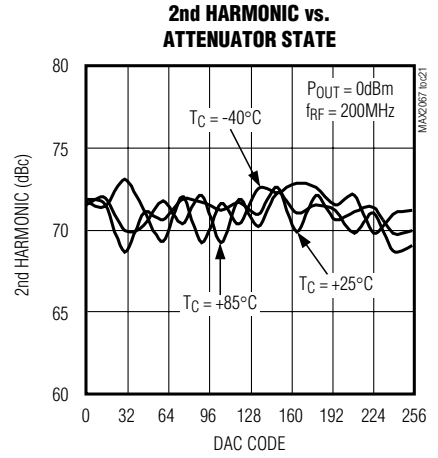
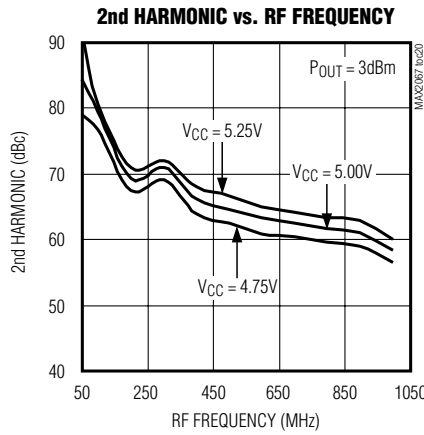
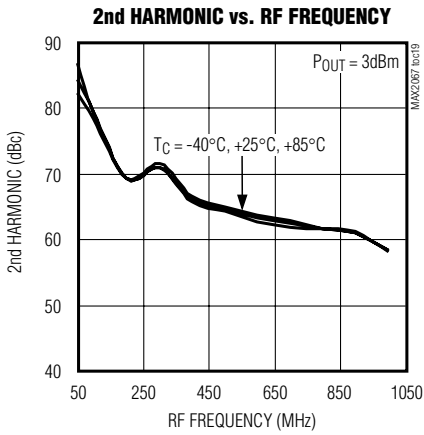
OUTPUT IP3 vs. ATTENUATOR STATE



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +5.0V$, HC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)

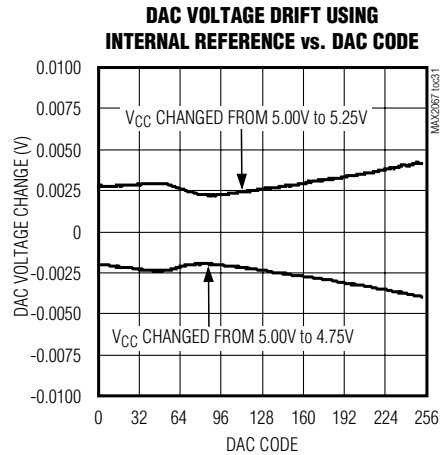
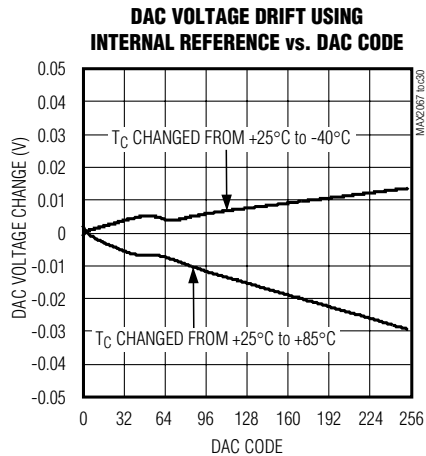
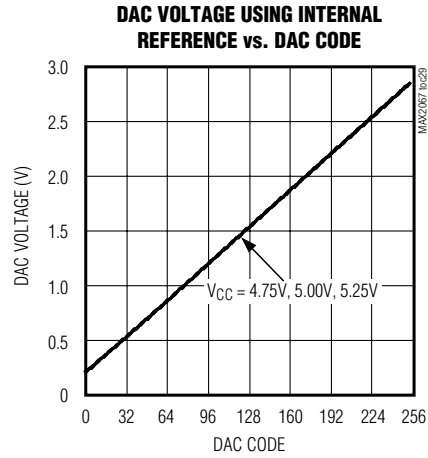
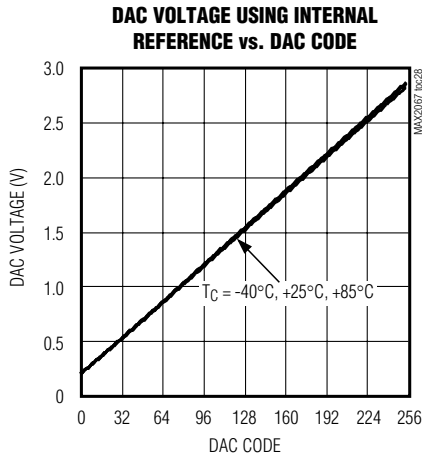


50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

Typical Operating Characteristics (continued)

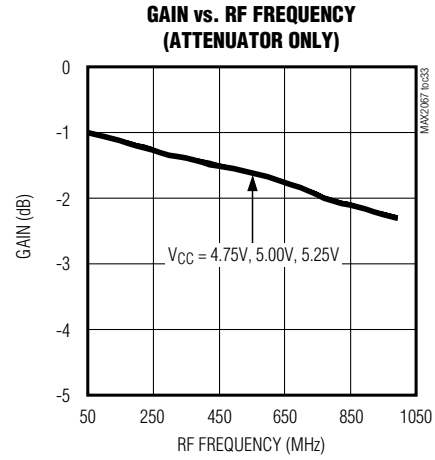
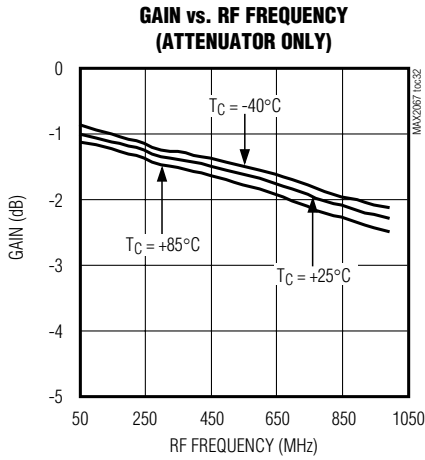
($V_{CC} = V_{DD} = +5.0V$, HC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +5.0V$, attenuator only, maximum gain, $P_{IN} = -20dBm$, and $T_C = +25^\circ C$, unless otherwise noted.)



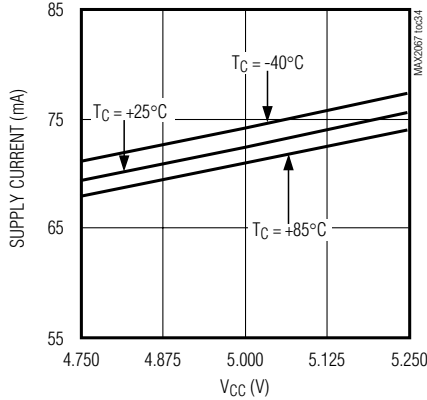
50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

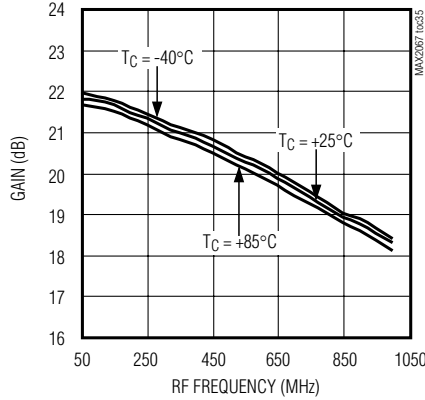
Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +5.0V$, LC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)

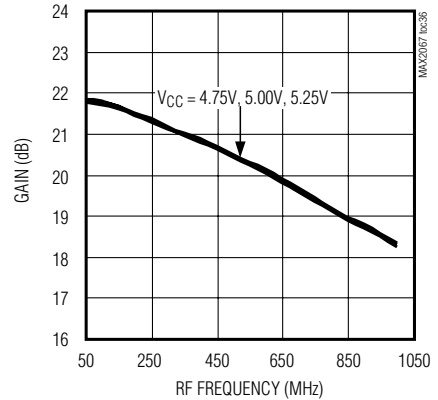
SUPPLY CURRENT vs. SUPPLY VOLTAGE (LOW-CURRENT MODE)



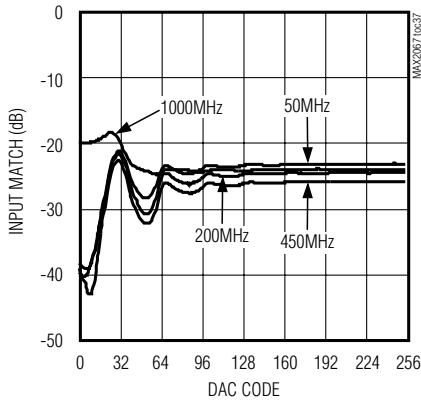
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



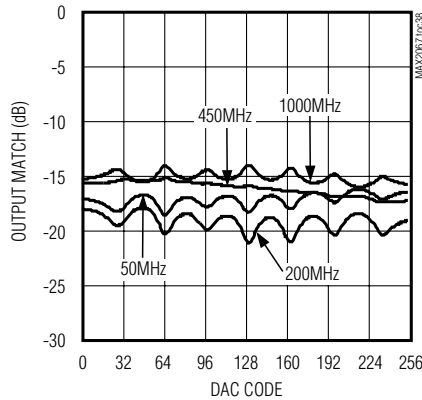
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



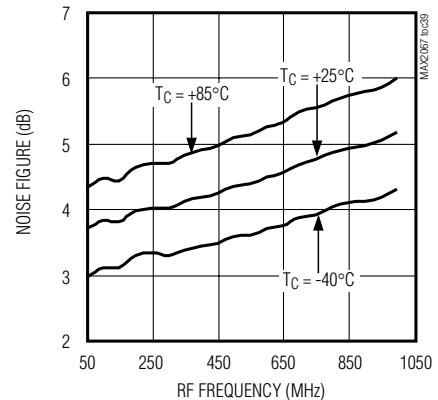
INPUT MATCH vs. ATTENUATOR SETTING (LOW-CURRENT MODE)



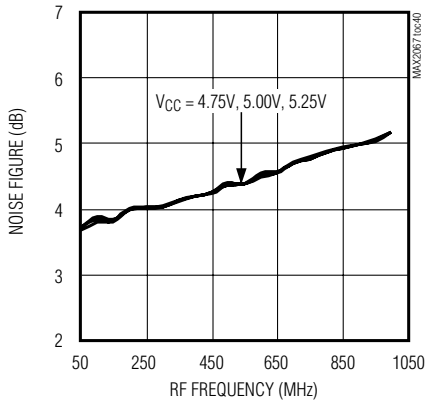
OUTPUT MATCH vs. ATTENUATOR SETTING (LOW-CURRENT MODE)



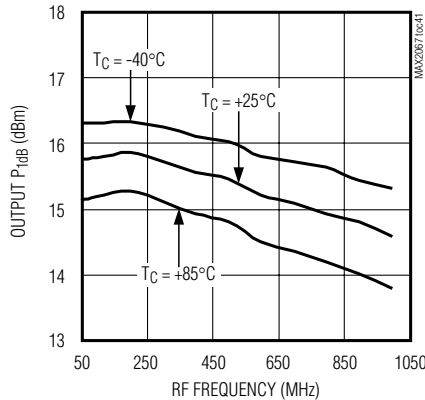
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



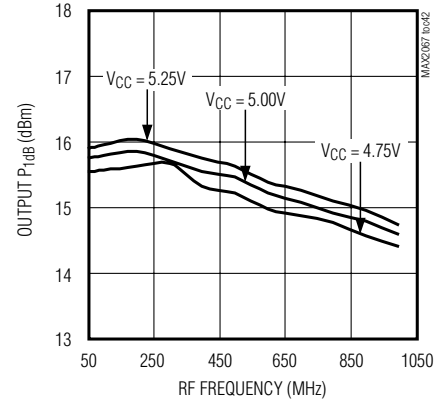
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



OUTPUT P1dB vs. RF FREQUENCY (LOW-CURRENT MODE)



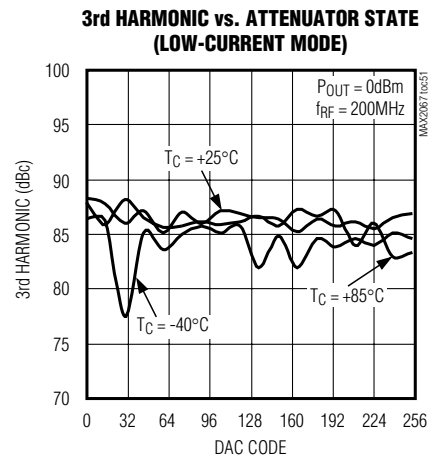
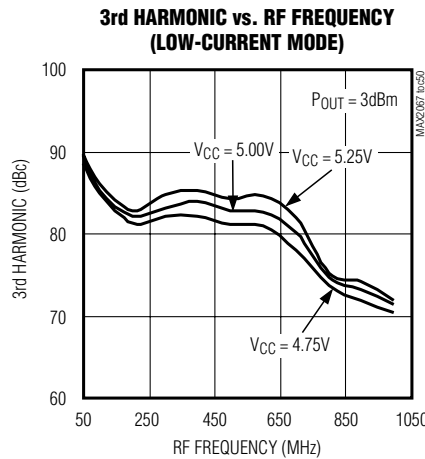
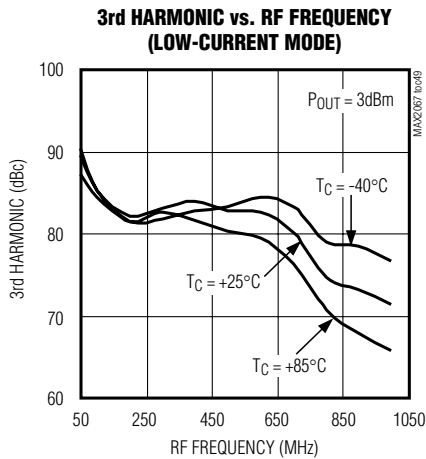
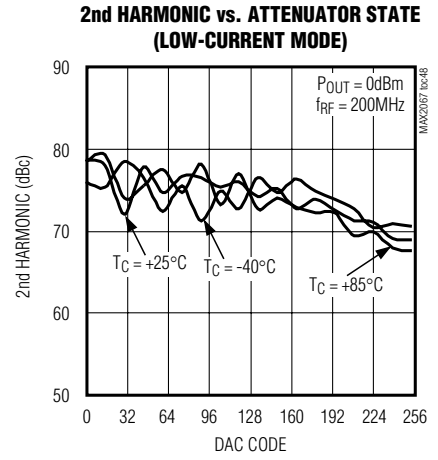
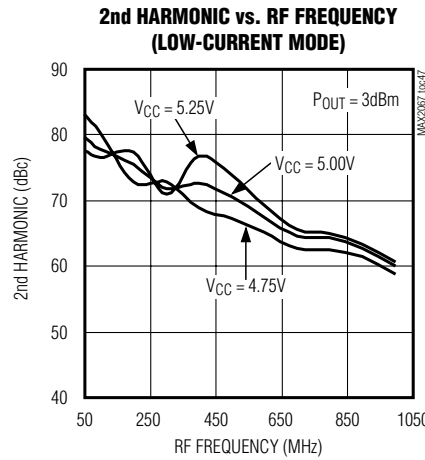
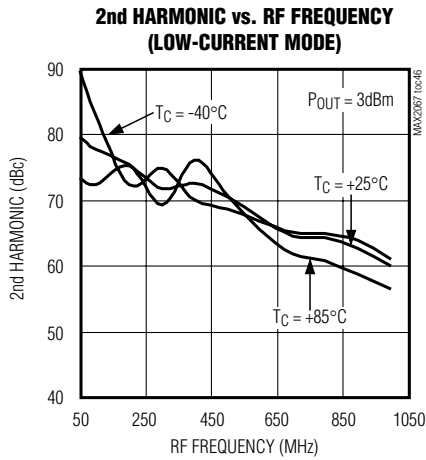
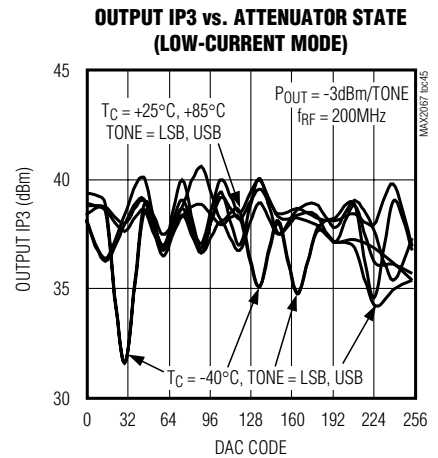
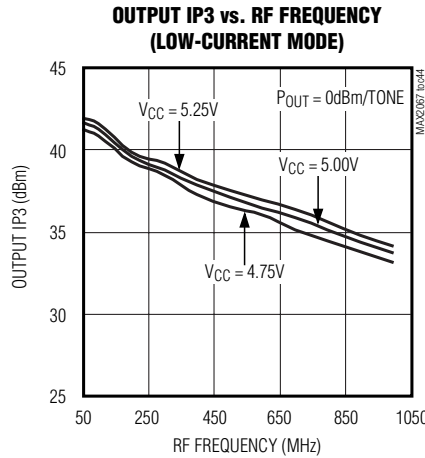
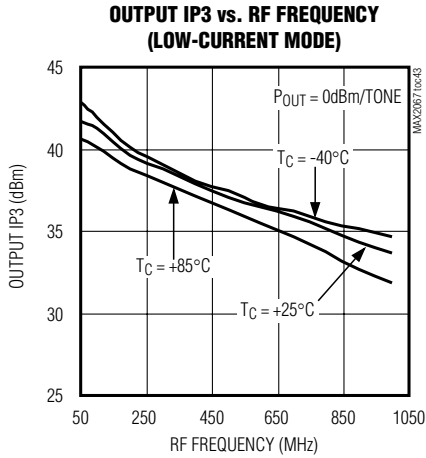
OUTPUT P1dB vs. RF FREQUENCY (LOW-CURRENT MODE)



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +5.0V$, LC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)

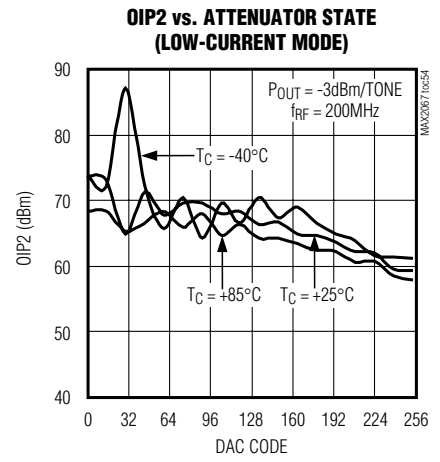
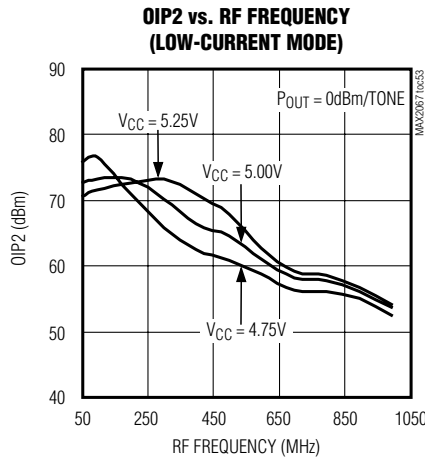
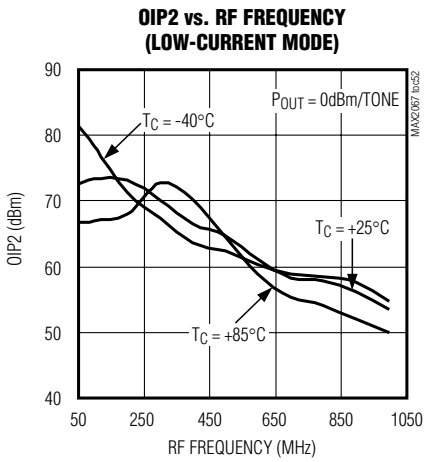


50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +5.0V$, LC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)

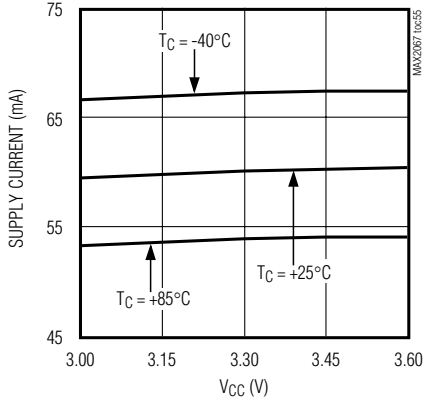


50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

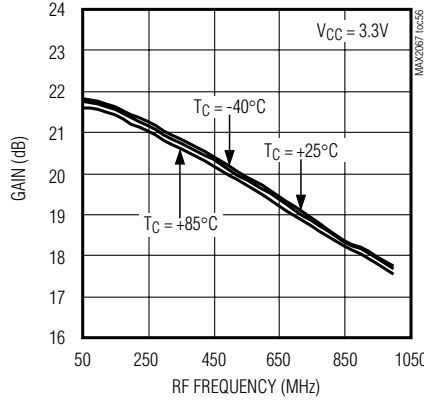
Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +3.3V$, HC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)

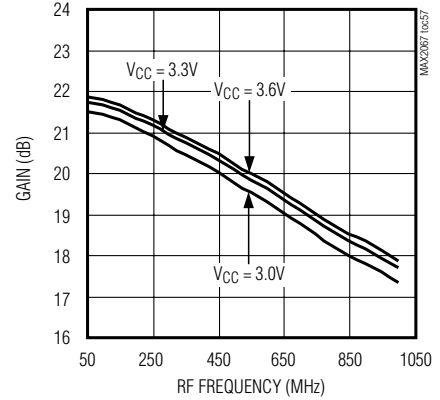
SUPPLY CURRENT vs. SUPPLY VOLTAGE



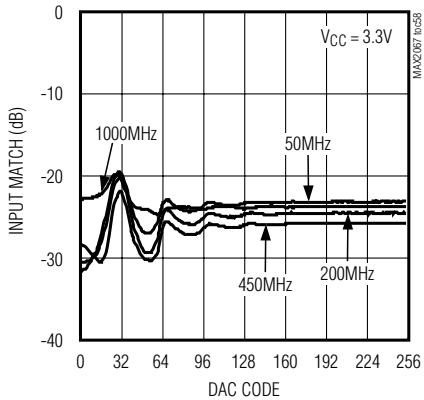
GAIN vs. RF FREQUENCY



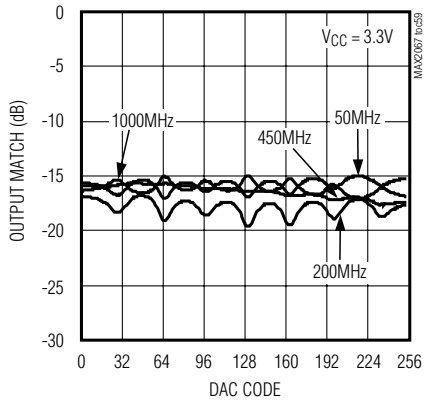
GAIN vs. RF FREQUENCY



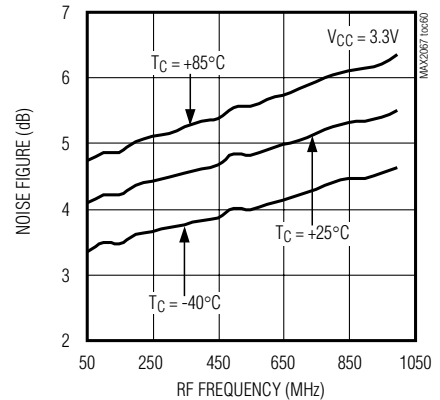
INPUT MATCH vs. ATTENUATOR SETTING



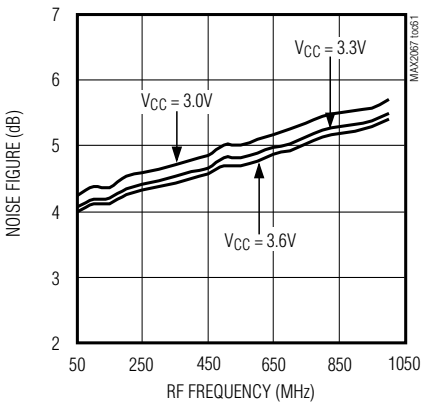
OUTPUT MATCH vs. ATTENUATOR SETTING



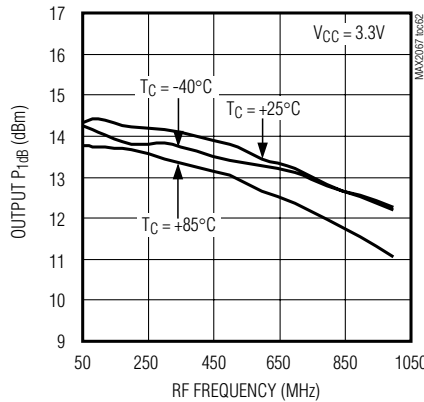
NOISE FIGURE vs. RF FREQUENCY



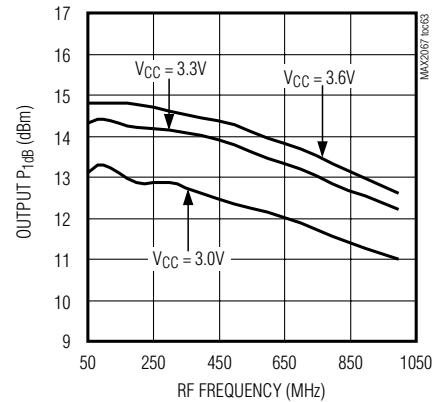
NOISE FIGURE vs. RF FREQUENCY



OUTPUT P1dB vs. RF FREQUENCY



OUTPUT P1dB vs. RF FREQUENCY

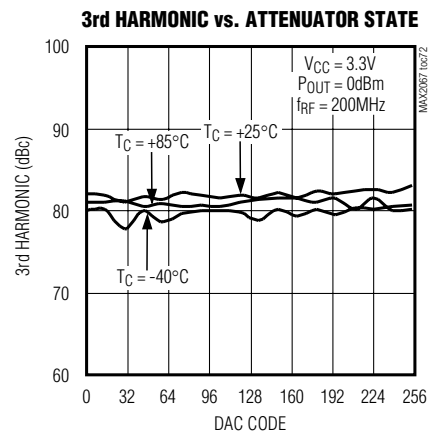
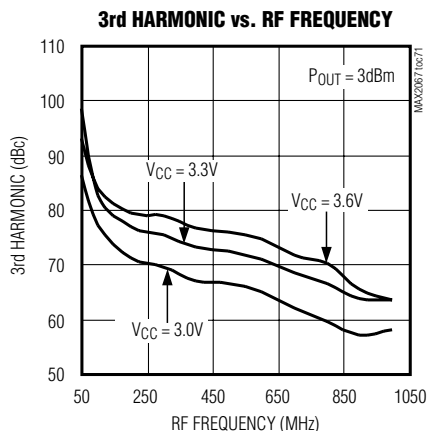
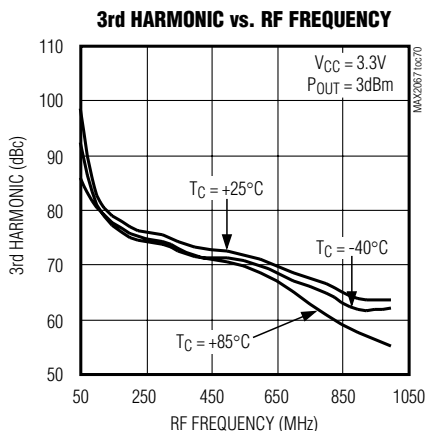
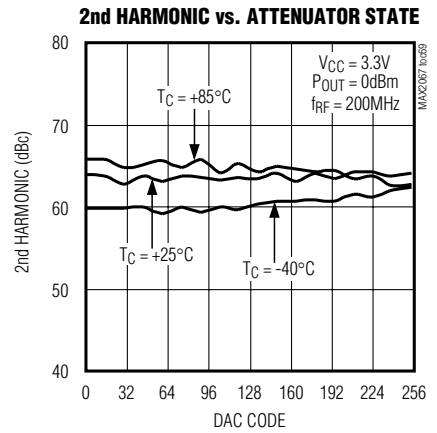
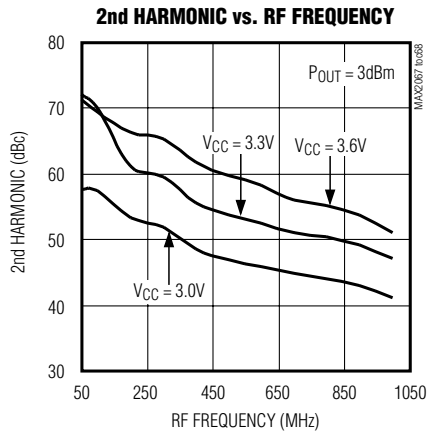
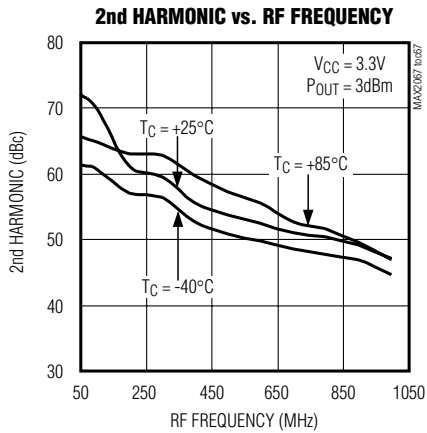
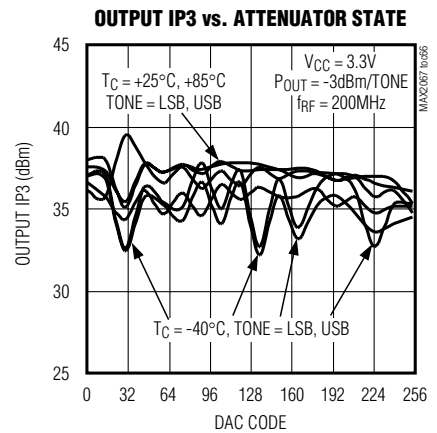
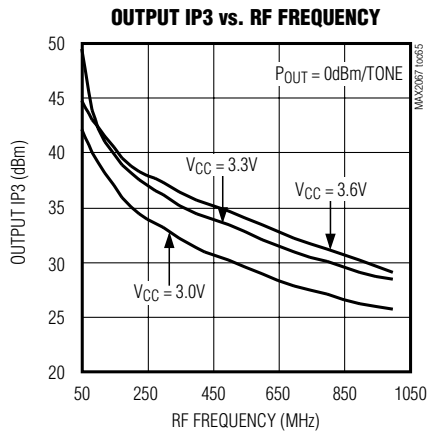
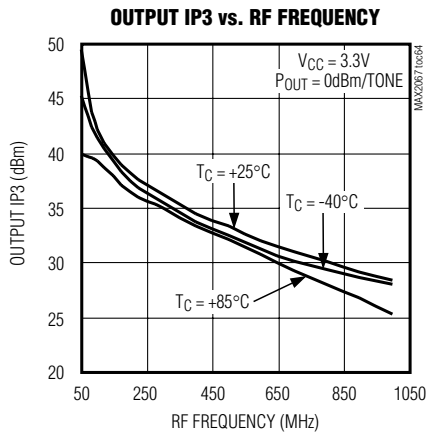


50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

Typical Operating Characteristics (continued)

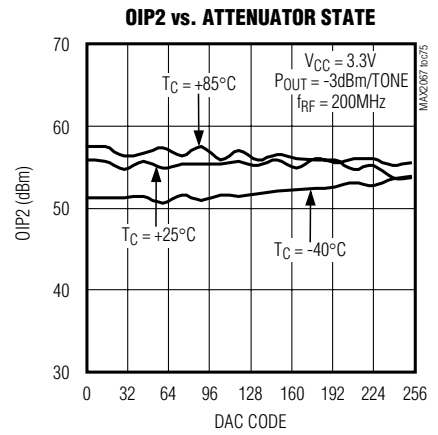
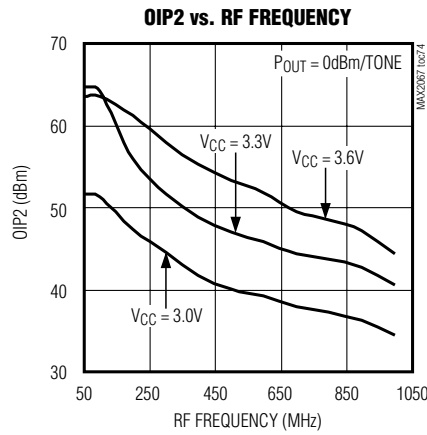
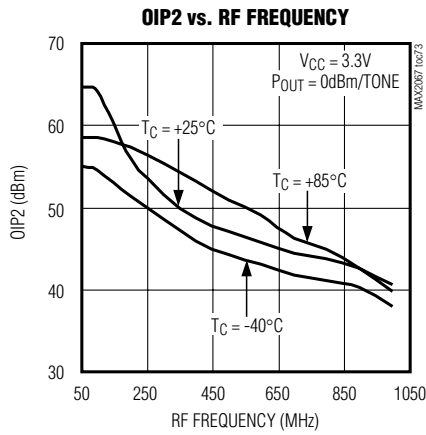
($V_{CC} = V_{DD} = +3.3V$, HC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Typical Operating Characteristics (continued)

($V_{CC} = V_{DD} = +3.3V$, HC mode, attenuator set for maximum gain, $P_{IN} = -20dBm$, $f_{RF} = 200MHz$, and $T_C = +25^\circ C$, internal DAC reference used, unless otherwise noted.)



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Pin Description

MAX2067

| PIN | NAME | DESCRIPTION |
|--|-----------------|---|
| 1, 16, 19, 22, 24–28, 30, 31, 33–36 | GND | Ground |
| 2 | VREF_SELECT | DAC Reference Voltage Selection Logic Input. Logic 1 = internal DAC reference voltage, Logic 0 = external DAC reference voltage. Logic input disabled (don't care) when VDAC_EN = Logic 0. |
| 3 | VDAC_EN | DAC Enable/Disable Logic Input. Logic 0 = disable DAC circuit, Logic 1 = enable DAC circuit. |
| 4 | DATA | SPI Data Digital Input |
| 5 | CLK | SPI Clock Digital Input |
| 6 | \overline{CS} | SPI Chip-Select Digital Input |
| 7 | VDD_LOGIC | Digital Logic Supply Input. Connect to the digital logic power supply, V _{DD} , Bypass to GND with a 10nF capacitor as close as possible to the pin. |
| 8–15, 23, 29 | GND | Ground. See the <i>Pin-Compatibility Considerations</i> section. |
| 17 | AMP_OUT | Driver Amplifier Output (50Ω). See the <i>Typical Application Circuit</i> for details. |
| 18 | RSET | Driver Amplifier Bias-Setting Input. See the <i>External Bias</i> section. |
| 20 | AMP_IN | Driver Amplifier Input (50Ω). See the <i>Typical Application Circuit</i> for details. |
| 21 | VCC_AMP | Driver Amplifier Supply Voltage Input. Connect to the V _{CC} power supply. Bypass to GND with 1000pF and 10nF capacitors as close as possible to the pin, with the smaller value capacitor closer to the part. |
| 32 | ATTEN_OUT | Analog Attenuator Output. Internally matched to 50Ω. Requires an external DC-blocking capacitor. |
| 37 | ATTEN_IN | Analog Attenuator Input. Internally matched to 50Ω. Requires an external DC-blocking capacitor. |
| 38 | VCC_ANALOG | Analog Bias and Control Supply Voltage Input. Bypass to GND with a 10nF capacitor as close as possible to the pin. |
| 39 | ANALOG_VCTRL | Analog Attenuator Voltage-Control Input |
| 40 | VREF_IN | External DAC Voltage Reference Input |
| — | EP | Exposed Pad. Internally connected to GND. Connect EP to ground for proper RF performance and enhanced thermal dissipation. |

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Detailed Description

The MAX2067 high-linearity analog variable-gain amplifier is a general-purpose, high-performance amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range.

The MAX2067 integrates an analog attenuator to provide 31dB of total gain control, as well as a driver amplifier optimized to provide high gain, high IP3, low noise figure, and low power consumption. For applications that do not require high linearity, the bias current of the amplifier can be adjusted by an external resistor to further reduce power consumption.

The analog attenuator is controlled using an external voltage or through the SPI-compatible interface using an on-chip DAC. Because each stage has its own external RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), or OIP3 (amplifier last). The device's performance features include 22dB stand-alone amplifier gain (amplifier only), 4dB NF at maximum gain (includes attenuator insertion loss), and a high OIP3 level of +43dBm. Each of these features makes the MAX2067 an ideal VGA for numerous receiver and transmitter applications.

In addition, the MAX2067 operates from a single +5V supply, or a single +3.3V supply with slightly reduced performance, and has adjustable bias to trade current consumption for linearity performance.

Analog Attenuator

The MAX2067's analog attenuator has a dynamic range of 31dB and is controlled using an external voltage or through the 3-wire SPI using an on-chip 8-bit DAC. See the *Applications Information* section and Table 1 for attenuator programming details. The attenuator can be used for both static and dynamic power control.

Driver Amplifier

The MAX2067 includes a high-performance driver with a fixed gain of 22dB. The driver amplifier circuit is optimized for high linearity for the 50MHz to 1000MHz frequency range.

Applications Information

Attenuator Control

The analog attenuator is controlled by either an external control voltage applied at ANALOG_VCTRL (pin 39) or by the on-chip 8-bit DAC. Through the utilization of this control DAC, the user can easily adjust the analog attenuation in 0.12dB increments through a simple SPI command. The DAC enable/disable logic-input pin (VDAC_EN), and the DAC reference voltage selection logic-input pin (VREF_SELECT) determine how the attenuator is controlled. When the DAC is enabled, either the on-chip voltage reference or the external voltage reference can be selected. See Table 1 for the attenuator and DAC operation truth table.

Although this on-chip DAC eliminates the need for an external analog control voltage, the user still has the option of disabling the DAC and using an external analog control voltage for instances where additional attenuation resolution is needed, or in cases where the gain trim/automatic gain-control (AGC) loop is purely analog.

SPI Interface and Attenuator Settings

The MAX2067 employs a 3-wire SPI/MICROWIRE™-compatible serial interface to program the on-chip DAC. Eight bits of data are shifted in MSB first and framed by \overline{CS} . When \overline{CS} is low, the clock is active and data is shifted on the rising edge of the clock. When \overline{CS} transitions high, the data is latched and the attenuator setting changes (Figure 1). See Table 2 for details on the SPI data format.

Table 1. Control Logic

| VDAC_EN | VREF_SELECT | ANALOG ATTENUATOR | D/A CONVERTER |
|---------|-------------|--|---|
| 0 | X | Controlled by external control voltage | Disabled |
| 1 | 1 | Controlled by on-chip DAC | Enabled (DAC uses on-chip voltage reference) |
| 1 | 0 | Controlled by on-chip DAC | Enabled (DAC uses external voltage reference) |

X = Don't care.

MICROWIRE is a trademark of National Semiconductor Corp.

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2067

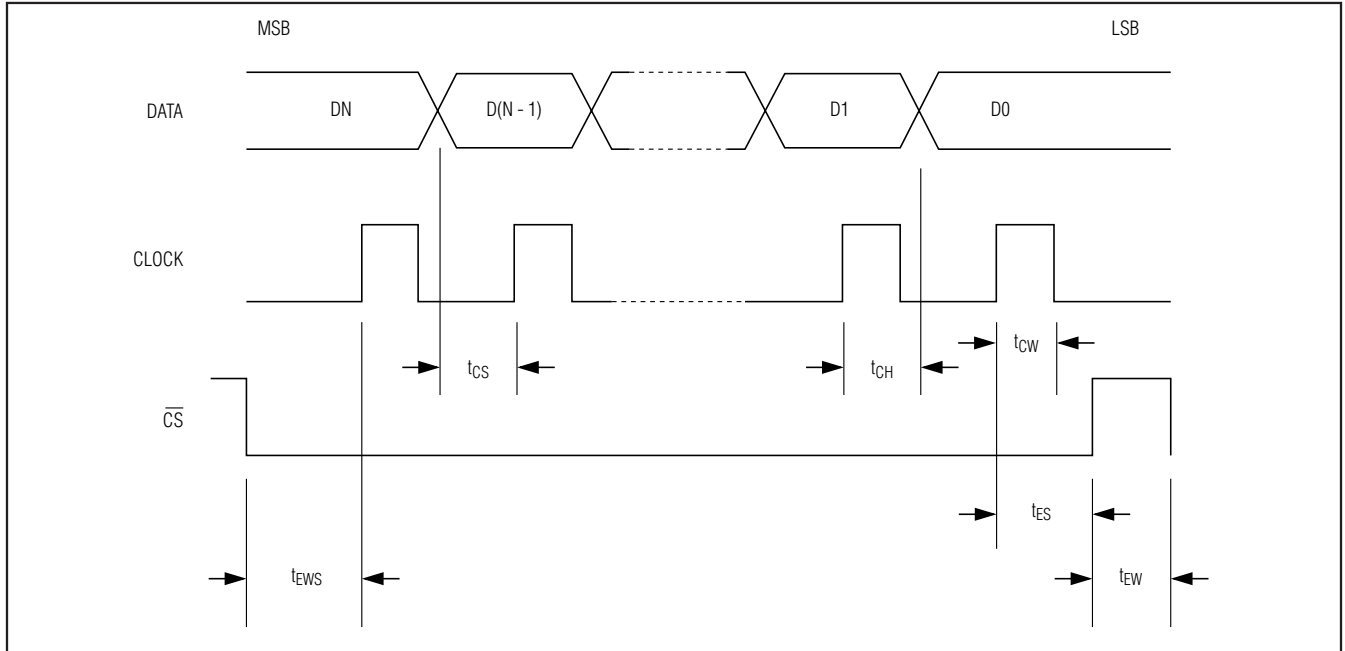


Figure 1. SPI Timing Diagram

Table 2. SPI Data Format

| FUNCTION | BIT | DESCRIPTION |
|-------------|----------|--|
| On-Chip DAC | D7 | Bit 7 (MSB) of on-chip DAC used to program the analog attenuator |
| | D6 | Bit 6 of DAC |
| | D5 | Bit 5 of DAC |
| | D4 | Bit 4 of DAC |
| | D3 | Bit 3 of DAC |
| | D2 | Bit 2 of DAC |
| | D1 | Bit 1 of DAC |
| | D0 (LSB) | Bit 0 (LSB) of the on-chip DAC |

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

External Bias

Bias currents for the driver amplifier are set and optimized through external resistors. Resistors R1 and R1A connected to RSET (pin 18) set the bias current for the amplifier. The external biasing resistor values can be increased for reduced current operation at the expense of performance. See Tables 4 and 5 for details.

Pin-Compatibility Considerations

The MAX2067 is a simplified version of the MAX2065 analog/digital VGA. The MAX2067 does not contain a digital attenuator and parallel inputs D0–D4. The associated input/output pins are internally connected to ground (Table 3). Ground the unused input/output pins to optimize isolation. (See the *Typical Application Circuit*.)

+5V and +3.3V Supply Voltage

The MAX2067 features an optional +3.3V supply voltage operation with slightly reduced linearity performance.

Layout Considerations

The pin configuration of the MAX2067 has been optimized to facilitate a very compact physical layout of the device and its associated discrete components.

The exposed paddle (EP) of the MAX2067's 40-pin thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the MAX2067 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **must** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Table 3. MAX2065/MAX2067 Pin Comparison

| PIN | MAX2065 | MAX2067 |
|-----|------------|---------|
| 8 | SER/PAR | GND |
| 9 | STATE_A | GND |
| 10 | STATE_B | GND |
| 11 | D4 | GND |
| 12 | D3 | GND |
| 13 | D2 | GND |
| 14 | D1 | GND |
| 15 | D0 | GND |
| 23 | ATTEN2_OUT | GND |
| 29 | ATTEN2_IN | GND |

Table 4. Typical Application Circuit Component Values (HC Mode)

| DESIGNATION | VALUE | SIZE | VENDOR | DESCRIPTION |
|---|--------------|--------------------------------|---------------------------------|------------------------|
| C1, C2, C7, C12 | 10nF | 0402 | Murata Mfg. Co., Ltd. | X7R |
| C3, C4, C6, C8, C9 | 1000pF | 0402 | Murata Mfg. Co., Ltd. | C0G ceramic capacitors |
| C10, C11 | 150pF | 0402 | Murata Mfg. Co., Ltd. | C0G ceramic capacitors |
| L1 | 470nH | 1008 | Coilcraft, Inc. | 1008CS-471XJLC |
| R1, R1A | 10 Ω | 0402 | Panasonic Corp. | 1% |
| R2 (+3.3V applications only) | 1k Ω | 0402 | Panasonic Corp. | 1% |
| R3 (+3.3V applications only) | 2k Ω | 0402 | Panasonic Corp. | 1% |
| R4 (+5V applications and using internal DAC only) | 47k Ω | 0402 | Panasonic Corp. | 1% |
| U1 | — | 40-pin thin QFN-EP (6mm x 6mm) | Maxim Integrated Products, Inc. | MAX2067ETL+ |

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

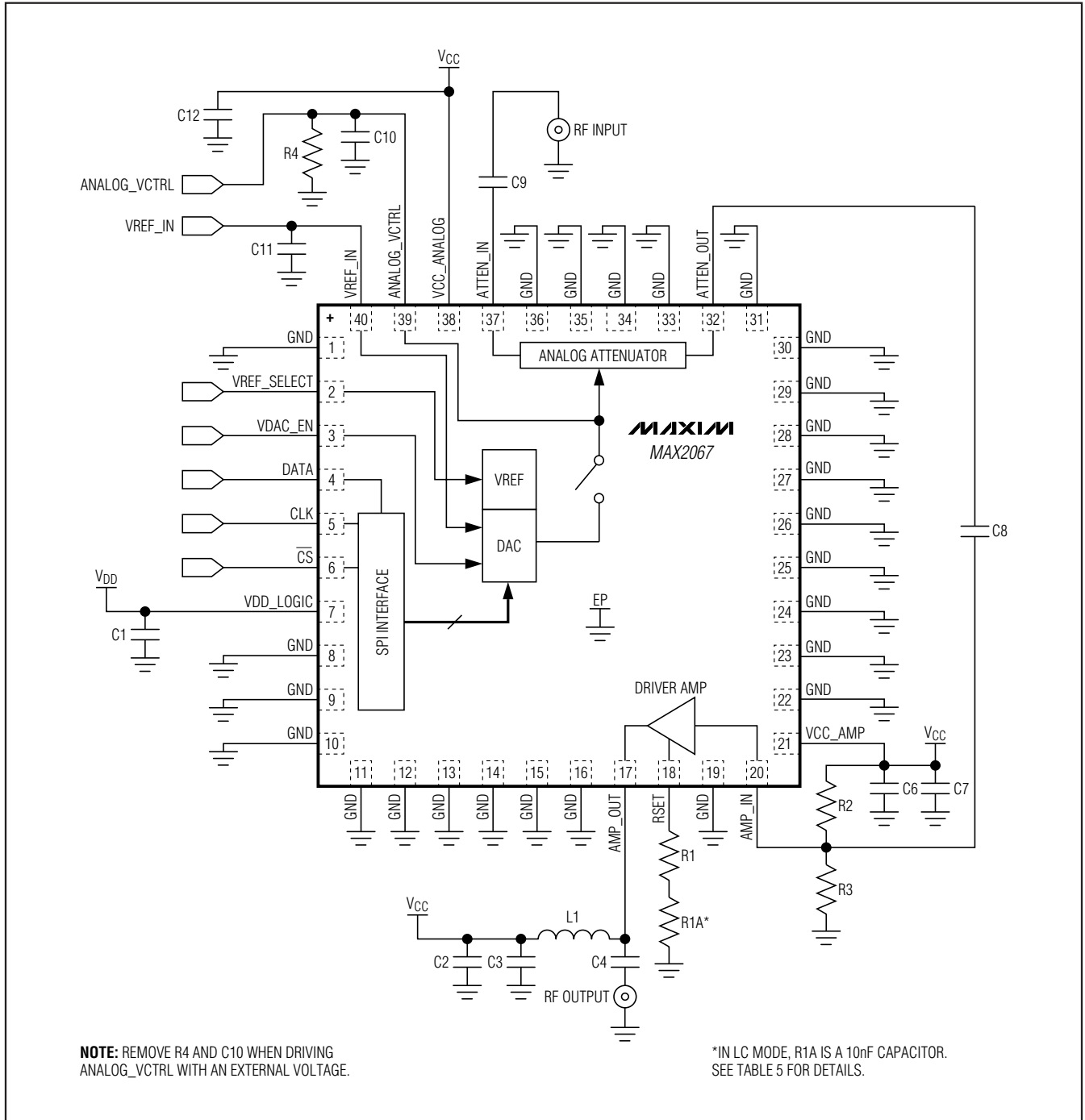
MAX2067

Table 5. Typical Application Circuit Component Values (LC Mode)

| DESIGNATION | VALUE | SIZE | VENDOR | DESCRIPTION |
|---|--------|-----------------------------------|------------------------------------|------------------------|
| C1, C2, C7, C12 | 10nF | 0402 | Murata Mfg. Co., Ltd. | X7R |
| C3, C4, C6, C8, C9 | 1000pF | 0402 | Murata Mfg. Co., Ltd. | COG ceramic capacitors |
| C10, C11 | 150pF | 0402 | Murata Mfg. Co., Ltd. | COG ceramic capacitors |
| L1 | 470nH | 1008 | Coilcraft, Inc. | 1008CS-471XJLC |
| R1 | 24Ω | 0402 | Vishay | 1% |
| R1A | 10nF | 0402 | Murata Mfg. Co., Ltd. | X7R |
| R2 (+3.3V applications only) | 1kΩ | 0402 | Panasonic Corp. | 1% |
| R3 (+3.3V applications only) | 2kΩ | 0402 | Panasonic Corp. | 1% |
| R4 (+5V applications and using internal DAC only) | 47kΩ | 0402 | Panasonic Corp. | 1% |
| U1 | — | 40-pin thin QFN-EP (6mm x 6mm) | Maxim Integrated Products, Inc. | MAX2067ETL+ |

50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

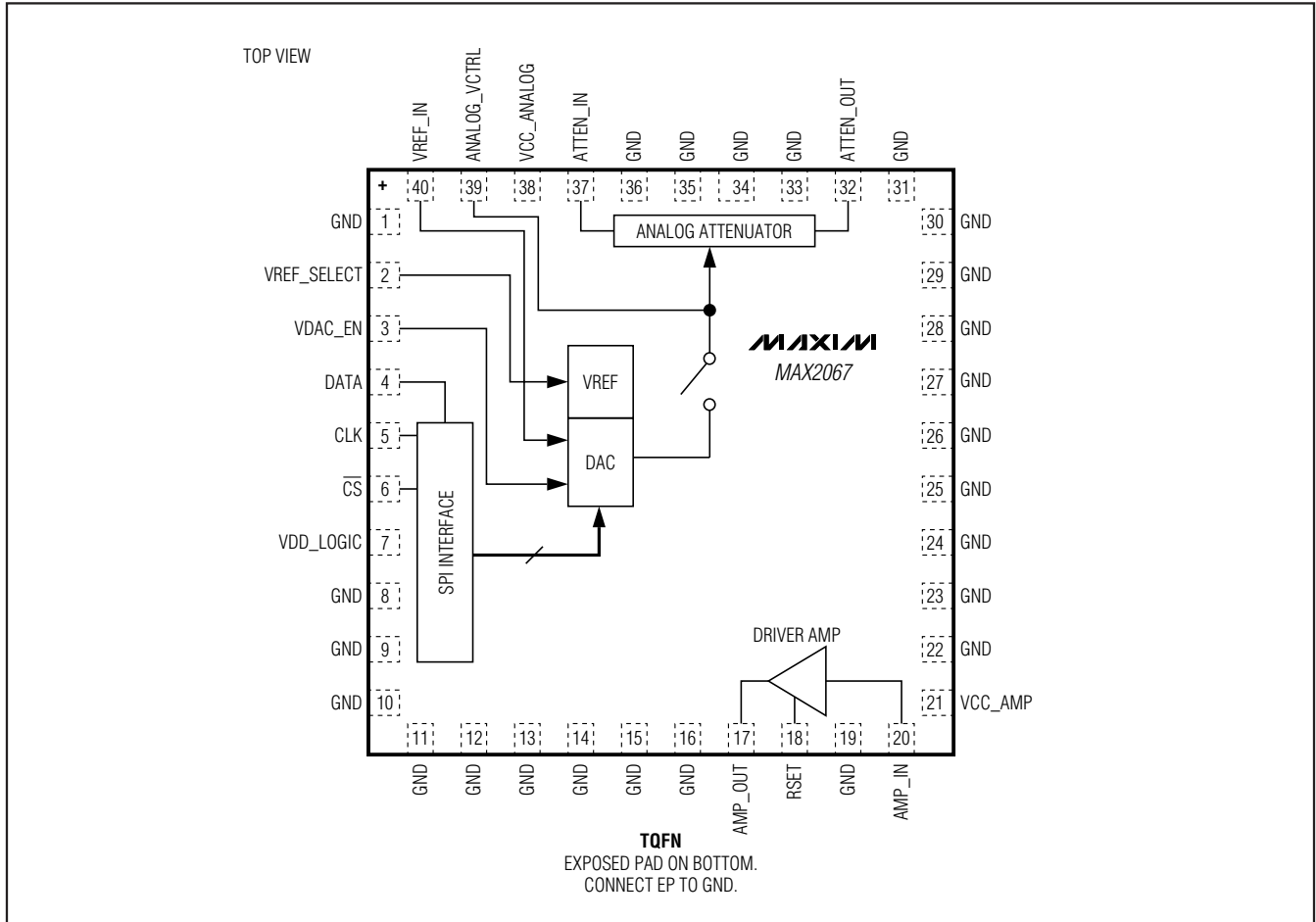
Typical Application Circuit



50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Pin Configuration/Functional Block Diagram

MAX2067



Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|----------------|--------------|-------------------------|
| 40 Thin QFN-EP | T4066-3 | 21-0141 |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 23

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View MAX2067ETL+T on WIN SOURCE](#)

 [Maxim Integrated](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management