

# 2.5 GHz Low Power Amplifier Module

## High Efficiency Pre-Driver

The AFLP5G25641 is an integrated multi-chip module. It consists of three stages of amplification and support circuitry to work at 3.3 V or 5 V with very low power consumption. The amplifier includes a 1.8 V logic control pin for bias enable/disable TDD operation.

- Typical Performance:  $V_{CC1} = 3.3 \text{ Vdc}$ ,  $V_{CC2} = 5 \text{ Vdc}$

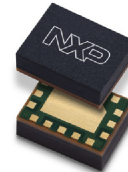
Frequency	$G_{ps}$ (dB)	$I_{CC}$ (mA)
2300 MHz	32.0	32
2400 MHz	32.4	32
2500 MHz	32.7	32
2600 MHz	32.8	32
2700 MHz	32.5	32

### Features

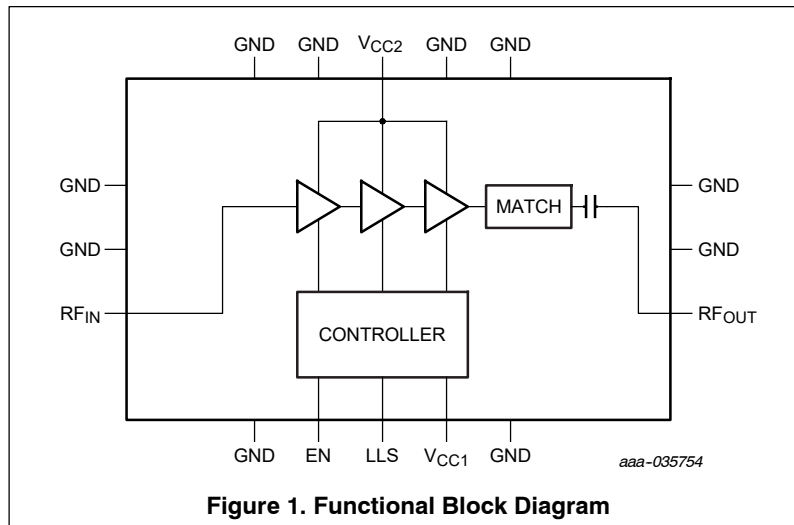
- Frequency: 2300–2700 MHz
- 3.3 V or 5 V supply for RF amplifier
- P1dB: 25 dBm @ 2500 MHz,  $V_{CC2} = 3.3 \text{ Vdc}$
- P1dB: 29 dBm @ 2500 MHz,  $V_{CC2} = 5 \text{ Vdc}$
- Power consumption:
  - 114 mW @  $V_{CC2} = 3.3 \text{ Vdc}$
  - 168 mW @  $V_{CC2} = 5 \text{ Vdc}$
- Fully matched (50 ohm input/output, DC blocked)
- Compact 4 mm × 3 mm LGA package

**AFLP5G25641**

**2300–2700 MHz, 32 dB, 29 dBm  
 AIRFAST PRE-DRIVER MODULE**



**4 mm × 3 mm Module**



**Figure 1. Functional Block Diagram**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC1}$	3.6	V
Supply Voltage	$V_{CC2}$	5.25	V
Supply Current	$I_{CC}$	330	mA
RF Input Power	$P_{in}$	25	dBm
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	125	°C

**Table 2. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

**Table 3. Moisture Sensitivity Level**

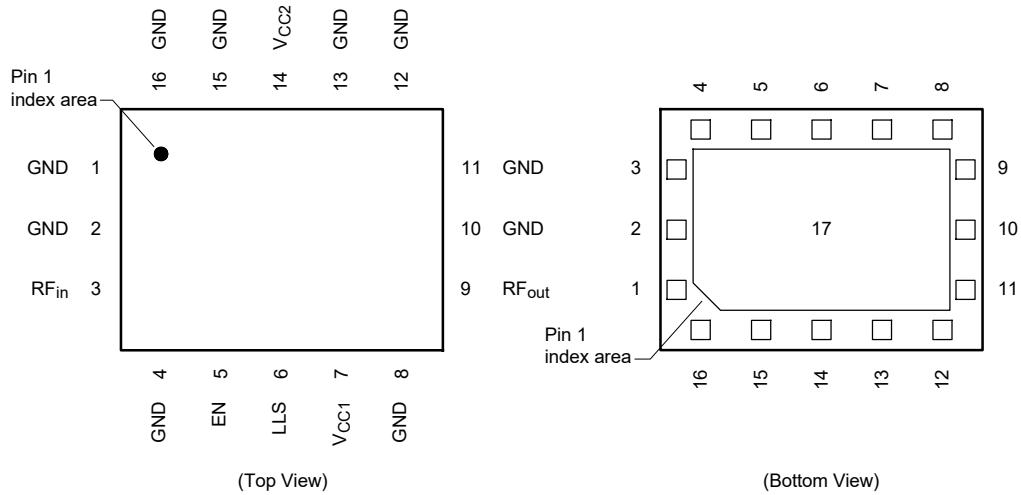
Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 4. Electrical Characteristics** ( $V_{CC1} = 3.3$  Vdc,  $V_{CC2} = 5$  Vdc, 2500 MHz,  $T_A = 25^\circ\text{C}$ , 50 ohm system, in NXP Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Small-Signal Gain (S21)	$G_p$	29.2	32.0	—	dB
Input Return Loss (S11)	IRL	—	15	—	dB
Output Return Loss (S22)	ORL	—	7	—	dB
Power Output @ 1dB Compression ( $V_{CC2} = 5$ Vdc)	P1dB	—	29	—	dBm
Quiescent Supply Current ( $V_{CC2}$ )	$I_{CQ2}$	—	32	—	mA
Supply Current ( $V_{CC1}$ )	$I_{CC1}$	—	2.2	—	mA

**Table 5. Ordering Information**

Device	Tape and Reel Information	Package
AFLP5G25641T6	T6 Suffix = 5,000 Units, 12 mm Tape Width, 13-inch Reel	4 mm × 3 mm Module

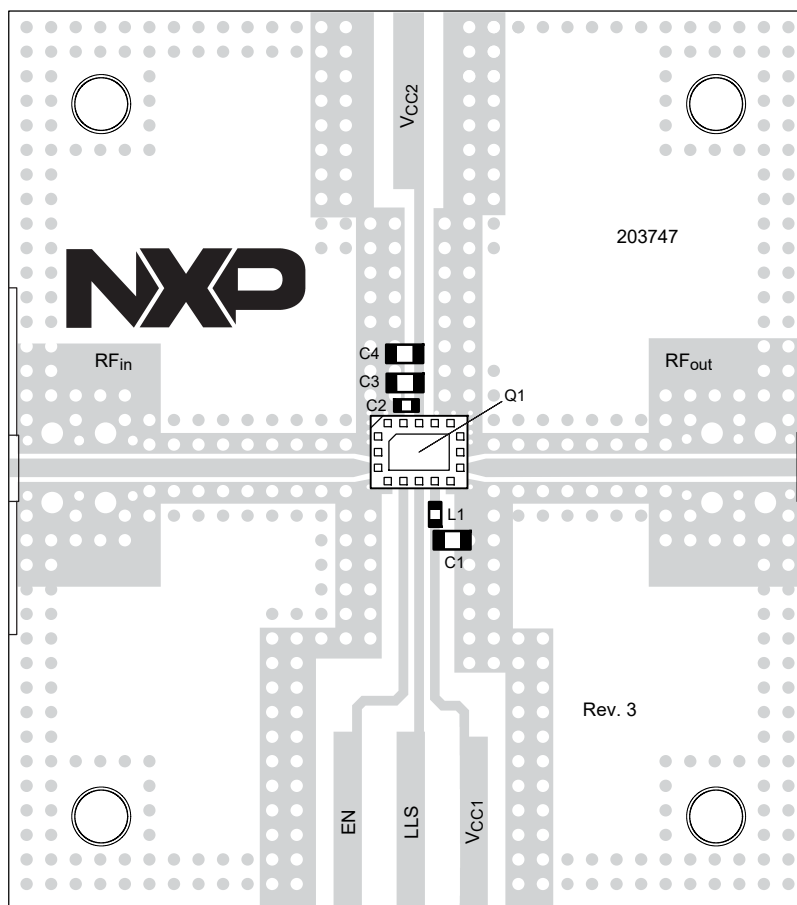


**Figure 2. Pin Connections**

**Table 6. Functional Pin Description**

Pin Number	Pin Function	Pin Description
1, 2, 4, 8, 10, 11, 12, 13, 15, 16, 17	GND	Ground
3	RF <sub>in</sub>	RF Input
5	EN	Bias Enable/Disable
6	LLS	Logic Level Select
7	V <sub>CC1</sub>	Power Supply for Controller
9	RF <sub>out</sub>	RF Output
14	V <sub>CC2</sub>	Power Supply for the RF Pre-driver

Note: LLS = 0 V, EN logic: VIL = -0.3 V to +0.4 V, VIH = +1.3 V to +2.5 V.  
 LLS = 1.8 V, EN logic: VIL and VIH per JEDEC Standard No. 8-7A, Normal Range, EN Logic: VIL = -0.3 V to +0.683 V,  
 VIH = +1.073 V to +2.25 V.



aaa-032914

Figure 3. AFLP5G25641 Application Circuit Component Layout

Table 7. AFLP5G25641 Application Circuit Designations and Values

Part	Description	Part Number	Manufacturer
C1, C3	1 $\mu$ F Chip Capacitor	GRM188R61A105KE15	Murata
C2	2.2 $\mu$ F Chip Capacitor	GRM155R60J225KE95	Murata
C4	2.2 $\mu$ F Chip Capacitor	GRM188R61A225KE34	Murata
L1	16 nH Chip Inductor	0402CS-16NXGLU	Coilcraft
Q1	Pre-driver Module	AFLP5G25641	NXP
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	203747	MTL

**NOTE: Correct Biasing Sequence**

**Turning the device ON**

1. Set  $V_{CC1}$  to 3.3 V,  $V_{CC2}$  to 5 V
2. Turn on EN to 1.8 V
3. Apply RF input power to desired level

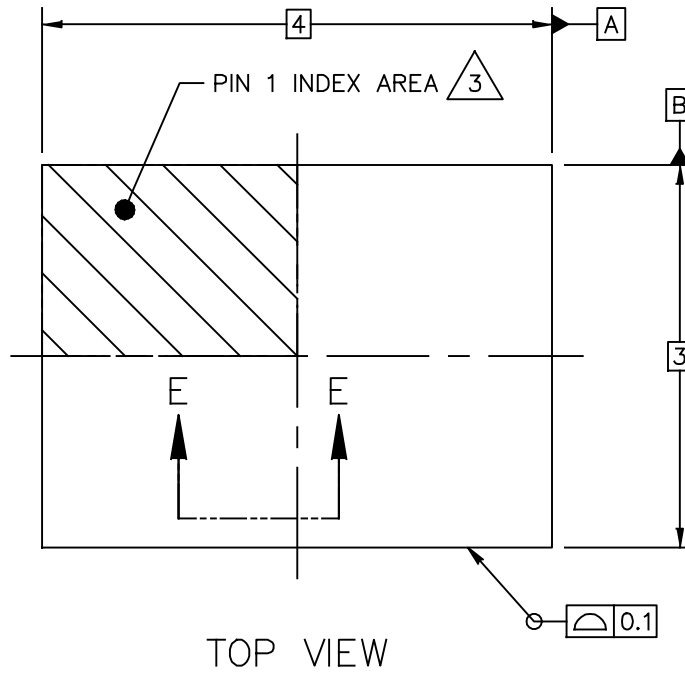
**Turning the device OFF**

1. Turn RF power off
2. Turn off EN to 0 V
3. Turn off  $V_{CC1}$  and  $V_{CC2}$

# PACKAGE DIMENSIONS

H-PLGA-17 I/O  
4 X 3 X 1.348 PKG, 0.65 PITCH

SOT1934-1



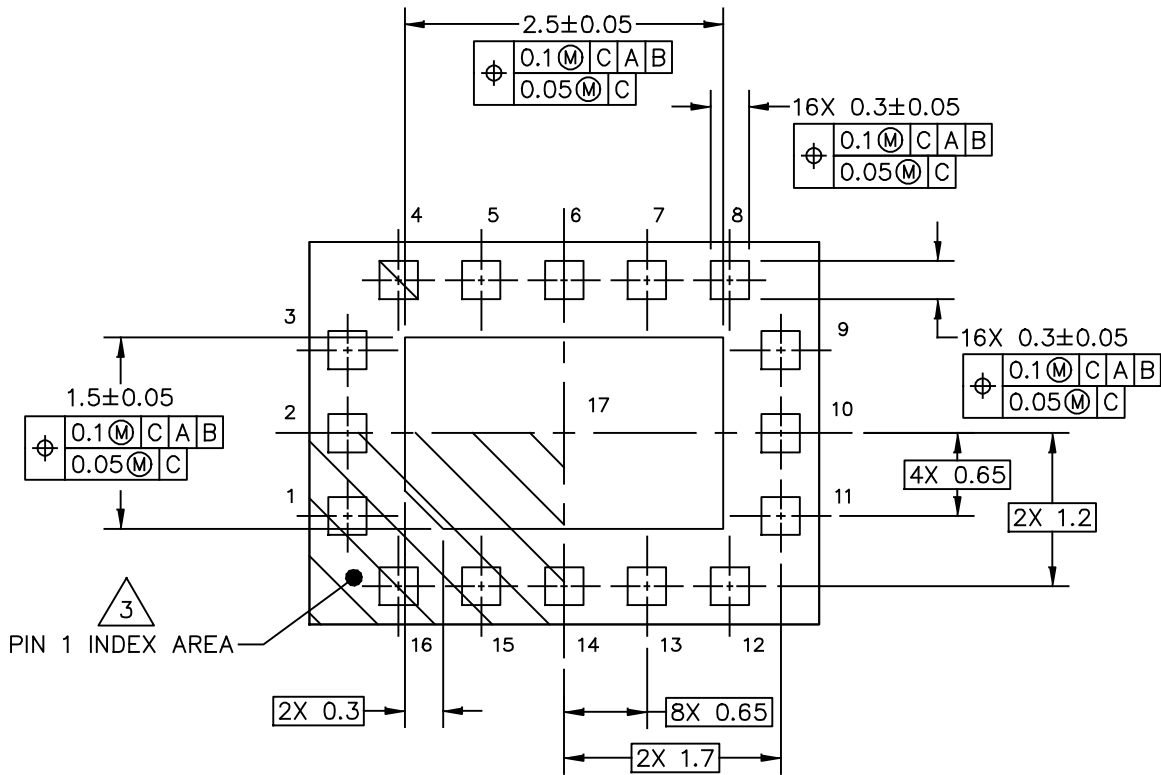
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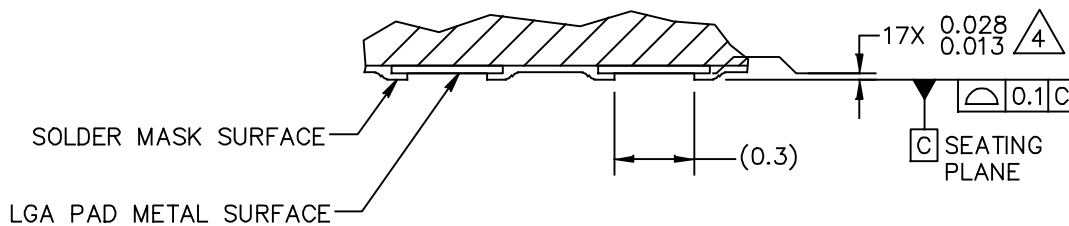
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AFLP5G25641



VIEW D-D  
 (BOTTOM VIEW)



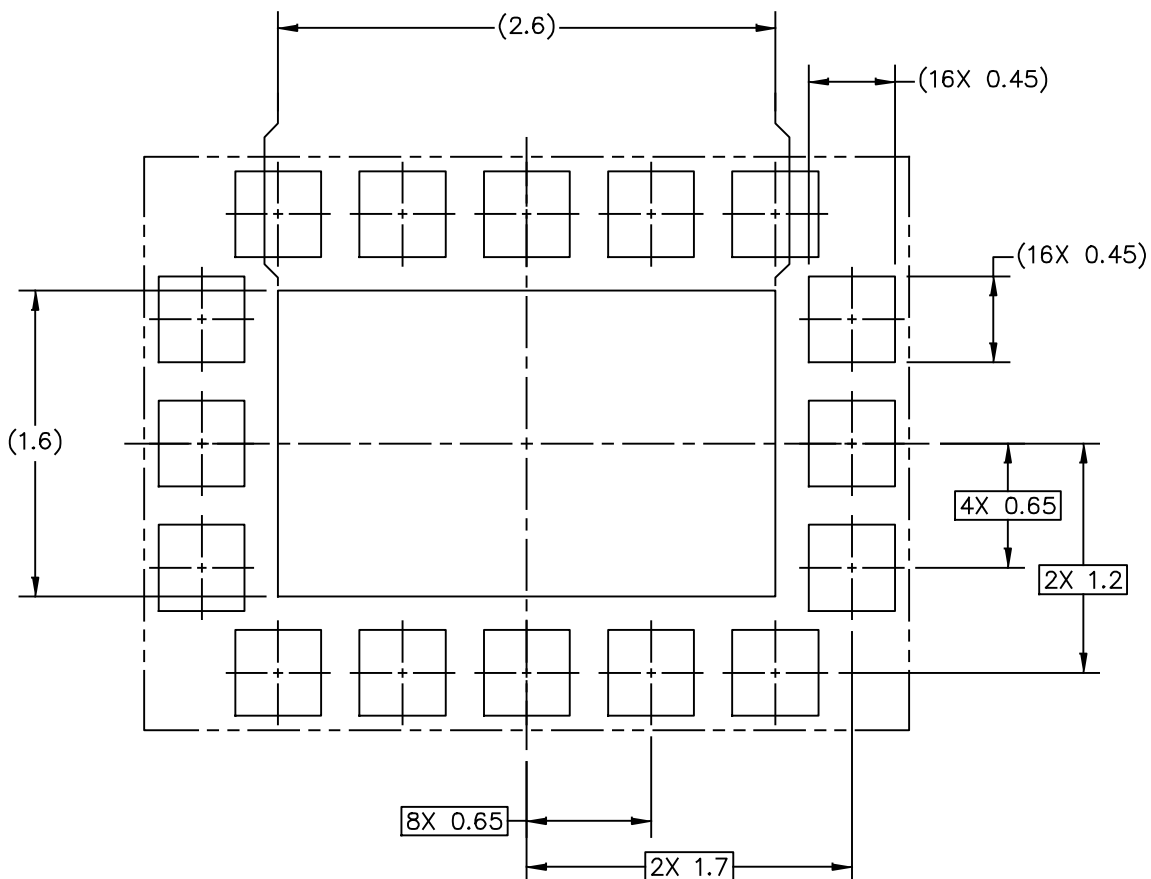
SECTION E-E

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### PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

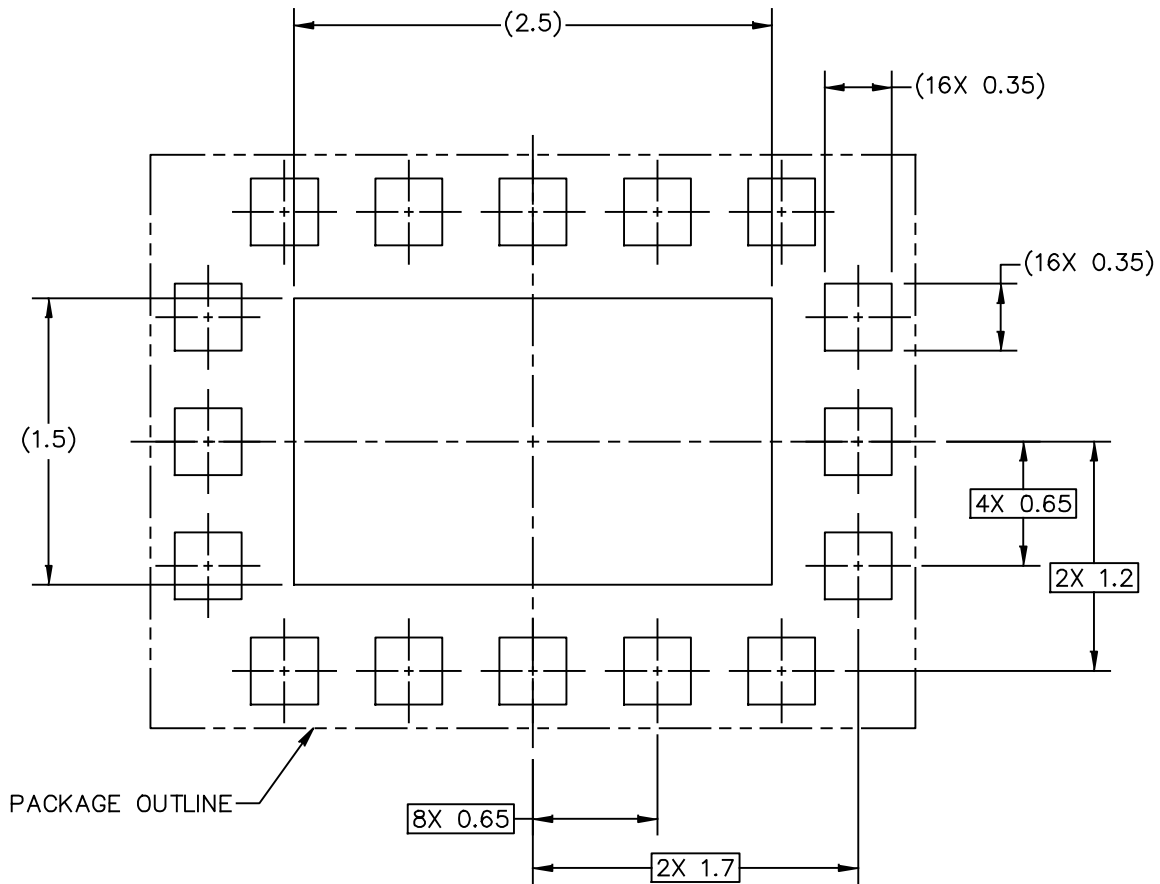
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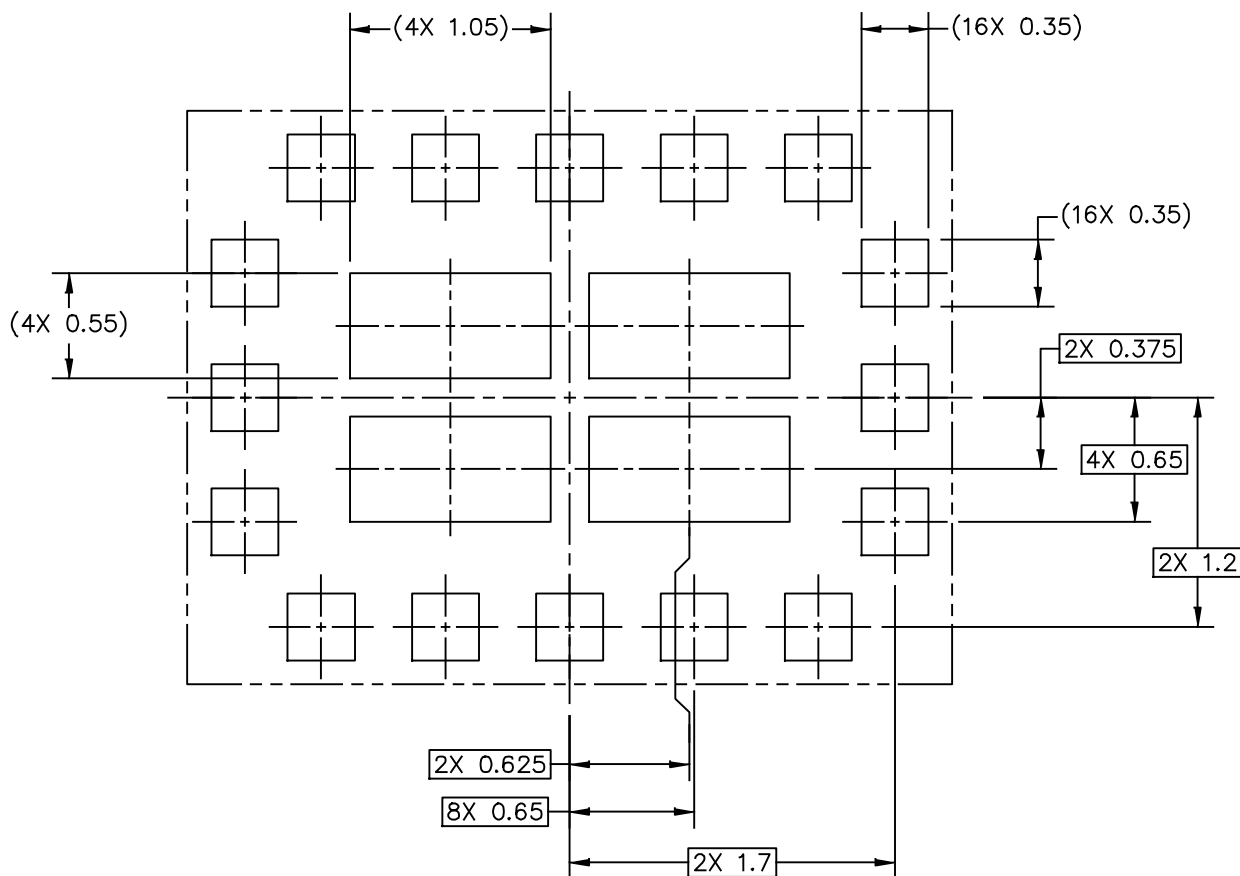
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RECOMMENDED STENCIL THICKNESS 0.125

### PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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AFLP5G25641

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. DIMENSION APPLIES TO ALL LEADS AND FLAG.

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## PRODUCT TOOLS

Refer to the following resource to aid your design process.

### Development Tools

- Printed Circuit Boards

## FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2019	• Initial release of data sheet
1	Jan. 2020	• Component layout PCB device file updated to reflect $V_{CC2}$ etching. Board revision number and MTL number updated, p. 4

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