QPA1111

8.5 – 10.5 GHz 30 Watt GaN Power Amplifier

Product Overview

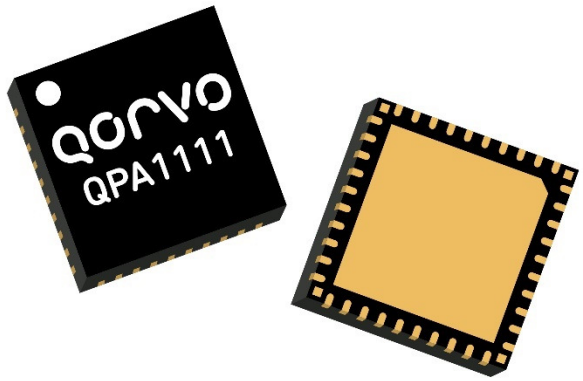
Qorvo's QPA1111 is a high power, packaged X-Band MMIC amplifier fabricated using Qorvo's production 0.15 um GaN-on-SiC process (QGaN15). The QPA1111 operates from 8.5 – 10.5 GHz, typically provides 30 W saturated output power with power-added efficiency of 45% and small signal gain of 38 dB.

To simplify system integration, the QPA1111 is fully matched to 50 ohms with DC grounded I/O ports for optimum ESD performance. Also, there are on-chip blocking capacitors following the DC grounds on the input and output ports.

The QPA1111 is ideal for supporting communications and radar applications in both commercial and military markets.

The QPA1111 is 100% DC and RF tested to ensure compliance to electrical specifications.

Lead-free and RoHS compliant

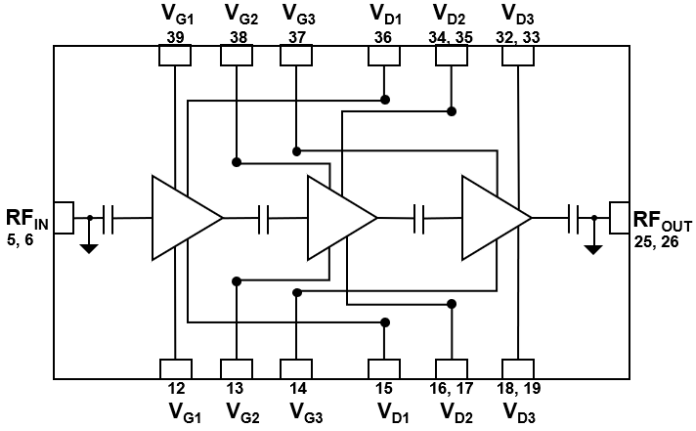


Key Features

- Frequency Range: 8.5 – 10.5 GHz
- P_{OUT} (P_{IN} = 18 dBm): 45 dBm
- PAE (P_{IN} = 18 dBm): 45 %
- Power Gain (P_{IN} = 18 dBm): 27 dBm
- Small Signal Gain: 38 dB
- Bias: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, V_G = -2.3 V typ. range
- Package Dimensions: 6.0 x 6.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Satellite Communications
- Radar
- Datalinks

Ordering Information

Part No.	Description
QPA1111	30 Watt GaN PA Package
QPA1111TR7	250 pieces on a 7” reel (standard)
QPA1111EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-4 V to 0 V
Drain Current (I_{D1}), 1-sided feed	1 A
Drain Current (I_{D2}), 1-sided feed	2 A
Drain Current (I_{D3}), 1-sided feed	8 A
Drain Current Total (I_D)	11 A
Gate Current (I_G)	See p. 20
Power Dissipation (P_{DISS}), CW, T_{BASE} = 85 °C	65 W
Input Power (P_{IN}), 50 Ω, Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%	T_{BASE} = -40 °C: 21 dBm T_{BASE} = +85 °C: 27 dBm
Input Power (P_{IN}), 3:1 VSWR, Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%	T_{BASE} = -40 °C: 18 dBm T_{BASE} = +85 °C: 25 dBm
Mounting Temperature (30 seconds)	260 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter		Min	Typ.	Max	Units
Pulsed (1)	Width		100	500	µs
	Duty Cycle		10	15	%
Drain Voltage (V_D) – Pulsed (1)			22	22	V
Drain Current Total I_D, Quiescent			620		mA
Drain Current Total, RF (I_{D_Drive})		See plot page 4, 5, 9, 12, 15			mA
Gate Voltage Typ. Range (V_G)		–1.6 to -3			V
Gate Current, RF (I_{G_Drive})		See plot page 4, 5			mA
Input Power, P_{IN}	T_{BASE} = -40 °C		15		dBm
	T_{BASE} = +25 °C		18		
	T_{BASE} = +85 °C		21		
Operating Temp. (T_{BASE}) (2)		–40		+85	ºC

1. CW operating requires thermal consideration
2. T_{BASE} is back side of QPA1111 (see p. 24 Offset Temperature based on Qorvo's EVB Cu filled vias for reference).

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

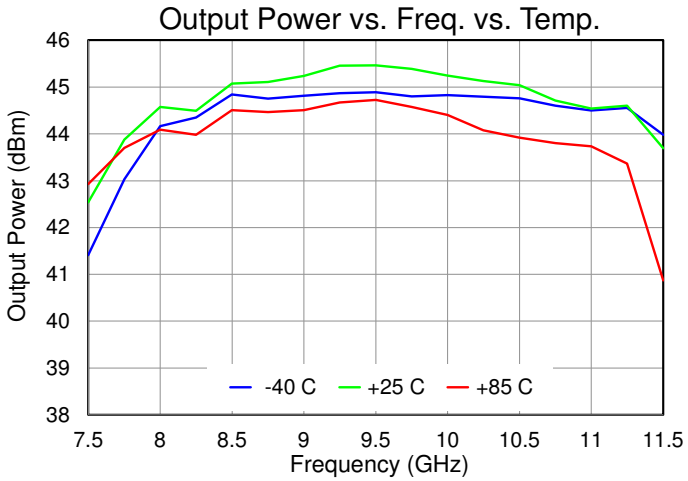
Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		8.5		10.5	GHz
Output Power, P_{OUT}	P_{IN} = 18 dBm		45		dBm
Power Added Efficiency, PAE	P_{IN} = 18 dBm		45		%
Power Gain	P_{IN} = 18 dBm		27		dBm
Small Signal Gain, S21	P_{IN} = -30 dBm		38		dB
Input Return Loss, IRL			15		
Output Return Loss, ORL			10		
P_{OUT} Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC; P_{IN} = 18 dBm		-0.05		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC		-0.10		dB/ºC

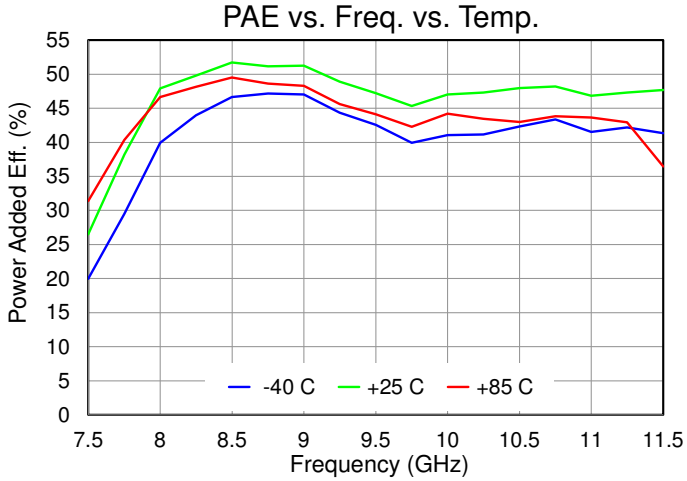
Notes:

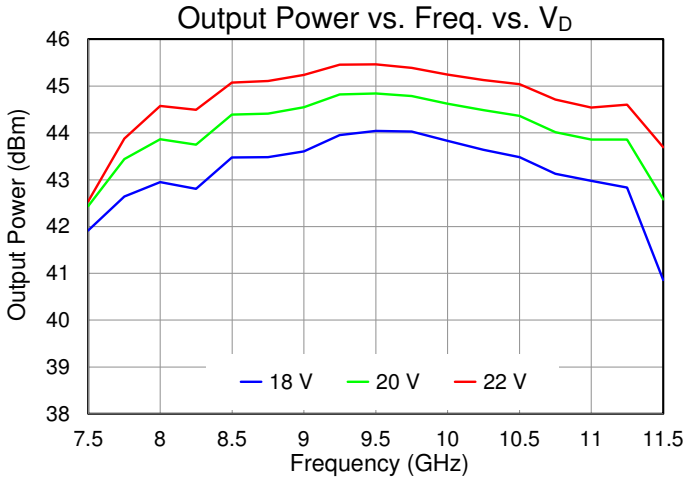
1. Test conditions unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, V_G = -2.3 V +/- 0.7V typical, T_{BASE} = +25ºC, Z_0 = 50 Ω (reference planes are at QPA1111).
2. T_{BASE} is back side of QPA1111 (see page 24 Offset Temperature based on Qorvo's EVB design for reference).

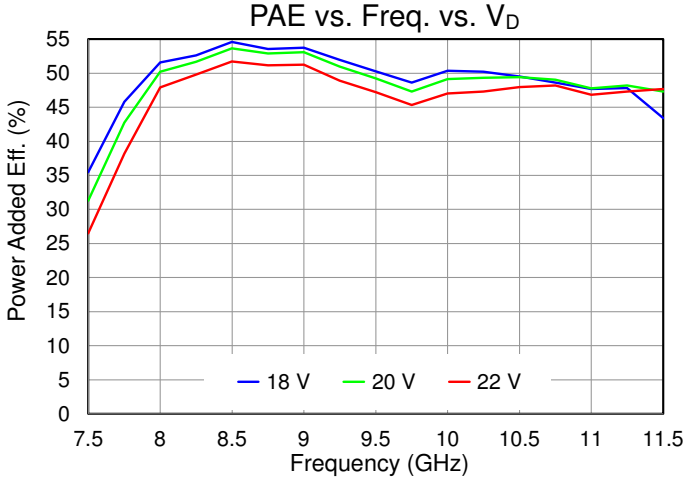
Performance Plots – Large Signal (Pulsed)

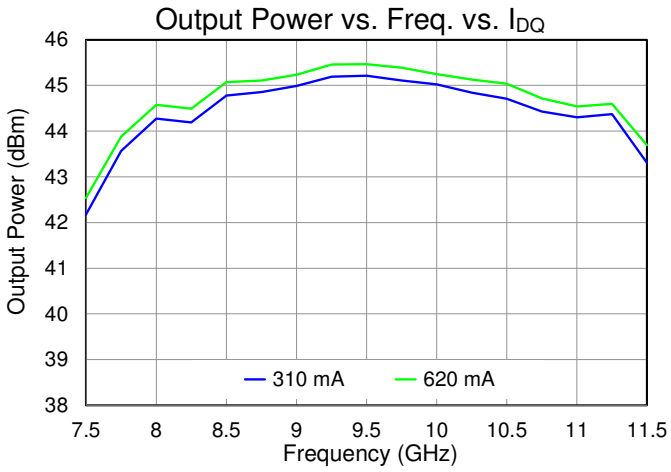
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = 17 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).

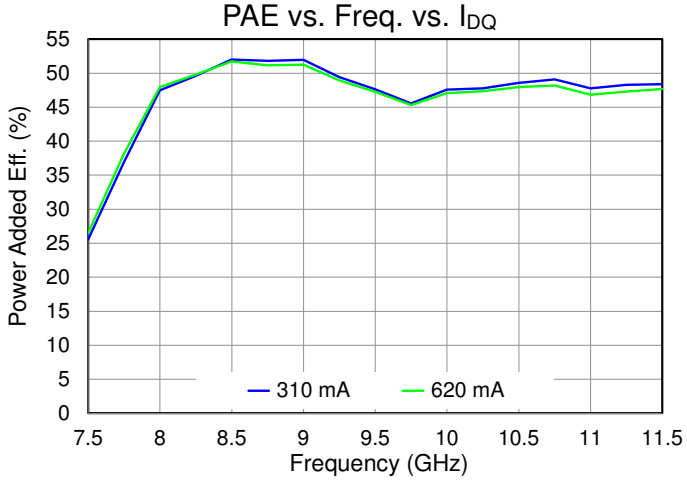












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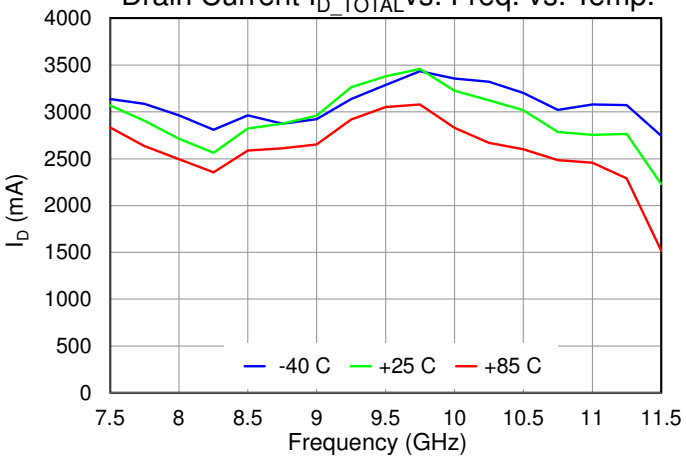
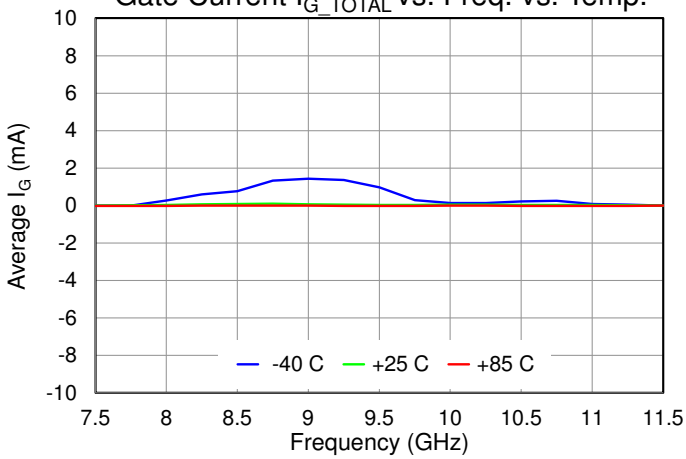
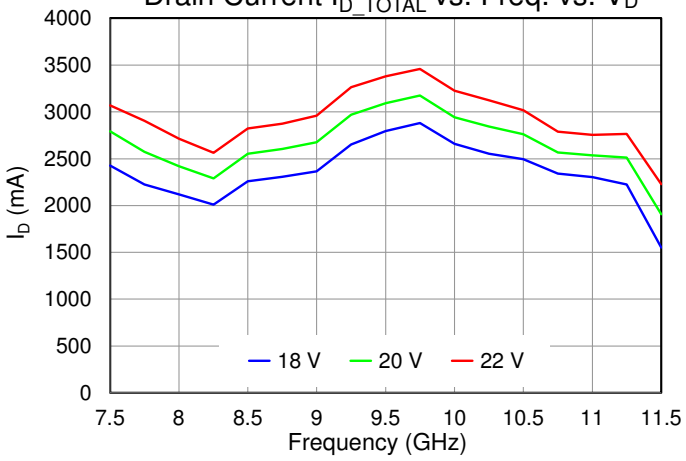
Drain Current I_{D_TOTAL} vs. Freq. vs. Temp.



Gate Current I_{G_TOTAL} vs. Freq. vs. Temp.



Drain Current I_{D_TOTAL} vs. Freq. vs. V_D



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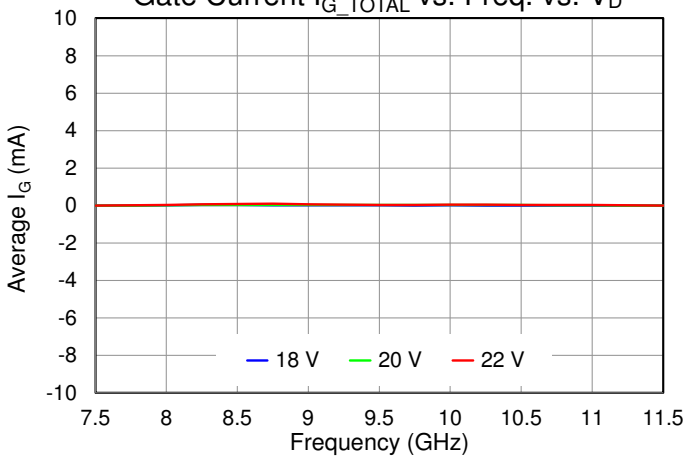
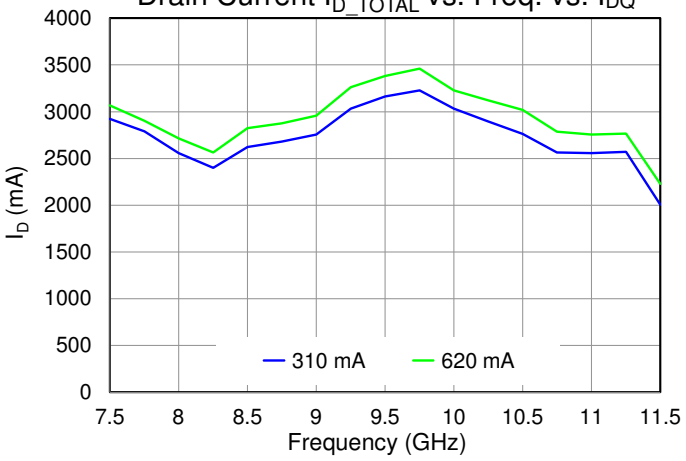


Drain Current I_{D_TOTAL} vs. Freq. vs. I_{DQ}



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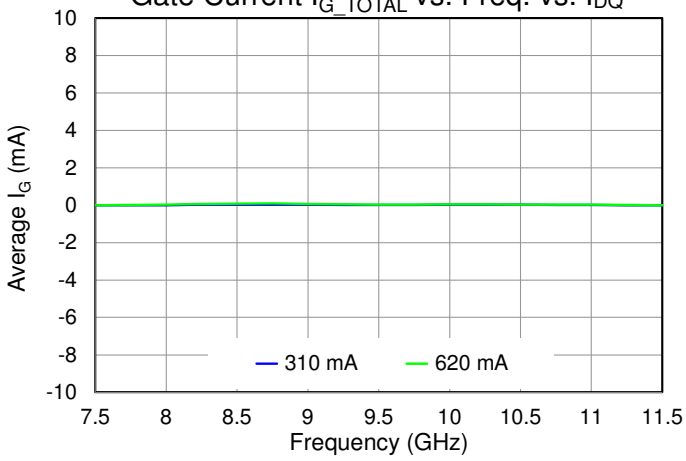

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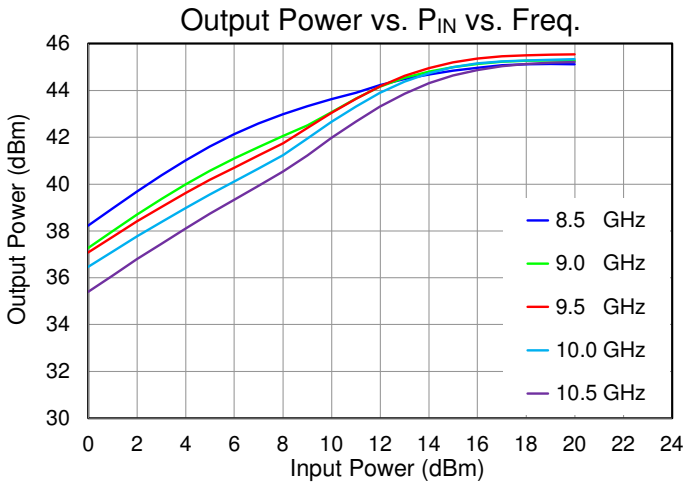

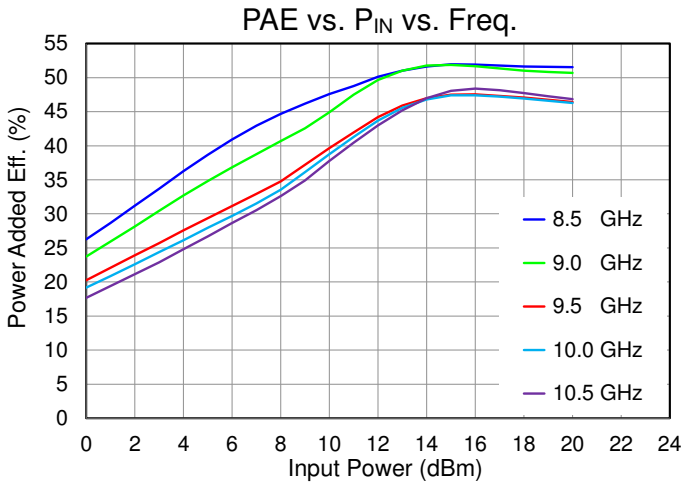

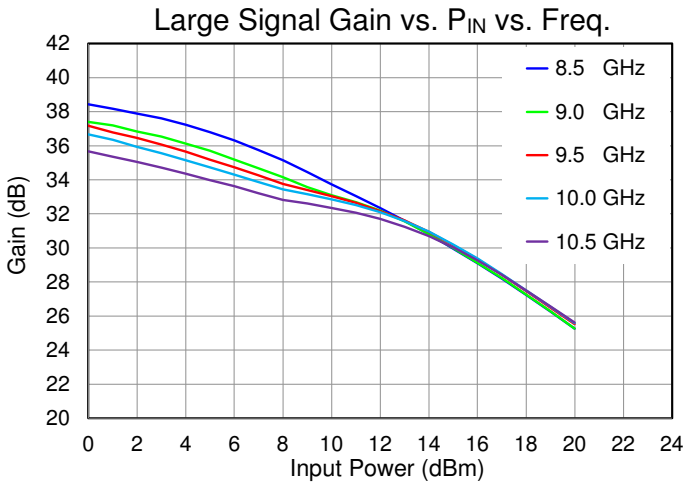

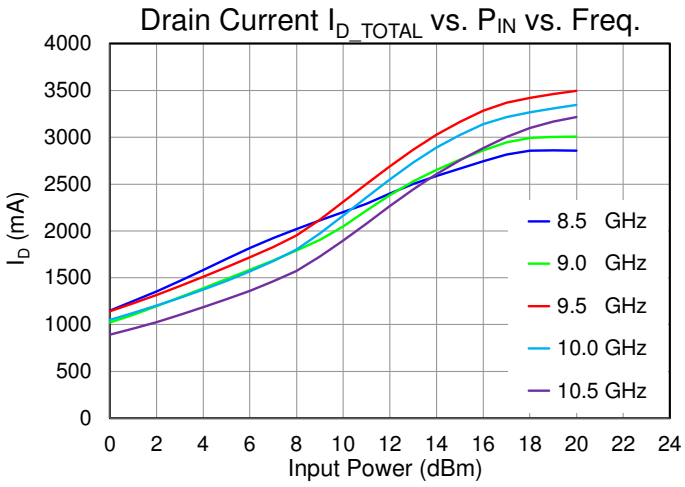

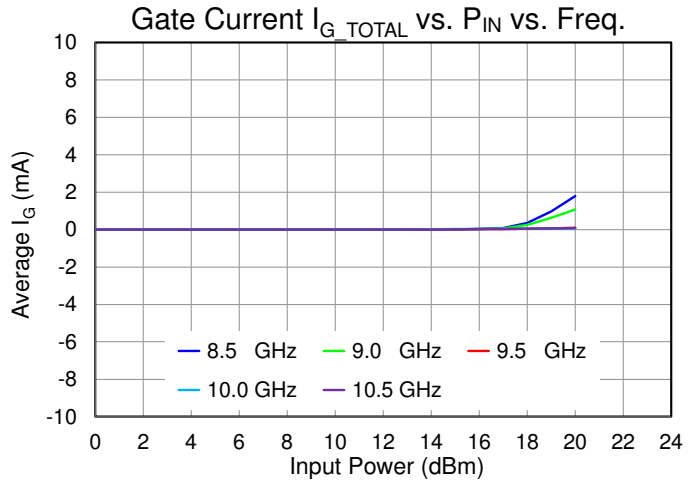

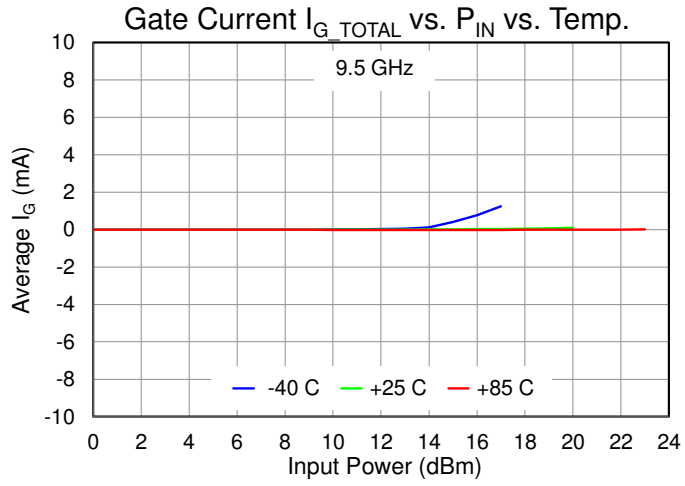

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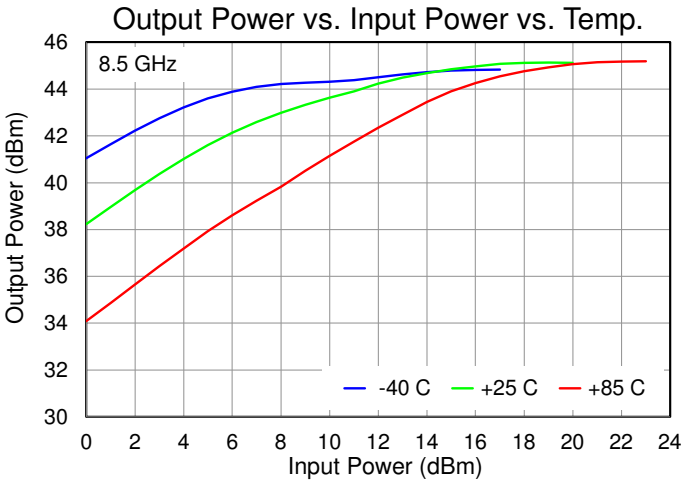

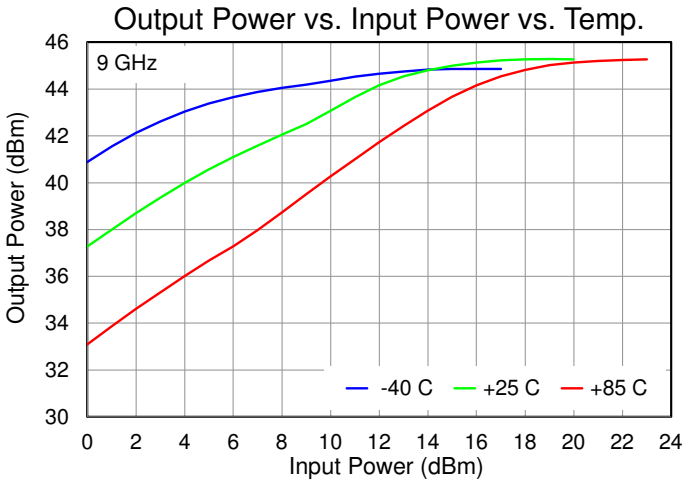

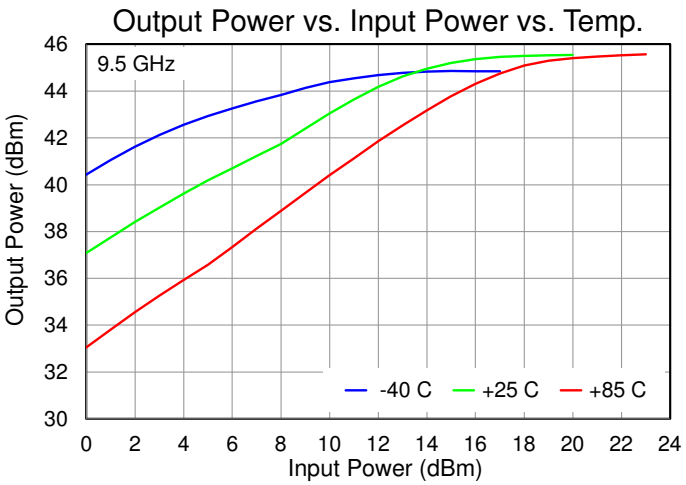

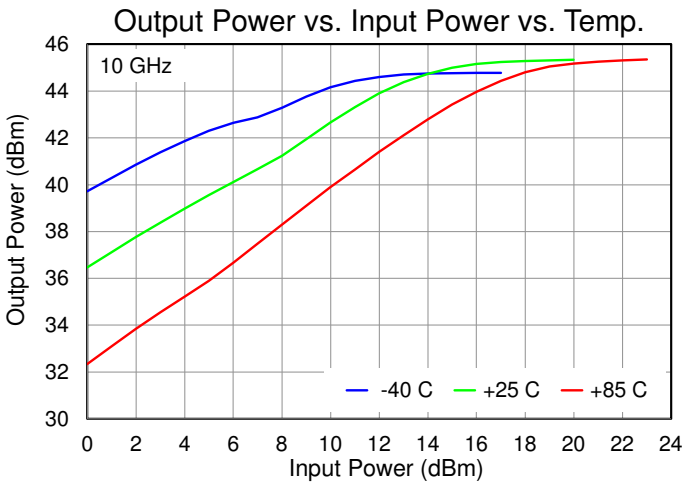

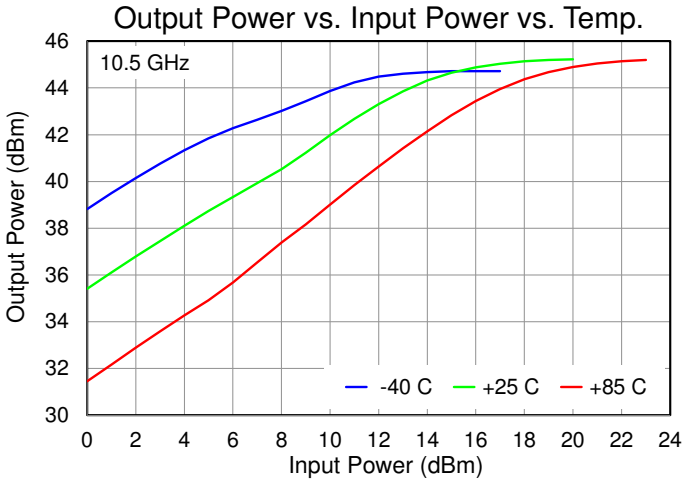

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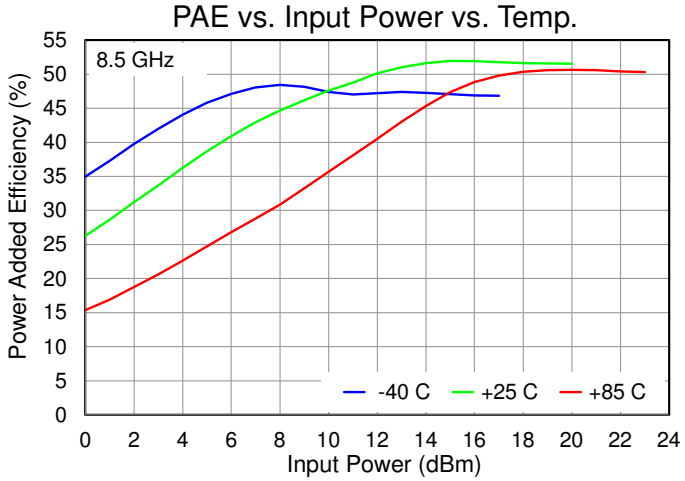

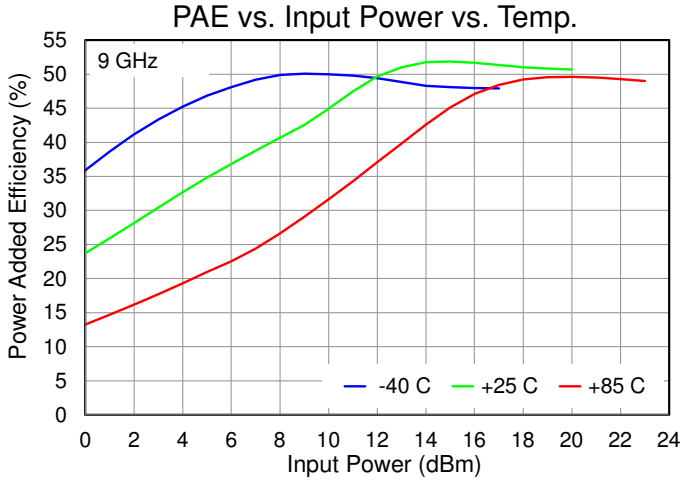

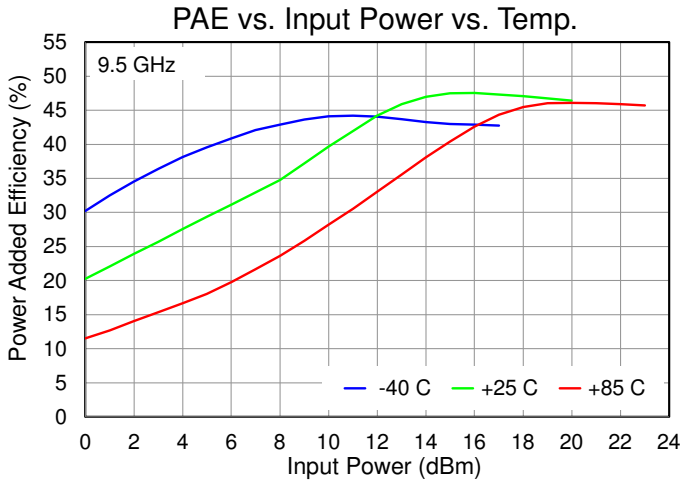

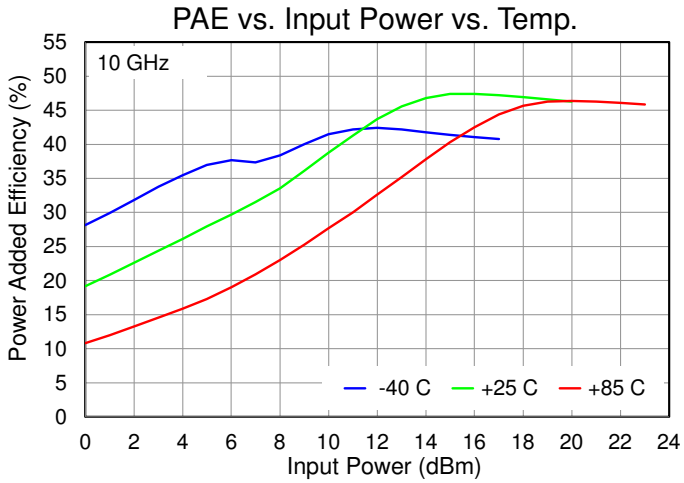

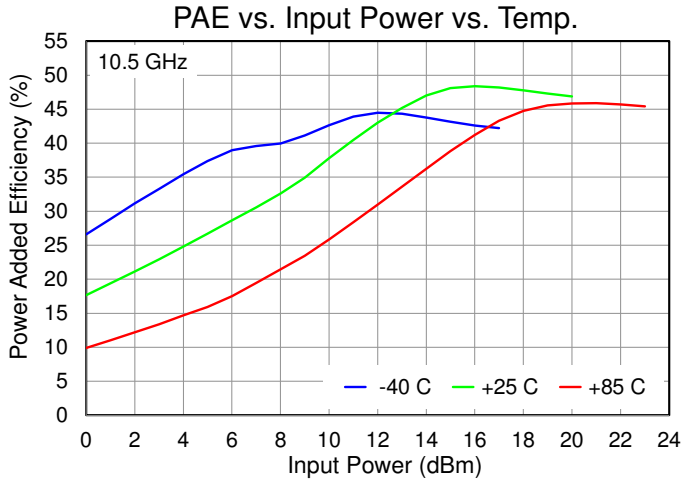

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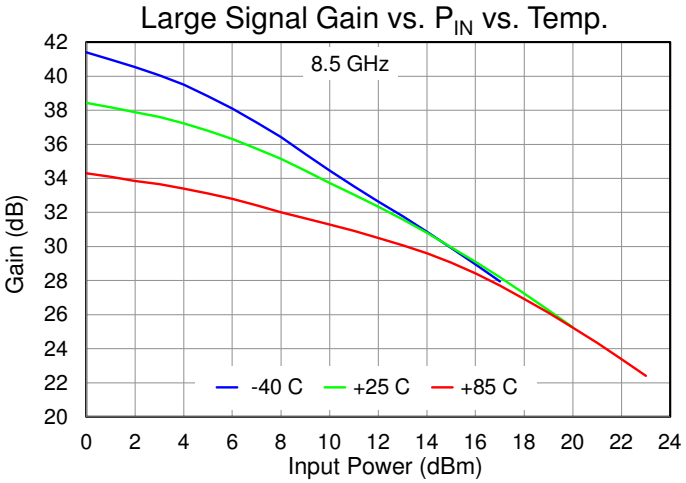

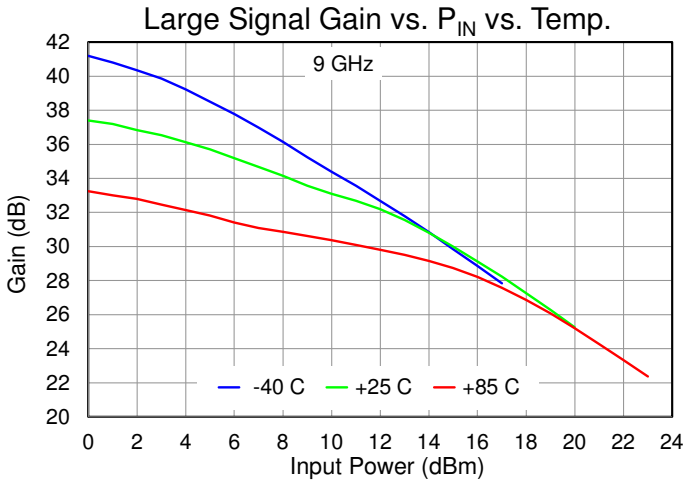

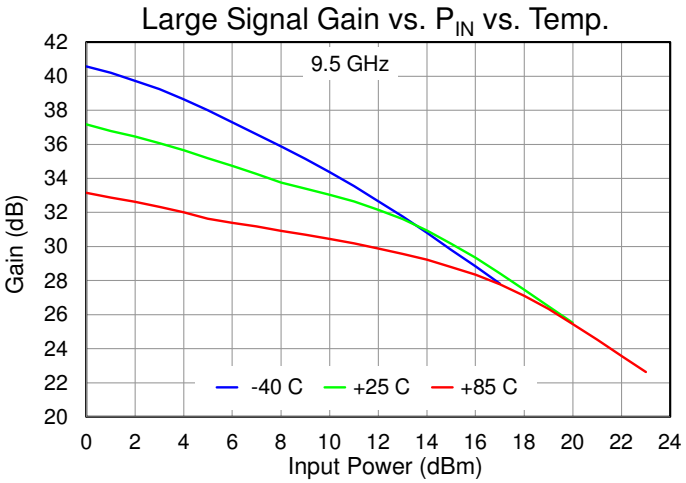

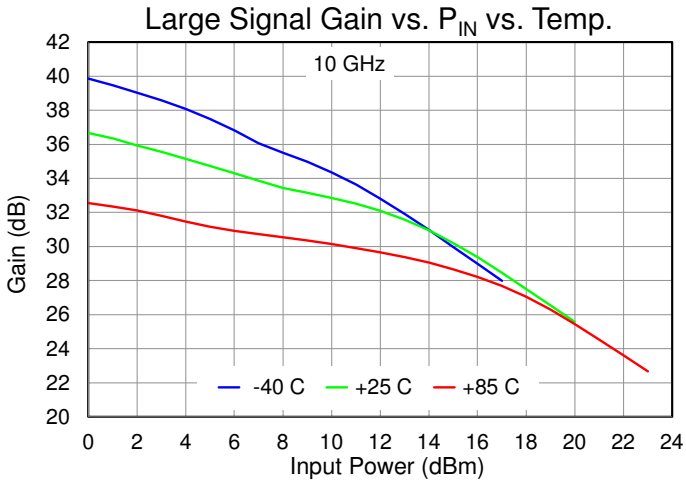

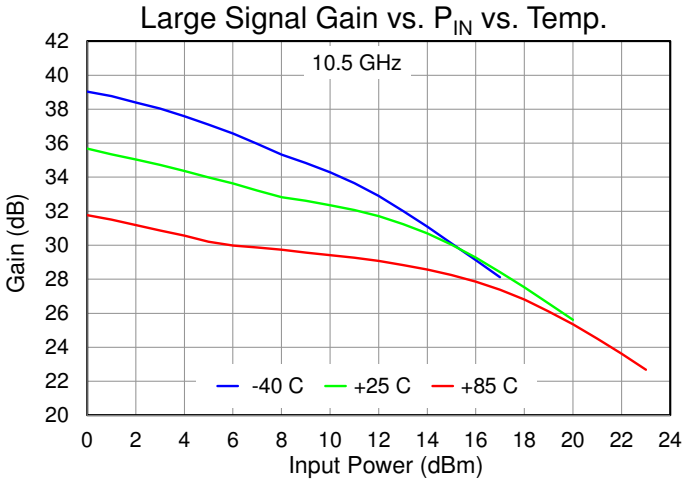

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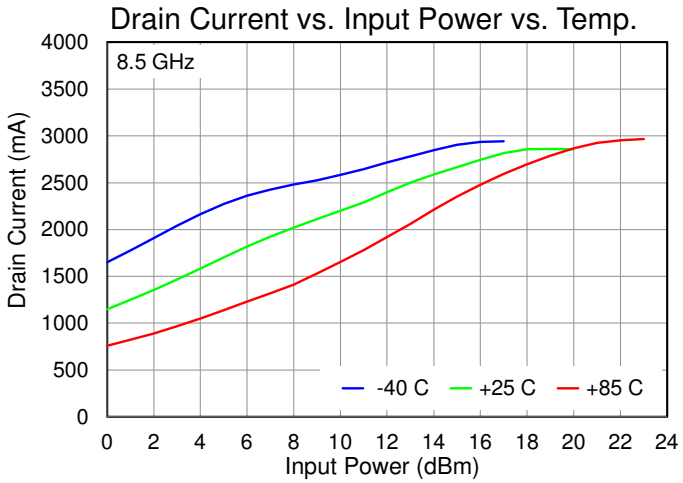

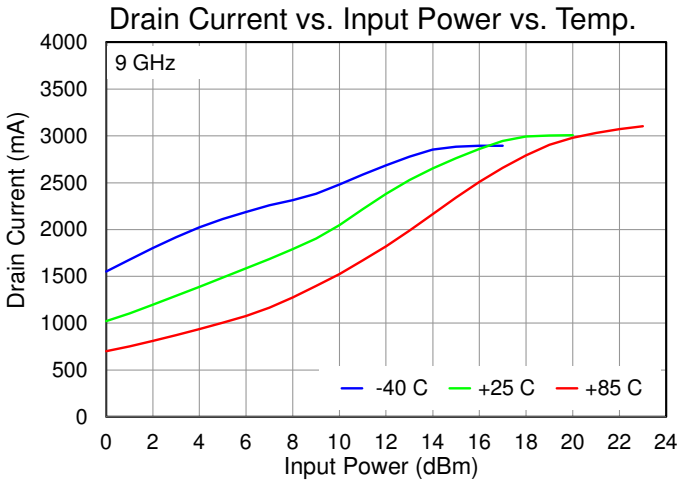

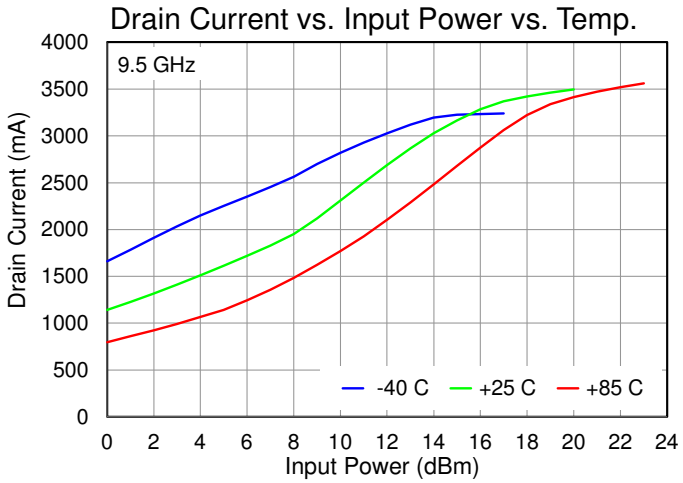

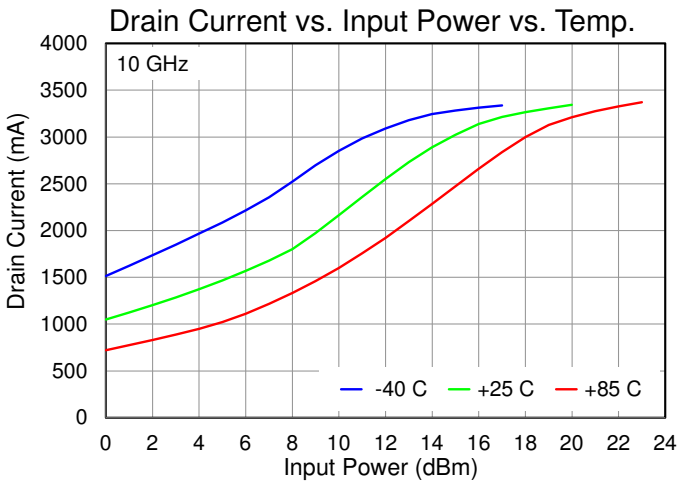

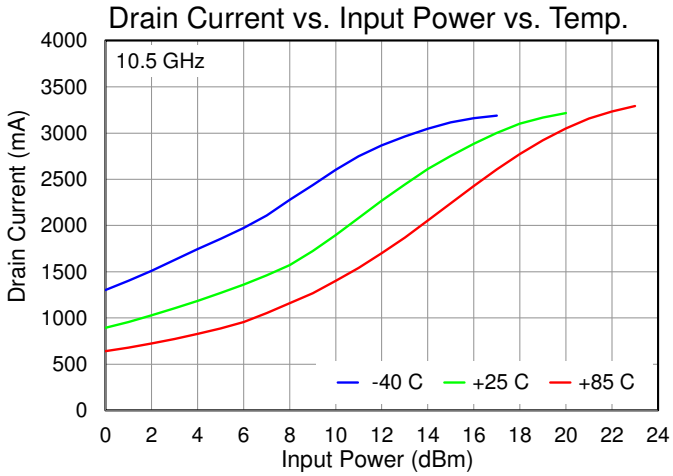

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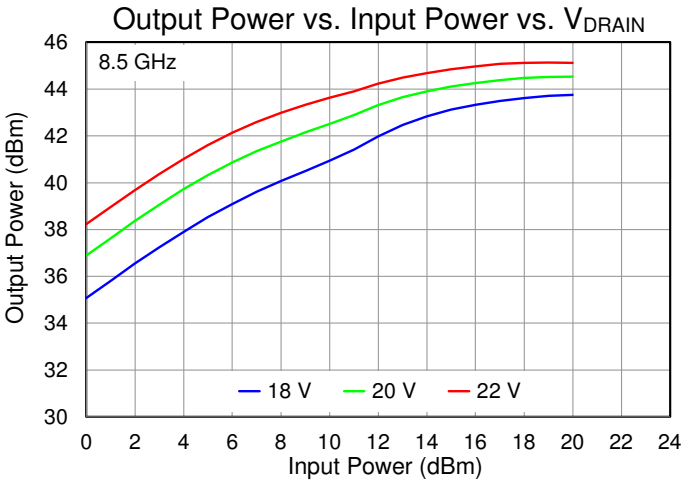
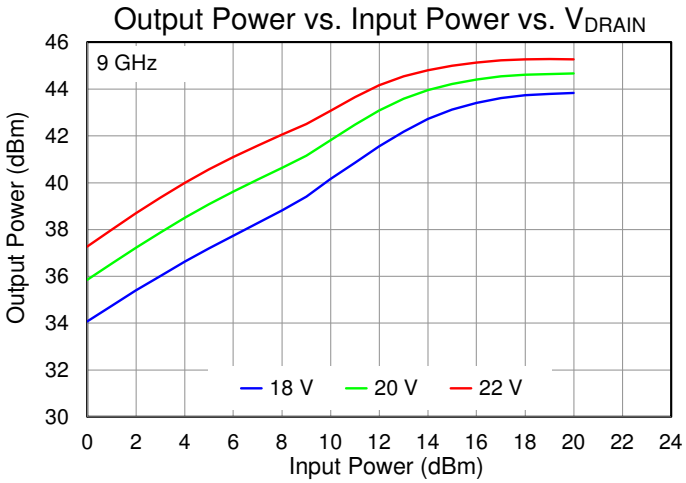
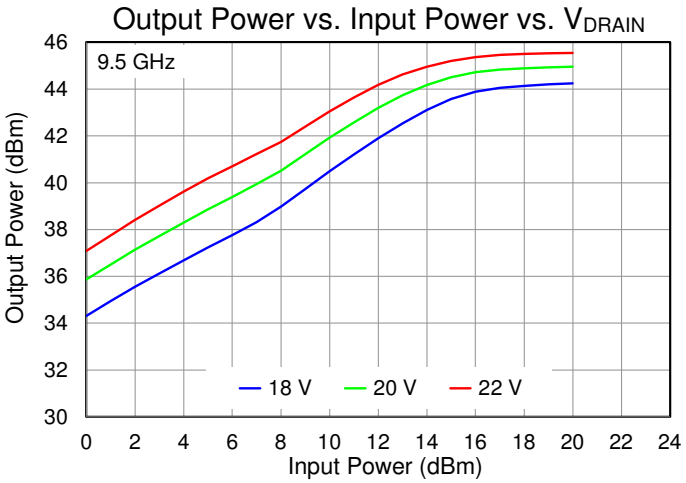
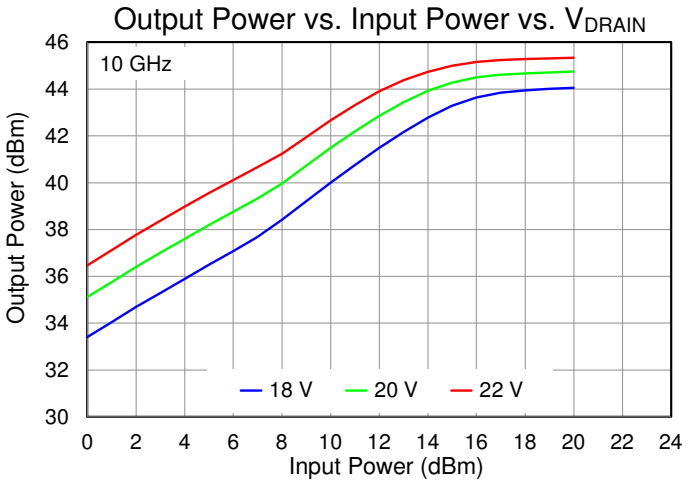
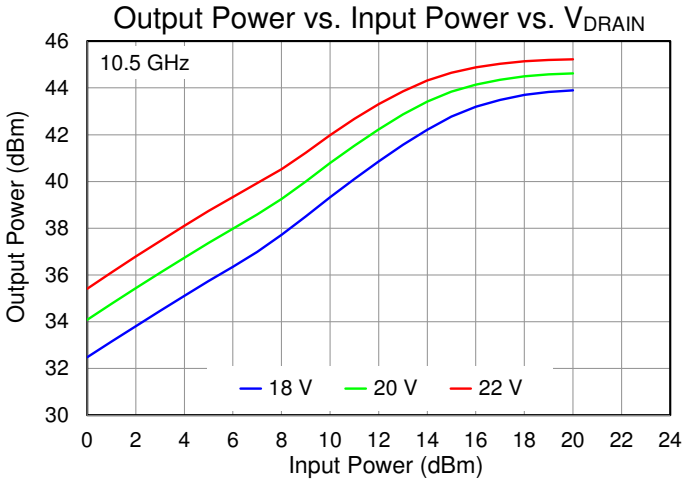




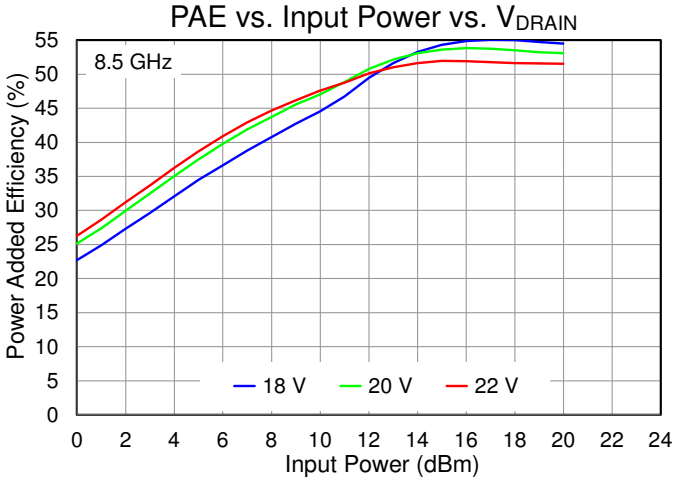


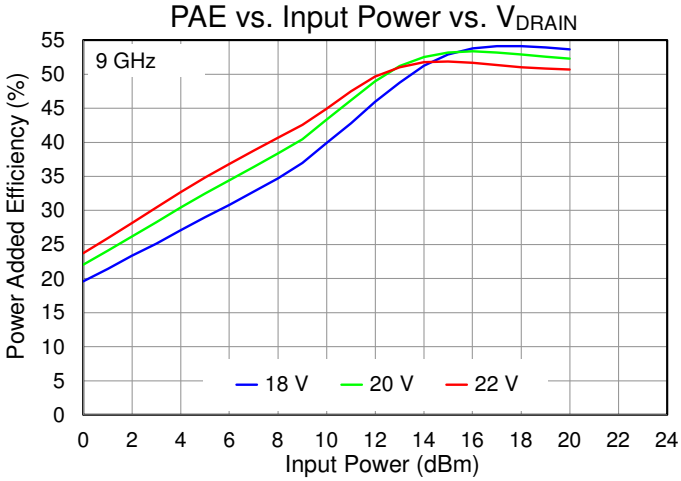


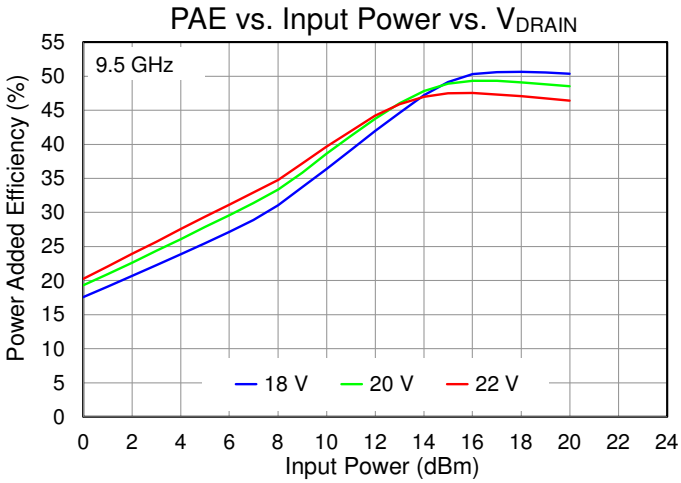


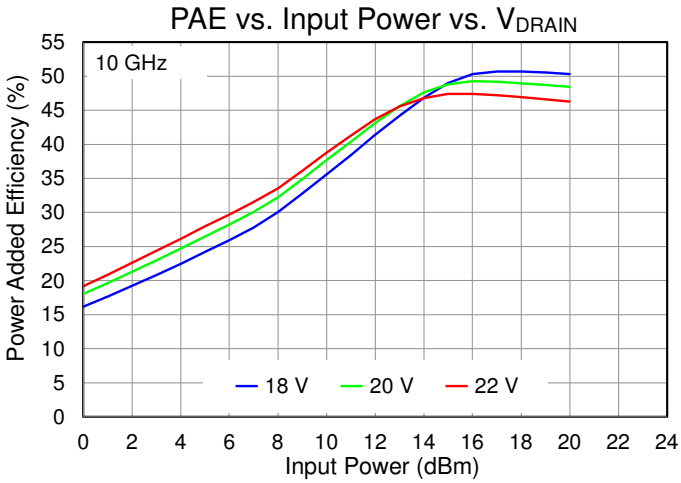
Performance Plots – Large Signal (Pulsed)

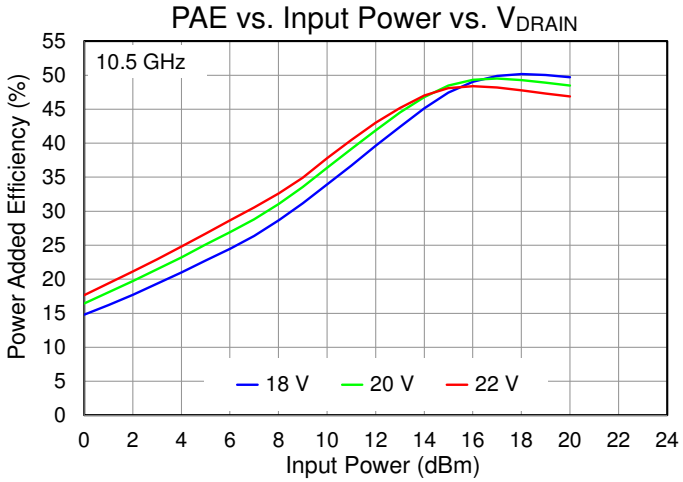
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = 17 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).





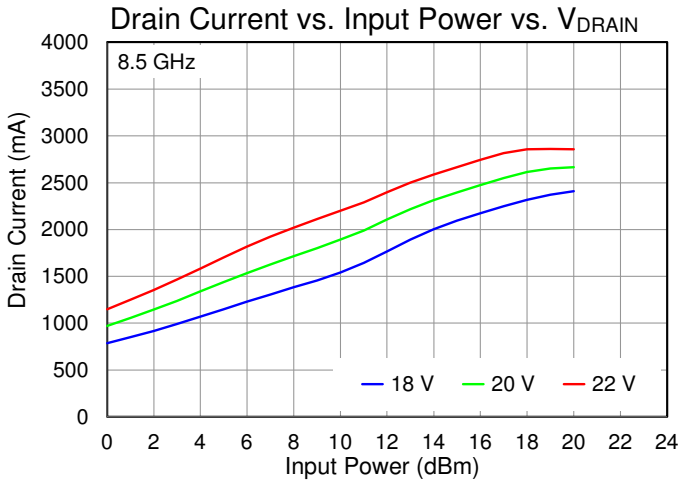


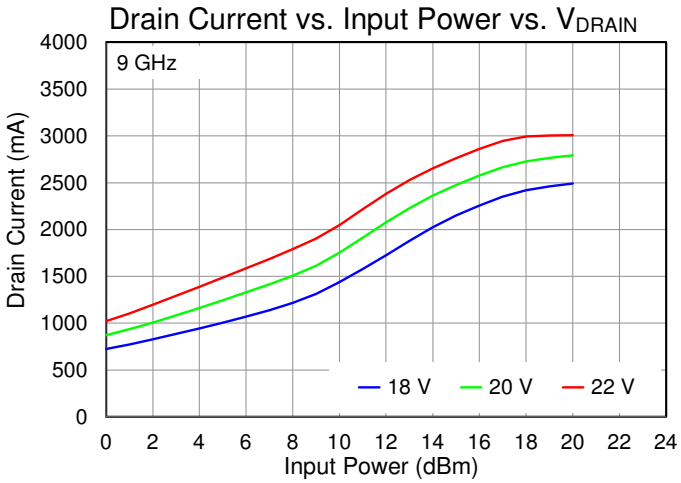


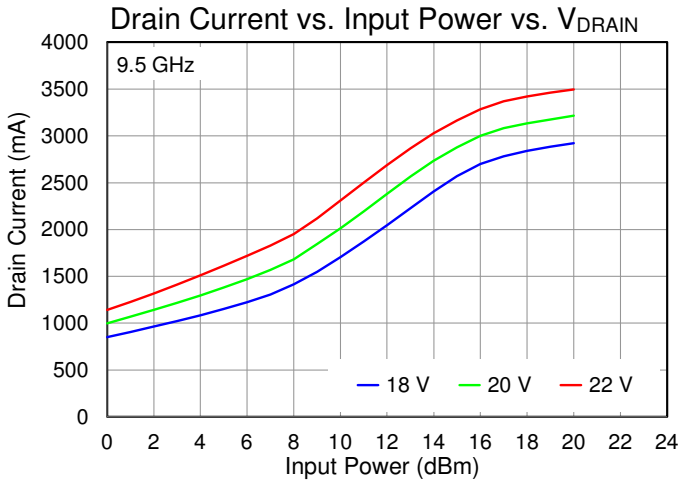


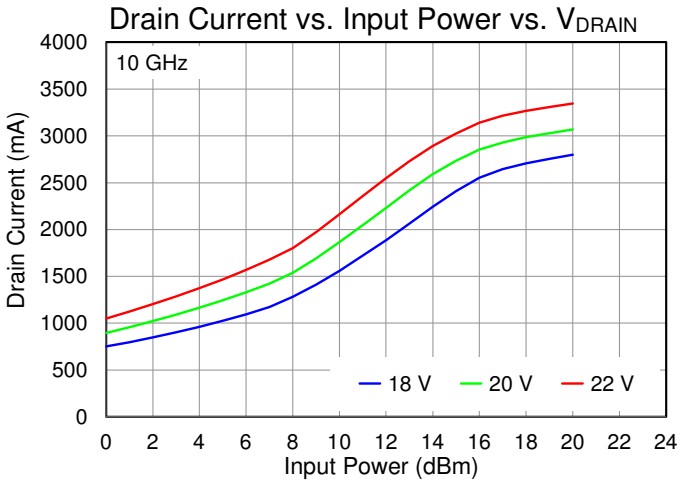
Performance Plots – Large Signal (Pulsed)

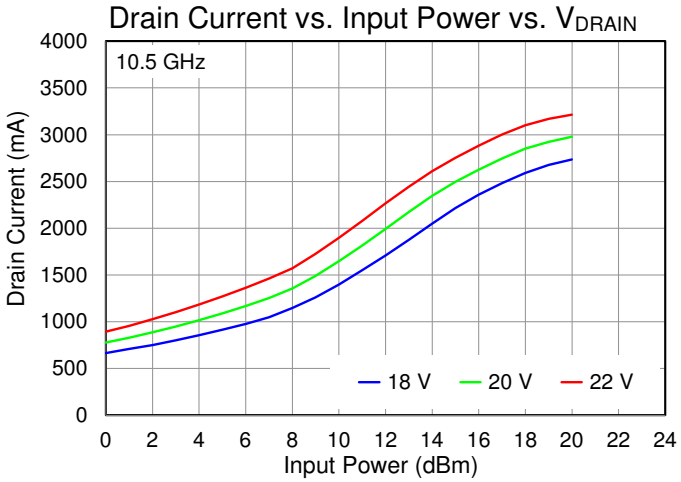
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = 17 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).





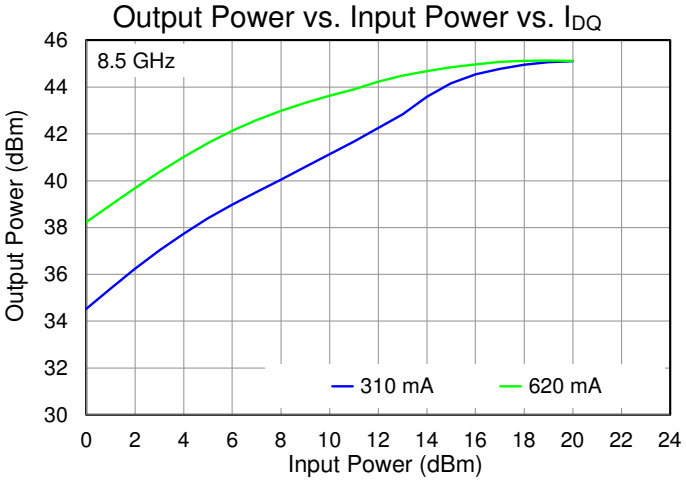


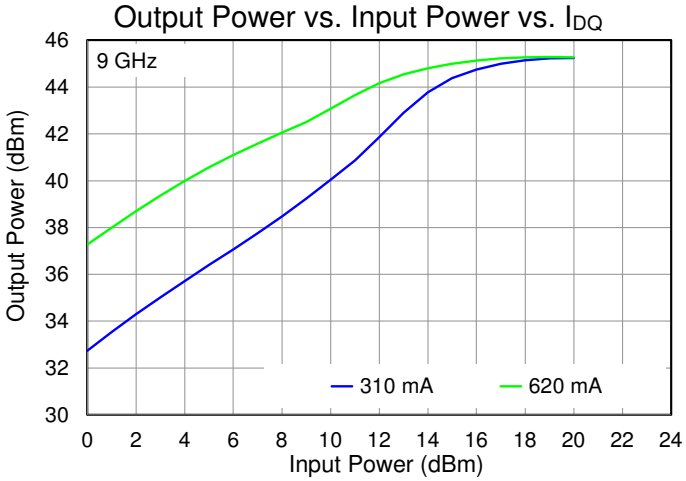


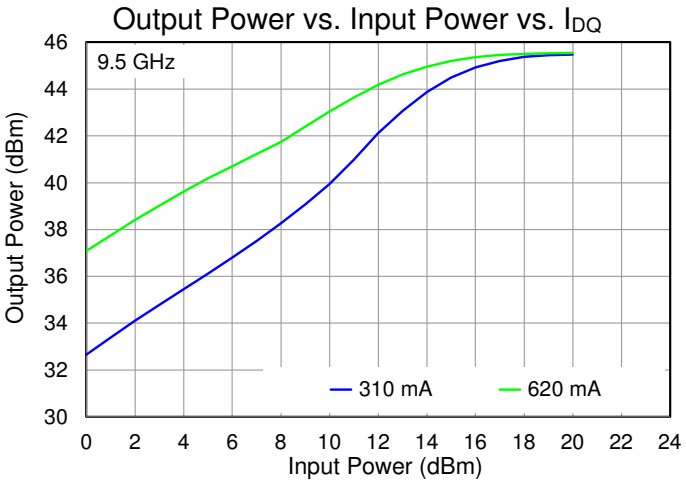


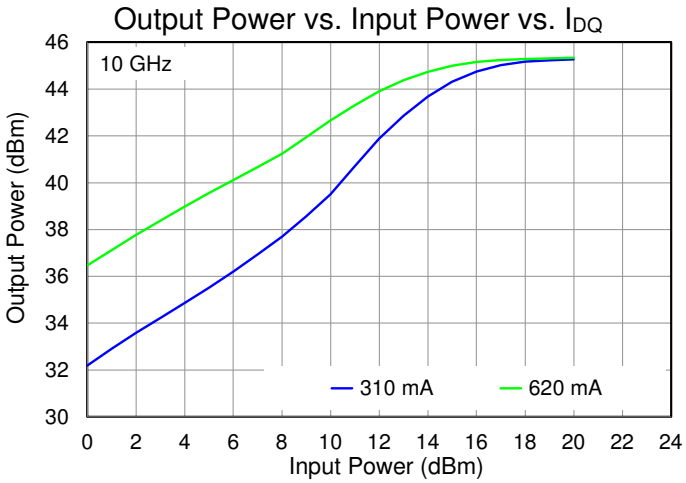
Performance Plots – Large Signal (Pulsed)

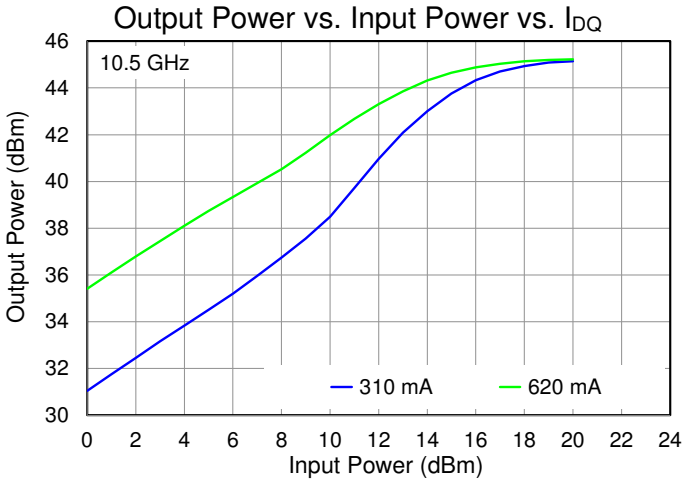
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = 17 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).





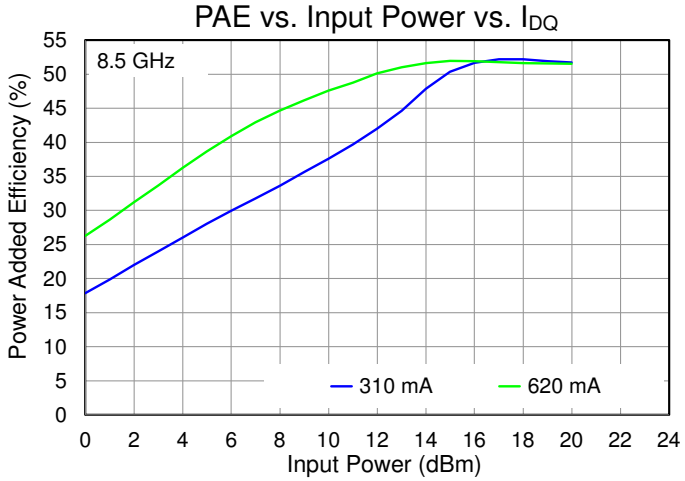


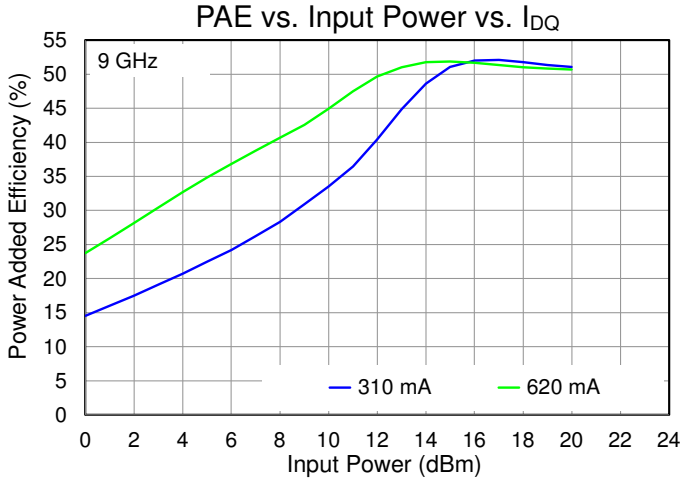


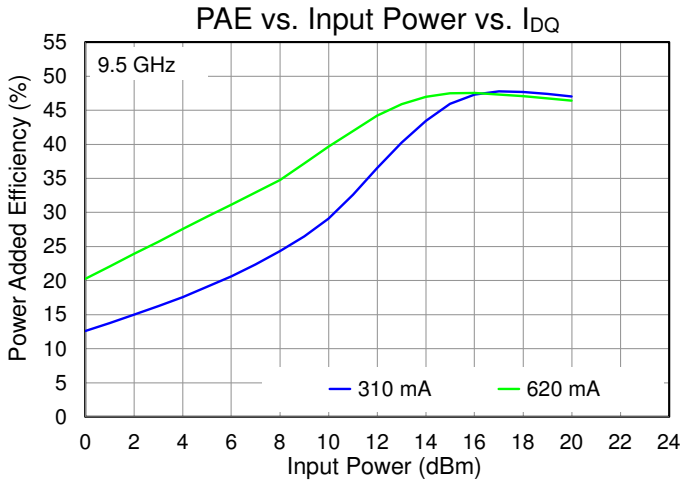


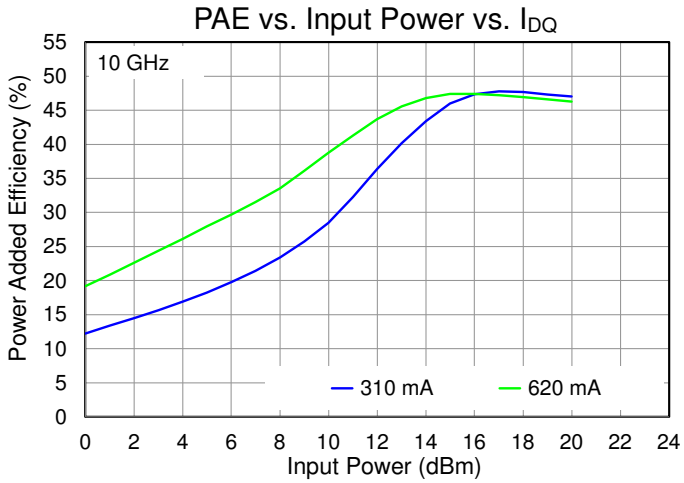
Performance Plots – Large Signal (Pulsed)

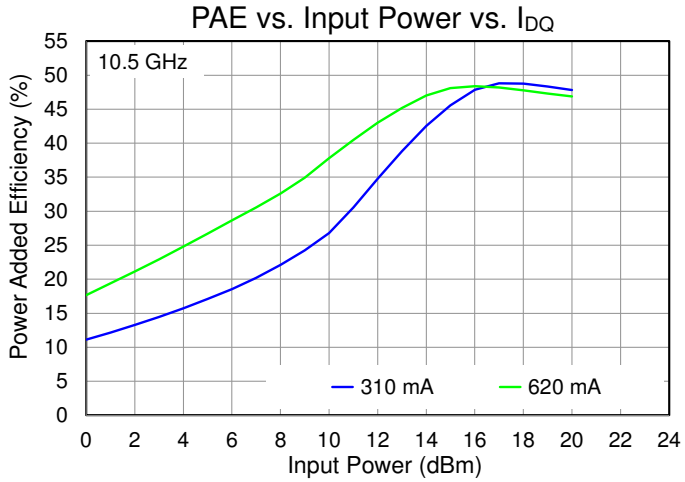
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = 17 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).





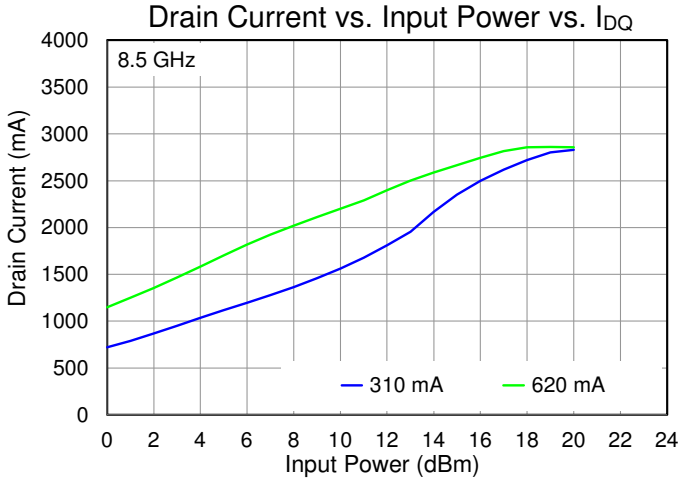


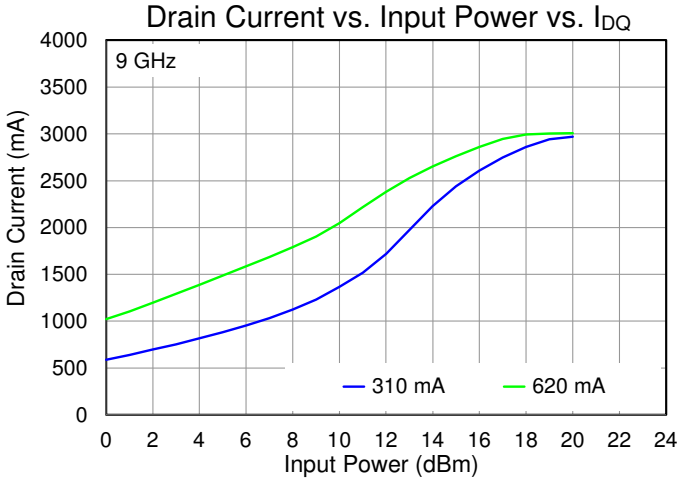


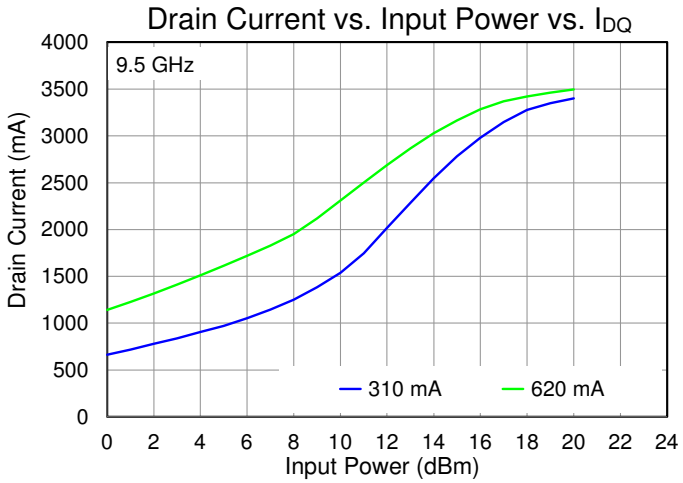


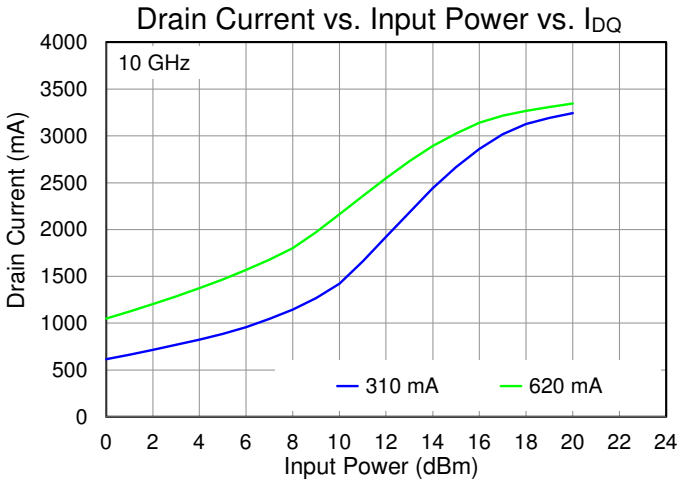
Performance Plots – Large Signal (Pulsed)

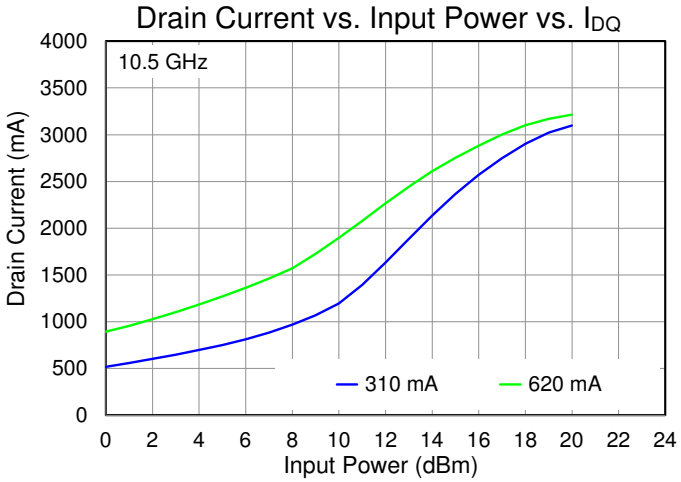
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = 17 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).





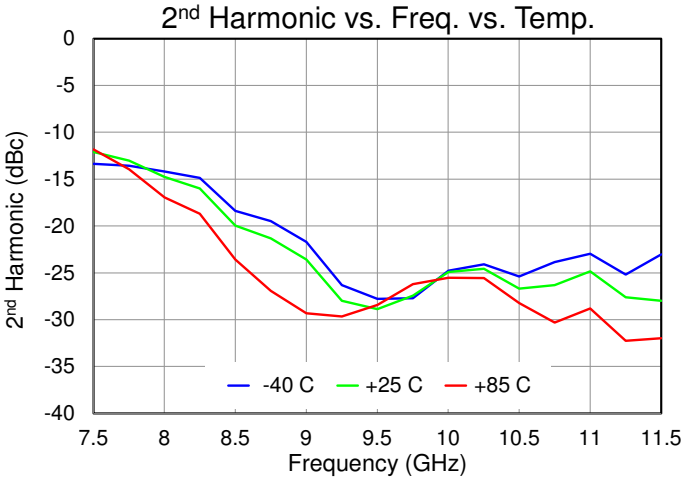


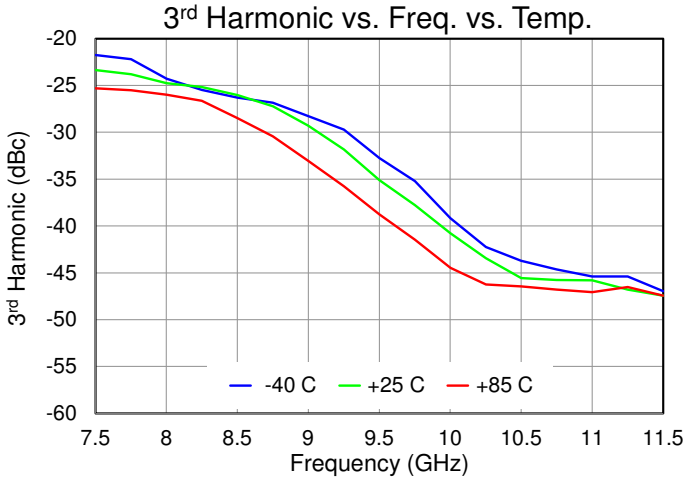


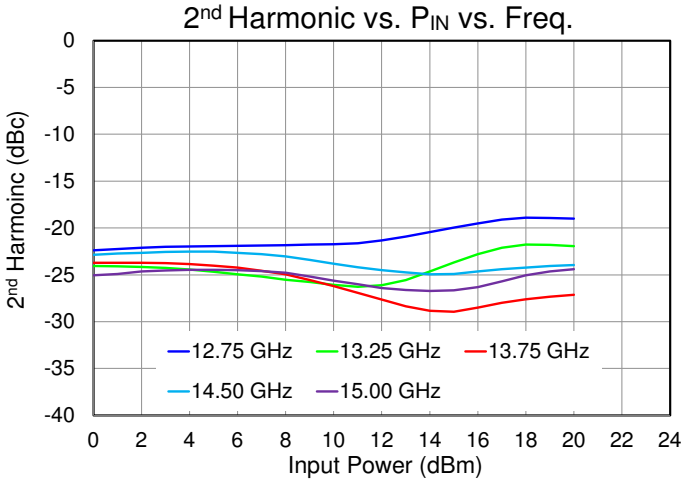


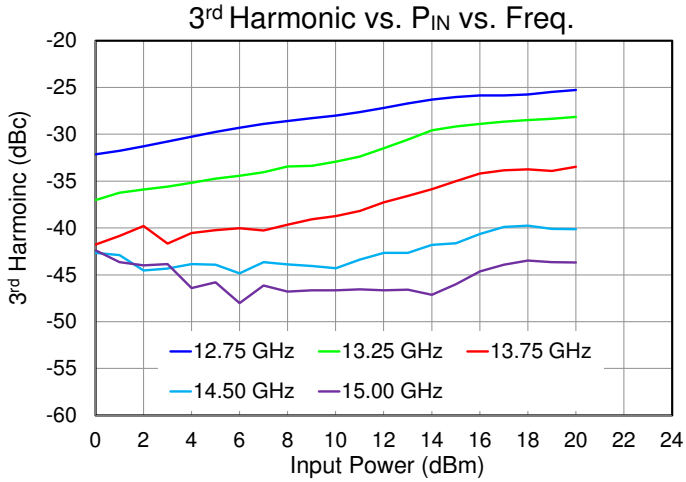
Performance Plots – Harmonics (Pulsed)

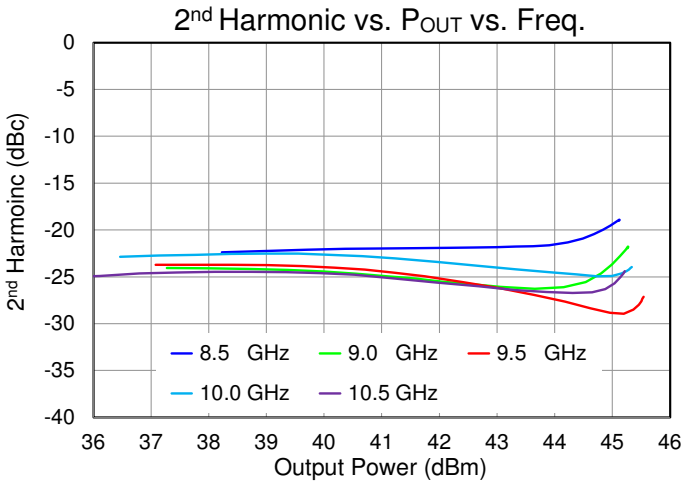
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).

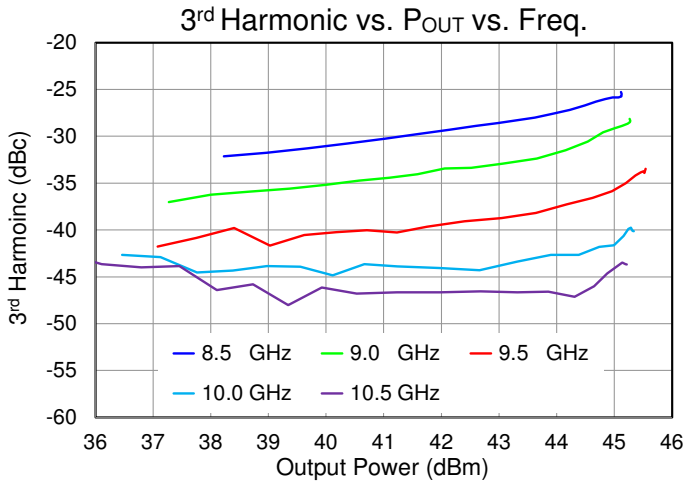






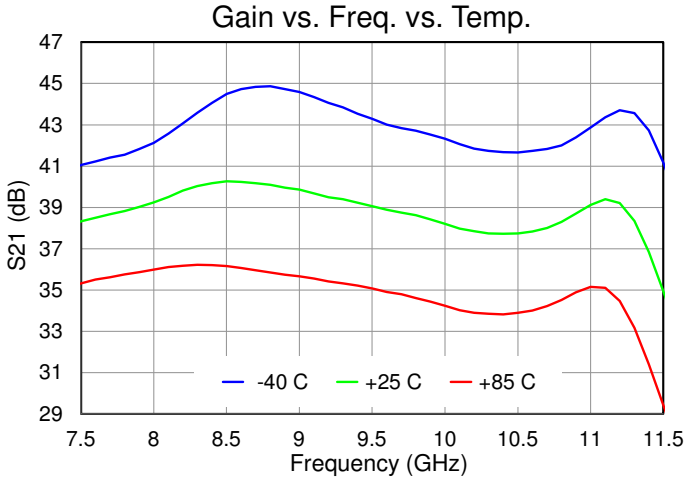


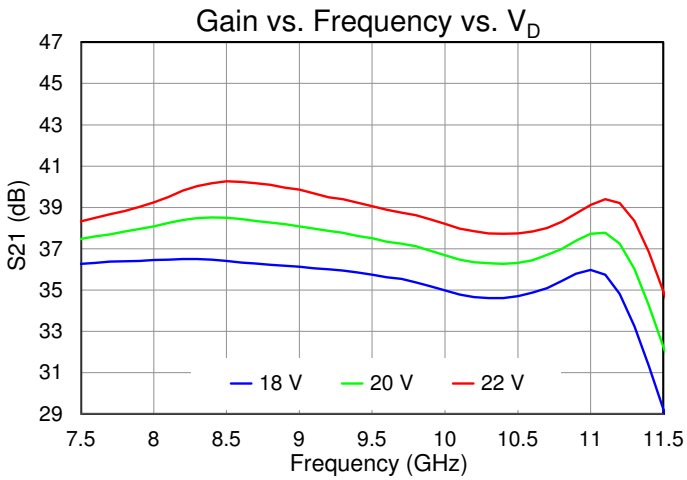


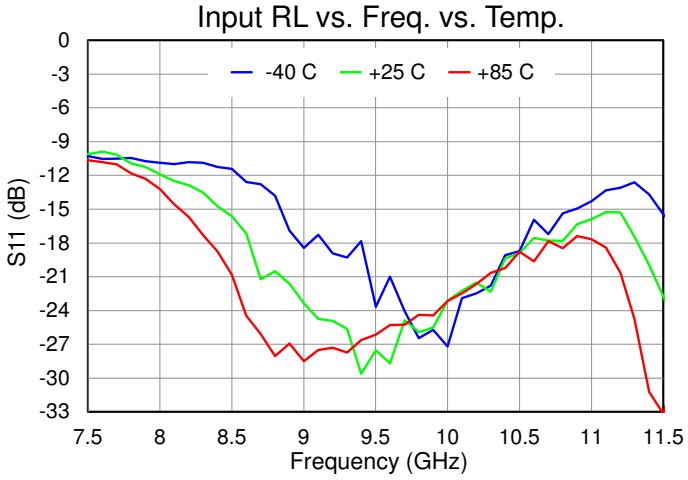


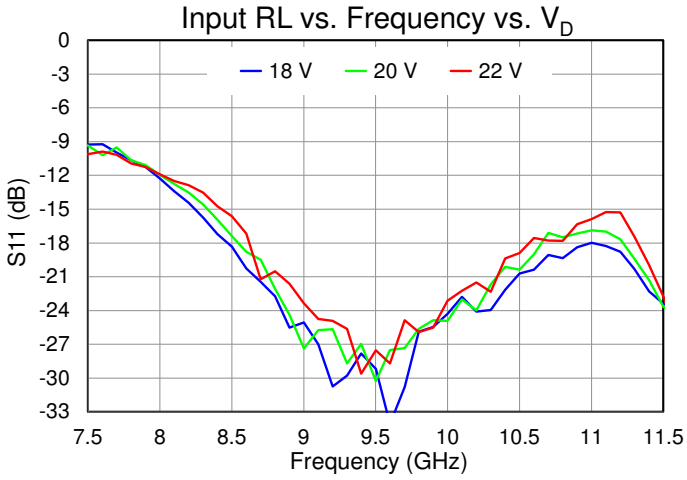
Performance Plots – Small Signal (Pulsed)

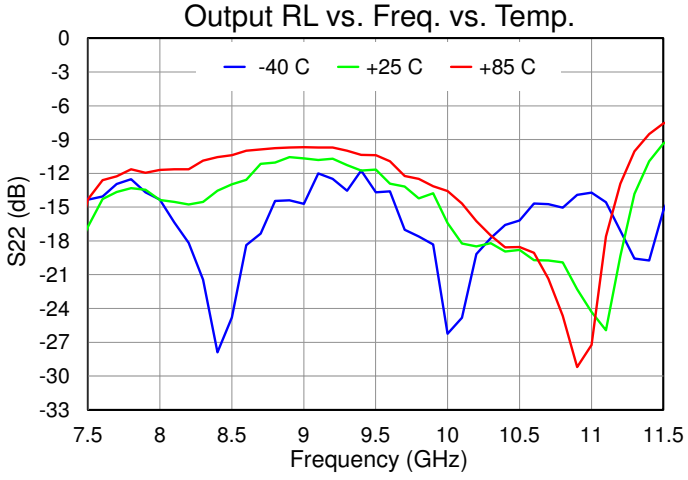
Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).

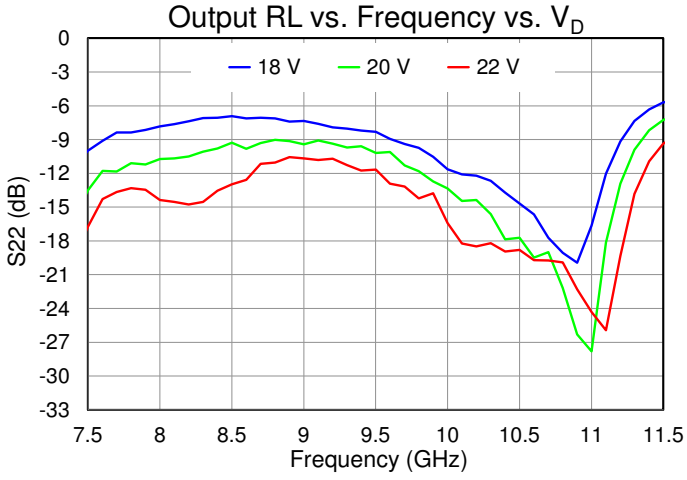






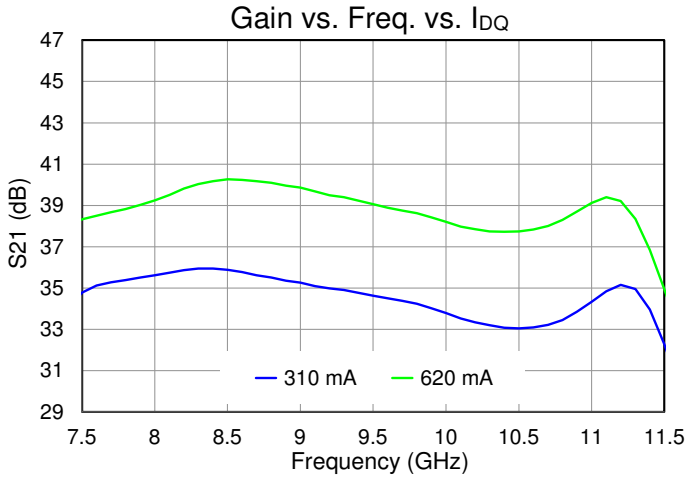


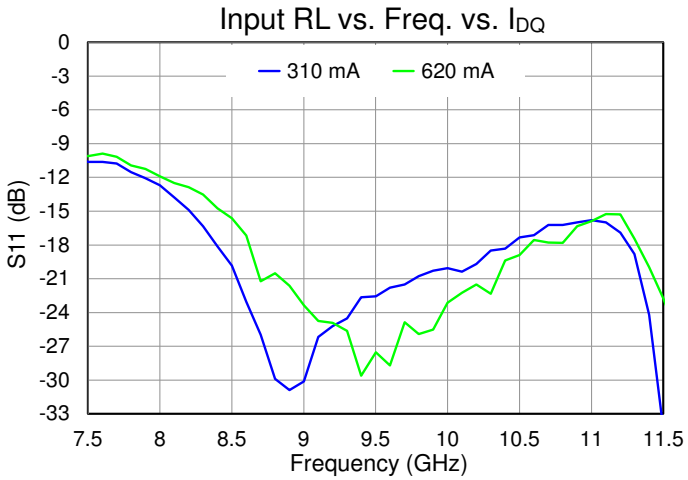


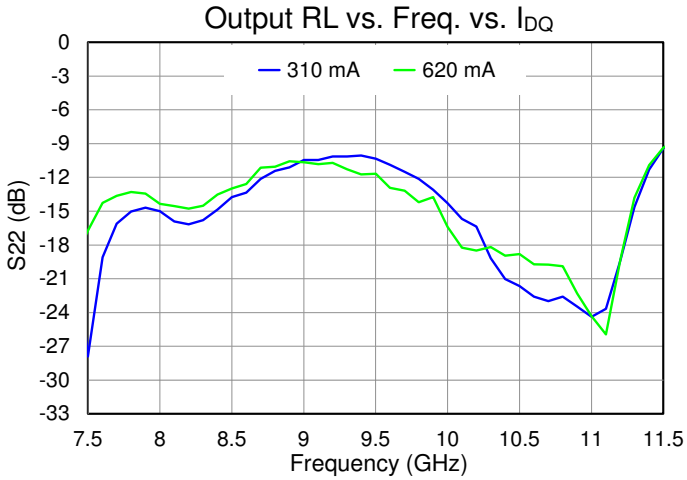


Performance Plots – Small Signal (Pulsed)

Test conditions, unless otherwise noted: Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA1111).







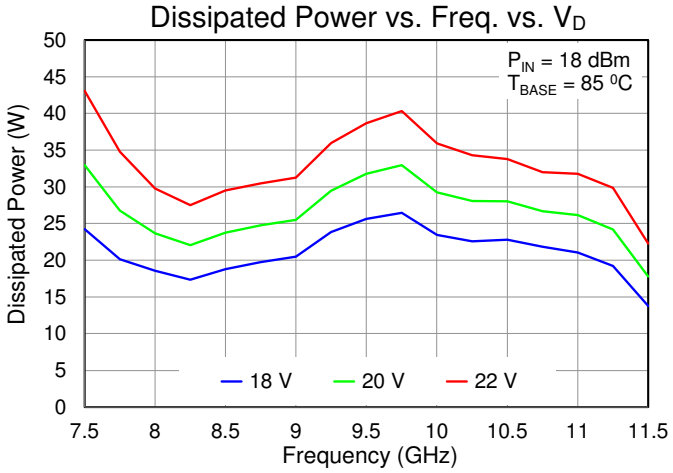
Thermal and Reliability Information

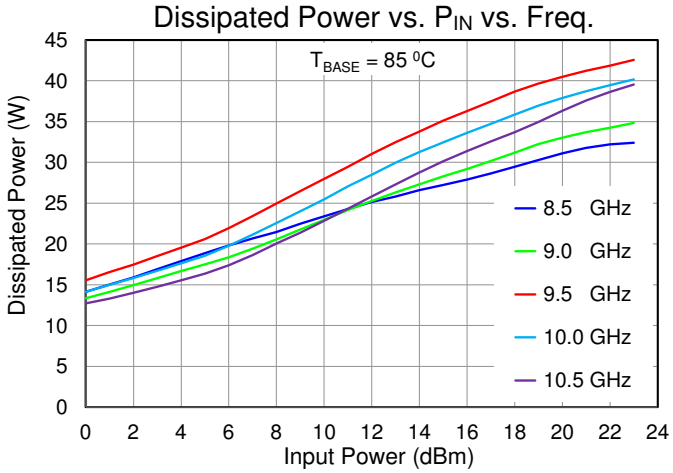
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent, no RF T_{BASE} = 85 °C, V_D = 22 V, I_{DQ} = 620 mA, P_{DISS} = 13.64 W	1.42	ºC/W
Channel Temperature, T_{CH} (2)		104	°C
Thermal Resistance, θ_{JC} (1)	Pulsed, P_{IN} = 18 dBm, T_{BASE} = 85 °C, V_D = 22 V, I_{DQ} = 620 mA, I_{D_DRIVE} = 3250 mA, PW = 100 µs, DC = 10%, Freq = 9.75 GHz, P_{OUT} = 45 dBm, P_{DISS} = 40 W.	1.50	ºC/W
Channel Temperature, T_{CH} (2)		145	°C

Notes:

1. Thermal resistance determined to T_{BASE} (T_{BASE} is backside of package QPA1111; see p. 24 offset temperature based on Qorvo's EVB design for reference).
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note "GaN Device TCHMAX Theta-JC and Reliability Estimates," located here https://www.qorvo.com/products/d/da006480

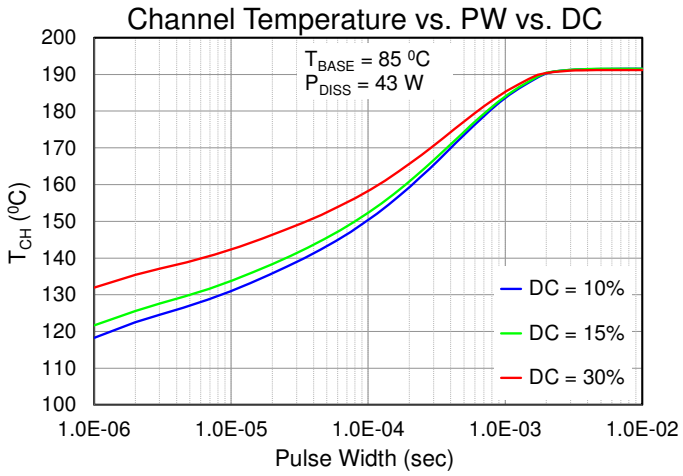
Dissipated Power





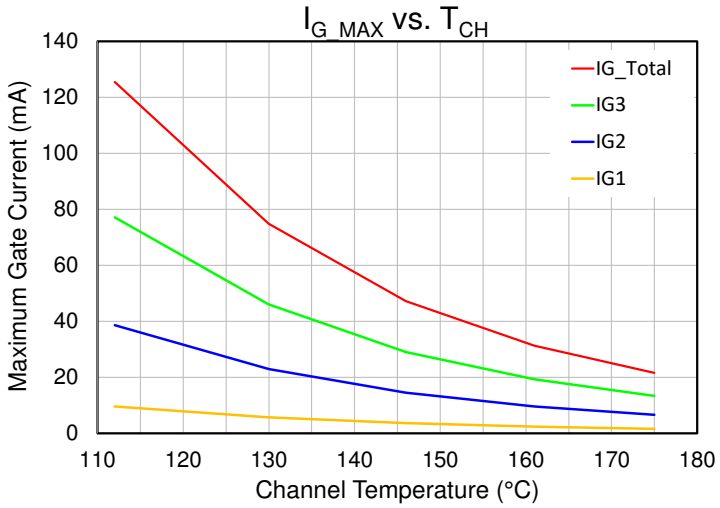
Test conditions, unless otherwise noted.
Pulsed V_D = 22 V, I_{DQ} = 620 mA, PW = 100 µs, DC = 10%, T_{BASE} = 85 ºC (T_{BASE} is back side of QPA1111)

Pulse Duration



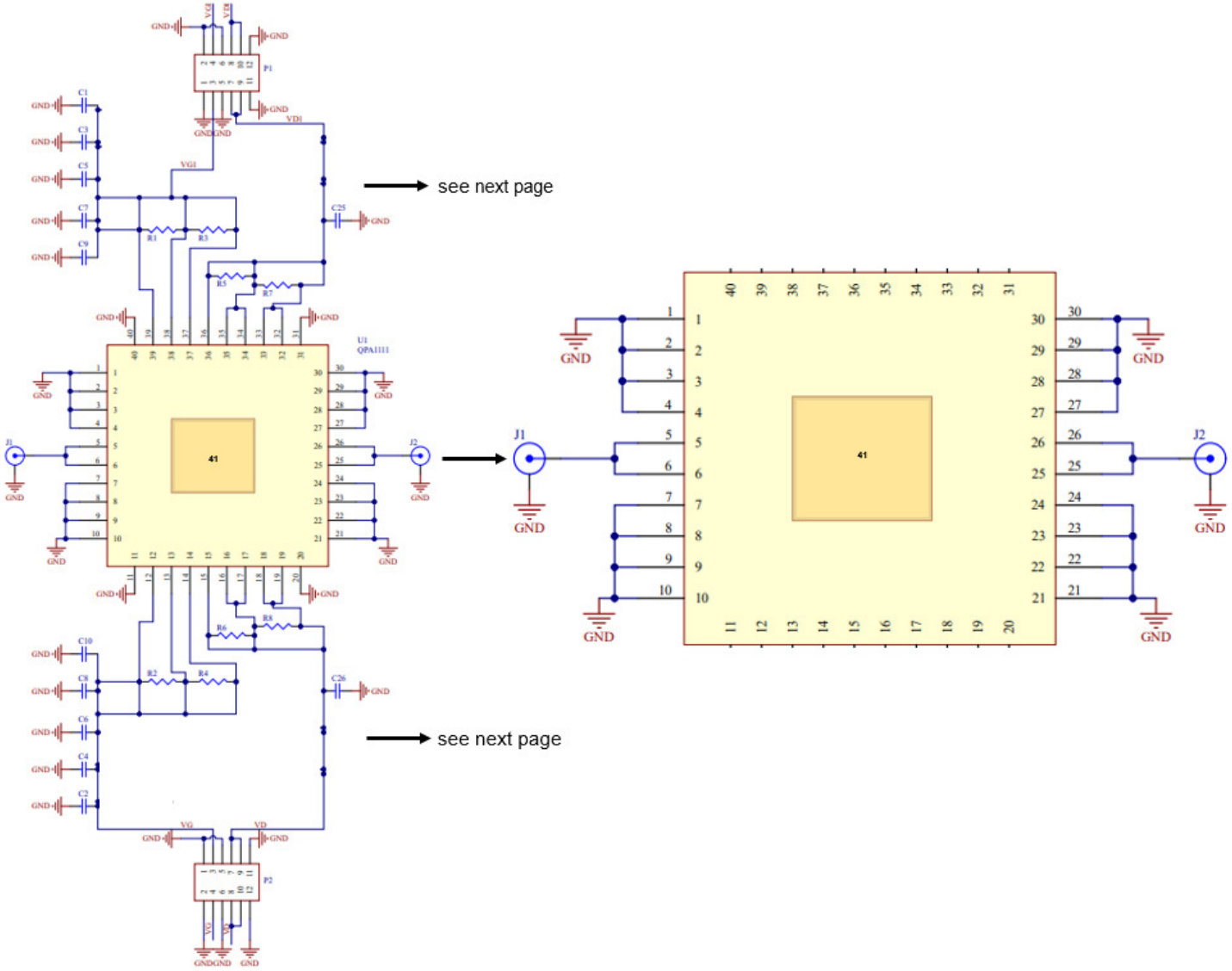
T_{BASE} is back side of QPA1111
Channel Temperature is an IR scan equivalent

Maximum Gate Current



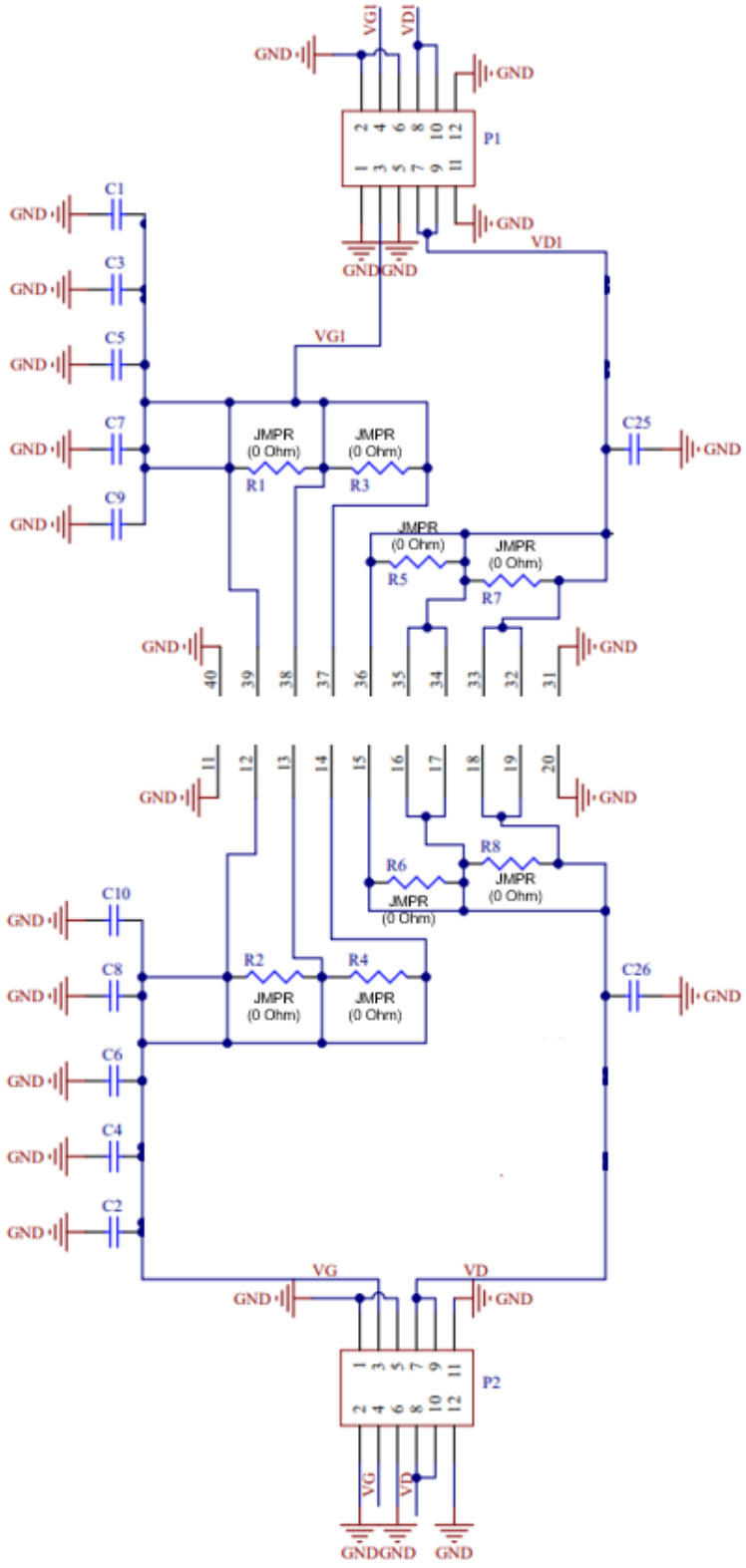
Channel Temperature is an IR scan equivalent

Applications Information



1. Drain and gate can be biased from both or either side; V_D both sides (or V_G both sides) can be tied together at the harness level.
2. The external bypassing components are required on both sides (even for non-biased side).

Applications Information (Cont.)



Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C2	2	10 µF	CAP, 10uF, ±20%, 25V, X5R, 0805	
C3, C4, C7, C8	4	1 µF	CAP, 1uF, ±10%, 50V, X5R, 0603	
C5, C6, C9, C10, C25, C26	6	0.1 µF	CAP, 0.1uF, ±10%, 50V, X7R, 0402	
R1 – R8	8	0 Ω	RES, 0 Ohm, JMPR, 0402	
PCB	1		PCB for QPA1111 (Cu-filled vias, see page 24)	Qorvo, Custom
H1, H2	2		DC Header, ST, 2x6, 0.100”, SMD	
J1, J2	2		RF Connector, 2.92mm, F, Pin 0.005, Diel 0.029	Southwest Microwave
H-Block	1		H-Block, Copper C110, 1.000 x 2.000 x 0.275 in	Qorvo, Custom
S1 – S4	4		Screw, Cap, Socket Head, 2-56X1/8”	
Solder Preform			Solder SAC305, Preform, 0.984 x 1.994 x 0.003 in	
Solder			Paste, solder, Syntech, Sn63/Pb37	

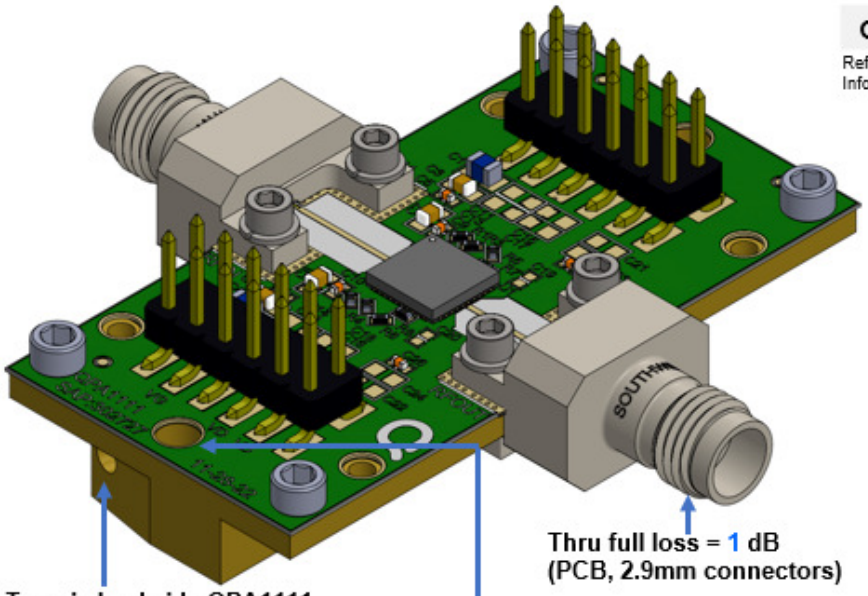
Bias-Up Procedure

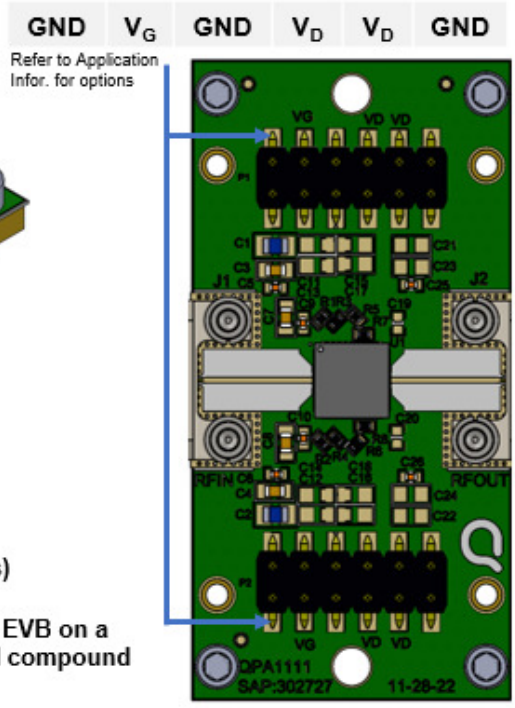
1. Set limit: I_D to 5 A, I_G to 40 mA each.
2. Set V_G = -3.5 V
3. Set V_D = +22 V. Ensure I_D ~ 0 mA
4. Adjust V_G more positive until I_D = 620 mA; $V_G \approx$ -2.3 ± 0.7 V typical range
5. Wait 15 seconds; then repeat step 4
6. Apply RF signal

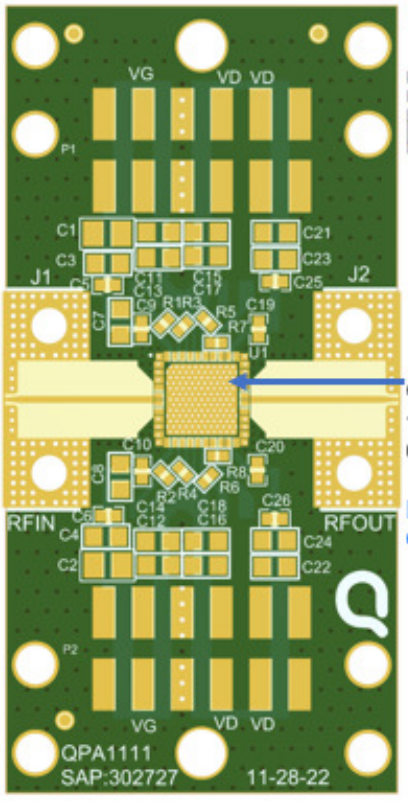
Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to -3.5 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Wait 5 seconds
6. Turn off V_G supply

Evaluation Board (EVB) Layout







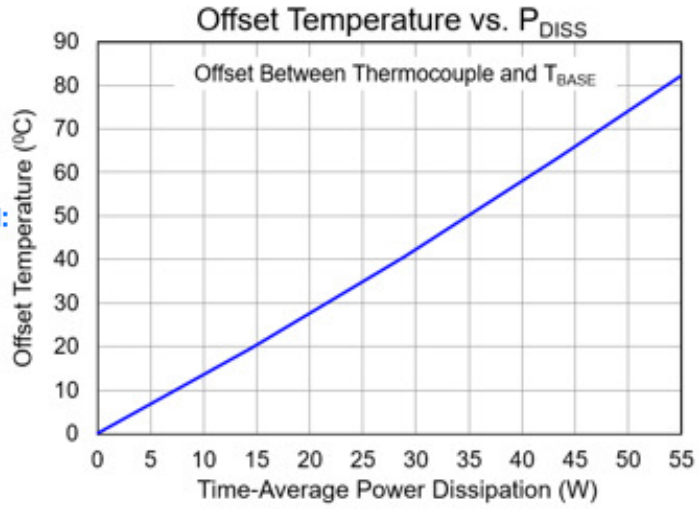
Cu-filled Vias
193 vias,
0.006" via dia.

Best recommended:
Cu coined via

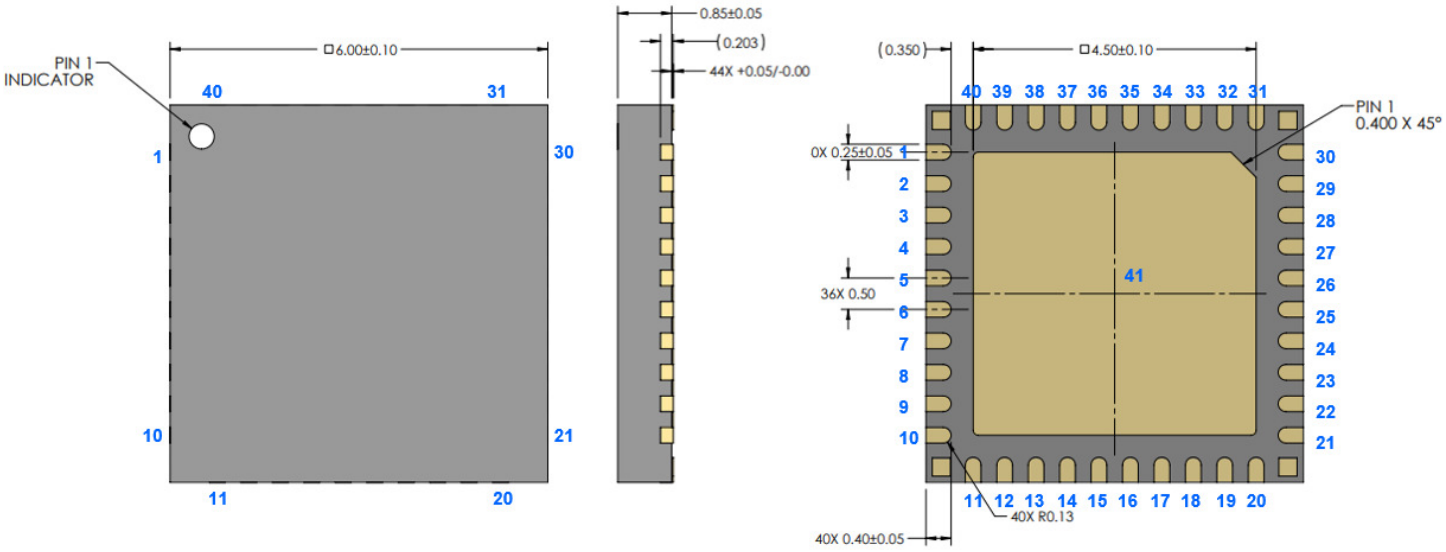
LAYER STACK LEGEND

Material	Layer	Thickness	Dielectric Material	Type
	Top Overlay			Legend
Surface Material	Top Solder	0.0004in	Solder Resist	Solder Mask
Copper	**Top Layer**	**0.0014in**		**Signal**
Core		*0.0080in*	*RO4003C*	*Dielectric*
Copper	**Bottom Layer**	**0.0014in**		**Signal**

Total thickness: 0.0112in



Mechanical Information



Dimensions (unless otherwise specified): mm.
Tolerances (unless noted): .xx = ± .25; .xxx = ± .100; .xxxx = ± .0254; angles = 0.5^0
Package is mold encapsulated, non-hermetic, leads are Au plated.

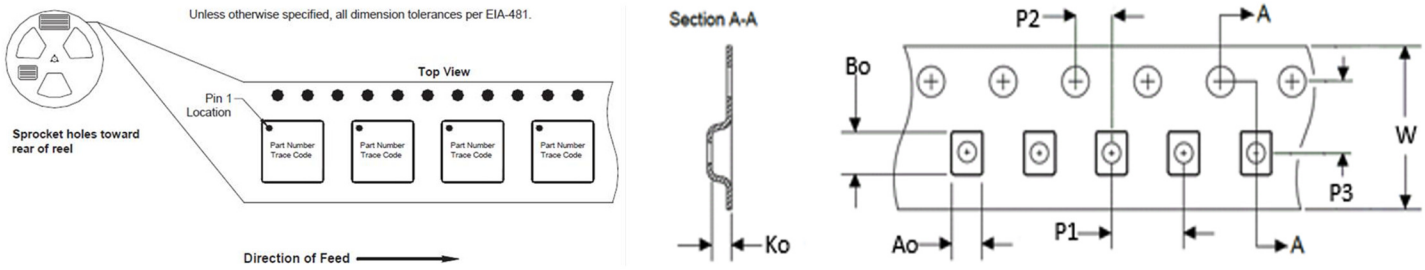
Pin Description

Pin Number	Symbol	Description
1 – 4, 7 – 11, 20 – 24, 27 – 31, 41	GND	Ground; grounded on PCB
5, 6	RF_{IN}	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
12, 39	V_{G1}	Gate voltage for stage 1 (1)
13, 38	V_{G2}	Gate voltage for stage 2 (1)
14, 37	V_{G3}	Gate voltage for stage 3 (1)
15, 10, 36	V_{D1}	Drain voltage for stage 1 (1)
16, 17, 34, 35	V_{D2}	Drain voltage for stage 2 (1)
18, 19, 32, 33	V_{D3}	Drain voltage for stage 3 (1)
25, 26	RF_{OUT}	RF Output. Matched to 50 Ω, DC blocked, DC shorted to ground
13	GND	Ground (backside paddle); grounded on PCB; Cu-filled vias should be employed to minimize inductance and thermal resistance (2)

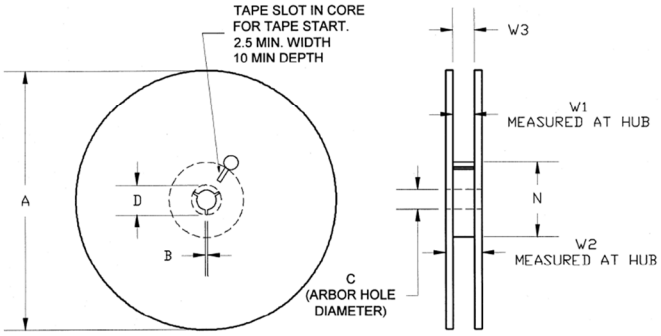
1. External bypassing required; refer to page 21 - 23 for recommendation.
2. Refer to page 24 for Cu-filled vias layout

Tape & Reel Information

Standard T/R size = 250 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.248	6.3
	Width	B0	0.248	6.3
	Depth	K0	0.047	1.2
	Pitch	P1	0.472	12
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	P3	0.295	7.50
Cover Tape	Width	C	0.524	13.3
Carrier Tape	Width	W	0.630	16.0

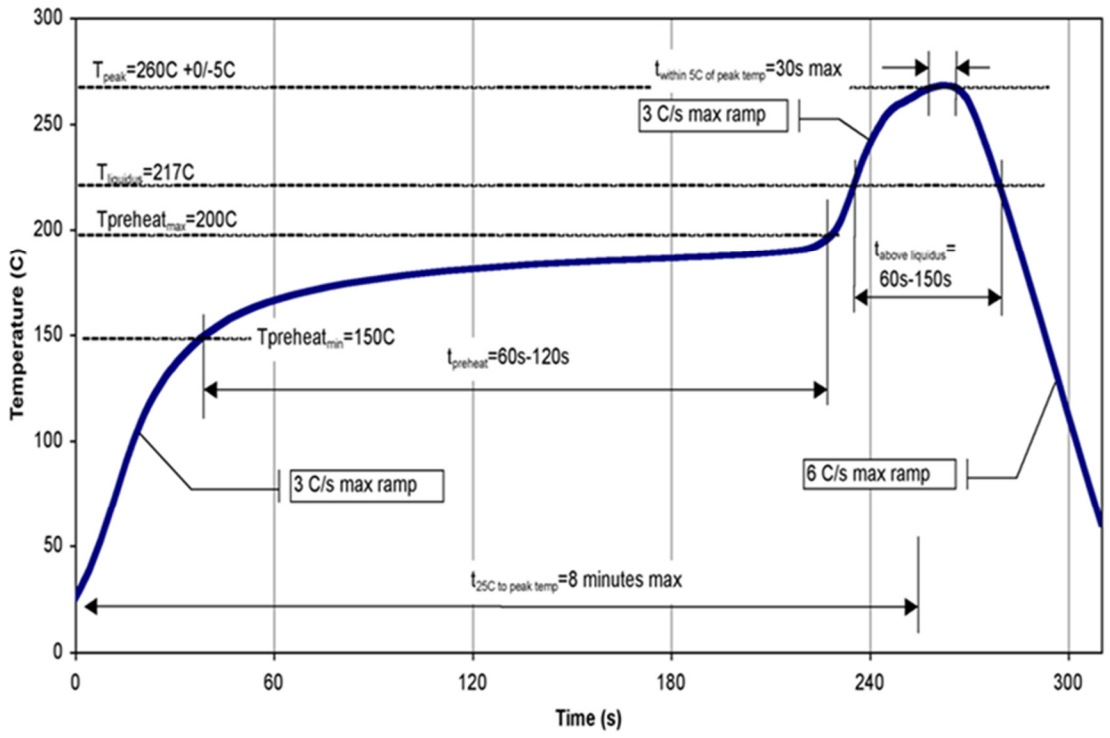


Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	0.882	22.4
	Space Between Flange	W1	.646	16.4
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	.795	20.2

Solderability

- Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C
- Do not expose the package lid to temperatures > 280 °C
- Contact plating: Ni-Au
- Solder rework not recommended.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!

ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free
- Halogen Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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