

### Product Overview

Qorvo’s QPM0106 is a packaged, high power amplifier fabricated on Qorvo’s production 0.25 um GaN on SiC process. The QPM0106 operates from 1.0–6.0 GHz and provides 45.4 dBm (35 W) of saturated output power with 22.4 dB of large signal gain and 41 % power-added efficiency.

The QPM0106 is packaged in a 10-lead 15.24 x 15.24 mm bolt-down package, with a pure copper base for superior thermal management. Both RF ports are internally DC blocked and matched to 50 ohms allowing for simple system integration.

The QPM0106 is ideally suited for both commercial and military EW and radar systems, communications systems, and test instrumentation.

RoHS compliant.

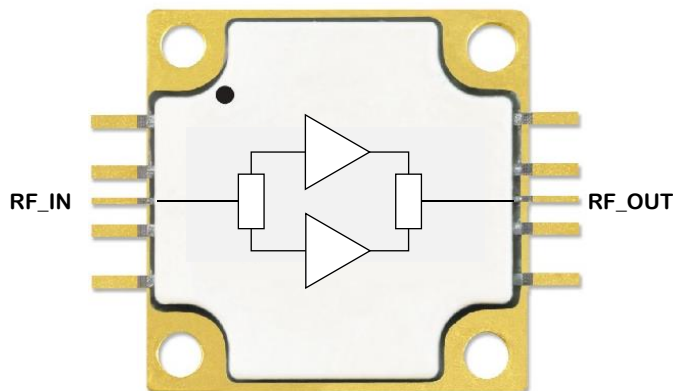


### Key Features

- Frequency Range: 1 – 6 GHz
- $P_{SAT}$  : 45.4 dBm ( $P_{IN} = 23$  dBm)
- PAE: 41% ( $P_{IN} = 23$  dBm)
- Power Gain: 22.4 dB ( $P_{IN} = 23$  dBm)
- Small Signal Gain: 30.2 dB
- Bias:  $V_D = 24$  V,  $I_{DQ} = 2044$  mA
- Package Dimensions: 15.24 x 15.24 x 3.51 mm

*Performance is typical across frequency. Please reference electrical specification table and data plots for more details.*

### Functional Block Diagram



Top View

### Applications

- Electronic Warfare
- Radar
- Test Instrumentation
- Communications

### Ordering Information

Part No.	Description
QPM0106	1 -6 GHz GaN Power Amplifier
QPM0106EVB	Evaluation Board for QPM0106

### Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage ( $V_D$ )	40 V
Gate Voltage Range ( $V_G$ )	-5 V to 0 V
Drain Current ( $I_D$ )	5.730 A
Gate Current ( $I_G$ )	See plot page 21
$P_{DISS}$ (under drive), 24V, 85 °C	112 W
Input Power, 50 $\Omega$ , $V_D=24$ V, $I_{DQ}=2044$ mA, CW, 85 °C	33 dBm
Input Power, 3:1 VSWR, $V_D=24$ V, $I_{DQ}=2044$ mA, CW, 85 °C	33 dBm
Storage Temperature	-55 to +125 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

### Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Drain Voltage ( $V_D$ )	18	22	26	V
Drain Current ( $I_{DQ}$ )		2044		mA
Operating Temperature	-40	25	85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

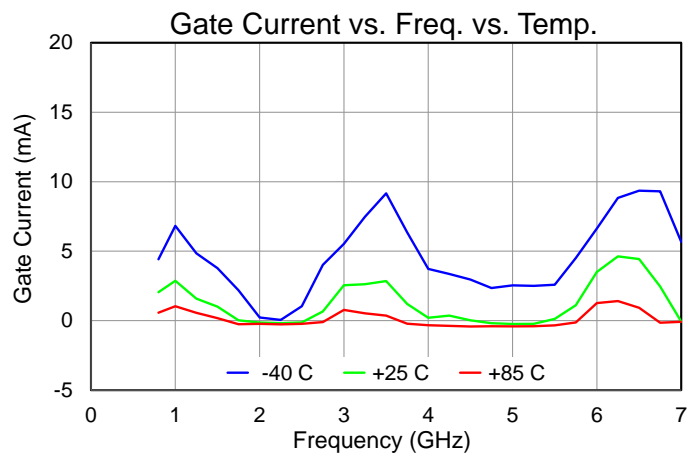
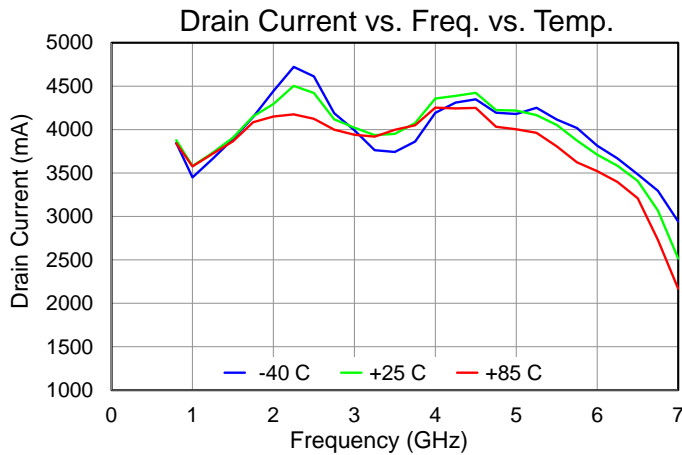
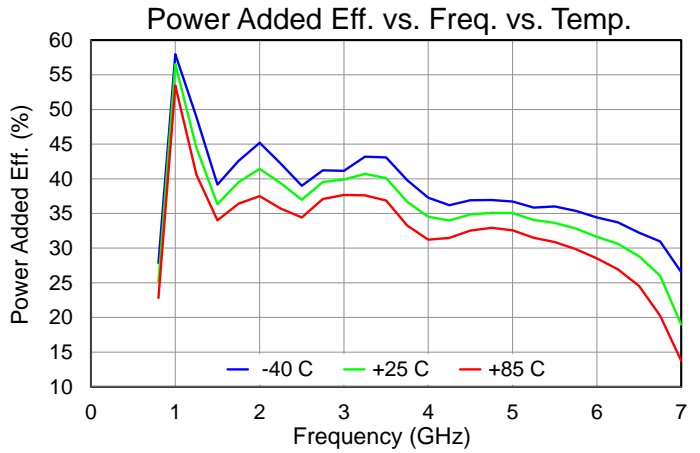
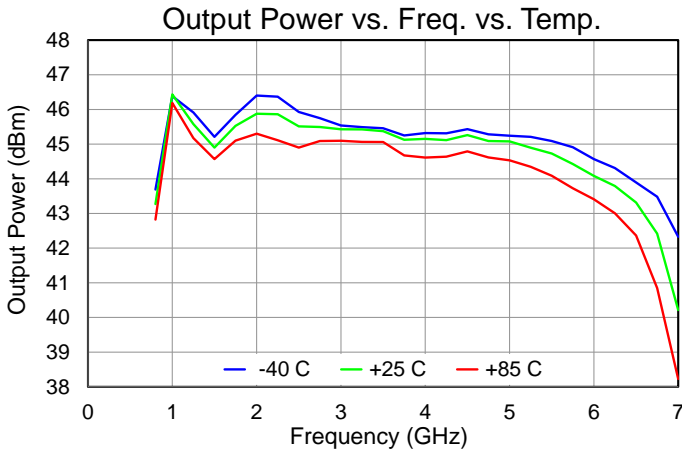
## Electrical Specifications

Parameter		Min	Typ	Max	Units
Operational Frequency		1		6	GHz
Output Power (P <sub>IN</sub> =23 dBm)	1 GHz		46.4		dBm
	2 GHz		45.9		dBm
	4 GHz		45.2		dBm
	6 GHz		44.1		dBm
PAE (P <sub>IN</sub> =23 dBm)	1 GHz		56.5		%
	2 GHz		41.4		%
	4 GHz		34.5		%
	6 GHz		31.6		%
Small Signal Gain	1 GHz		30.8		dB
	2 GHz		31.0		dB
	4 GHz		30.8		dB
	6 GHz		28.3		dB
Input Return Loss	1 GHz		13		dB
	2 GHz		13		dB
	4 GHz		28		dB
	6 GHz		13		dB
Output Return Loss	1 GHz		12		dB
	2 GHz		14		dB
	4 GHz		16		dB
	6 GHz		17		dB
Second Harmonic Level (P <sub>IN</sub> =23 dBm)	1 GHz		-23		dBc
	2 GHz		-17		dBc
	4 GHz		-52		dBc
	6 GHz		-39		dBc
Third Harmonic Level (P <sub>IN</sub> =23 dBm)	1 GHz		-14		dBc
	2 GHz		-12		dBc
	4 GHz		-42		dBc
	6 GHz		-63		dBc
Third Order IM Distortion (P <sub>OUT</sub> /tone = 36 dBm)	1 GHz		-30		dBc
	2 GHz		-28		dBc
	4 GHz		-26		dBc
	6 GHz		-28		dBc
P <sub>OUT</sub> Temp. Coeff. (85 °C to -40 °C, P <sub>IN</sub> = 23 dBm)			-0.006		dB/°C
Sm. Sig. Gain Temp. Coefficient (85 °C to -40 °C)			-0.035		dB/°C
Gate Leakage Current (V <sub>D</sub> = +10 V, V <sub>G</sub> = -5.0 V)		-42			mA

Test conditions, unless otherwise noted: T = 25 °C, V<sub>D</sub> = 24 V, I<sub>DQ</sub> = 2044 mA

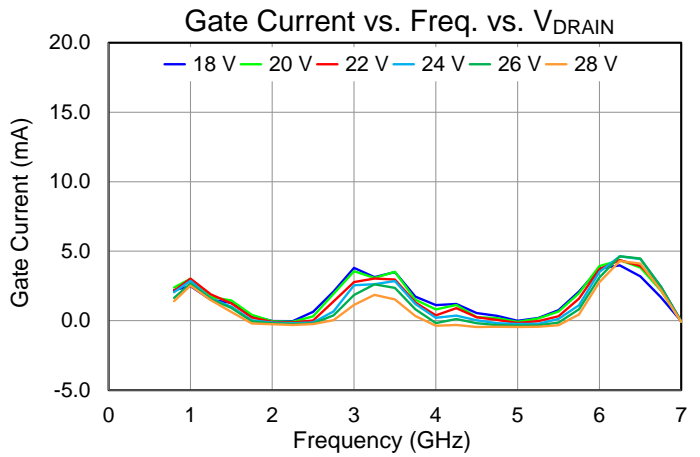
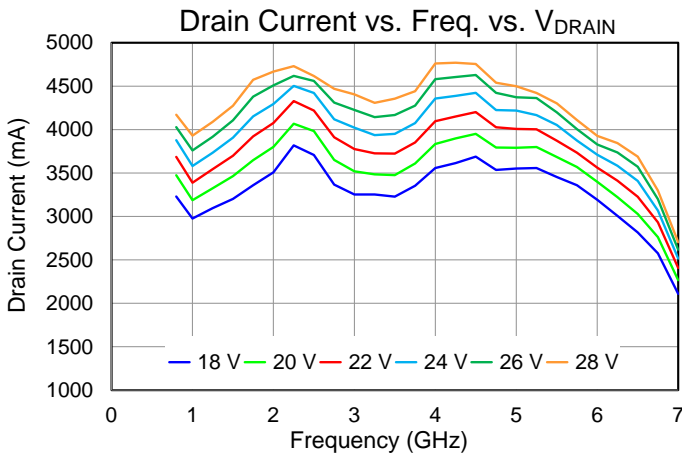
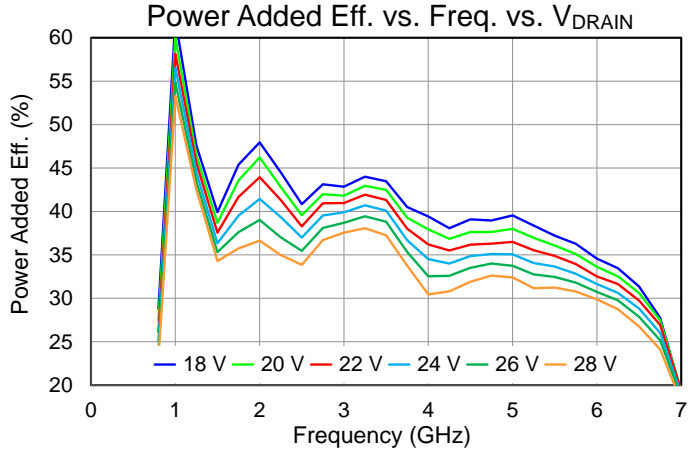
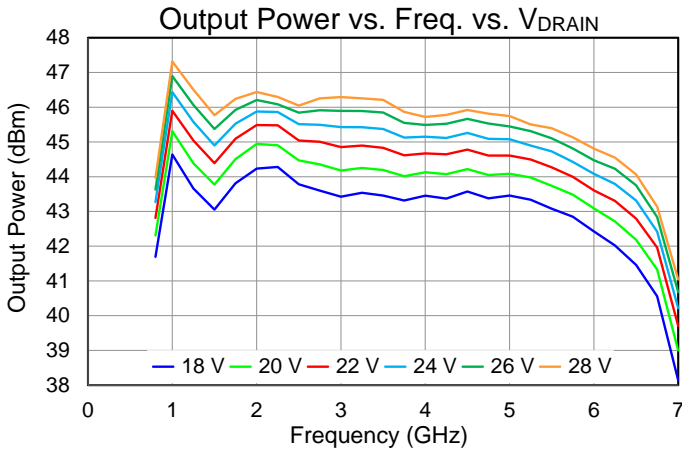
## Performance Plots – Large Signal

Test conditions, unless otherwise noted:  $V_D = 24\text{ V}$ ,  $I_{DQ} = 2044\text{ mA}$ ,  $T = +25\text{ }^\circ\text{C}$ ,  $P_{IN} = 23\text{ dBm}$ , CW



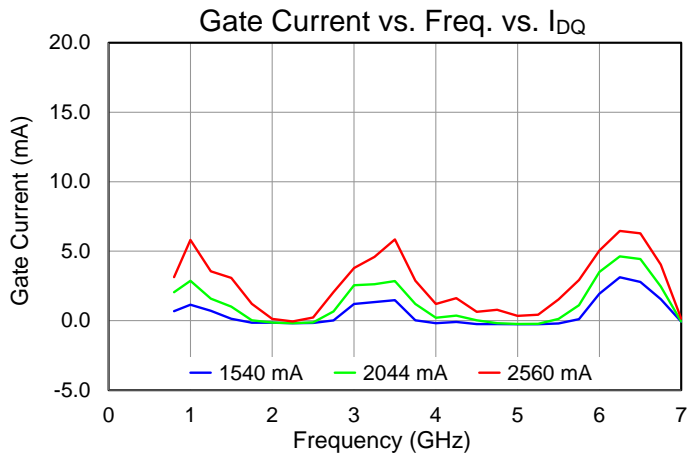
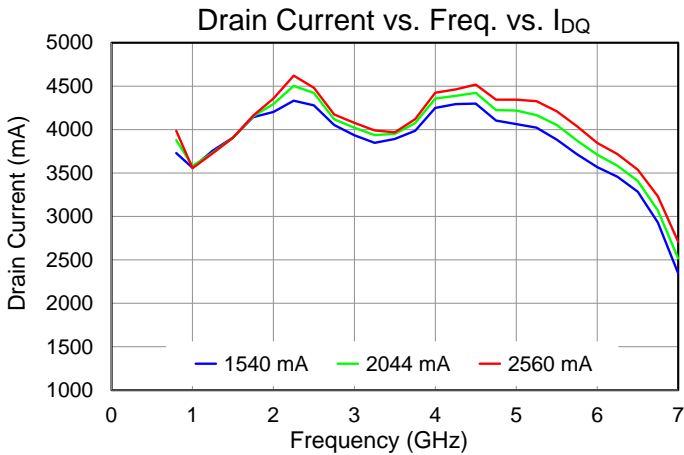
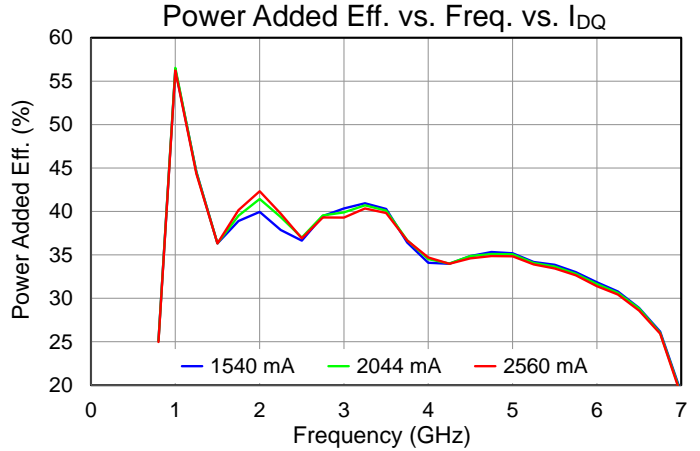
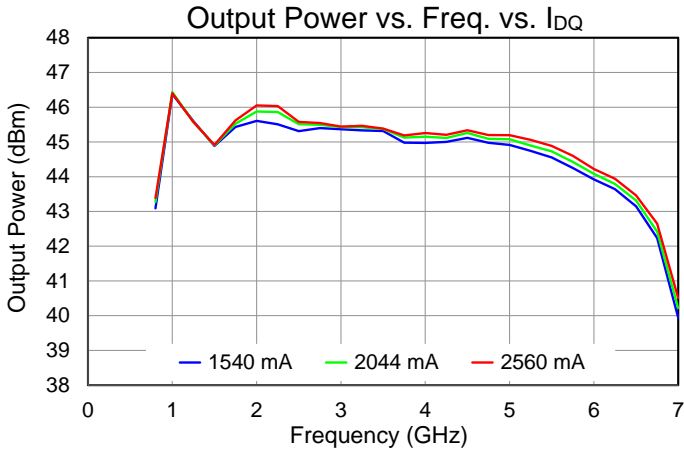
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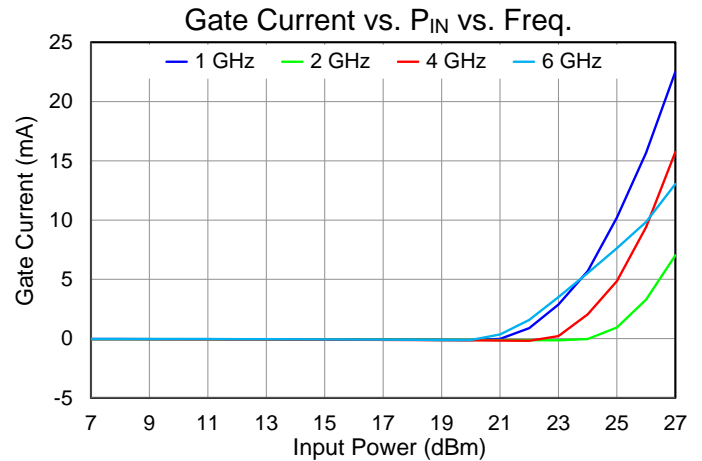
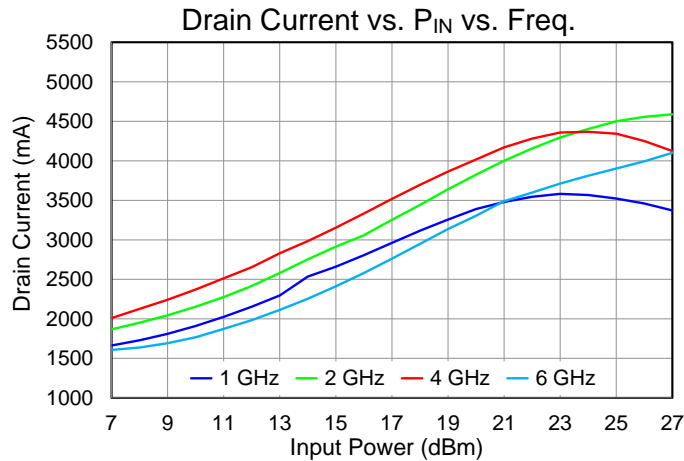
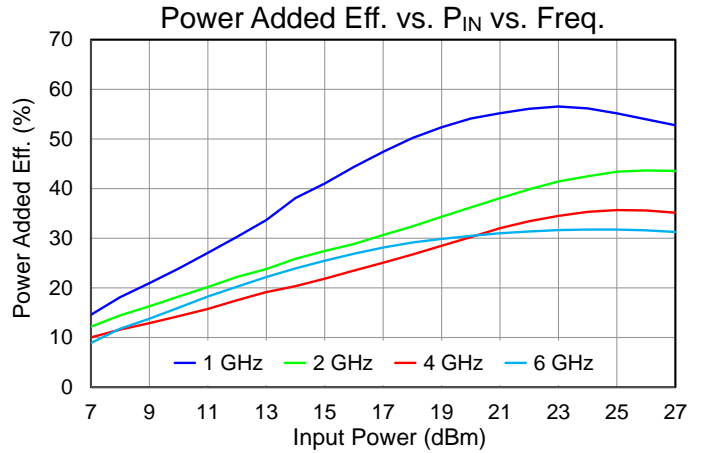
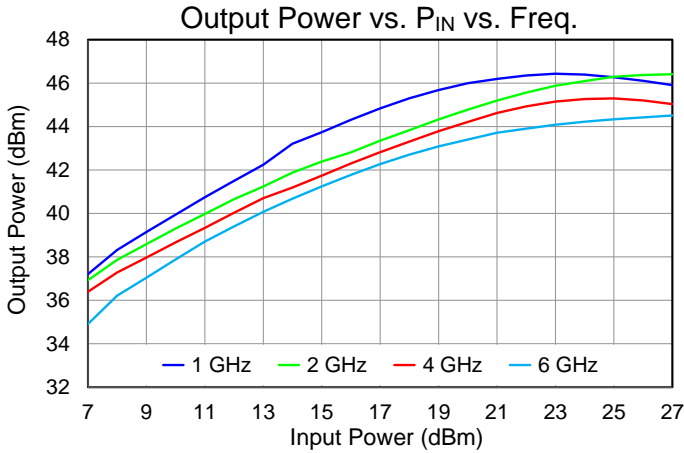
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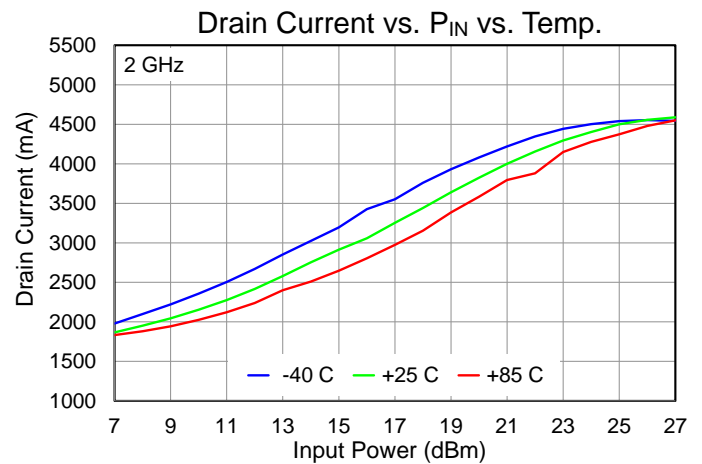
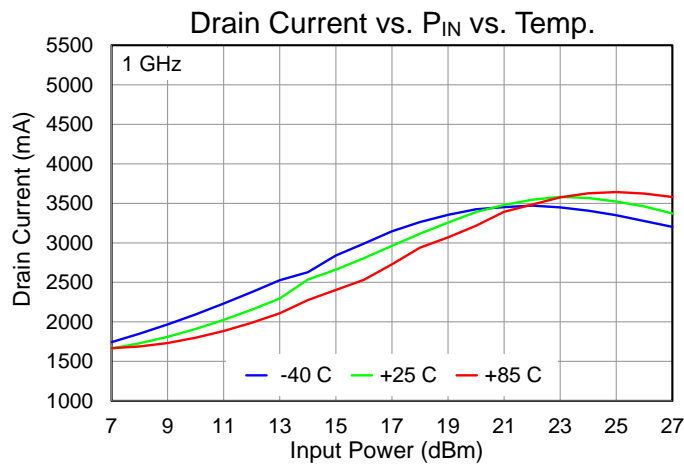
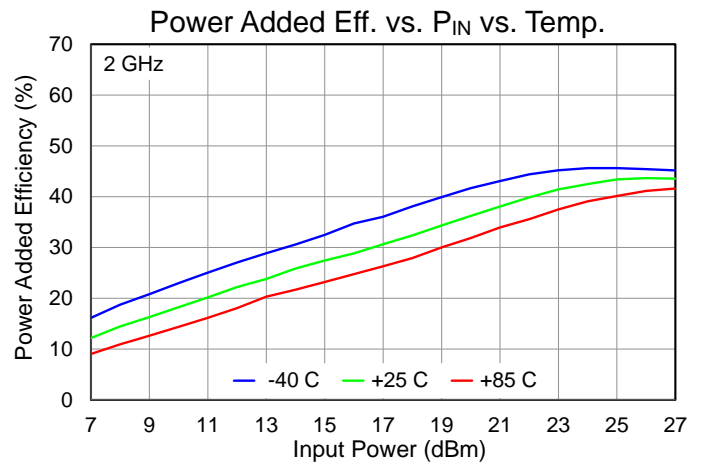
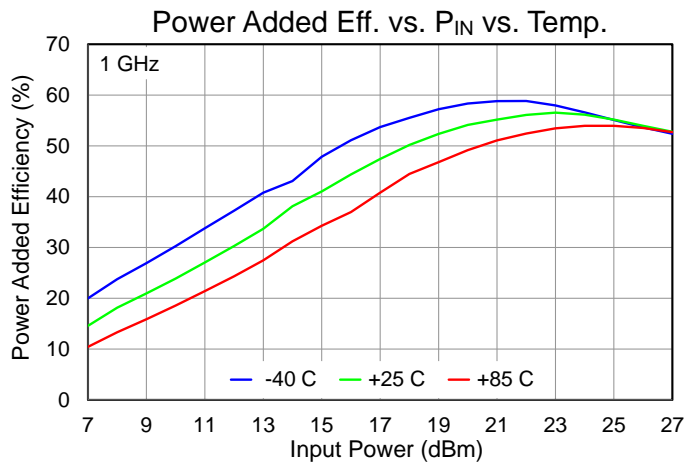
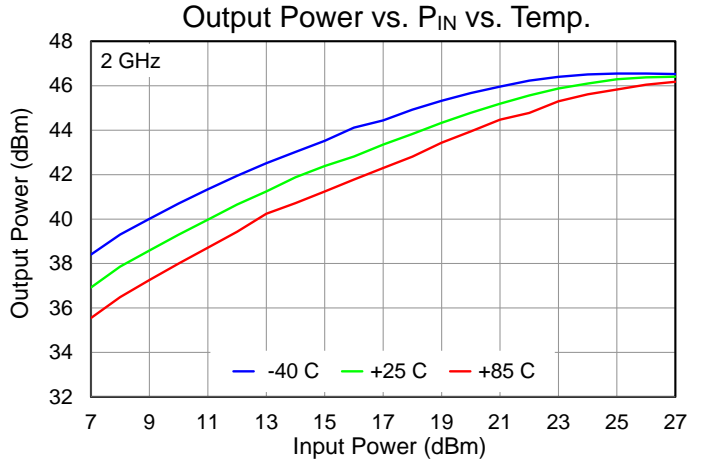
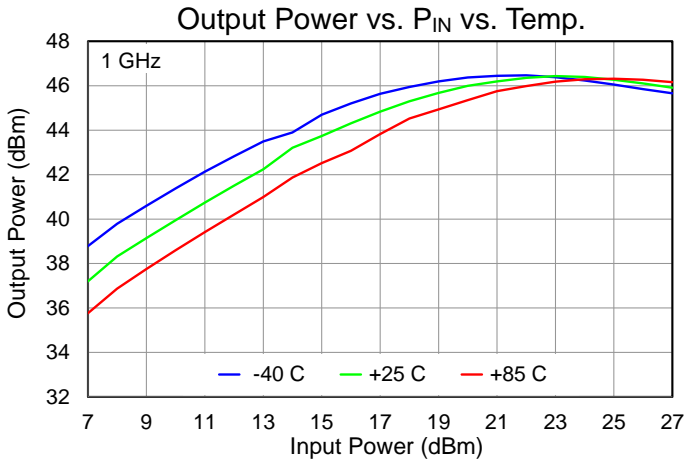
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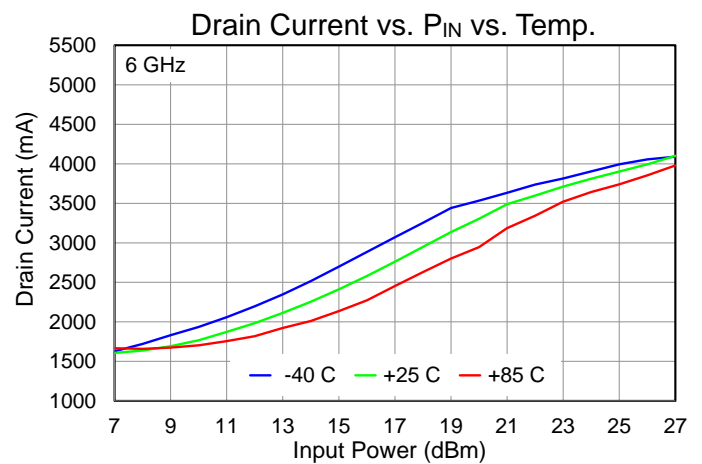
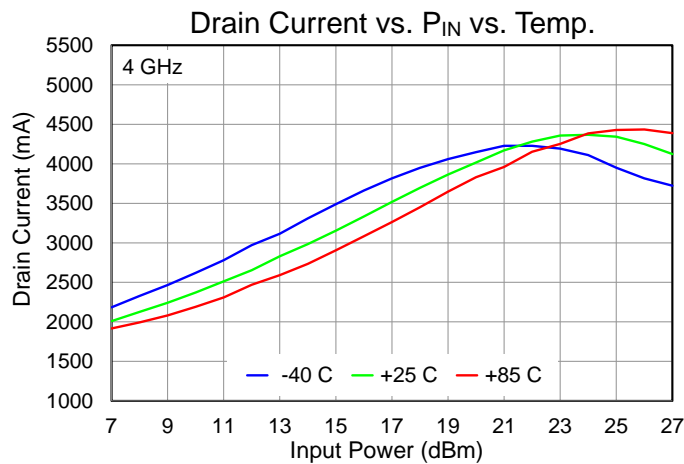
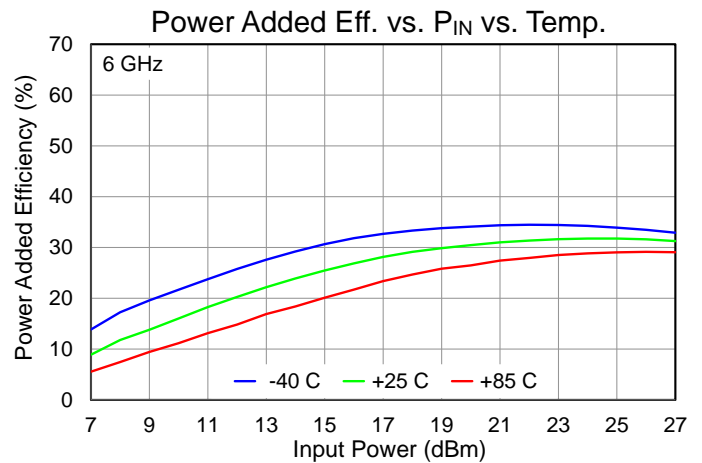
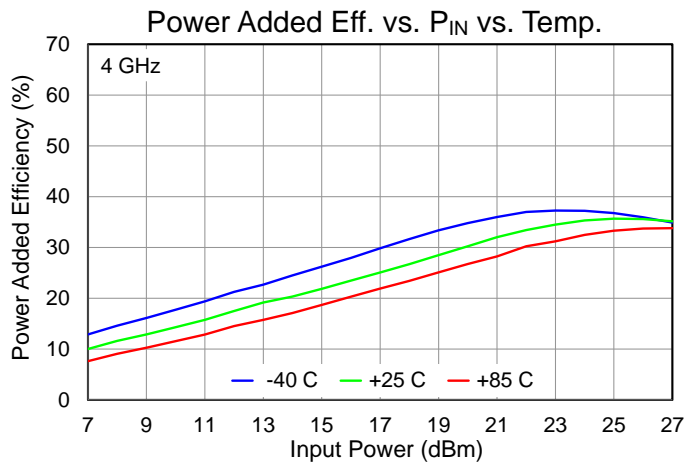
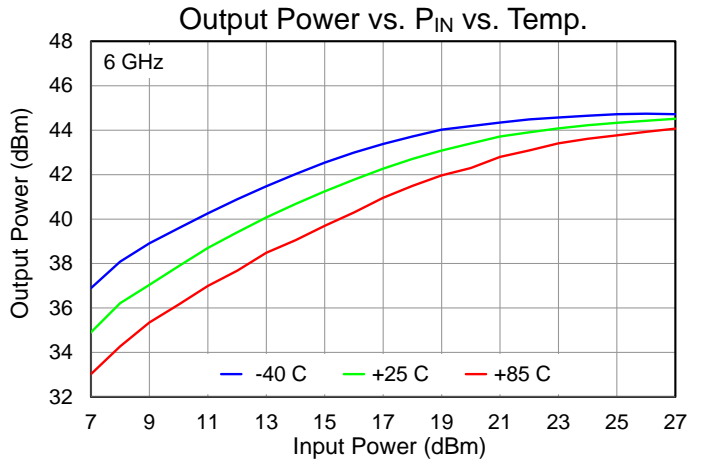
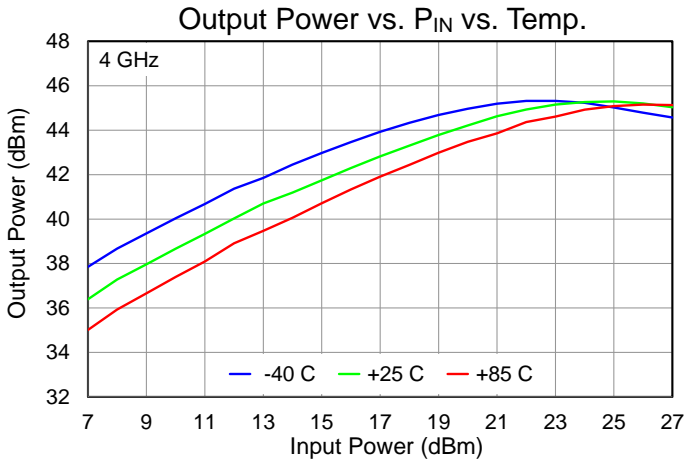
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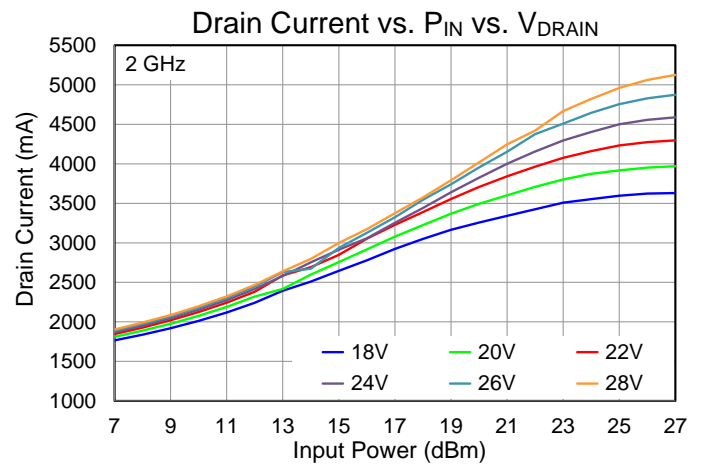
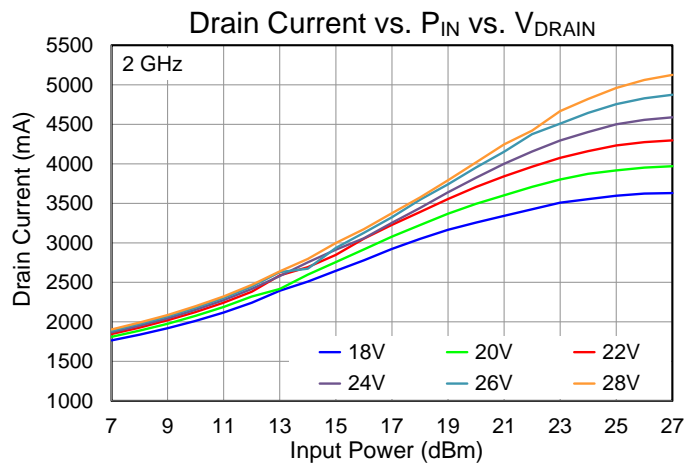
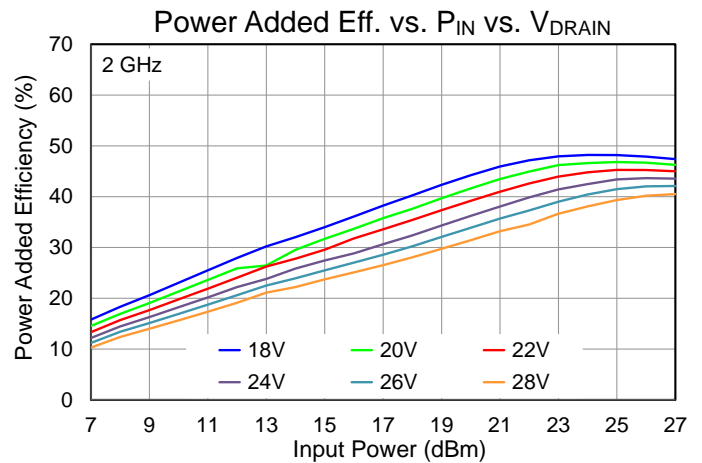
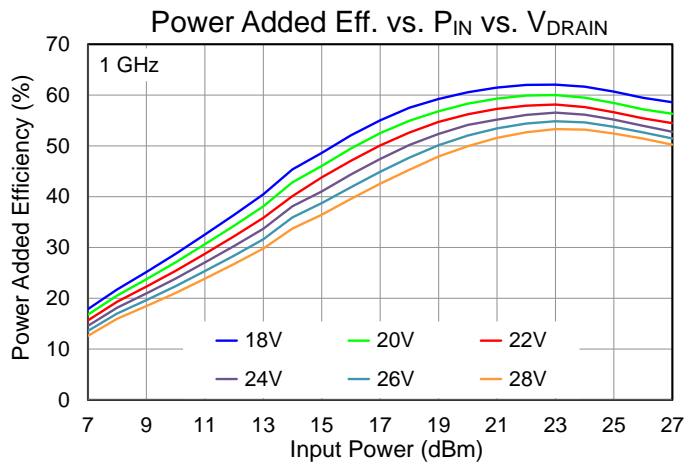
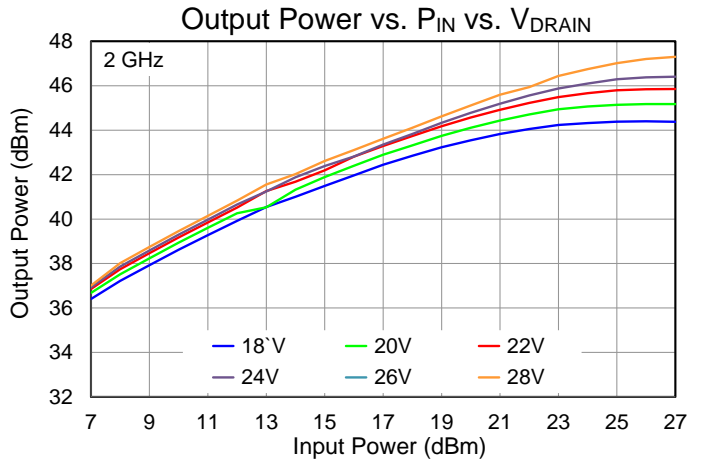
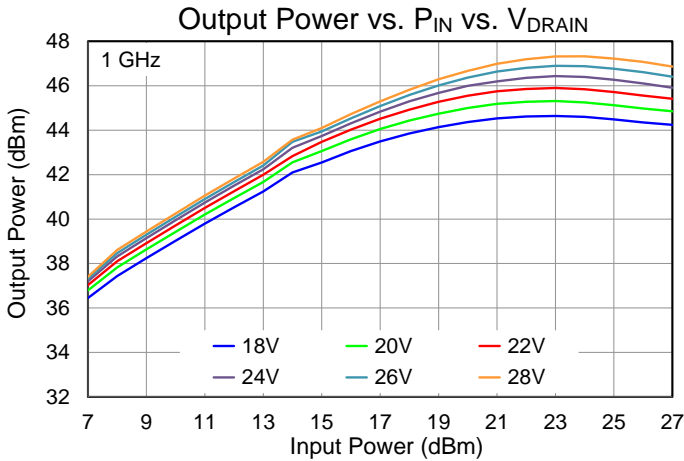
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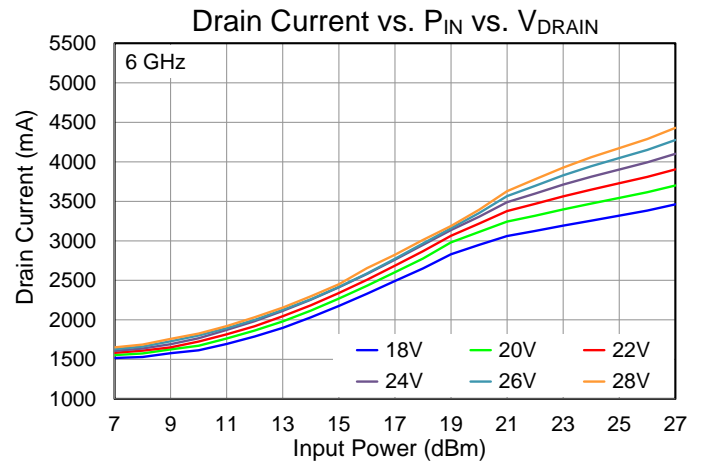
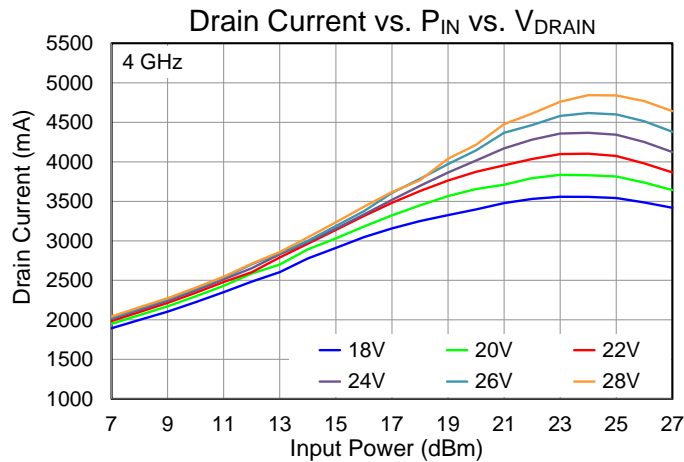
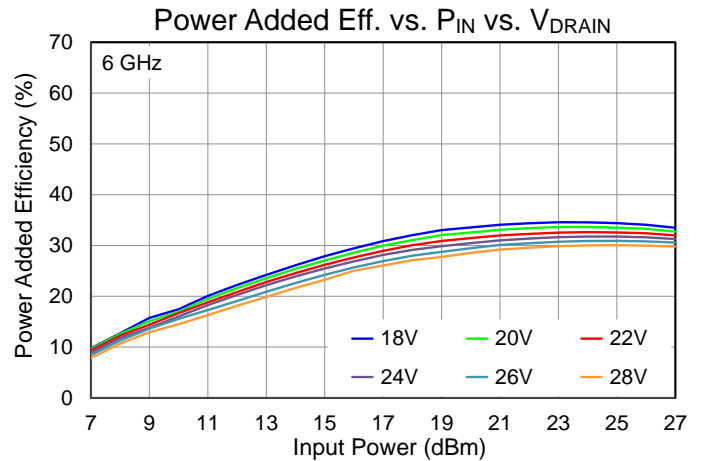
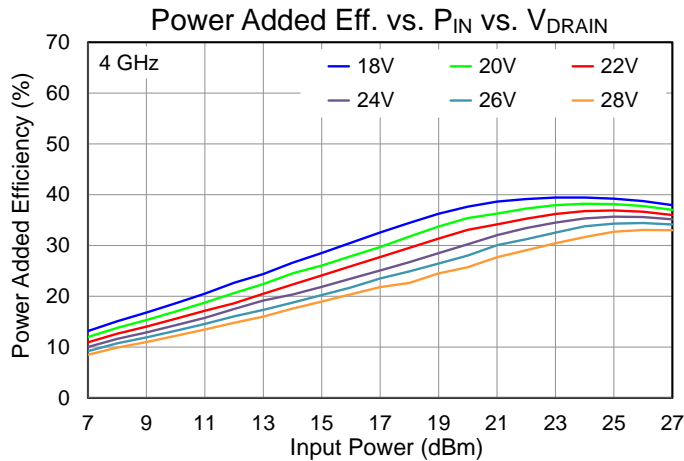
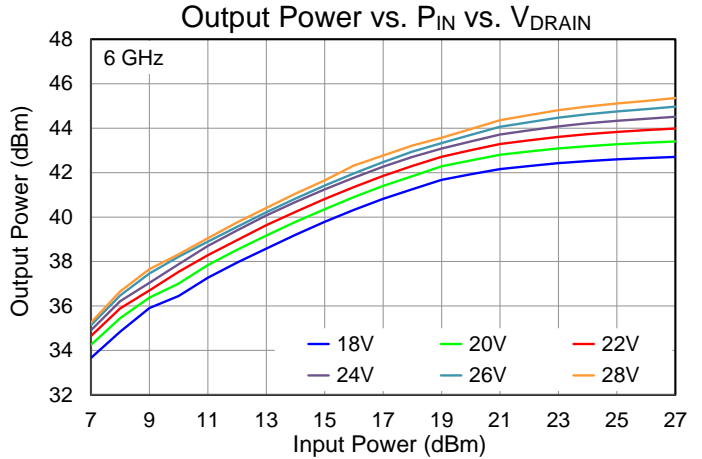
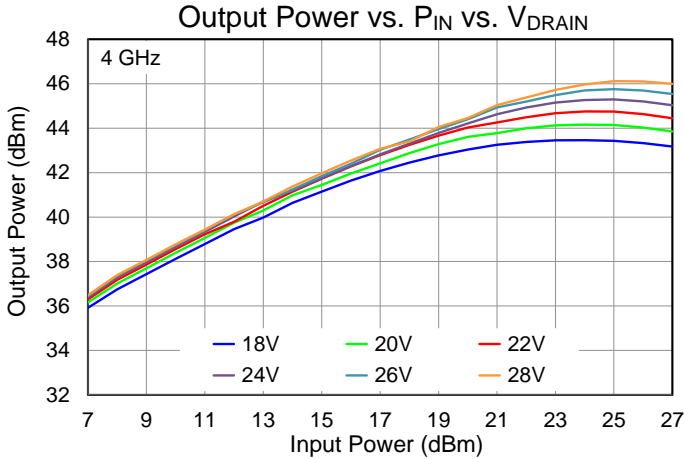
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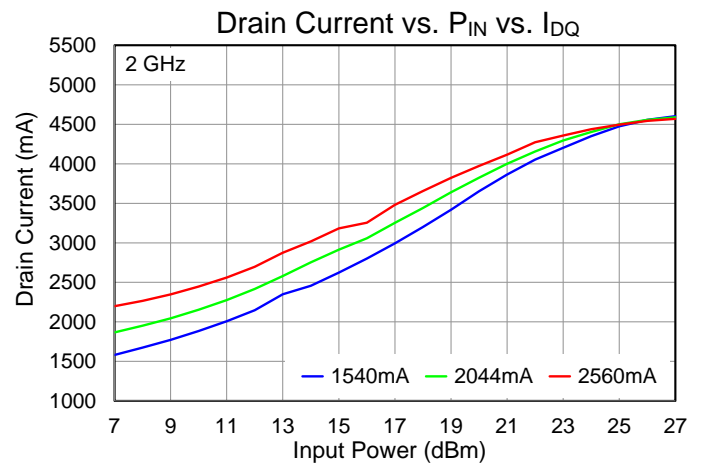
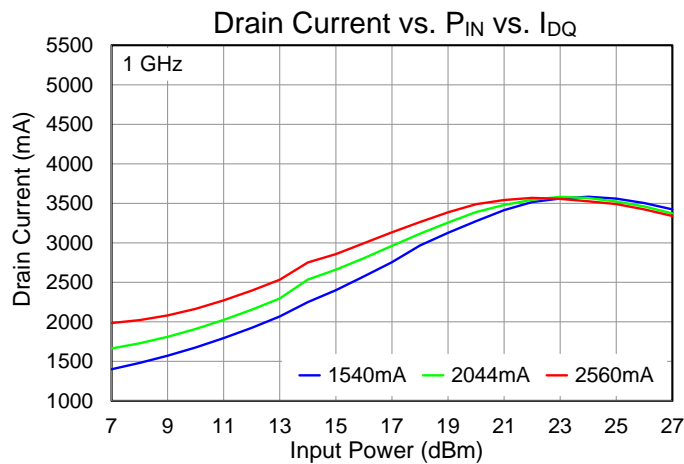
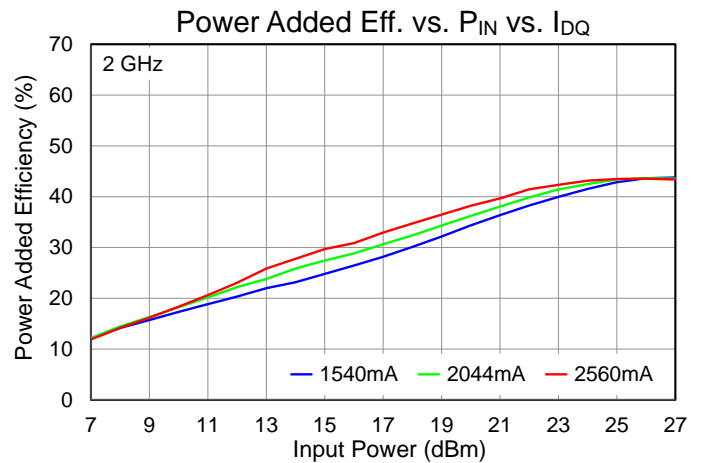
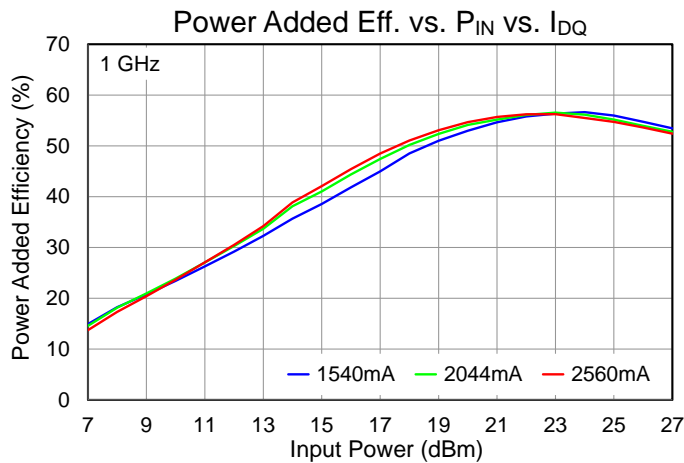
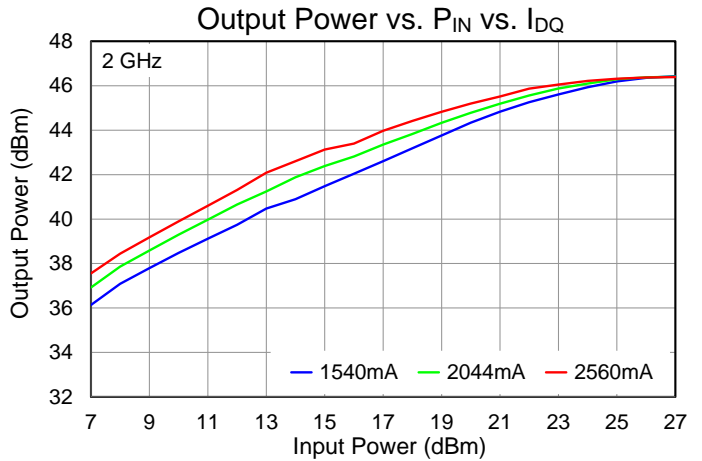
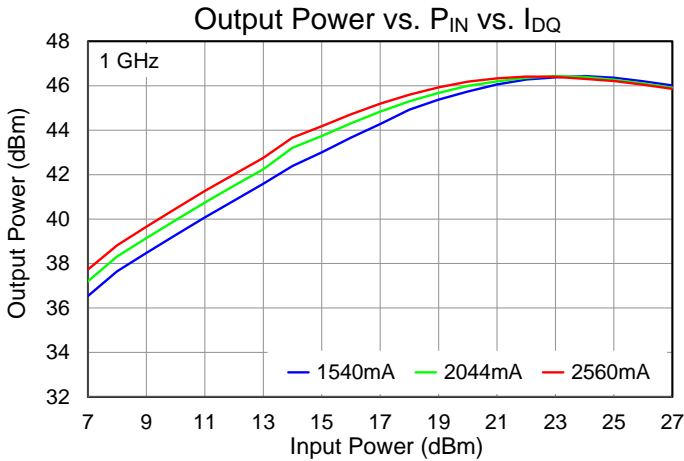
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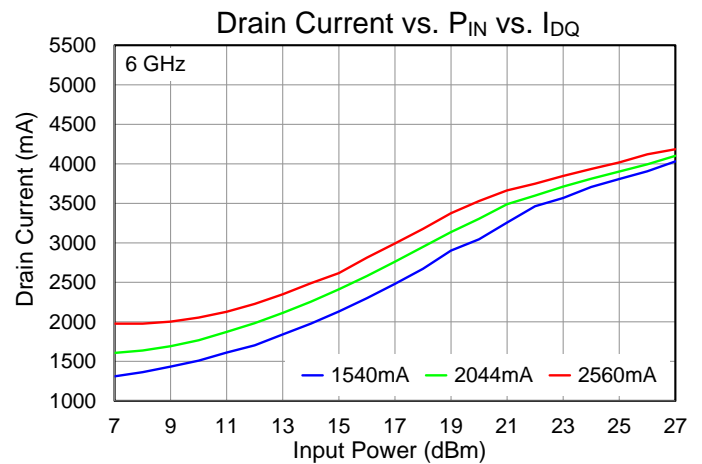
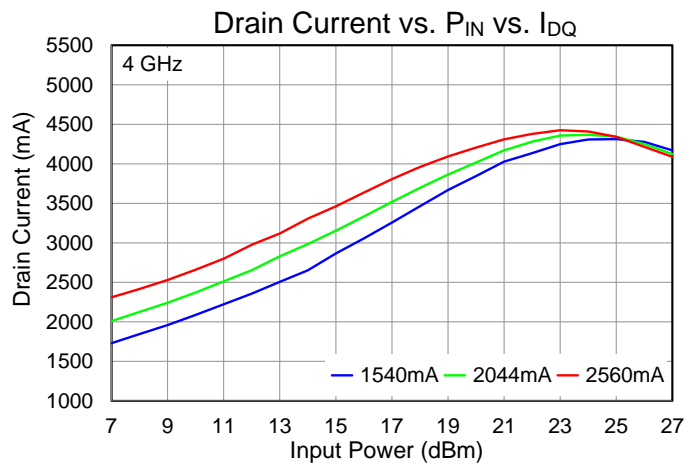
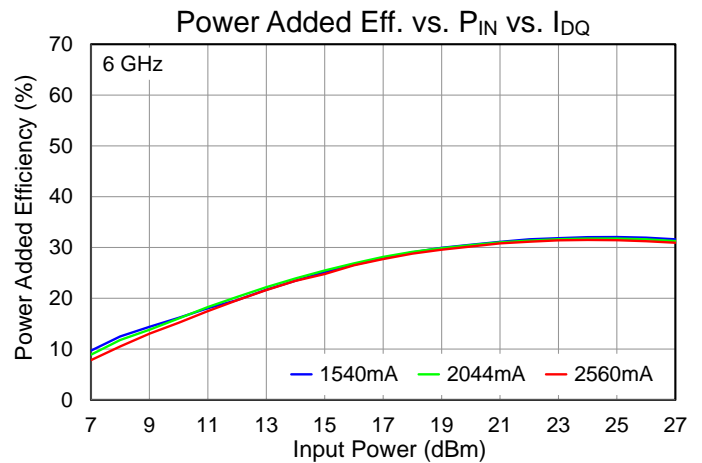
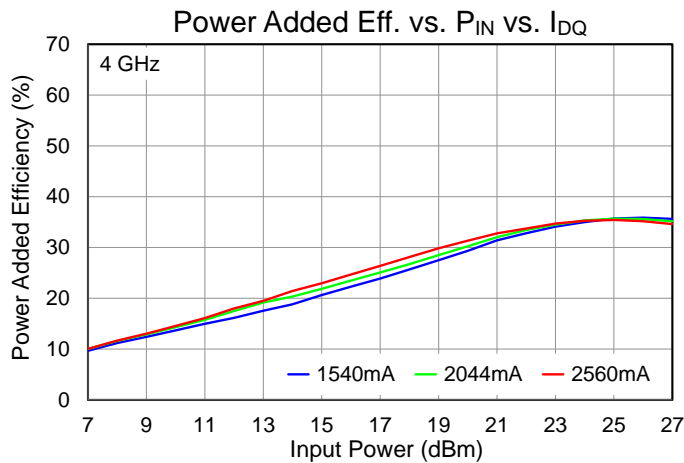
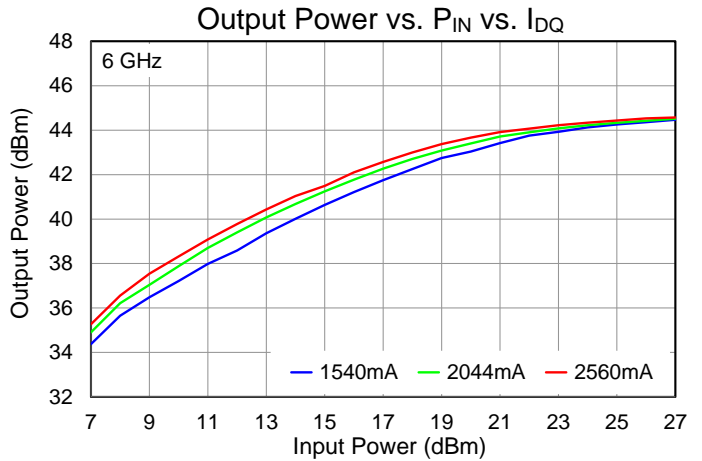
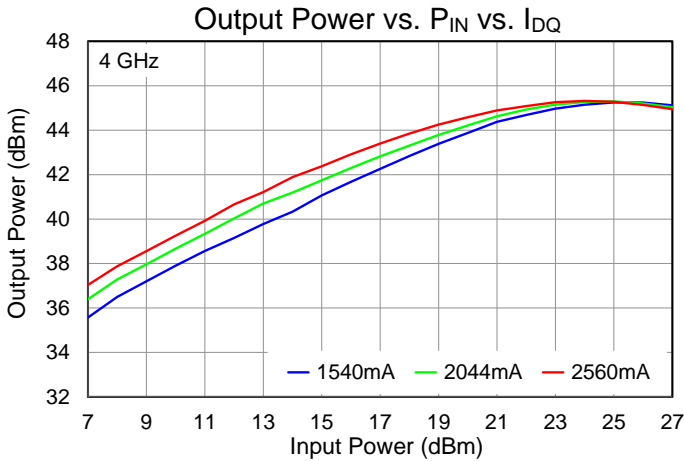
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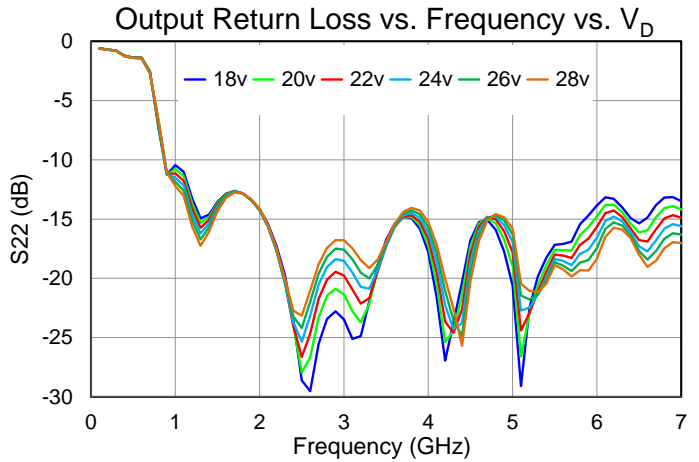
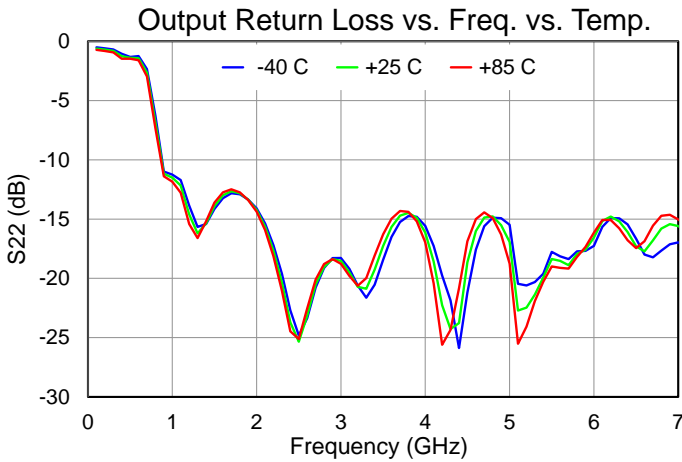
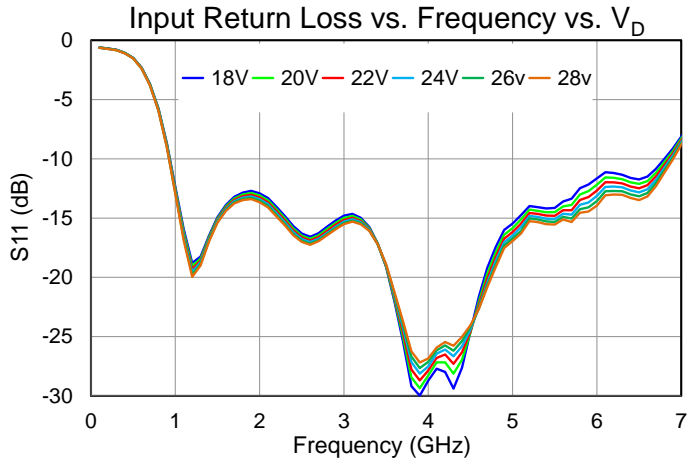
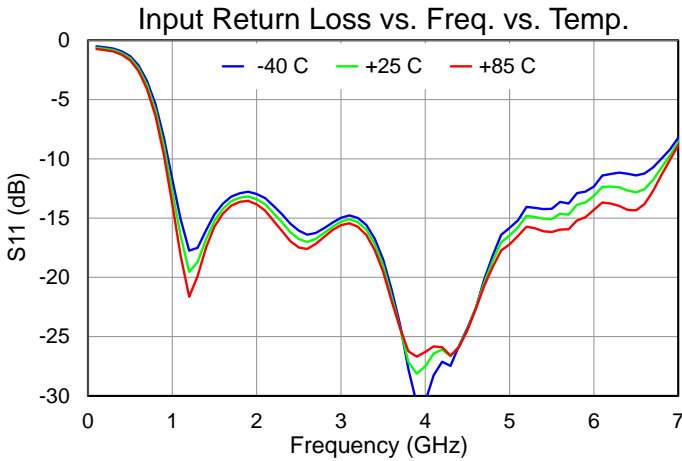
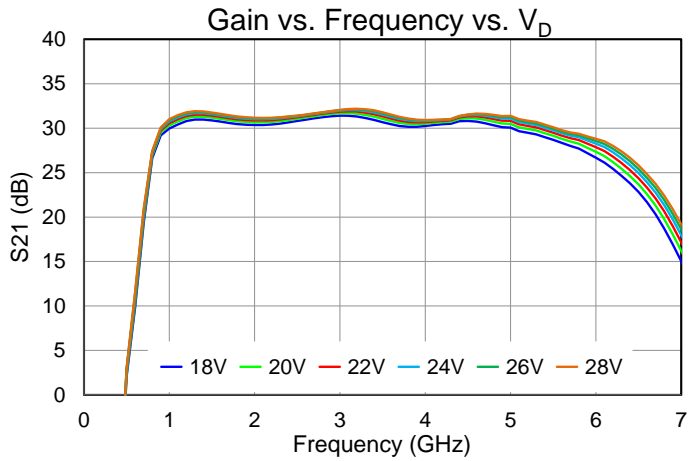
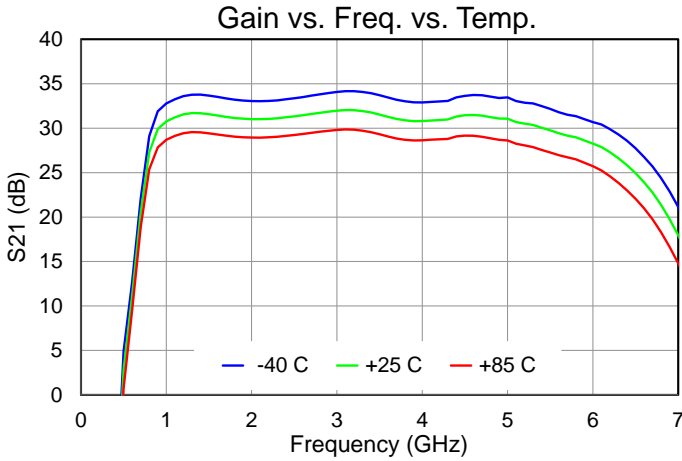
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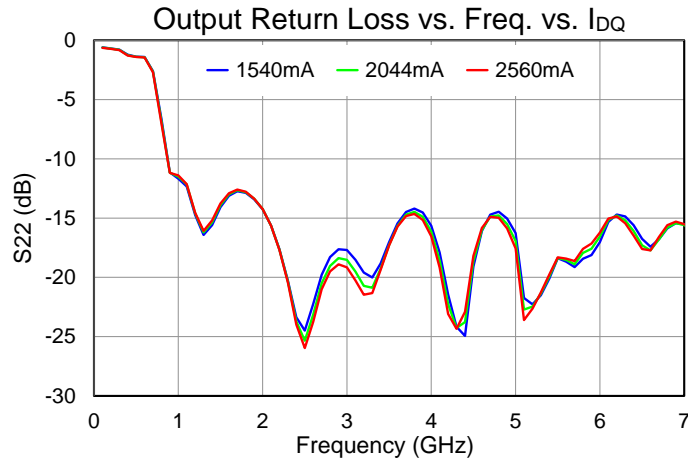
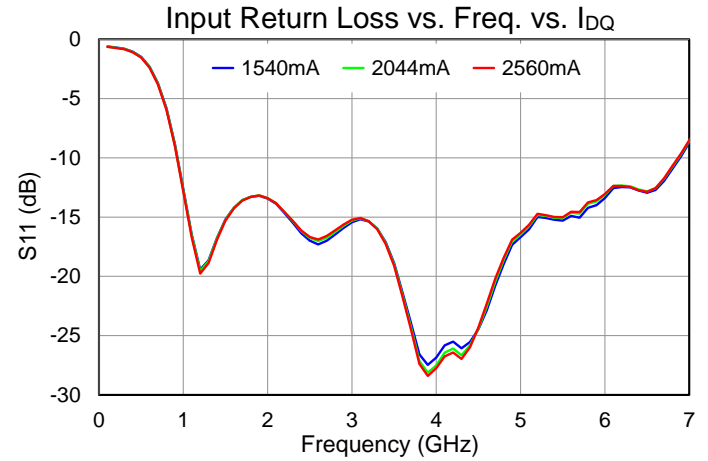
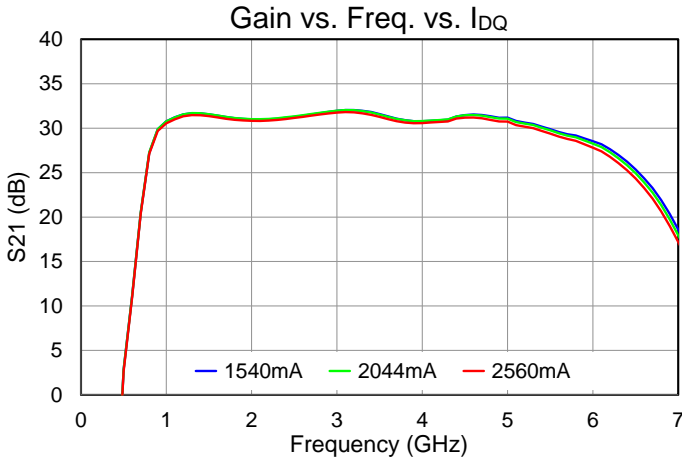
Performance Plots – Small Signal

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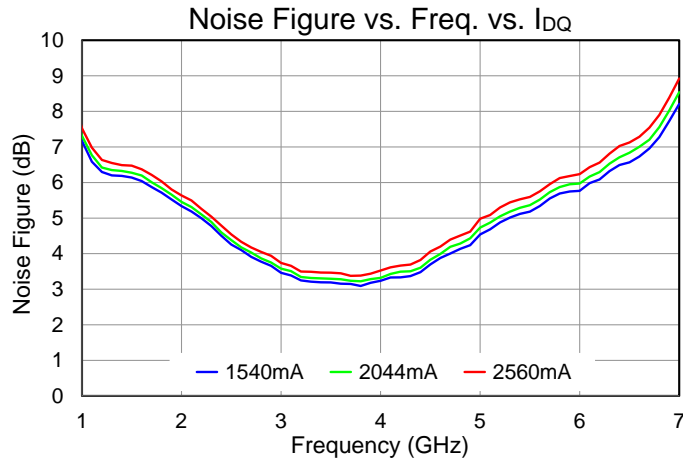
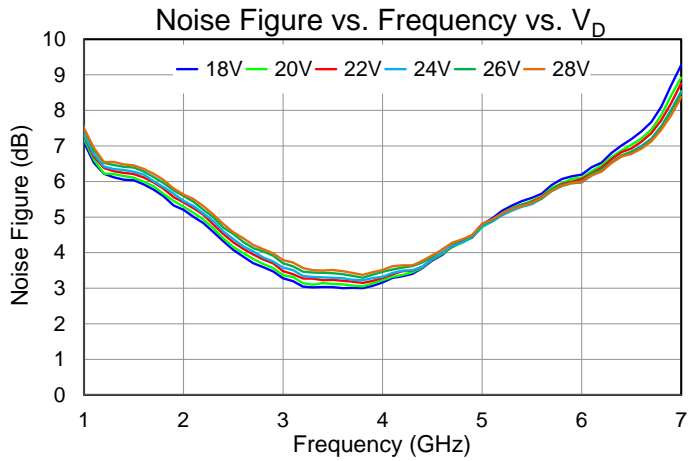
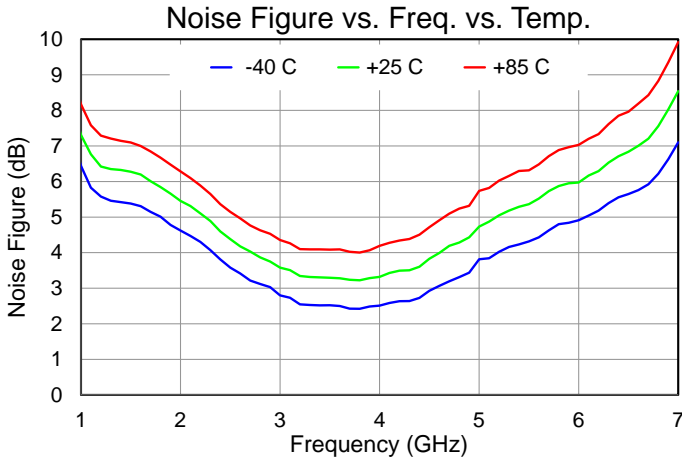
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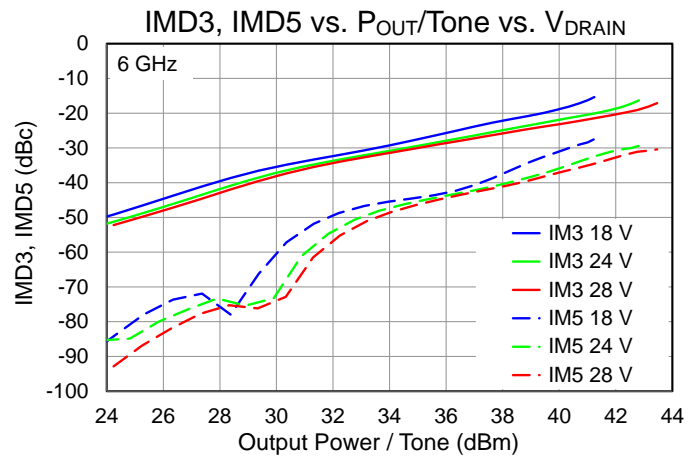
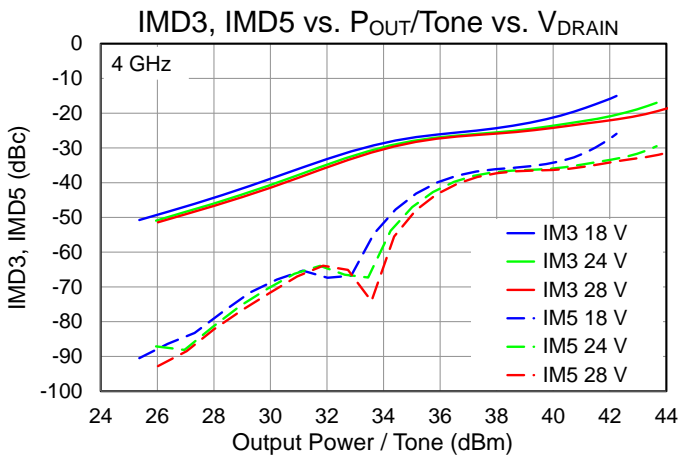
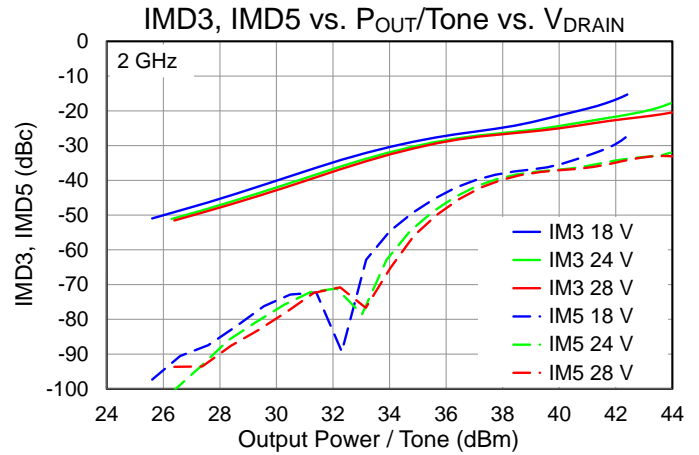
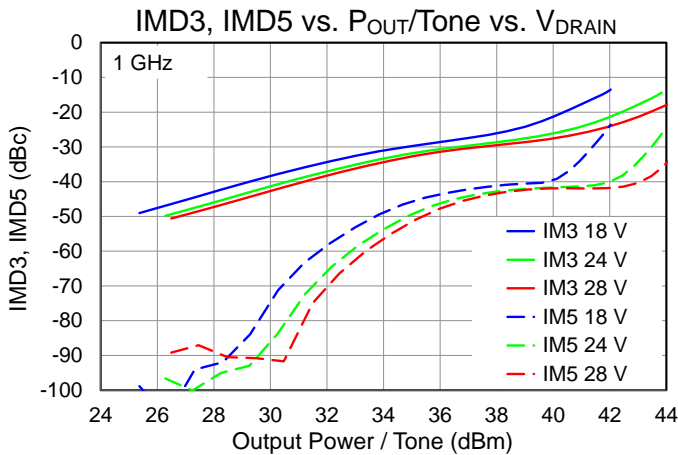
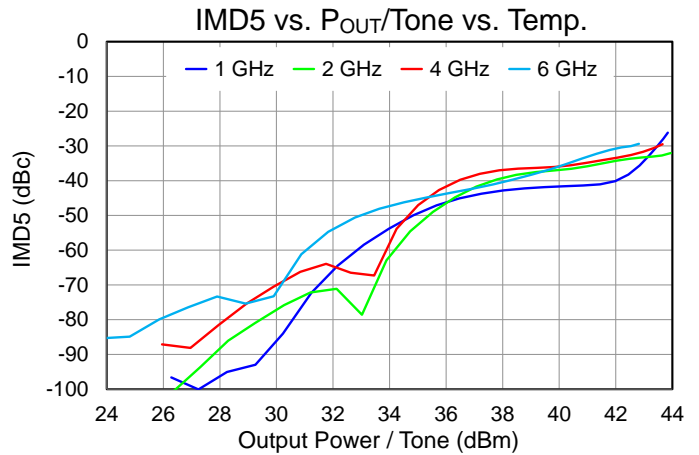
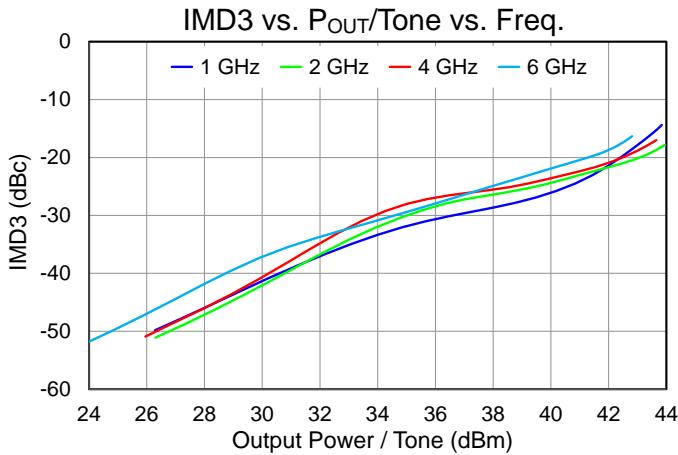
Performance Plots – Noise Figure

Test conditions, unless otherwise noted:  $V_D = 24\text{ V}$ ,  $I_{DQ} = 2044\text{ mA}$ ,  $T = +25\text{ }^\circ\text{C}$ , CW



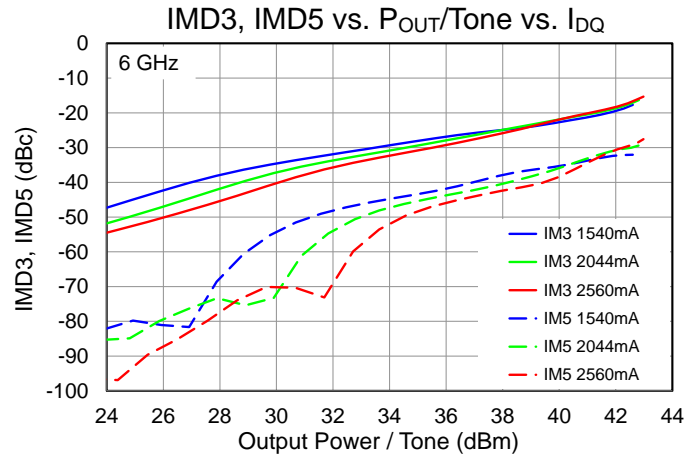
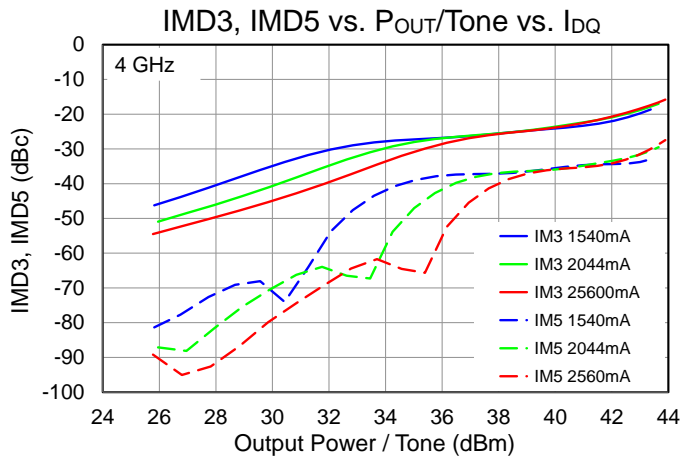
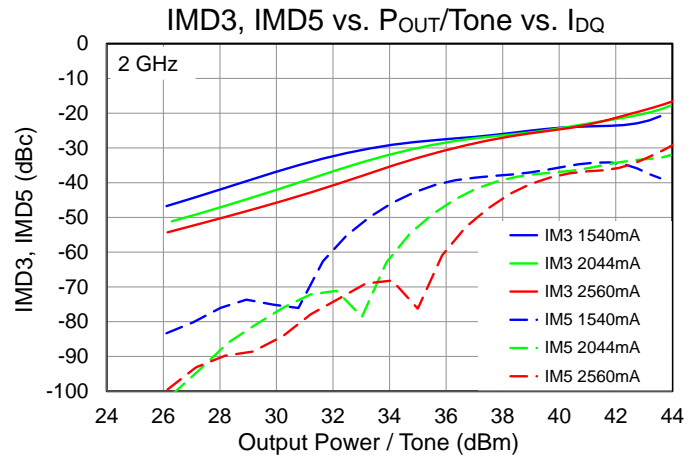
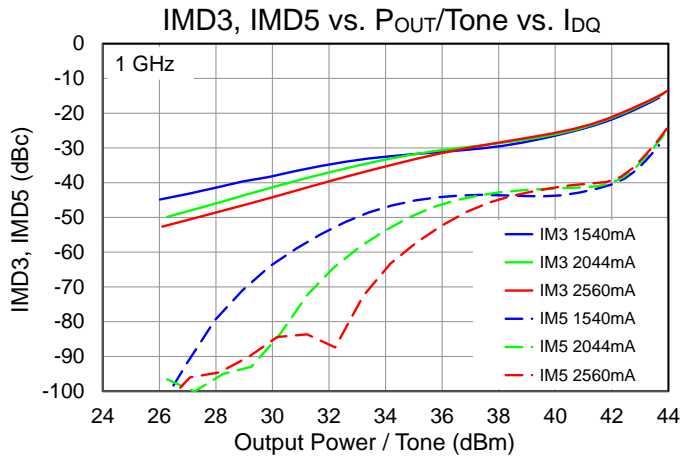
Performance Plots – Linearity

Test conditions, unless otherwise noted:  $V_D = 24\text{ V}$ ,  $I_{DQ} = 2044\text{ mA}$ ,  $T = +25\text{ }^\circ\text{C}$ , CW, Tone Spacing = 10 MHz



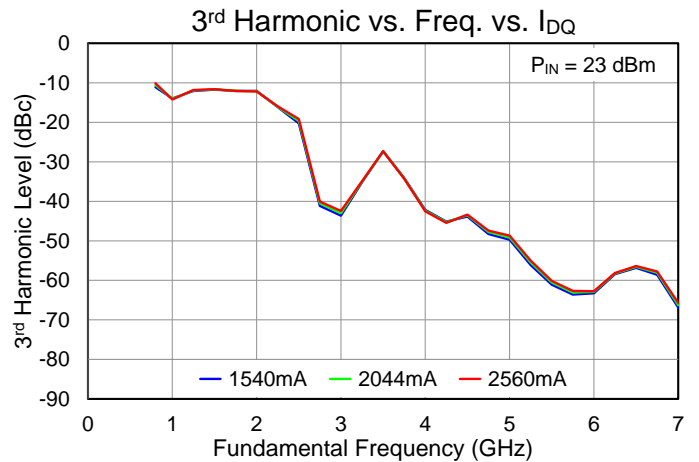
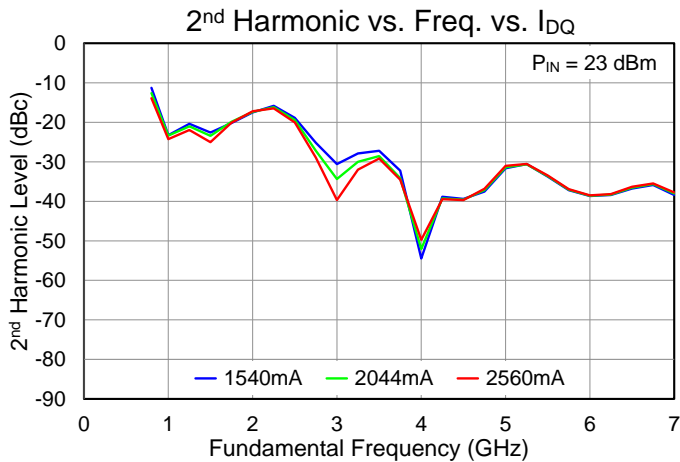
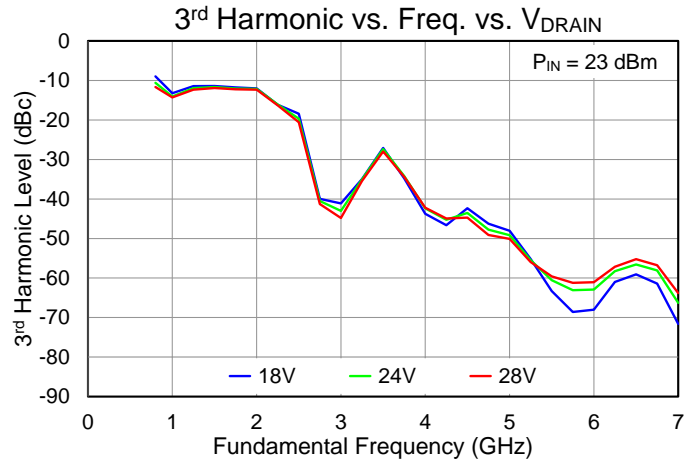
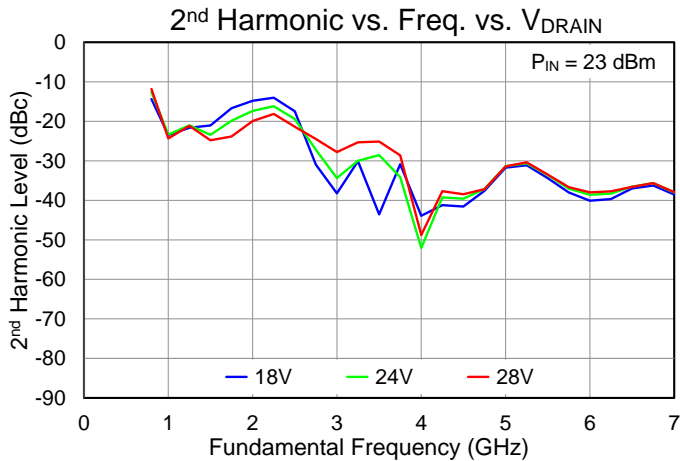
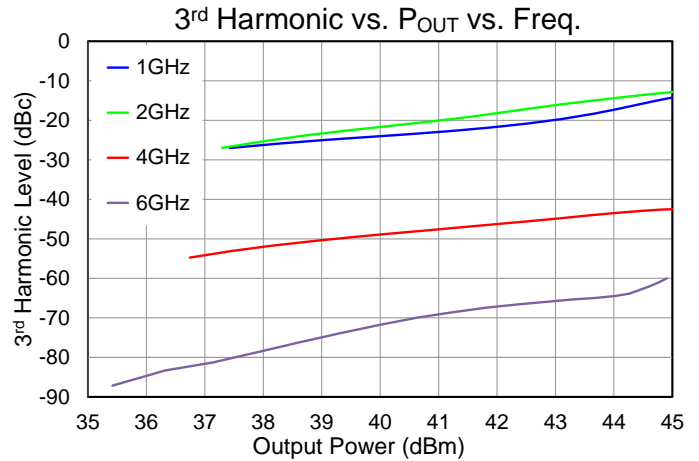
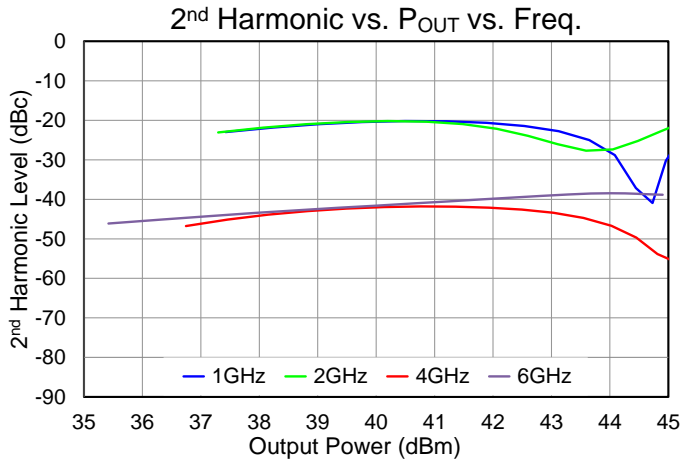
## Performance Plots – Linearity

Test conditions, unless otherwise noted:  $V_D = 24\text{ V}$ ,  $I_{DQ} = 2044\text{ mA}$ ,  $T = +25\text{ }^\circ\text{C}$ , CW, Tone Spacing = 10 MHz



Performance Plots – Harmonics

Test conditions, unless otherwise noted:  $V_D = 24\text{ V}$ ,  $I_{DQ} = 2044\text{ mA}$ ,  $T = +25\text{ }^\circ\text{C}$ ,  $P_{IN} = 23\text{ dBm}$ , CW



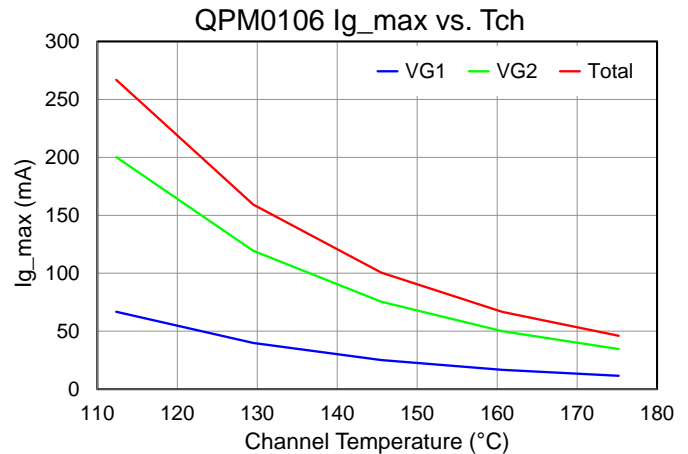
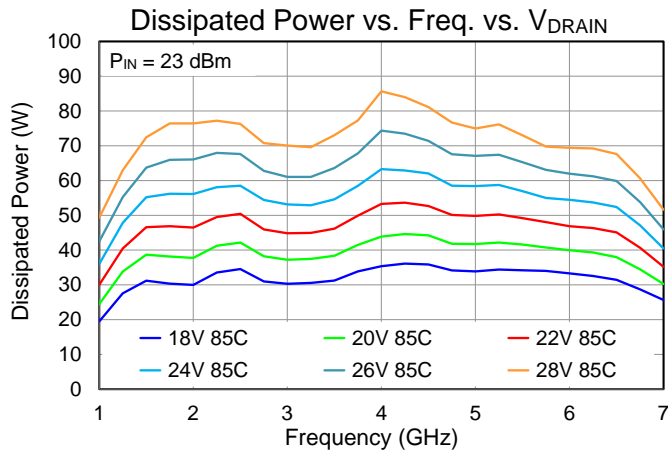
## Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{base} = 85\text{ }^{\circ}\text{C}$ , $V_D = 24\text{ V}$ , $I_{DQ} = 2044\text{ mA}$ , $P_{DISS} = 49.056\text{ W}$ (Quiescent; no RF drive)	1.692	$^{\circ}\text{C/W}$
Channel Temperature, $T_{CH}$ (Quiescent) <sup>(2)</sup>		168.0	$^{\circ}\text{C}$
Thermal Resistance ( $\theta_{JC}$ ) <sup>(1)</sup>	$T_{base} = 85\text{ }^{\circ}\text{C}$ , $V_D = 24\text{ V}$ , $I_{DQ} = 2044\text{ mA}$ , Freq = 4.0 GHz, $I_{D\_Drive} = 2088\text{ mA}$ , $P_{IN} = 23\text{ dBm}$ , $P_{OUT} = 44.61\text{ dBm}$ , $P_{DISS} = 63.27\text{ W}$	0.735	$^{\circ}\text{C/W}$
Channel Temperature, $T_{CH}$ (w/ RF drive) <sup>(2)</sup>		131.5	$^{\circ}\text{C}$

**Notes:**

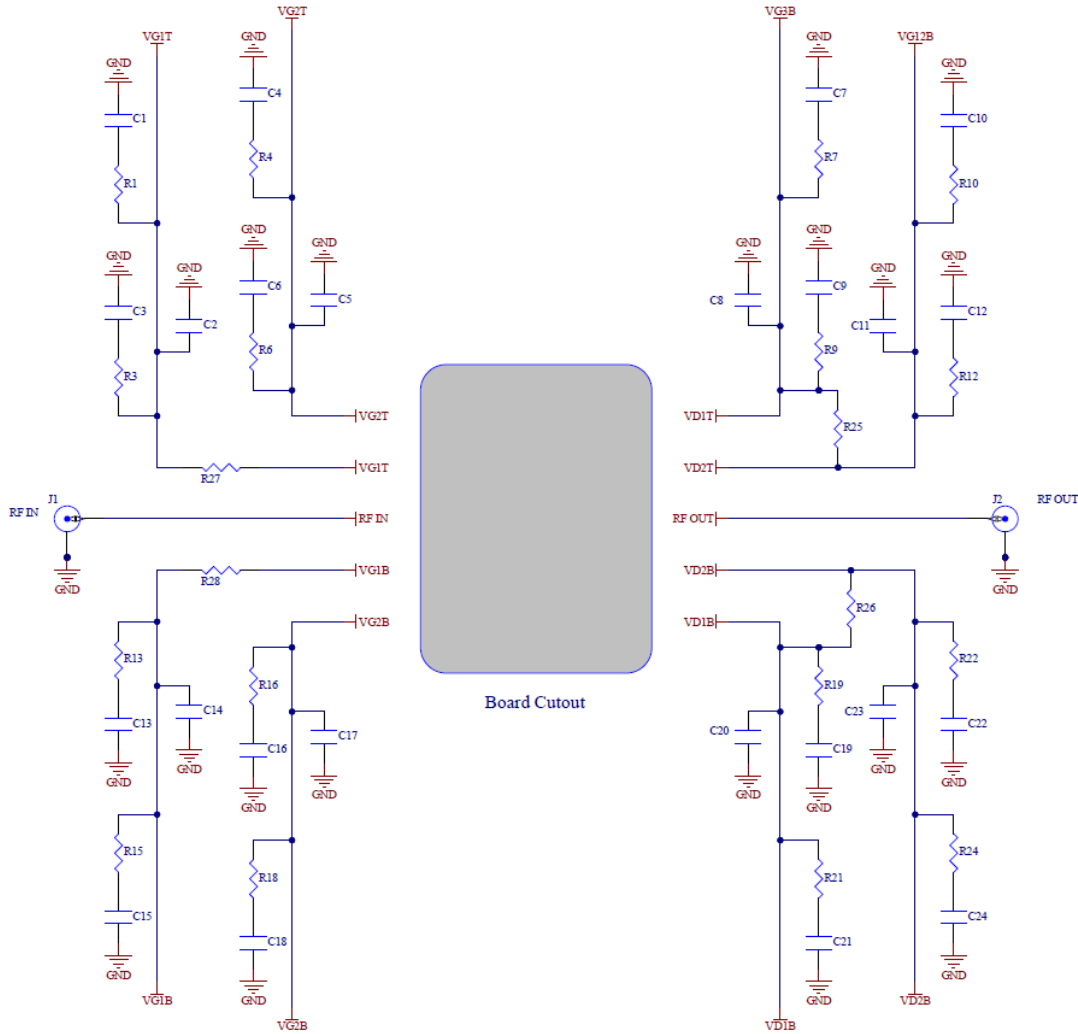
1. Thermal resistance determined to the back of package,  $T_{base}$  (85  $^{\circ}\text{C}$ )
2.  $T_{CH}$  values are IR Scan equivalent temperatures. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

## Dissipated Power and Maximum Gate Current



Test conditions, unless otherwise noted:  $V_D = 22\text{ V}$ ,  $I_{DQ} = 1022\text{ mA}$ ,  $T = +25\text{ }^{\circ}\text{C}$ ,  $P_{IN} = 19\text{ dBm}$

Applications Information



VG1 and VG2, top and bottom, may be tied together.  
VD1 and VD2, top and bottom, should be tied together.

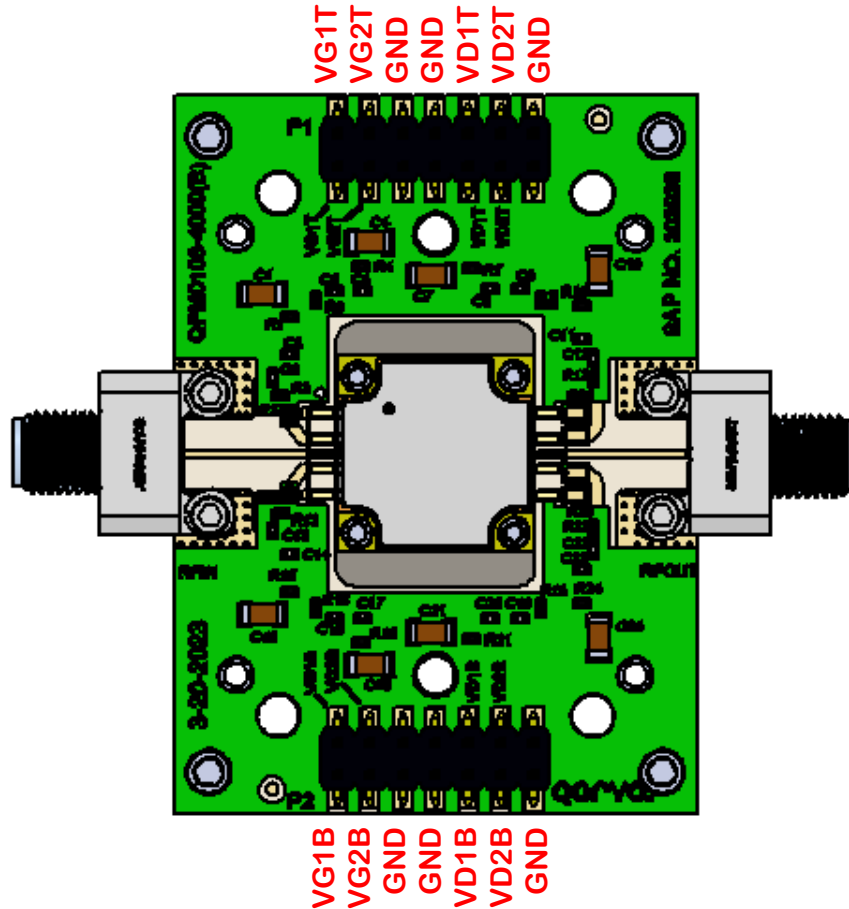
Bias-Up Procedure

- Turn on  $V_G$  supply and set  $V_G = -4V$ ,  $I_G$  limit to 60 mA
- Turn on  $V_D$  supply and set  $V_D = 0V$ ,  $I_D$  limit to 5.0 A
- Adjust  $V_D$  to 24 V
- Adjust  $V_G$  to obtain desired  $I_{DQ}$  (2044 mA)

Bias-Down Procedure

- Set  $V_G = -4 V$
- Set  $V_D = 0 V$
- Turn off  $V_D$  Supply
- Turn off  $V_G$  Supply

Evaluation Board (EVB) Layout Assembly



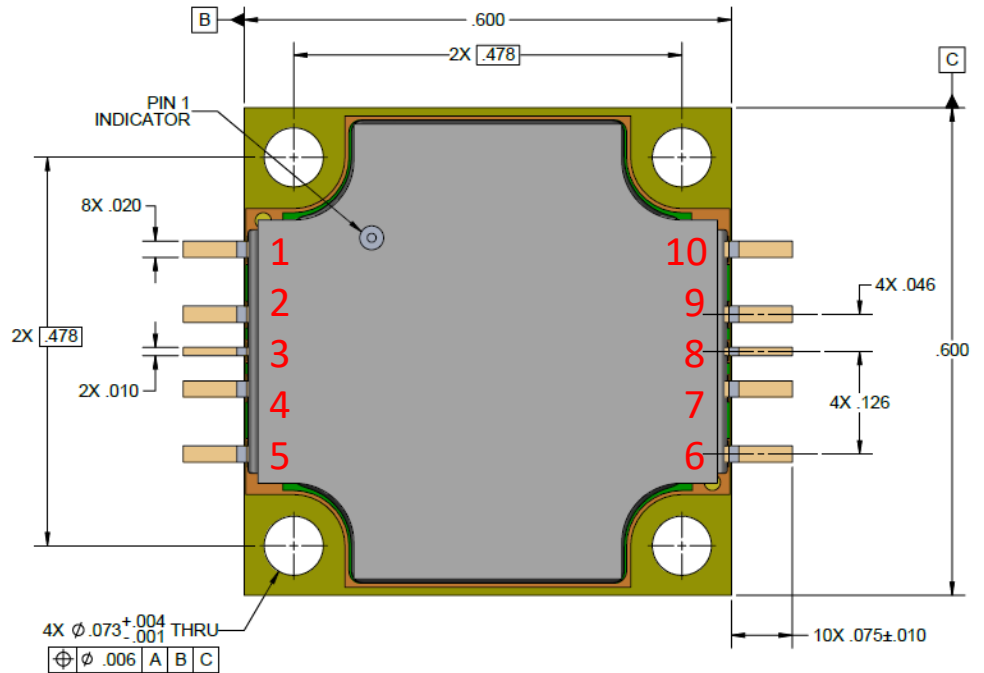
Copper layers are 0.5 oz. both sides.

VG1 and VG2, top and bottom, may be tied together or VG1 and VG2 may be biased separately.  
VD1 and VD2, top and bottom, should be tied together.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part No.
C3,C6,C9,C12,C13,C16,C19,C22	100 pF	CAP, 100pF, 10%, 50V, STD, 0402		
C2,C5,C8,C11,C14,C17,C20,C23	0.01 uF	CAP, 0.01uF, 10%, 50V, X7R, 0402		
C1,C4,C7,C10,C15,C18,C21,C24	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206		
R1,R4,R7,R10	5.1 Ω	RES, 5.1 OHM, 5%, 50V, 0402		
R3,R6,R9,R12,R13,R15,R16,R18,R19,R21,R22,R24	0 Ω	RES, 0 OHM, 5%, 1/10W, 0402		
R27,R28	20 Ω	RES, 20 OHM, 5%, 1/10W, 0402		
J1, J2	2.92 mm	CONN, 2.92, END, F, PIN .007, DIEL .048	Southwest Microwave	1092-04A-12

## Mechanical Information



TOLERANCES  
 XX = ± .01  
 XXX = ± .005  
 .XXXX = ± .0010

**NOTES:**

1. MATERIALS:  
 PACKAGE BASE: COPPER  
 LEADS: ALLOY 194  
 FINISH: PACKAGE EXPOSED METALLIZATION IS GOLD PLATED  
 LID: LAMINATE
2. PART IS EPOXY SEALED.



Dimensions are in inches

## Bond Pad Description

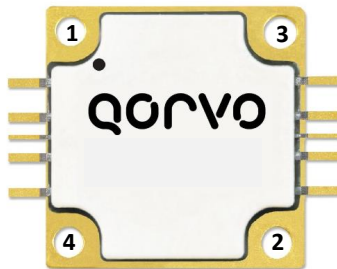
Pad No.	Symbol	Description
1	VG1T	VG1 Top. Bias network is required; see Application Circuit on page 22
2	VG2T	VG2 Top. Bias network is required; see Application Circuit on page 22
3	RF IN	RF input. 50 Ohms. DC blocked
4	VG1B	VG1 Bottom. Bias network is required; see Application Circuit on page 22
5	VG2B	VG2 Bottom. Bias network is required; see Application Circuit on page 22
6	VD1B	VD1 Bottom. Bias network is required; see Application Circuit on page 22
7	VD2B	VD2 Bottom. Bias network is required; see Application Circuit on page 22
8	RF OUT	RF output. 50 Ohms. DC blocked
9	VD2T	VD2 Top. Bias network is required; see Application Circuit on page 22
10	VD1T	VD1 Top. Bias network is required; see Application Circuit on page 22

Assembly Notes

- Carefully clean the PC board, base plate, and package leads with alcohol. Allow it to dry fully.
- To improve the thermal and RF performance, Qorvo recommends attaching a heat sink to the bottom of the package and apply either a thermal compound (Arctic Silver 5 recommended) or a .004 inch (maximum thickness) Indium shim between the heat sink and the package. Refer to the applications note [Application of Arctic Silver 5 Thermal Compound and Indium Shims for Qorvo CP-style Packaged Components](#) for more information.
- The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the QPM0106. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. The package lead temperature should not exceed 260 deg C. Each solder connection should be completed within 2 to 5 seconds. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable.
- The leads should be soldered in a staggered or star pattern from side to side, and never solder two adjacent leads. This allows the heat to dissipate on each lead, and not cause the adjacent leads to become de-soldered and damaged or displaced.



- The packaged part should not be subjected to conventional SMT automated solder reflow processes.
- (The following is for information only. There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.) Use screws to attach the component to the heat sink. A suggested final torque value is 16 in-oz. for a 0-80 screw. Start with screws finger tight, then torque to 8 in-oz., then torque to final value. Use the following tightening pattern:



## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ESDA / JEDEC JS-001-2017
ESD – Charge Device Model (CDM)	C3	ESDA / JEDEC JS-002-2018
MSL – Moisture Sensitivity Level	NA	



Caution!

ESD-Sensitive Device

## RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Tel:** 1-844-890-8163

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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