



TGA2307-SM

4.5-6.5 GHz 50 Watt GaN Power Amplifier

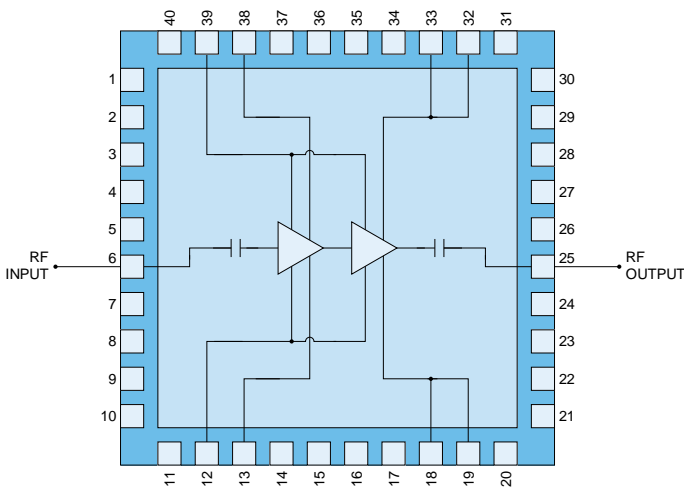
General Description

Qorvo's TGA2307-SM is a packaged power amplifier fabricated on Qorvo's production 0.25 μm GaN on SiC process. Operating from 4.5-6.5 GHz, the TGA2307-SM produces greater than 47 dBm of saturated output power with a power-added efficiency greater than 44% and a large signal gain greater than 20 dB.

The TGA2307-SM is offered in a 6 x 6 mm plastic overmold QFN to support low cost board assembly techniques. In addition, the package uses a copper alloy base that offers superior thermal management. With both RF ports fully matched to 50 ohms with integrated DC blocking capacitors, the TGA2307 is ideally suited to support both commercial and military applications.

Lead-free and RoHS compliant.

Functional Block Diagram



Product Features

- Frequency Range: 4.5 to 6.5 GHz
- Output Power ($P_{IN} = 27 \text{ dBm}$): $> 47 \text{ dBm}$
- Power Added Efficiency ($P_{IN} = 27 \text{ dBm}$): $> 44.4 \%$
- Small Signal Gain: $> 26 \text{ dB}$
- Input Return Loss: $> 17 \text{ dB}$
- Large Signal Gain ($P_{IN} = 27 \text{ dBm}$): $> 20 \text{ dB}$
- Bias Condition: $V_D = 28 \text{ V}$, $I_{DQ} = 500 \text{ mA}$
- Pulsed Operation
- Plastic Overmold QFN Package
- Package Dimensions: 6.00 x 6.00 x 0.85 mm

Applications

- C-Band Radar
- Satellite Communication

Ordering Information

Part	Description
TGA2307-SM	4.5–6.5 GHz 50 W GaN Power Amplifier
TGA2307-SM EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Drain Current (I_D)	7.5 A
Gate Voltage range (V_G)	-5 to 0 V
Gate Current (I_G)	See plot pg. 3
Input P_{IN} , Pulsed ¹ , 50 Ω , 85 °C	34 dBm
Input P_{IN} , Pulsed ¹ , 3:1 VSWR, 85 °C	34 dBm
Mounting Temperature (30 s max)	260 °C
Storage Temperature	-40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Note:

1. Pulse conditions: PW = 100 us, Duty Cycle = 1%

Recommended Operating Conditions

Parameter	Value/Range
Drain Voltage (V_D)	28 V
Drain Current, quiescent (I_{DQ})	1000 mA
Operating Temperature	-40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

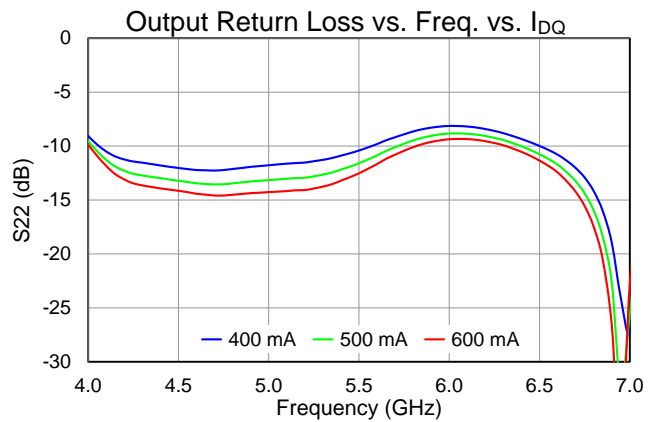
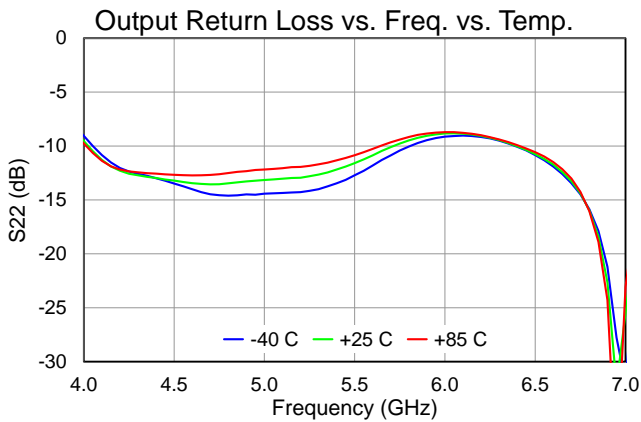
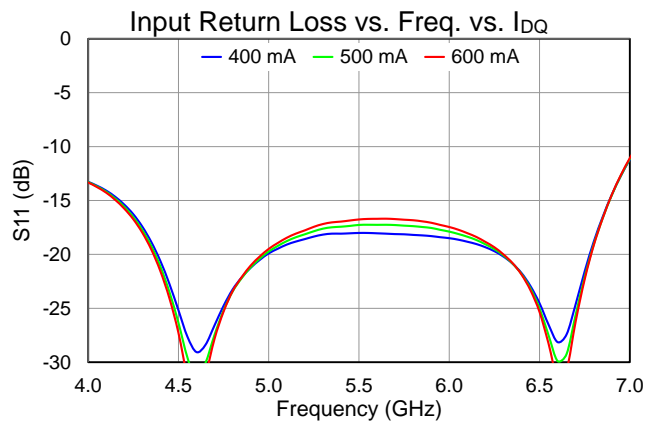
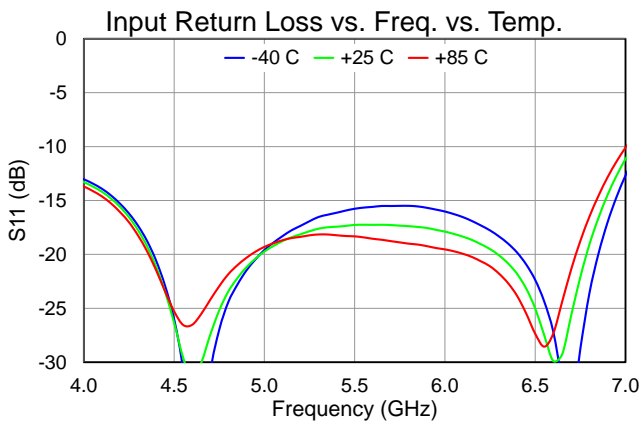
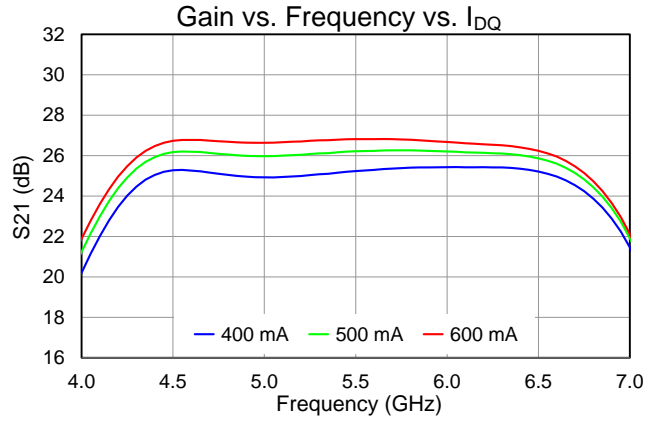
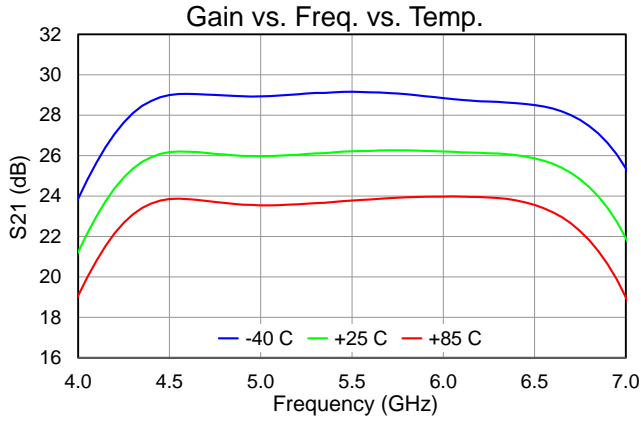
Electrical Specifications

Test conditions unless otherwise noted: 25 °C, I_{DQ} = 500 mA, Pulse Conditions PW = 100 us, Duty Cycle = 1 %

Parameter	Min	Typical	Max	Units
Operational Frequency Range	4.5		6.5	GHz
Small Signal Gain		> 26		dB
Input Return Loss		> 17		dB
Output Return Loss		> 8.5		dB
Output Power (P_{IN} = 27 dBm)		> 47		dBm
Large Signal Gain (P_{IN} = 27 dBm)		> 20		dB
Power Added Efficiency (P_{IN} = 27 dBm)		> 44.4		%
2 nd Harmonic Level (P_{OUT} = 45 dBm , Freq. = 5.5 GHz)		< -47		dBc
Sm. Sig. Gain Temp. Coeff.		-0.042		dB/ °C
Output Power Temp. Coeff.		-0.007		dB/ °C

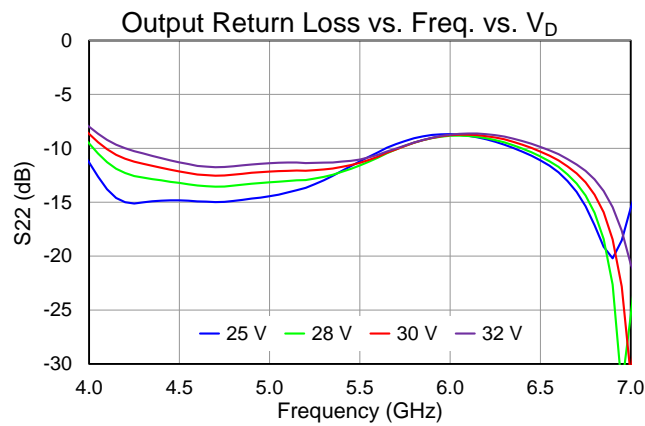
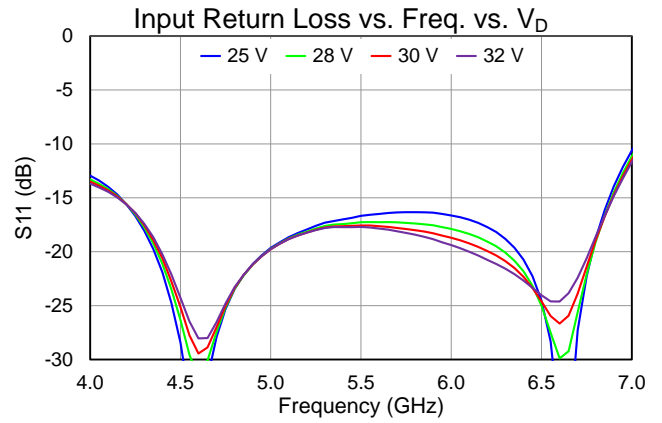
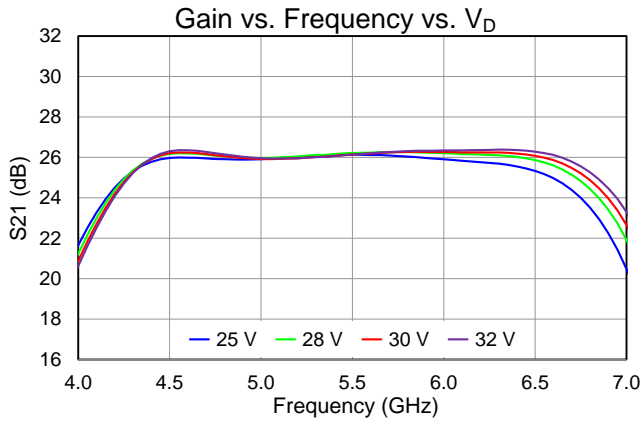
Typical Performance (Small Signal)

Test conditions unless otherwise noted: 25 °C, $V_D = 28$ V, $I_{DQ} = 500$ mA



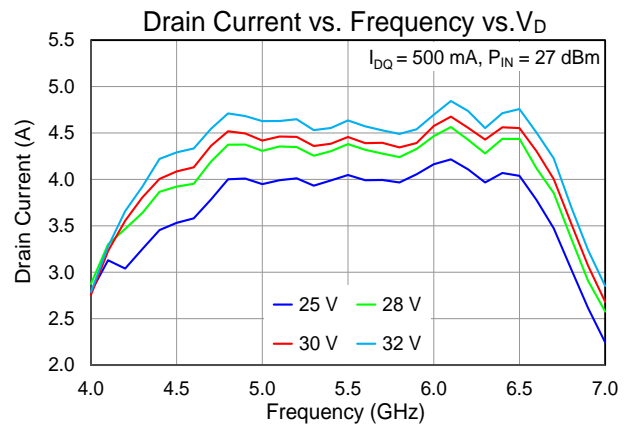
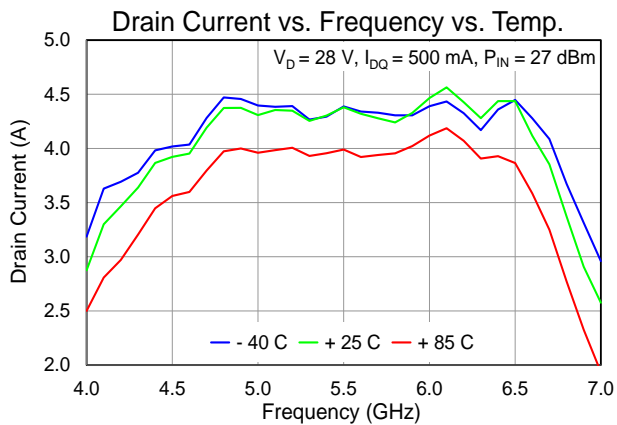
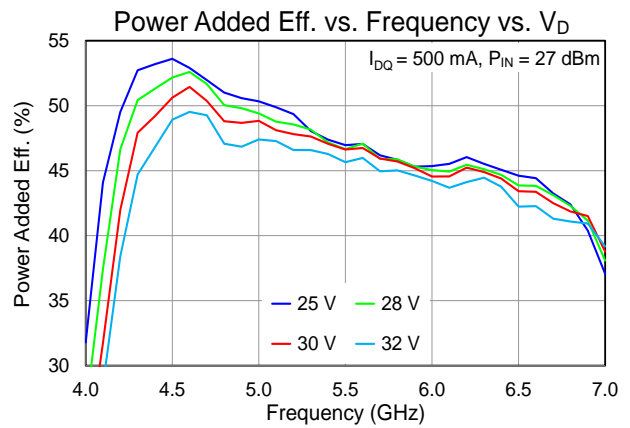
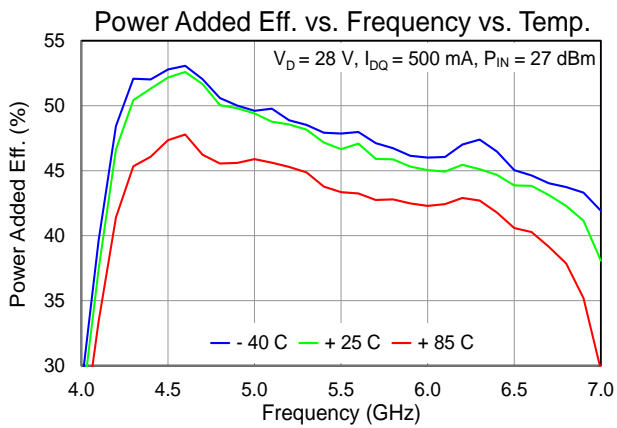
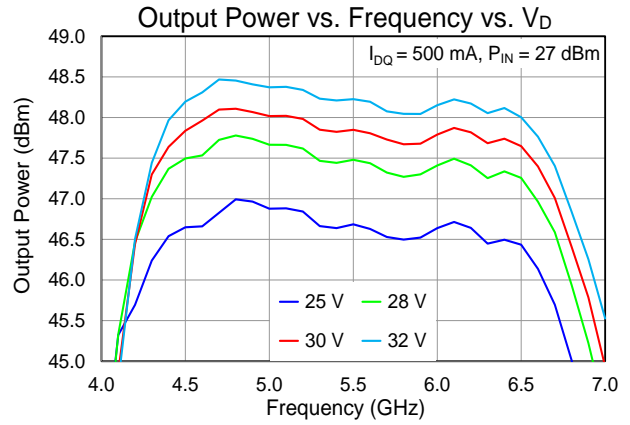
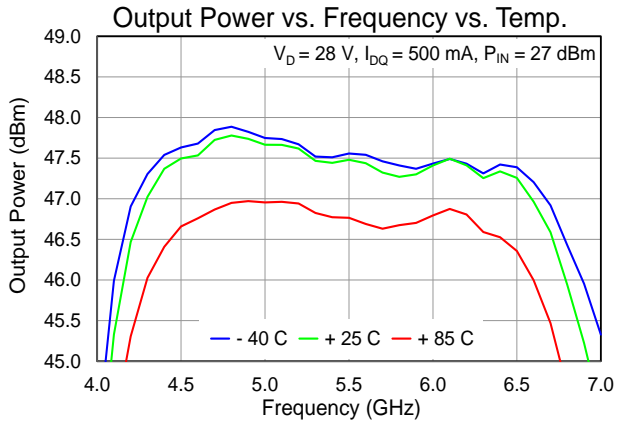
Typical Performance (Small Signal)

Test conditions unless otherwise noted: 25 °C, $V_D = 28\text{ V}$, $I_{DQ} = 500\text{ mA}$



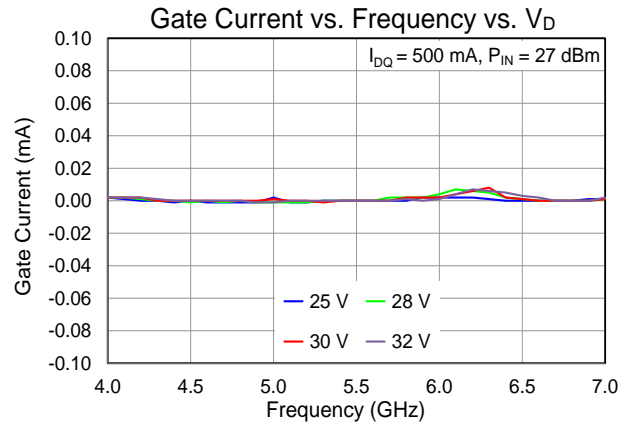
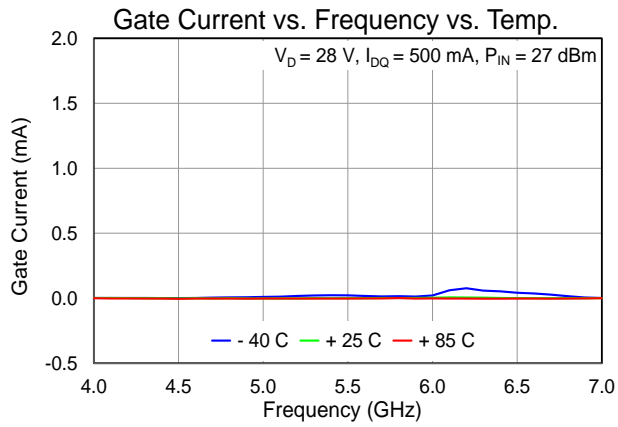
Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%



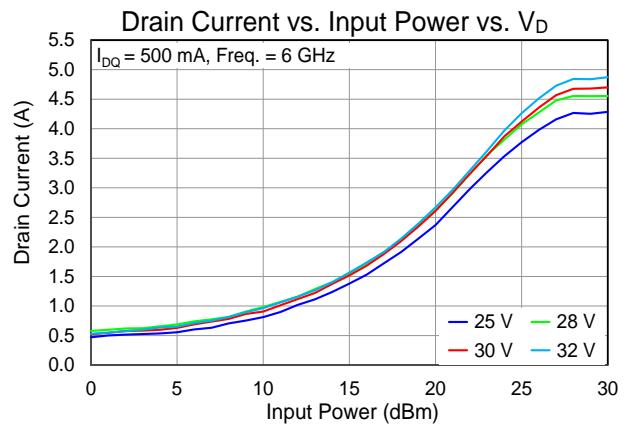
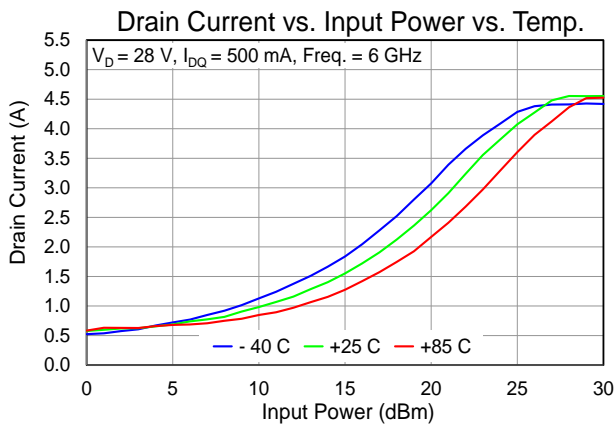
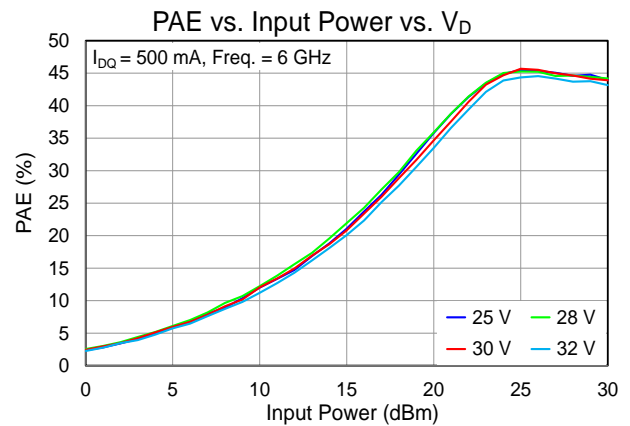
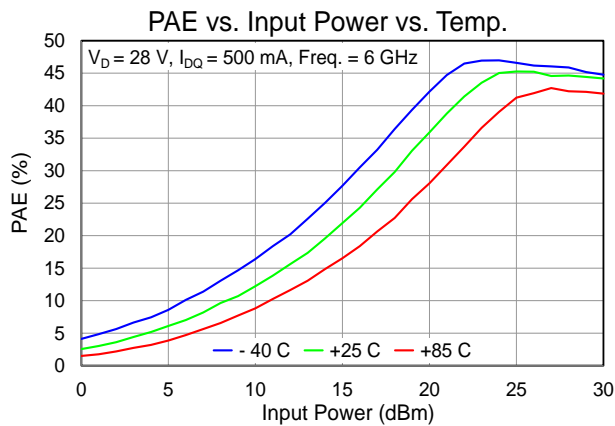
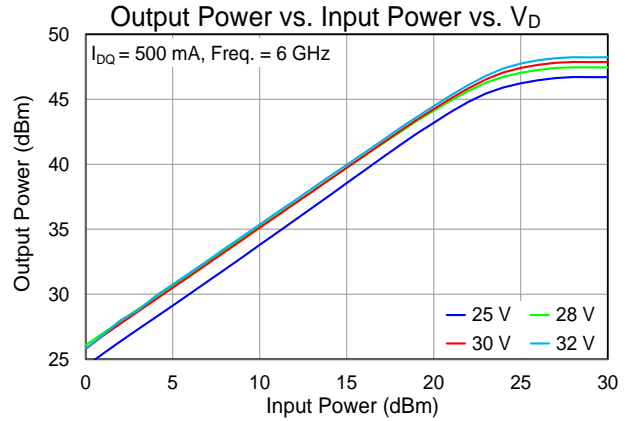
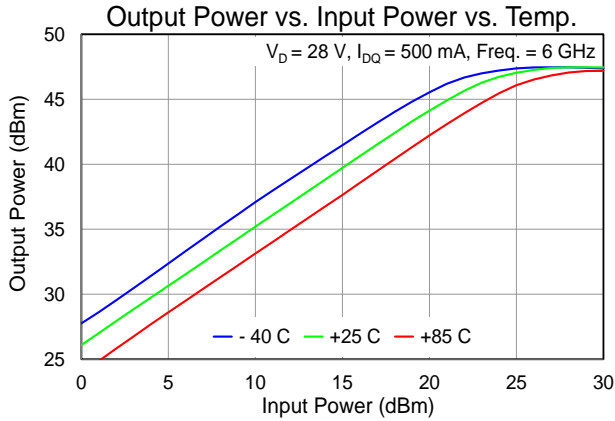
Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%



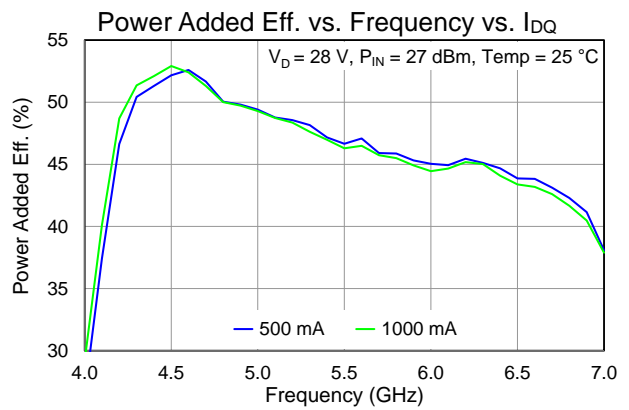
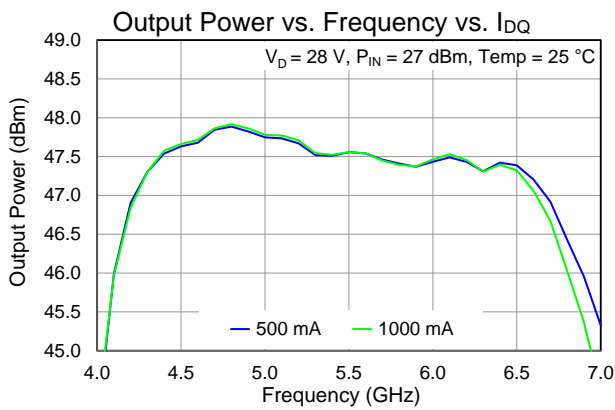
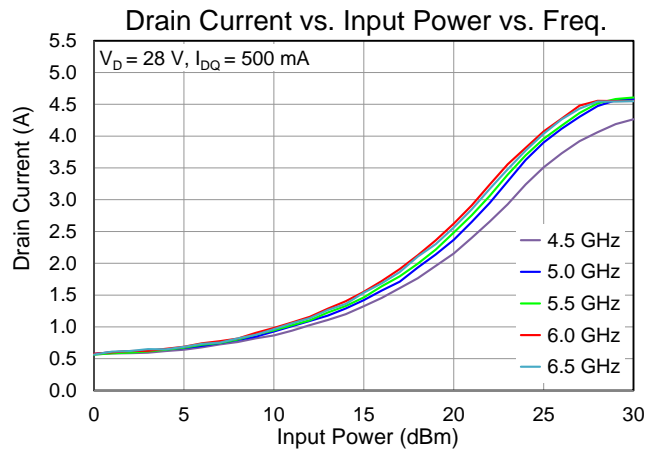
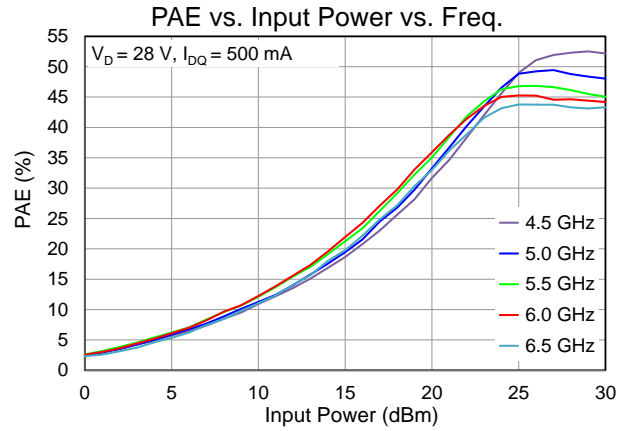
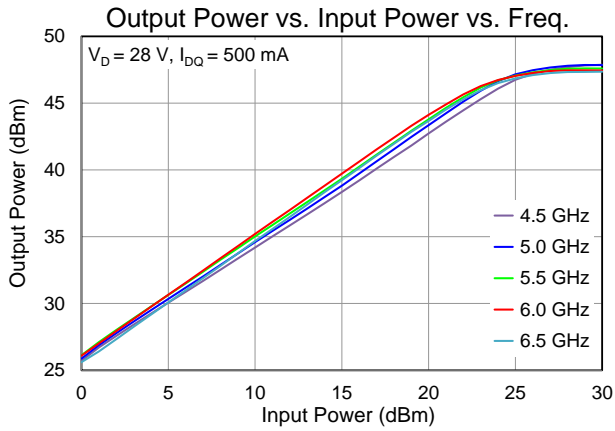
Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%



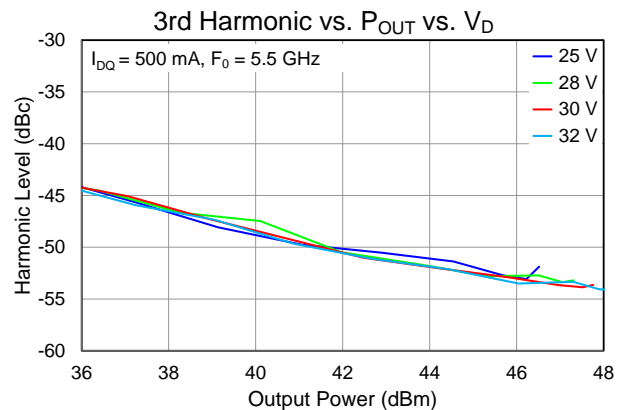
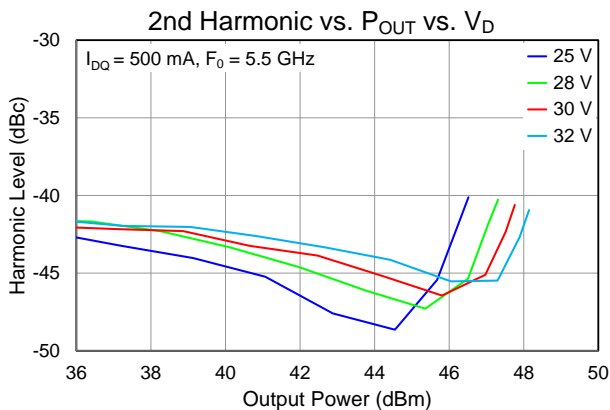
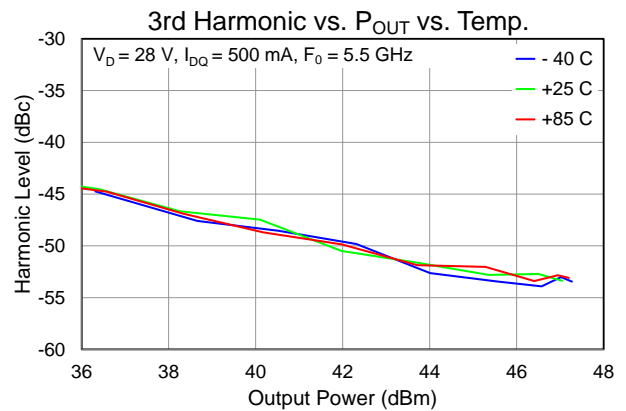
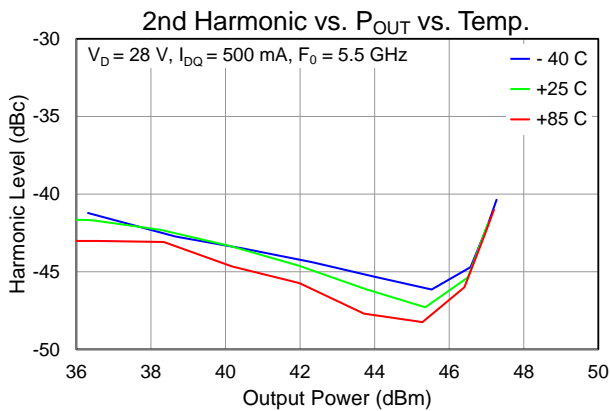
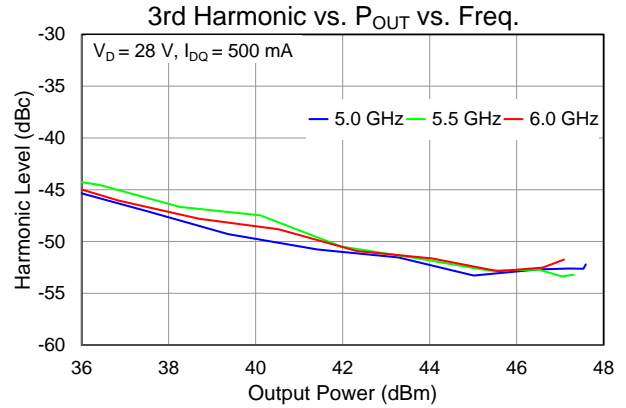
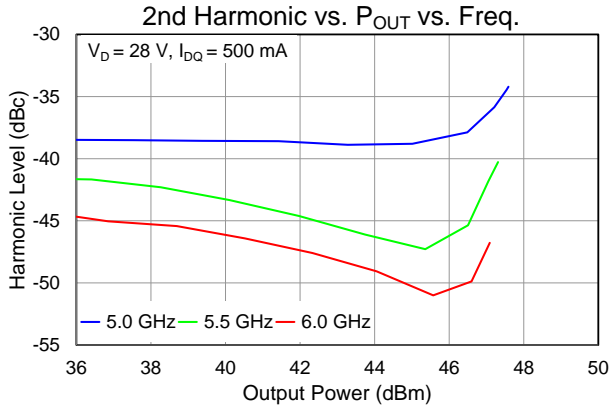
Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%



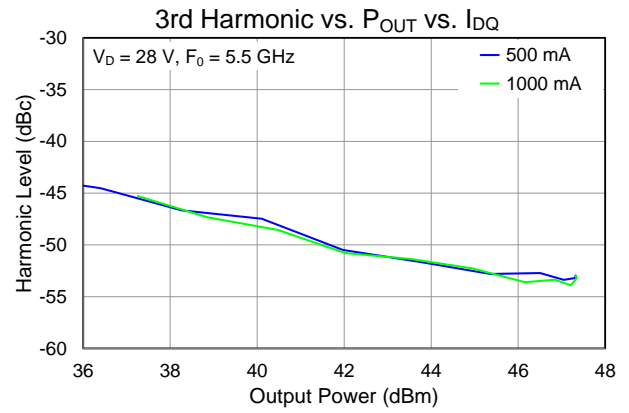
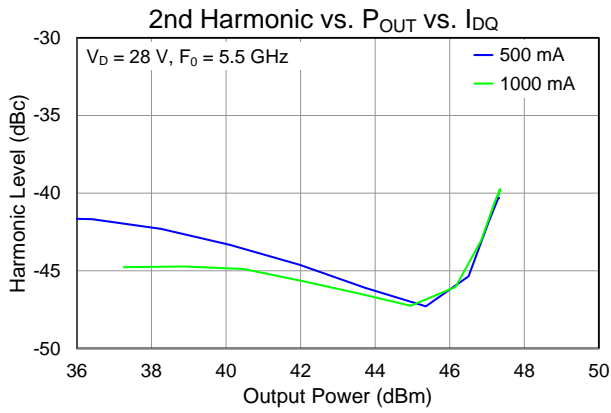
Typical Performance: 2nd Harmonic Level (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%



Typical Performance: Large Signal (Pulsed)

Test conditions unless otherwise noted: 25 °C, Pulse Conditions PW = 100 us, Duty Cycle = 1%



Thermal and Reliability Information

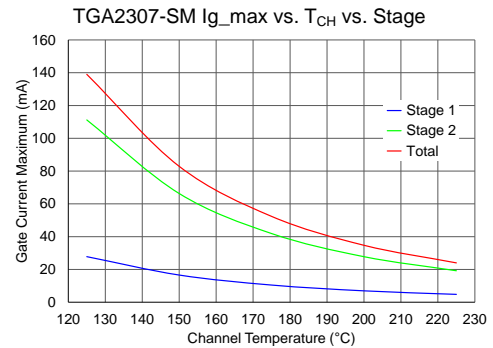
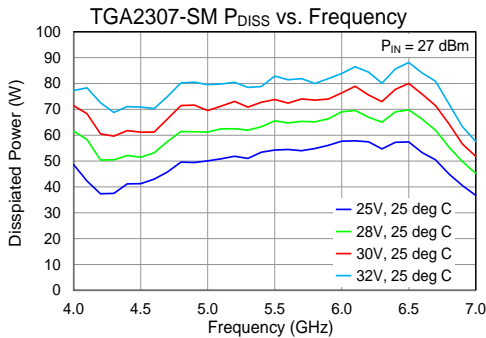
Parameter	Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_D = 1.0\text{ A}$ (quiescent), $P_{DISS} = 28\text{ W}$	0.823	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH})		108.0	$^{\circ}\text{C}$
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_D = 4.3\text{ A}$, $P_{IN} = 27\text{ dBm}$, $P_{OUT} = 47.3\text{ dBm}$, $PW = 100\text{ }\mu\text{s}$, $DC = 10\%$, $P_{DISS} = 62\text{ W}$	0.610	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH})		122.8	140
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = 32\text{ V}$, $I_D = 5.1\text{ A}$, $P_{IN} = 24\text{ dBm}$, $P_{OUT} = 48.0\text{ dBm}$, $PW = 100\text{ }\mu\text{s}$, $DC = 10\%$, $P_{DISS} = 80\text{ W}$	0.654	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH})		137.3	$^{\circ}\text{C}$

Notes:

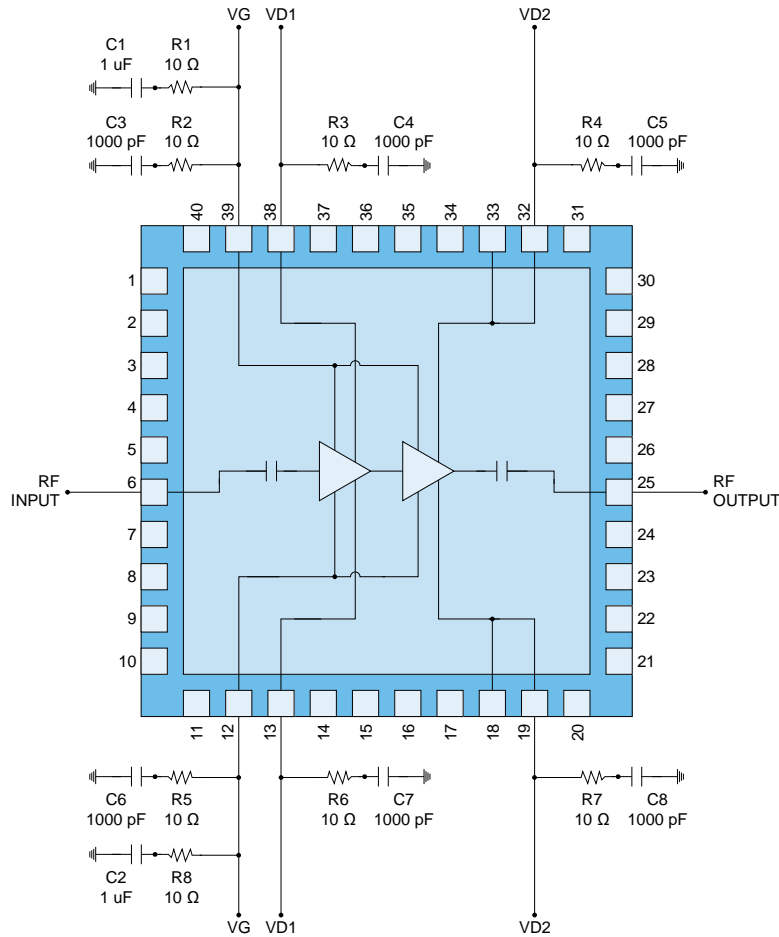
1. Thermal resistance measured to back of package.
2. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Power Dissipation and Maximum Gate Current

Pulse condition: $PW = 100\text{ }\mu\text{s}$, Duty Cycle = 1%



Application Circuit



Notes:

1. V_G and V_{D1} , V_{D2} must be biased from both sides (top and bottom).
2. V_{D1} and V_{D2} can be connected.

Bias-up Procedure

Set I_D limit to 6000 mA, I_G limit to 140 mA

Set V_G to -5.0 V

Set V_D +28 V

Adjust V_G more positive to achieve desired quiescent current (I_{DQ}) ($V_G \sim -2.4$ V Typical)

Apply RF signal

Bias-down Procedure

Turn off RF signal

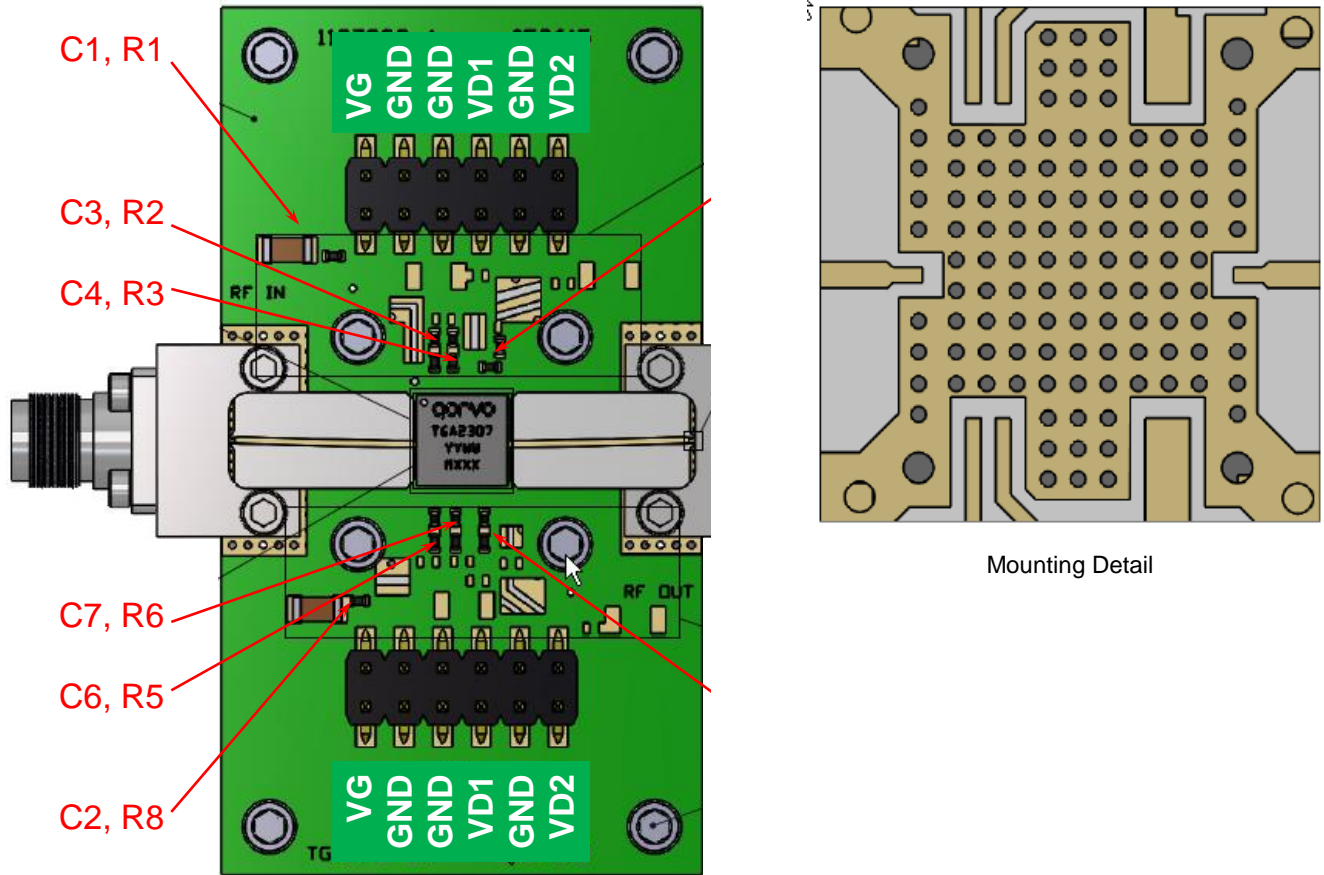
Reduce V_G to -5.0 V. Ensure $I_{DQ} \sim 0$ mA

Set V_D to 0 V

Turn off V_D supply

Turn off V_G supply

Applications Information – Evaluation Board (EVB)



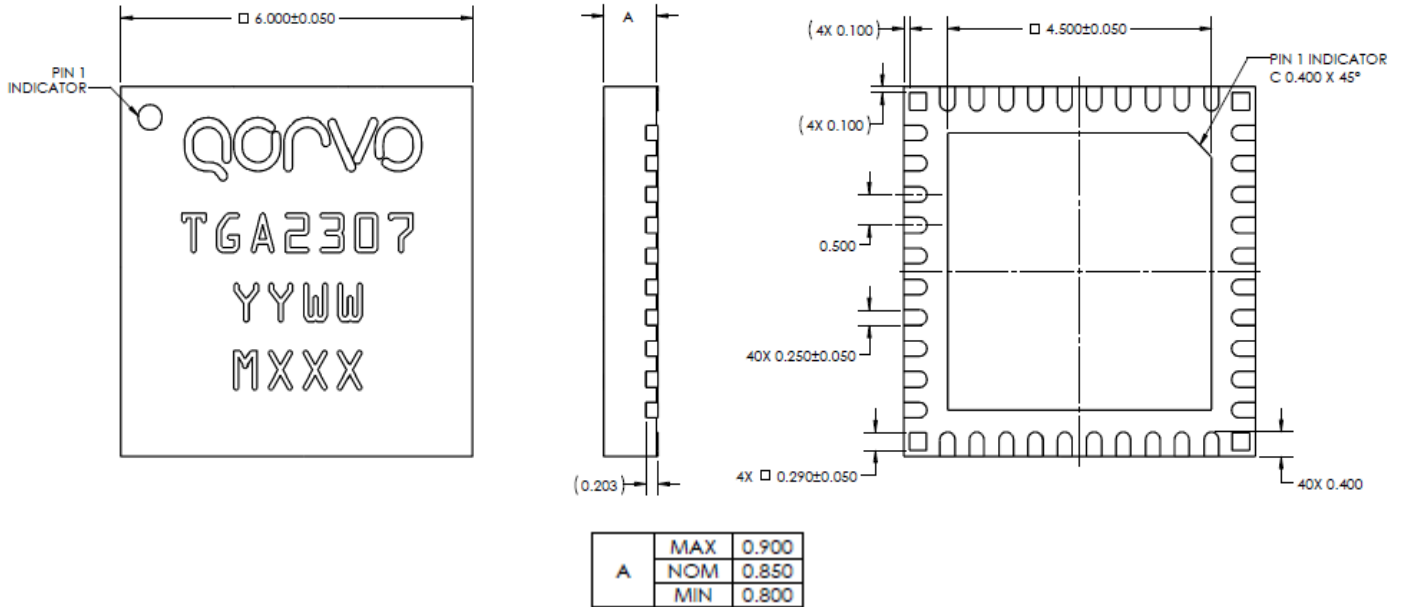
RF layer is 0.008" thick Rogers RO4003C, $\epsilon_r = 3.38$. Metal layers are 0.5-oz copper. The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-01A-5..

Reference Design	Component	Value	Manufacture
R1-R8	Surface Mount Res	10 Ohm, 5 % (0402)	Various
C1, C2	Surface Mount Cap	1 uF, 5 %, 50 V (1206), X7R	Various
C3-C8	Surface Mount Cap	1000 pF, 10 %, 100 V (0402), X7R	Various

Note:

1. Multiple copper-filled vias should be employed under die to minimize inductance and thermal resistance.
2. A coined PCB is recommended for higher duty cycle operation.

Mechanical Drawing & Pad Description



Units: mm

Tolerances: unless specified

x.xx = ± 0.25

x.xxx = ± 0.127

Materials:

All metalized features are gold plated

Part is mold encapsulated

Marking:

2307: Part number

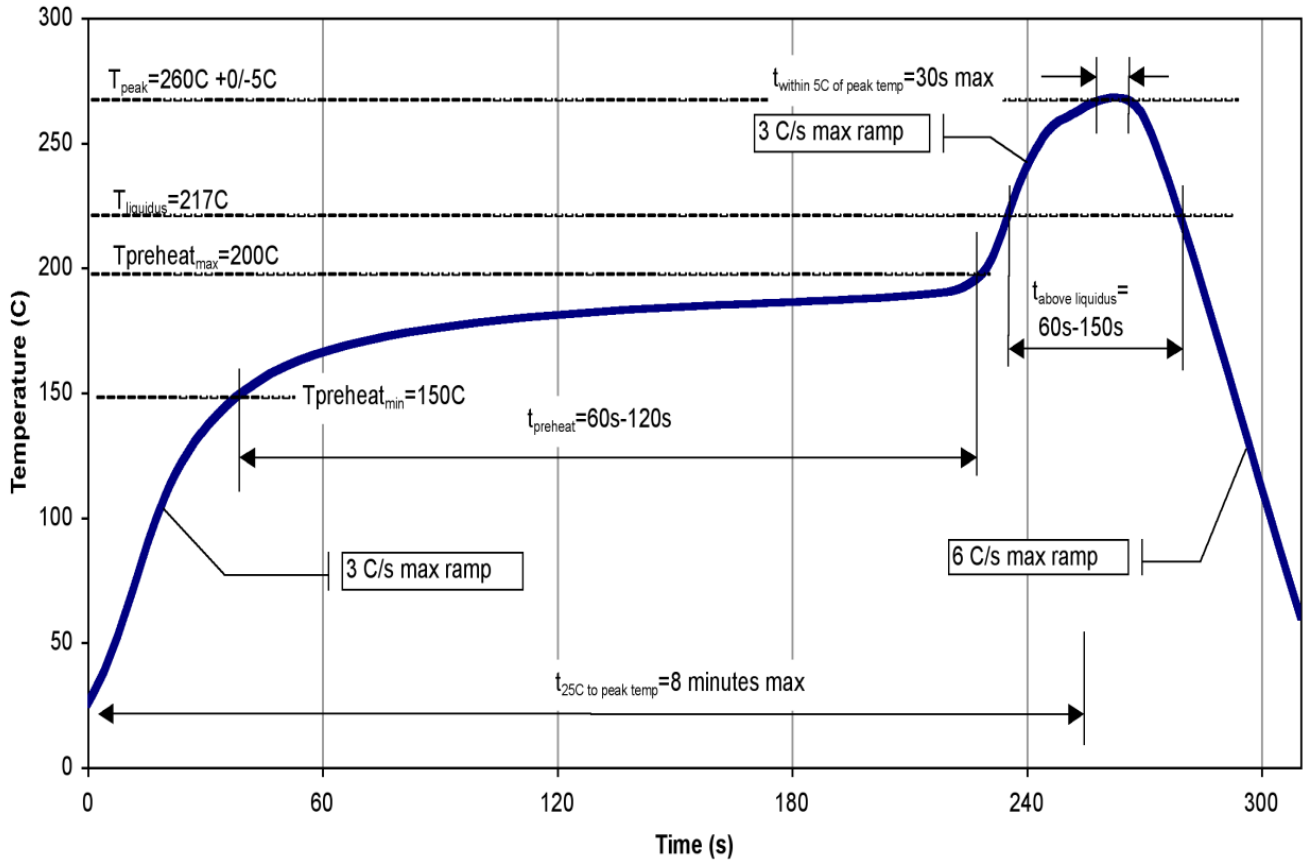
YY: Part Assembly year

WW: Part Assembly week

MXXX: Batch ID

Package Pad	Symbol	Description
1-5, 7-11, 14-17, 20-24, 26-31, 34-37, 40	NC	No connection, recommend to be grounded on PCB
6	RF Input	RF Input, matched to 50 Ω , DC blocked
12, 39	V _G	Gate voltage
13, 38	V _{D1}	Drain Voltage, stage 1
18-19, 32-33	V _{D2}	Drain Voltage, stage 2
25	RF Output	RF Output, matched to 50 Ω , DC blocked
41 (center pad)	GND	Ground on PCB, multiple copper-filled vias should be employed under the center pad (41) to minimize inductance and thermal resistance

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	0B	JEDEC/JESD22-A114
ESD – Charge Device Model (CDM)	C2A	JEDEC/JESD22-C101
MSL – Moisture Sensitivity Level	MSL3	JEDEC/IPC/JEDEC J-STD-202



Caution!
 ESD-Sensitive Device

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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