TGA2830-SM

2.7 to 3.5 GHz, 18 W GaN Power Amplifier

Product Overview

Qorvo's TGA2830-SM is a packaged MMIC power amplifier which operates from 2.7 to 3.5 GHz. The TGA2830-SM is designed using Qorvo's TQGaN25 0.25-µm GaN on SiC process.

The TGA2830-SM typically provides more than 42.5 dBm of saturated output power, 54% power-added efficiency, and 30.5 dB small signal gain. It can operate under both pulse and CW conditions.

The TGA2830-SM is available in a low-cost, surface mount 24 lead 5 x 5 Overmold QFN. It is ideally suited to support both commercial and defense related radar applications.

Both RF ports have integrated DC blocking capacitors and are fully matched to 50 ohms.

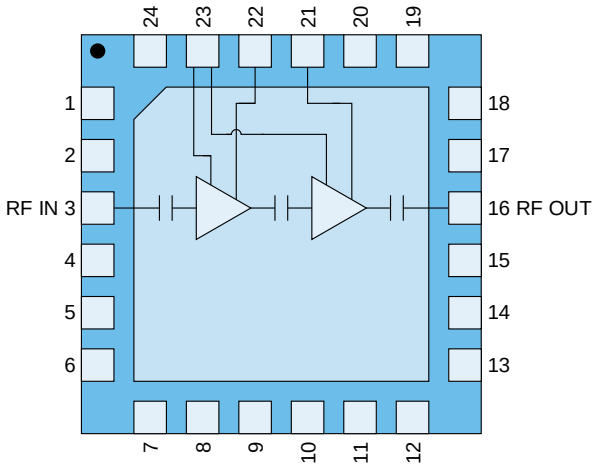
Lead-free and RoHS compliant

QFN 5x5 mm 24L

Product Features

- Frequency Range: 2.7-3.5 GHz
- P_{SAT}: > 42.5 dBm (P_{IN} = 18 dBm)
- PAE: > 54 % (P_{IN} = 18 dBm)
- Small Signal Gain: > 30.5 dB
- Return Loss: > 11 dB
- Bias: V_D = 20-32 V, I_{DQ} = 225 mA
- Pulsed V_D: PW = 100 us, DC = 10 %
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Functional Block Diagram



Applications

- Commercial and Military Radar

Ordering Information

Part	Description
TGA2830-SM	2.7-3.5 GHz, 18 W GaN Power Amplifier
TGA2830-SM_EVB	TGA2830-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	−8 to 0 V
Drain Current (I_{D1})	225 mA
Drain Current (I_{D2})	1250 mA
Gate Current (I_G)	See Graph (page 3)
Power Dissipation (P_{DISS}), 85 °C	35 W
Input Power (P_{IN}), CW, 50 Ω, 85 °C	30 dBm
Input Power (P_{IN}), CW, V_{SWR} 10:1, V_D = 28 V, 85 °C	23 dBm
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value/Range
Drain Voltage (V_D)	20–32 V
Drain Current (I_{DQ})	175–275 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 8
Gate Voltage Range (V_G)	−2.9 to −2.0 V
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 8
Operating Temperature Range	−40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

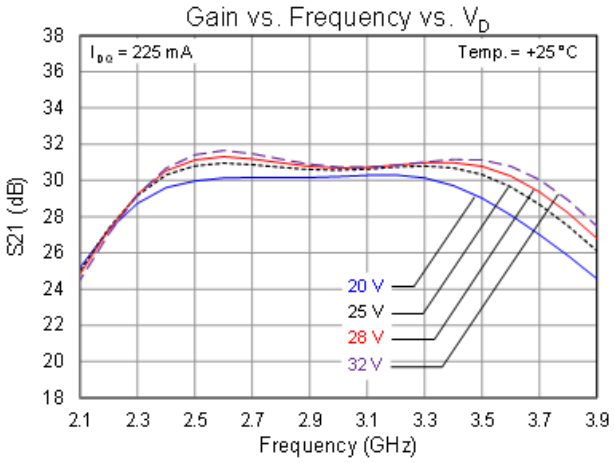
Electrical Specifications

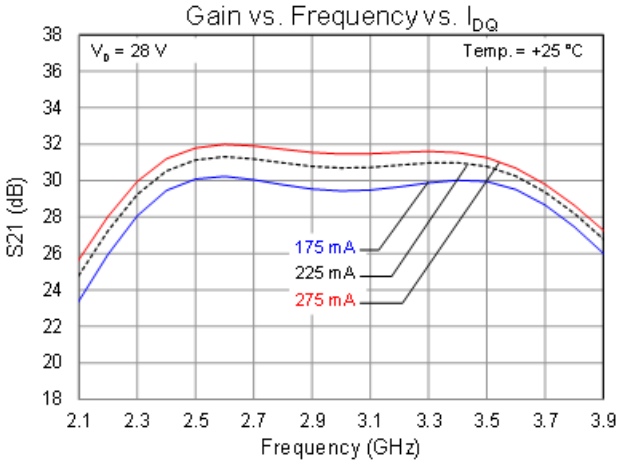
Test conditions unless otherwise noted: 25 °C, V_D = 28 V, I_{DQ} = 225 mA, Pulsed V_D: PW = 100 us, DC = 10 %

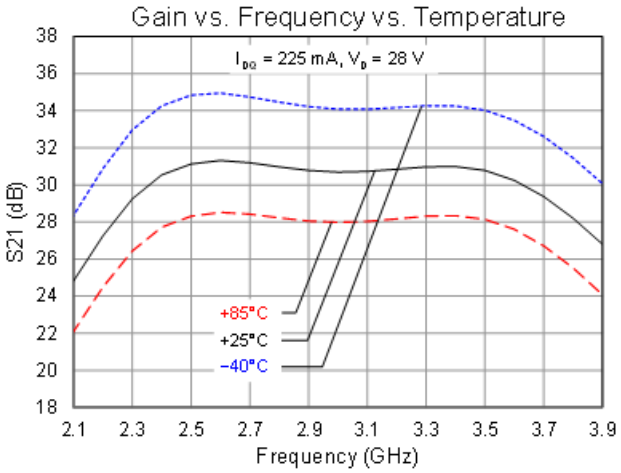
Parameter	Min	Typical	Max	Units
Operational Frequency Range	2.7		3.5	GHz
Small Signal Gain		>30.5		dB
Input Return Loss		>15		dB
Output Return Loss		>11		dB
Output Power at Saturation (P_{IN} = 18 dBm)		>42.5		dBm
Power-Added Efficiency (P_{IN} = 18 dBm)		>54		%
Gate Leakage (V_D = 10 V, V_G = −3.7 V)	−7.83		−0.0001	mA
Gain Temperature Coefficient		−0.05		dB/°C
Power Temperature Coefficient		−0.004		dBm/°C

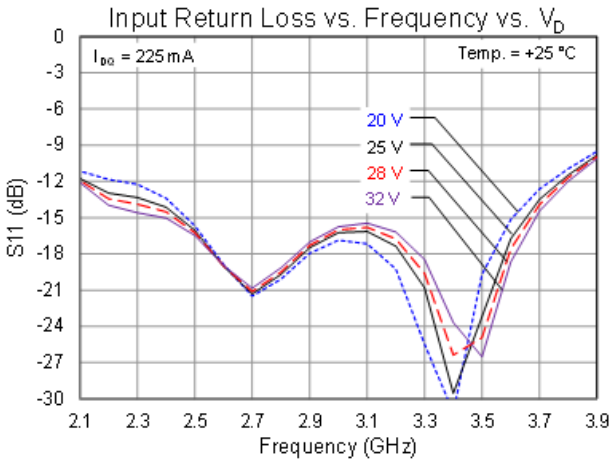
Typical Performance (Small Signal)

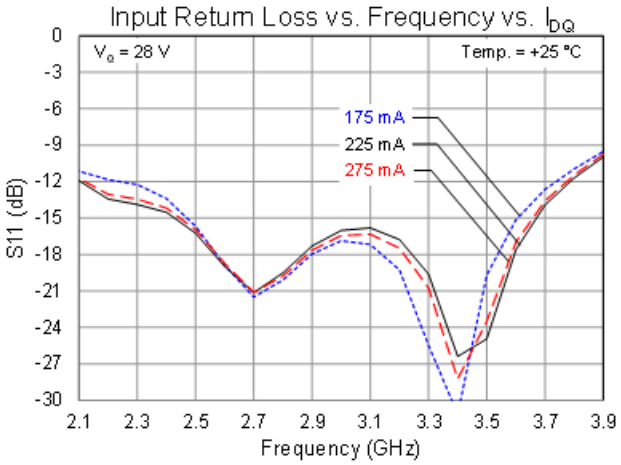
Condition: CW





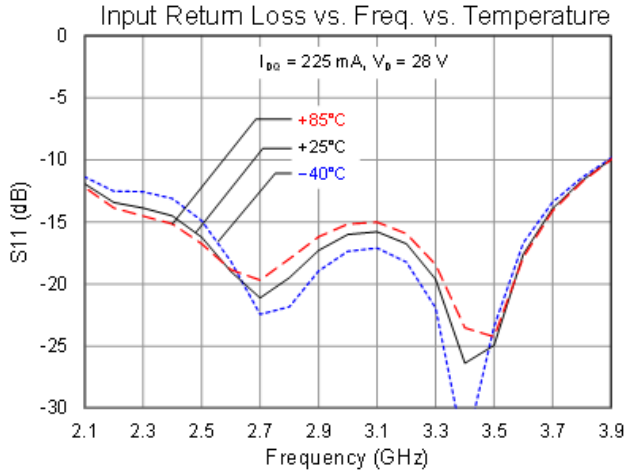


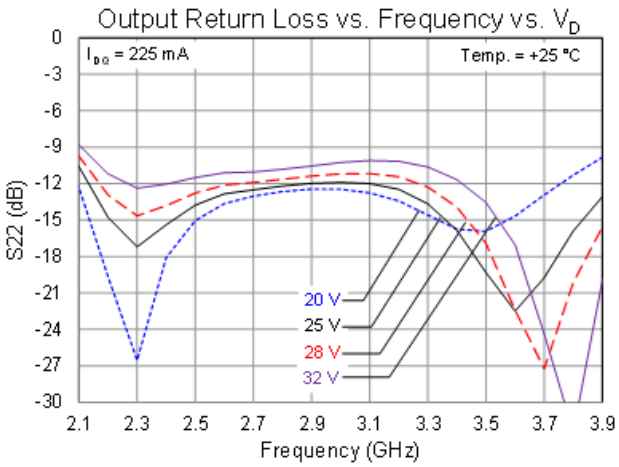


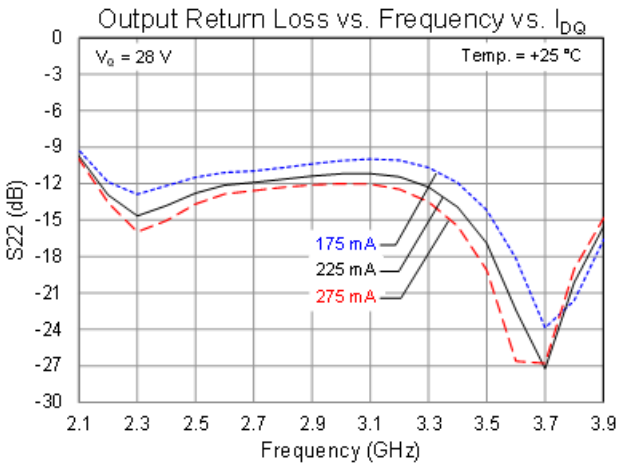


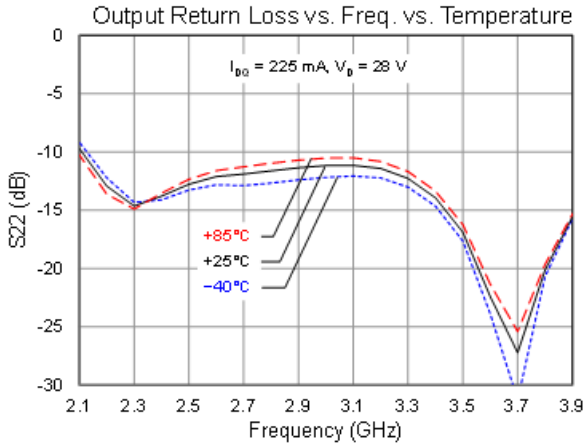
Typical Performance: Small Signal

Condition: CW



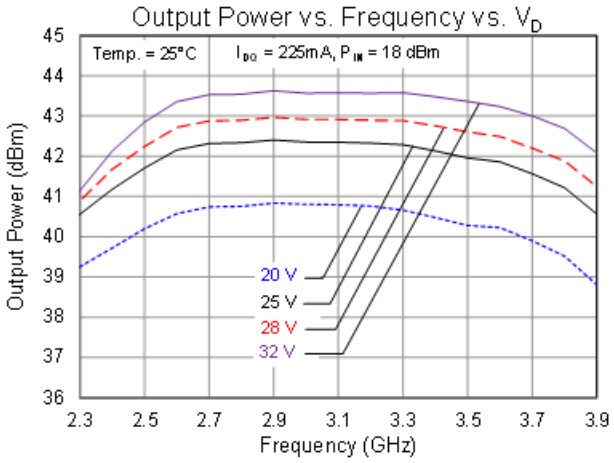


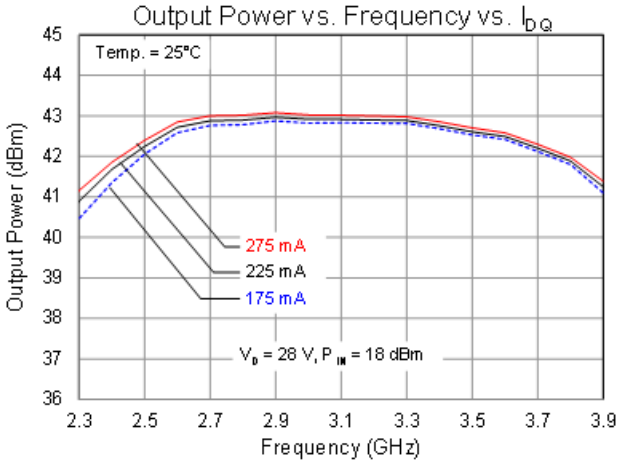


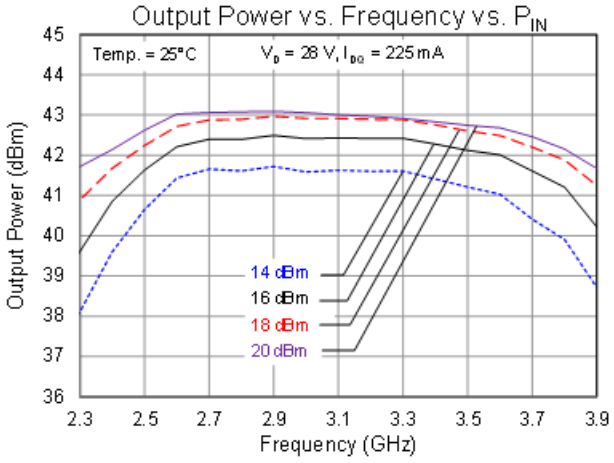


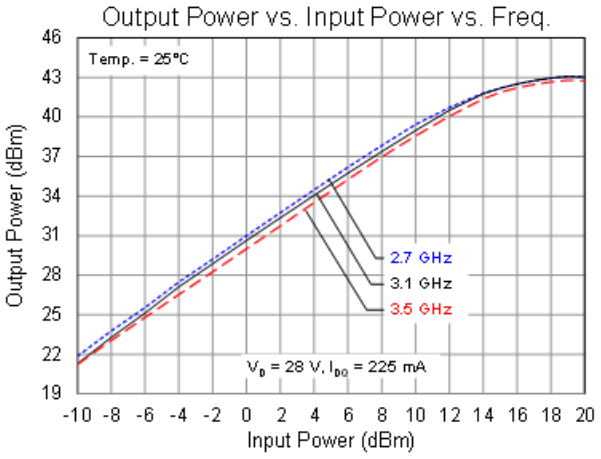
Typical Performance: Large Signal

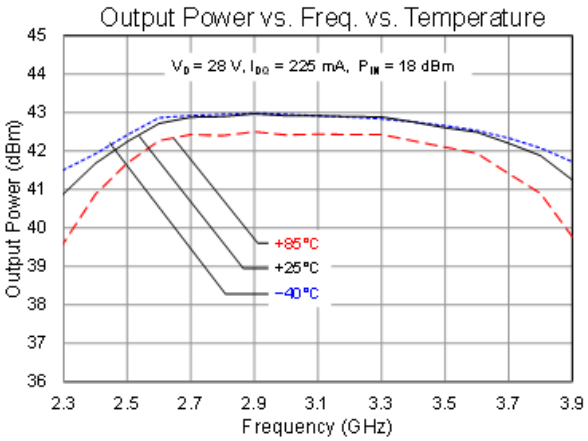
Condition: Pulsed V_D, Pulse Width = 100 us, Duty Cycle = 10%

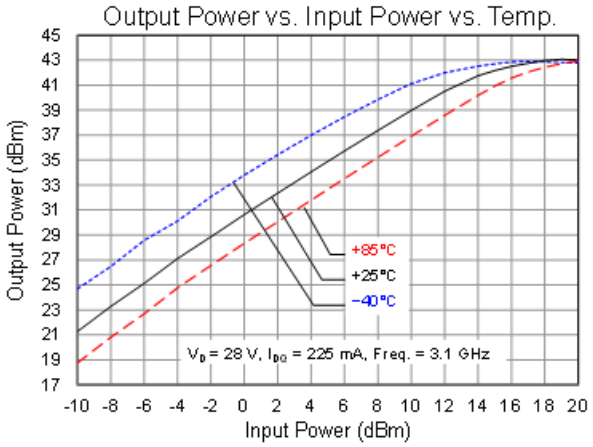








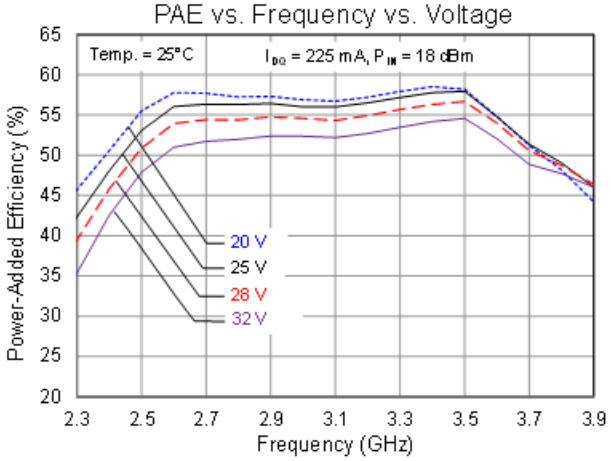




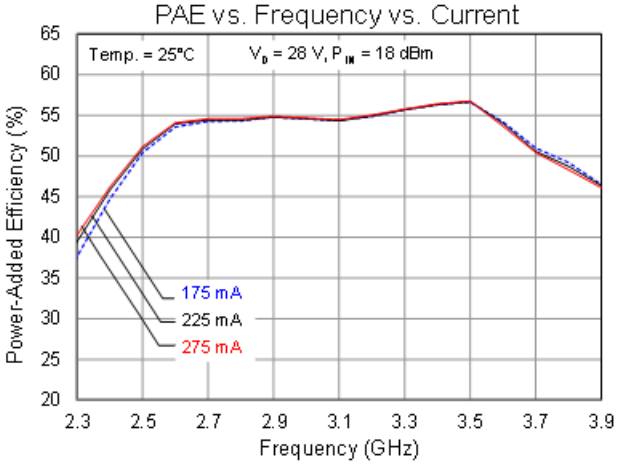
Typical Performance: Large Signal

Condition: Pulsed V_D, Pulse Width = 100 us, Duty Cycle = 10%

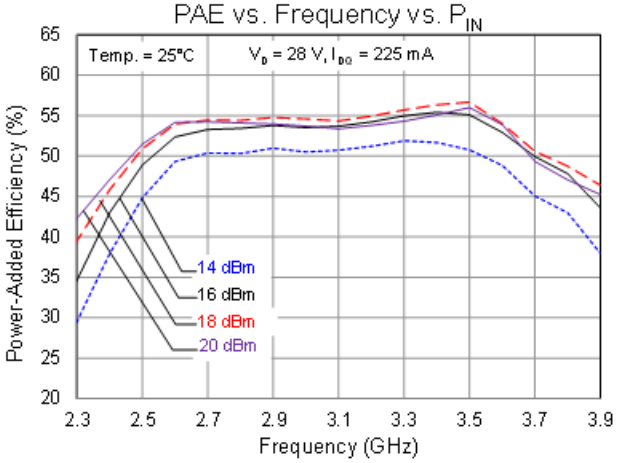
PAE vs. Frequency vs. Voltage



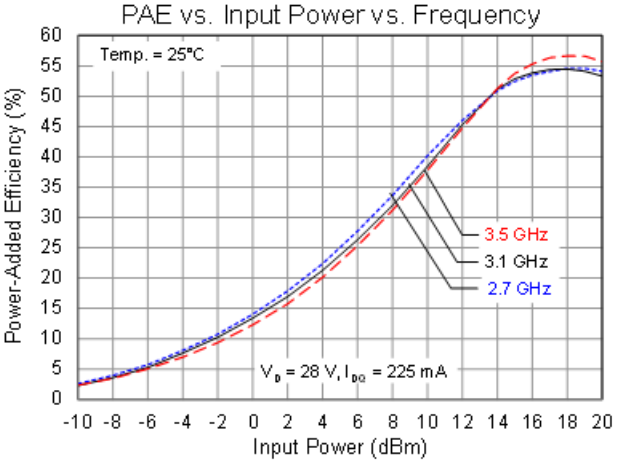
PAE vs. Frequency vs. Current



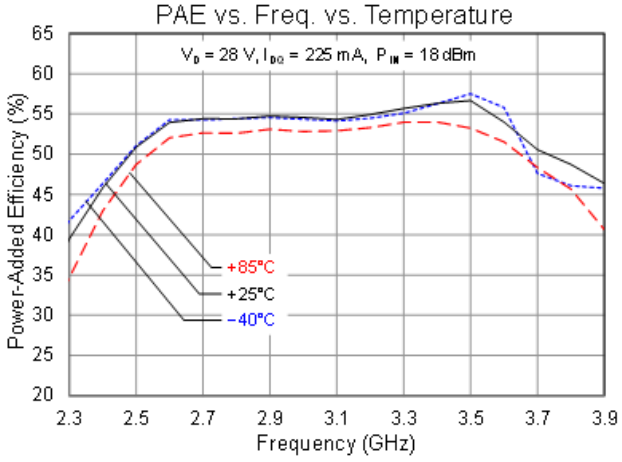
PAE vs. Frequency vs. P_{IN}



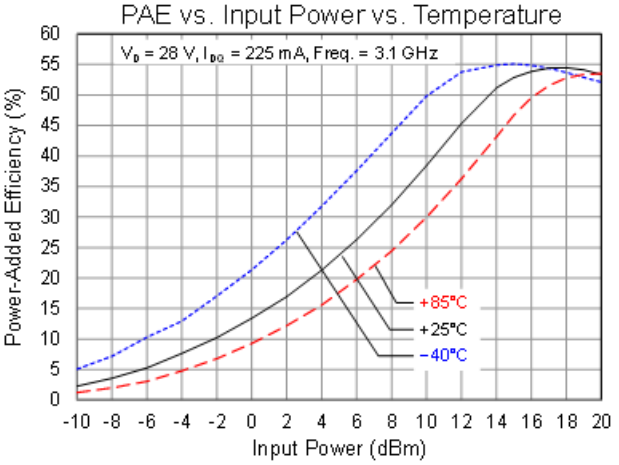
PAE vs. Input Power vs. Frequency



PAE vs. Freq. vs. Temperature

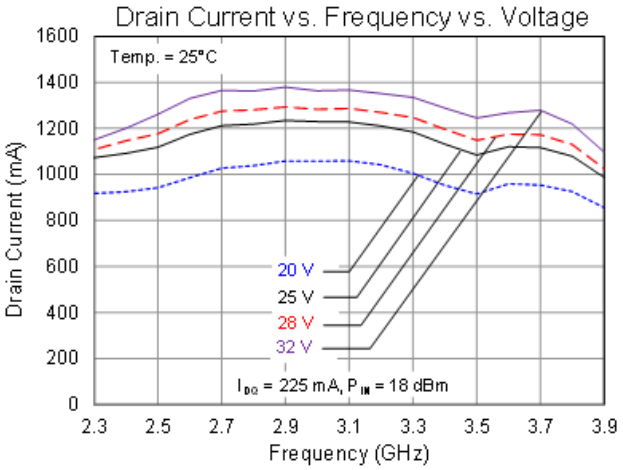


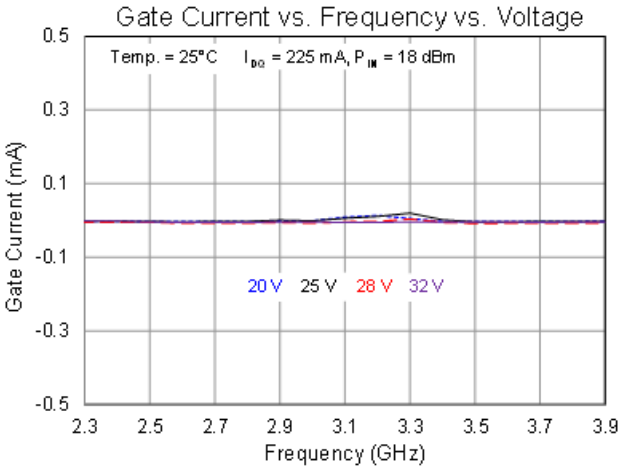
PAE vs. Input Power vs. Temperature

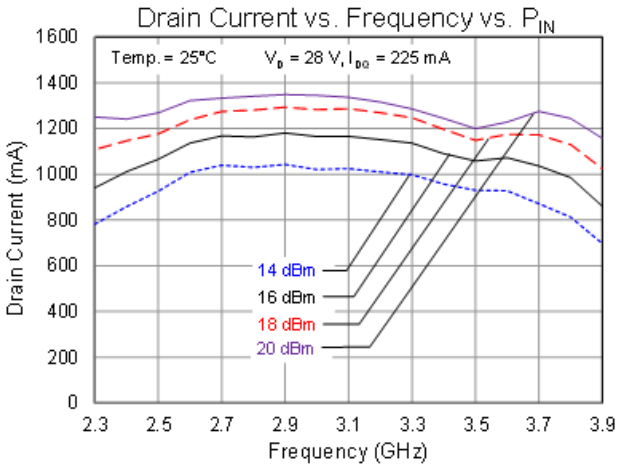


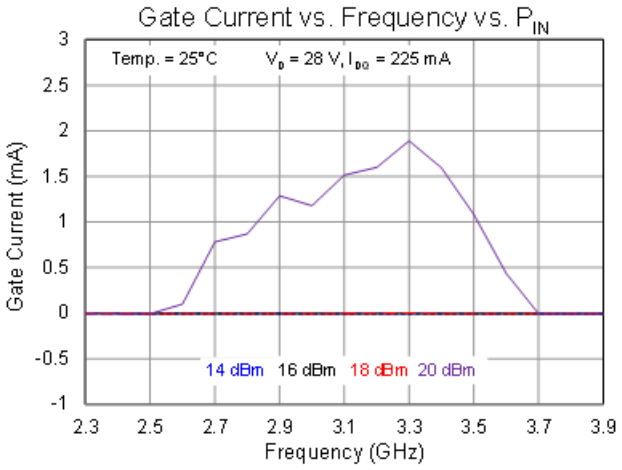
Typical Performance: Large Signal

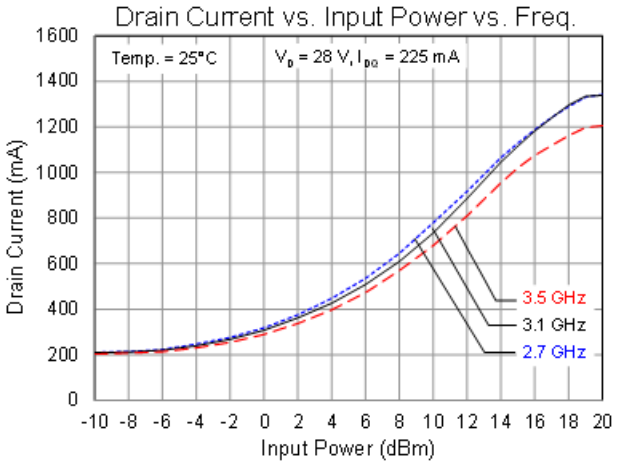
Condition: Pulsed V_D, Pulse Width = 100 us, Duty Cycle = 10%

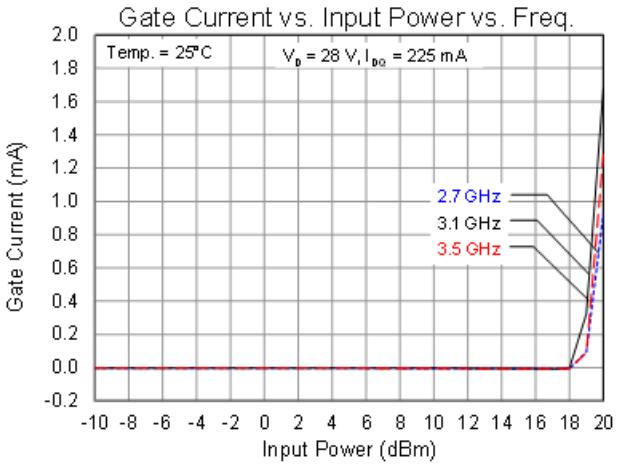






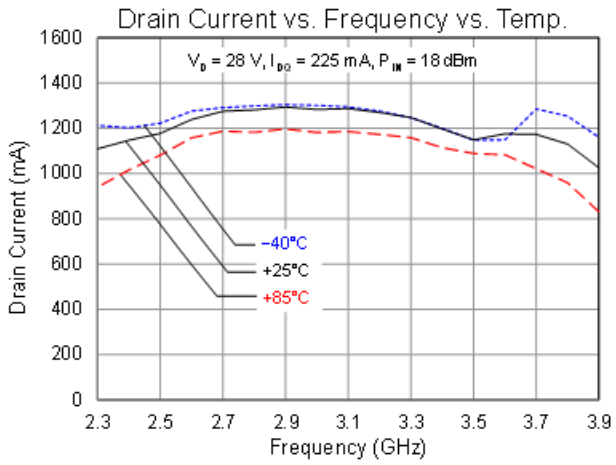


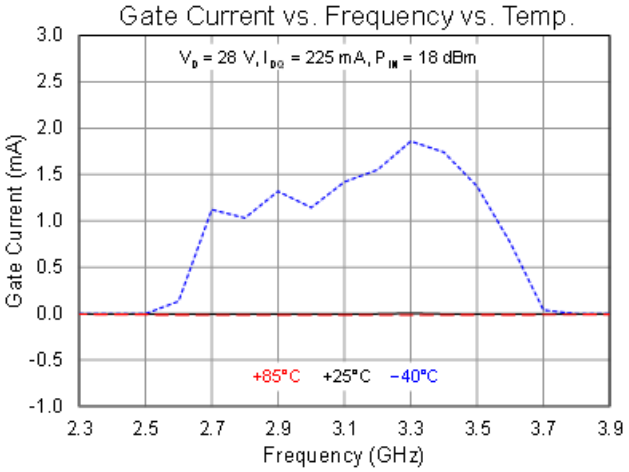


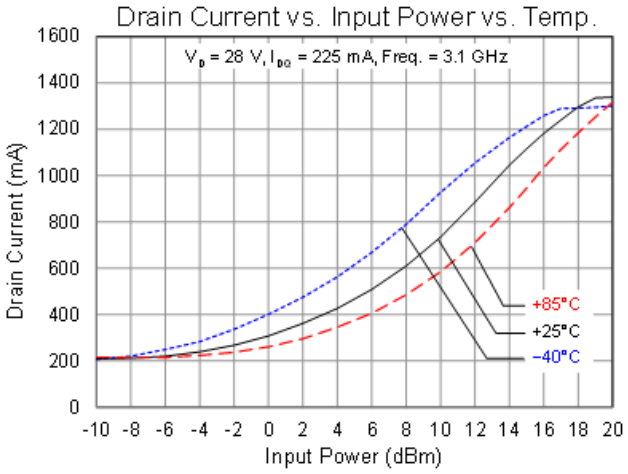


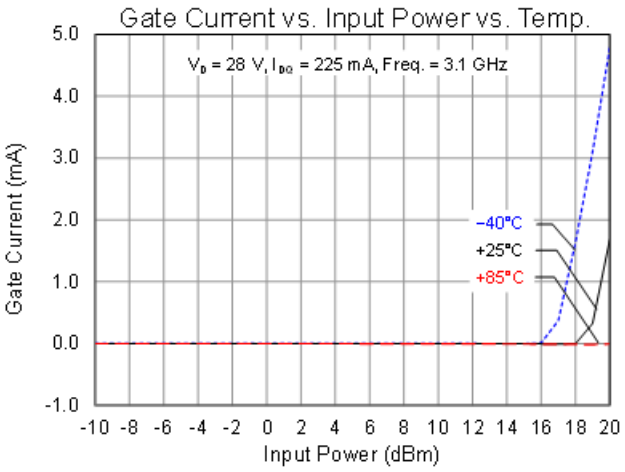
Typical Performance: Large Signal

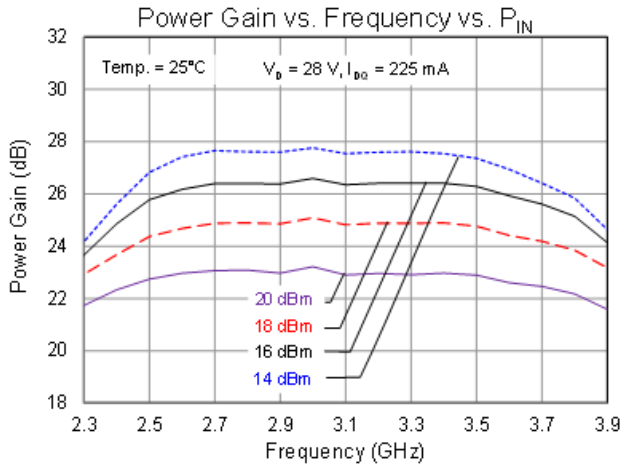
Condition: Pulsed V_D, Pulse Width = 100 us, Duty Cycle = 10%

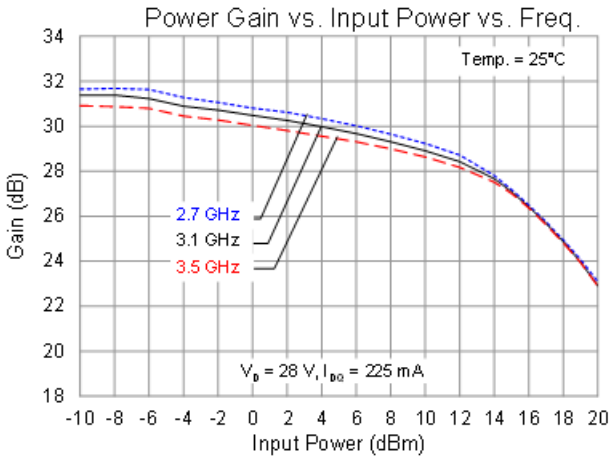






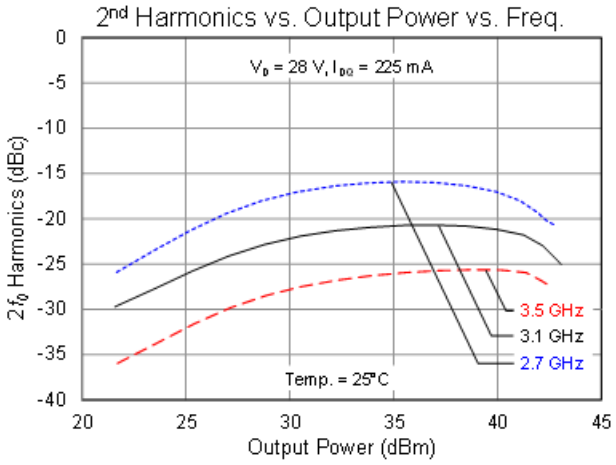


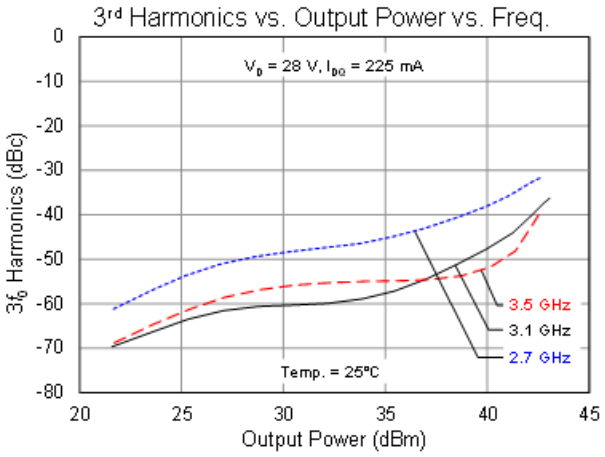


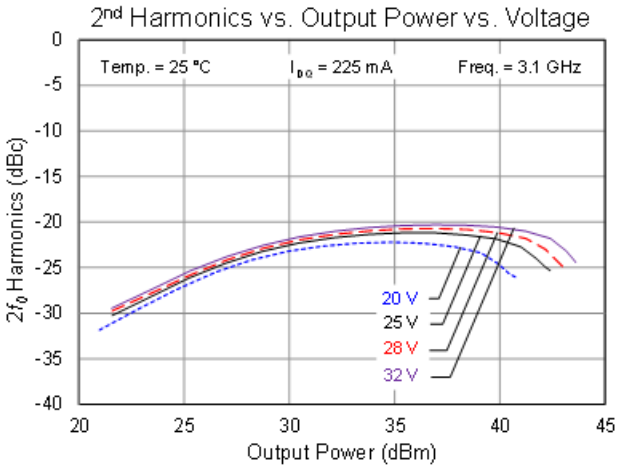


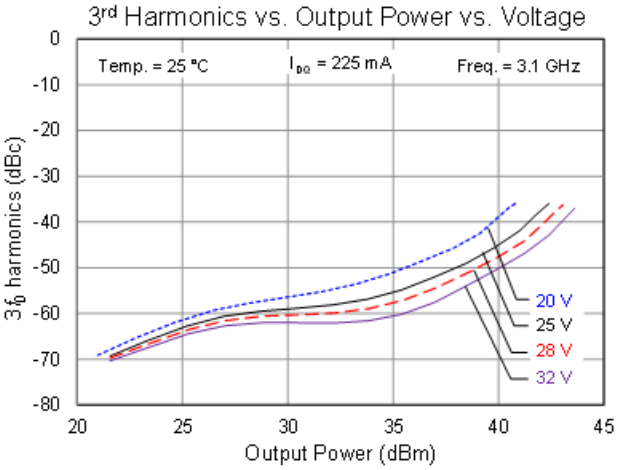
Typical Performance: Large Signal and Linearity

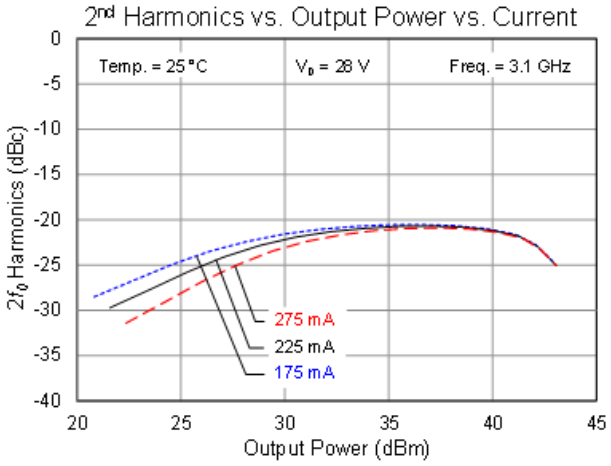
Condition: CW

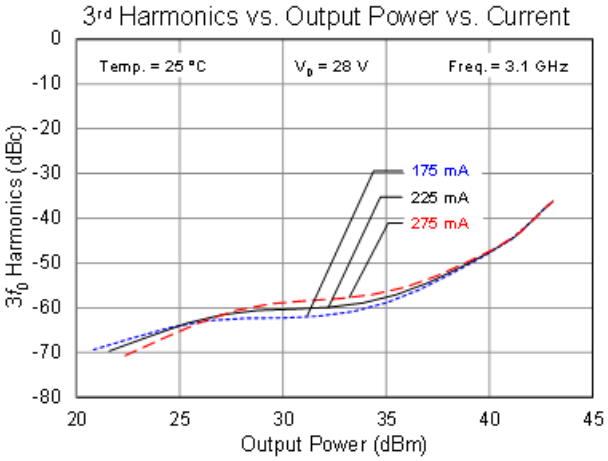






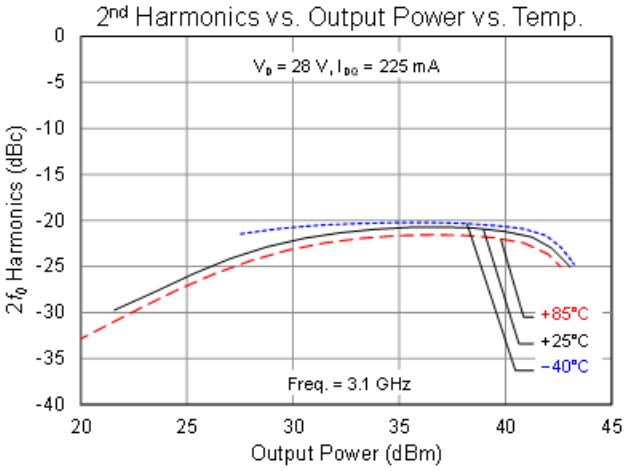


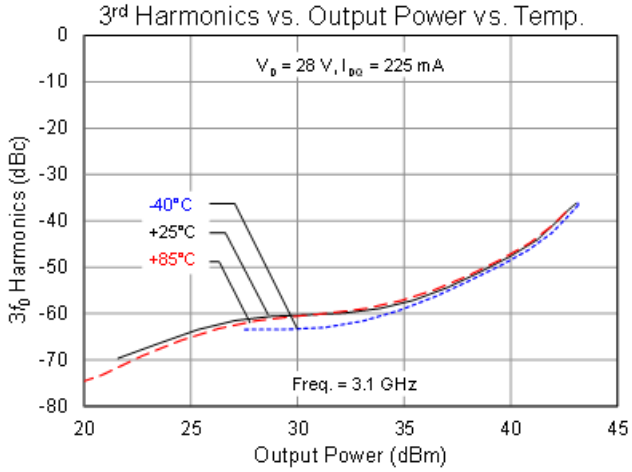


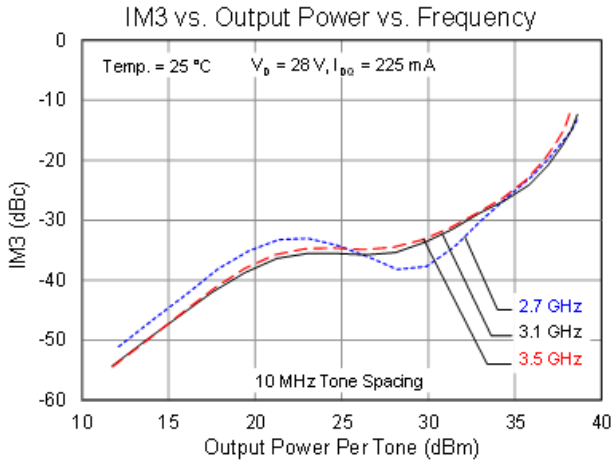


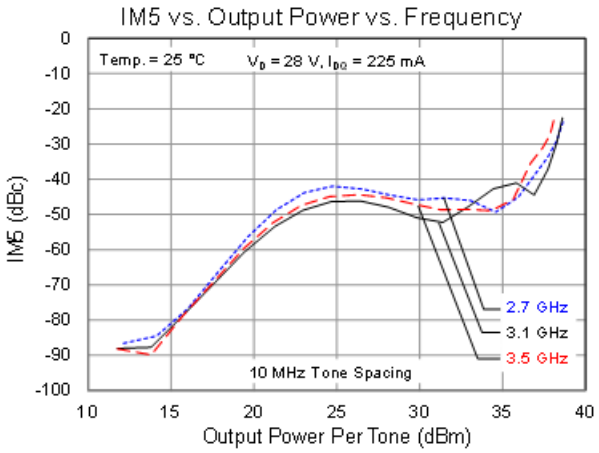
Typical Performance: Large Signal & Linearity

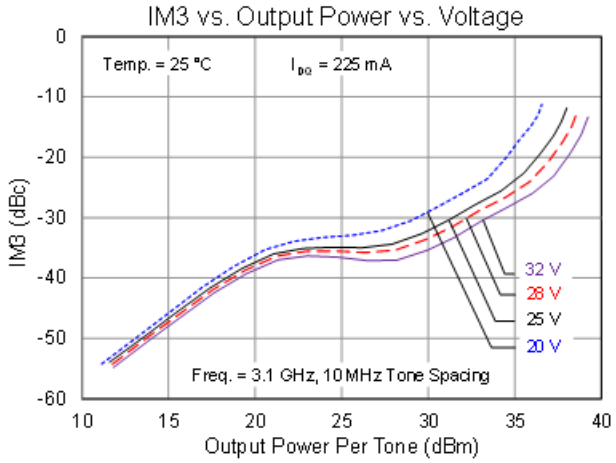
Condition: CW

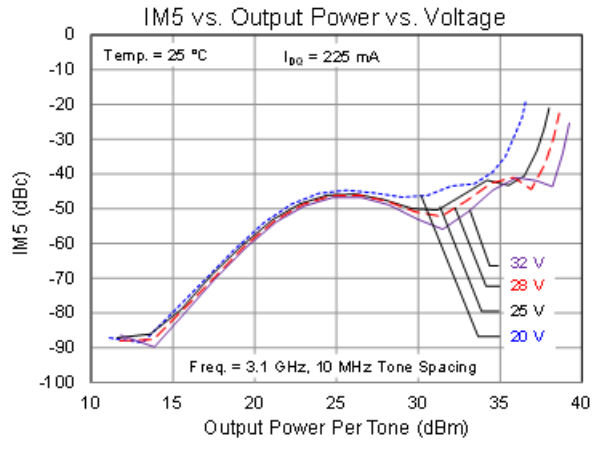






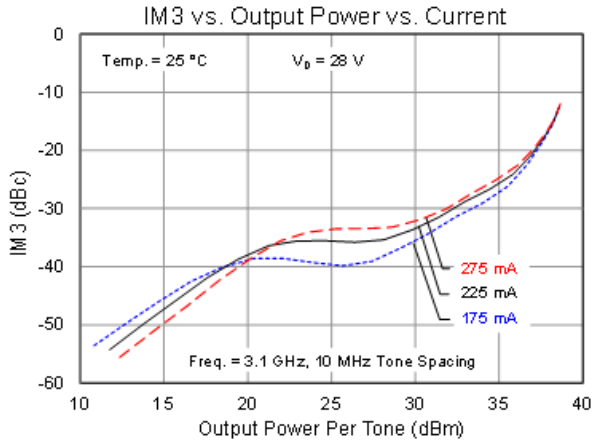


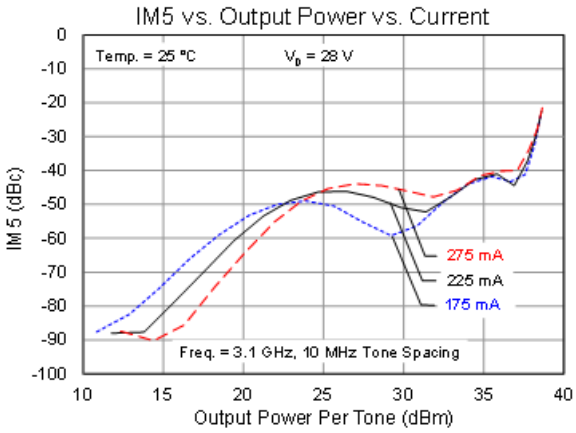


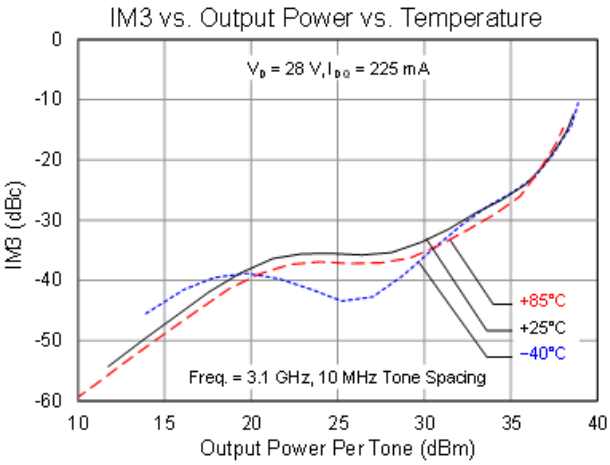


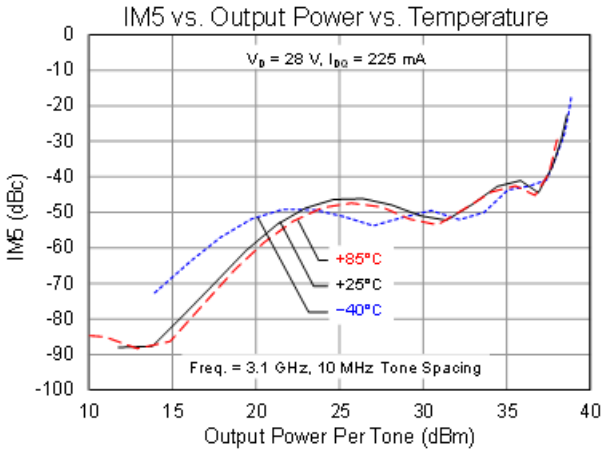
Typical Performance: Large Signal & Linearity

Condition: CW







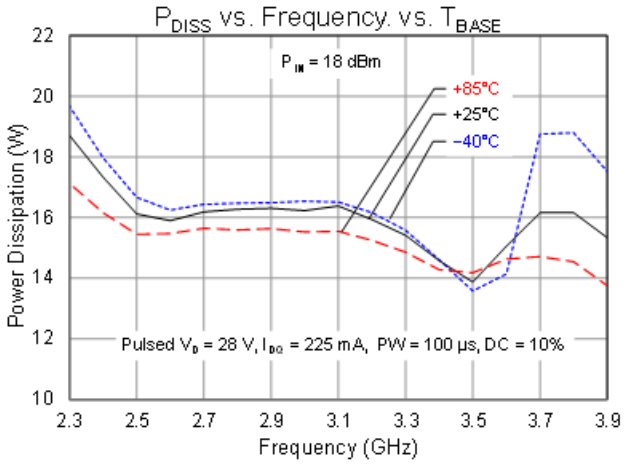


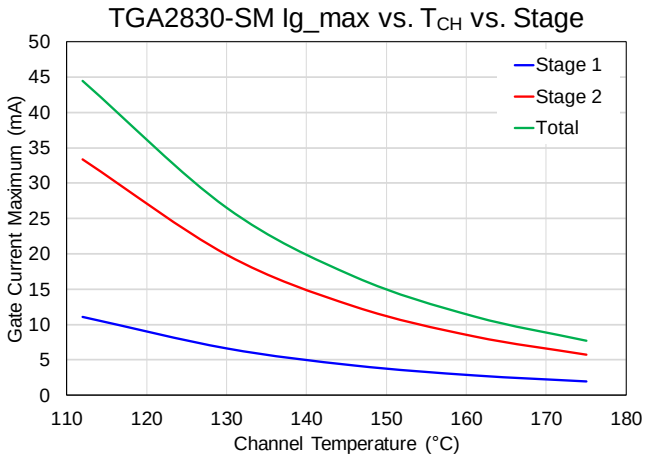
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})(1)	T_{BASE} = 85 °C, V_D = 28 V, I_{DQ} = 225 mA (Quiescent DC, CW), P_{DISS} = 6.3 W	2.129	°C/W
Channel Temperature (T_{CH})(2)		98.4	°C
Thermal Resistance (θ_{JC})(1)	T_{BASE} = 85 °C, V_D = 28 V, I_{D_Drive} = 1185 mA (PW = 100 µs, DC = 10%), Freq. = 3.1 GHz: P_{IN} = 18 dBm, P_{OUT} = 42.5 dBm, P_{DISS} = 15 W	1.825	°C/W
Channel Temperature (T_{CH}) (Under RF drive)(2)		112.4	°C

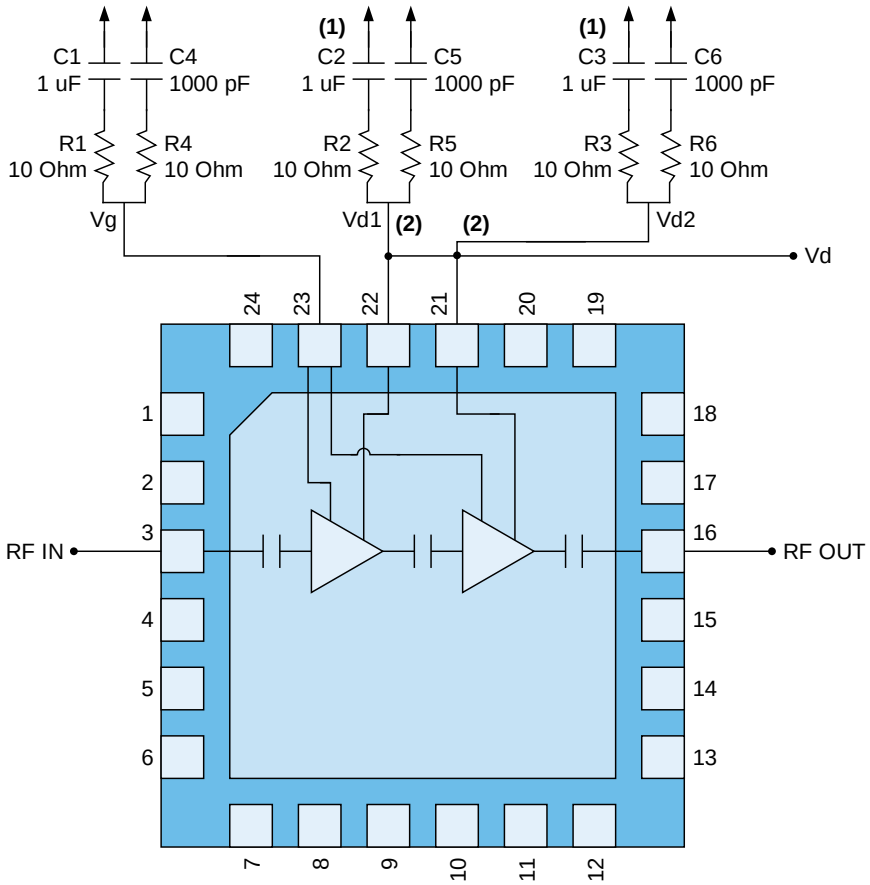
Notes:
1. Thermal resistance measured to back of package.
2. IR Scan equivalent temperatures. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Max. Gate Current





Application Information

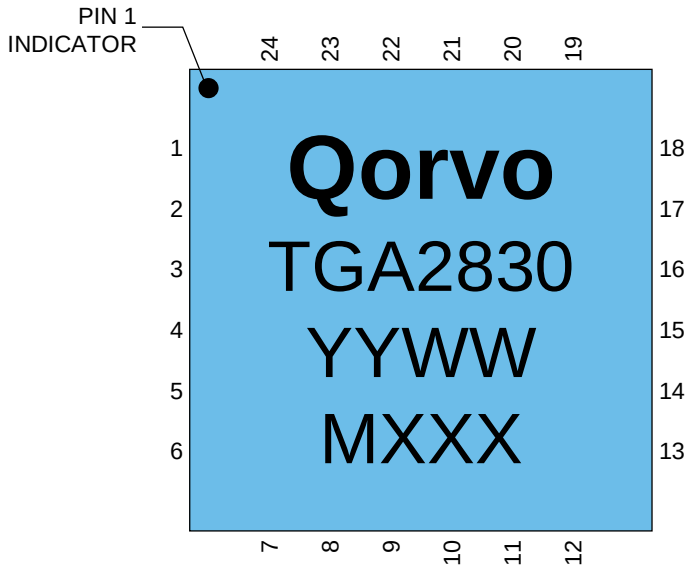


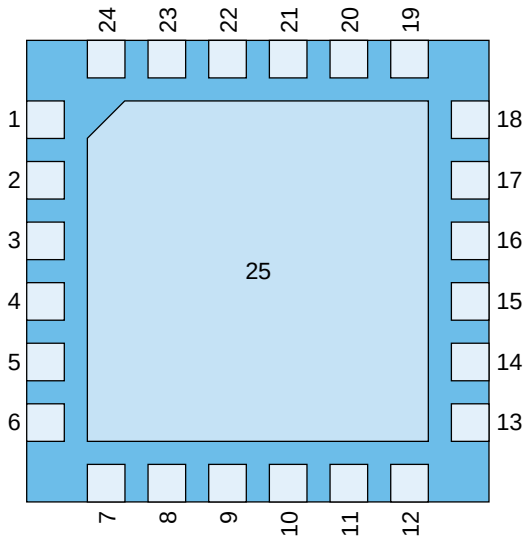
Notes:
1. Remove 1 uF capacitors if pulsing on drain
2. V_D: Tied V_{D1} & V_{D2} together

Bias-up Procedure
Set I_D limit to 1.4 A, I_G limit to 8 mA
Apply −5 V to V_G
Apply +28 V to V_D; ensure I_{DQ} is approx. 0 mA
Adjust V_G until I_{DQ} = 225 mA
Turn on RF supply

Bias-down Procedure
Turn off RF supply
Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
Set V_D to 0 V
Turn off V_D supply
Turn off V_G supply

Pin Layout

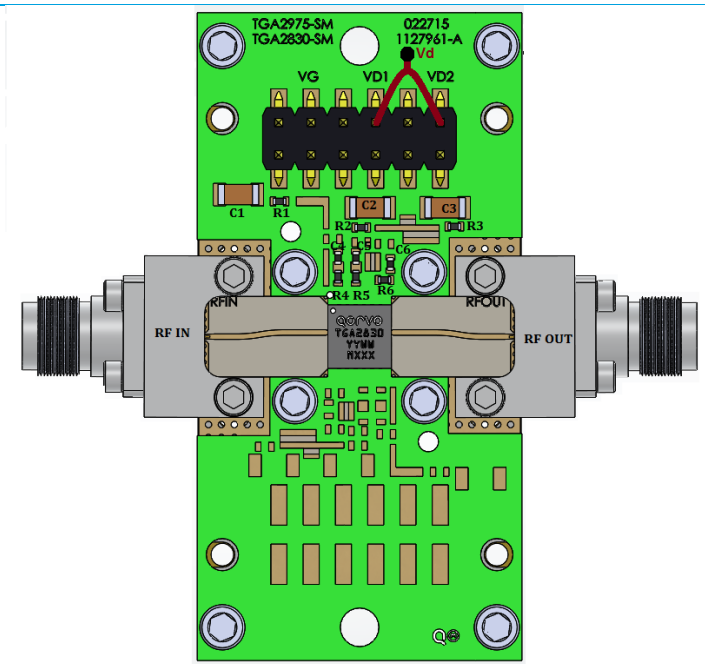




Pin Description

Pin No.	Symbol	Description
1, 2, 4–15, 17–20, 24	NC	No internal connection; can be grounded on PCB or left open
3	RF IN	Input; matched to 50 Ω; DC blocked
16	RF OUT	Output; matched to 50 Ω; DC blocked
21	DRAIN 2	Drain voltage; bias network is required; see recommended Application Information on page 13
22	DRAIN 1	Drain voltage; bias network is required; see recommended Application Information on page 13
23	GATE	Gate voltage; bias network is required; see recommended Application Information on page 13
25	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

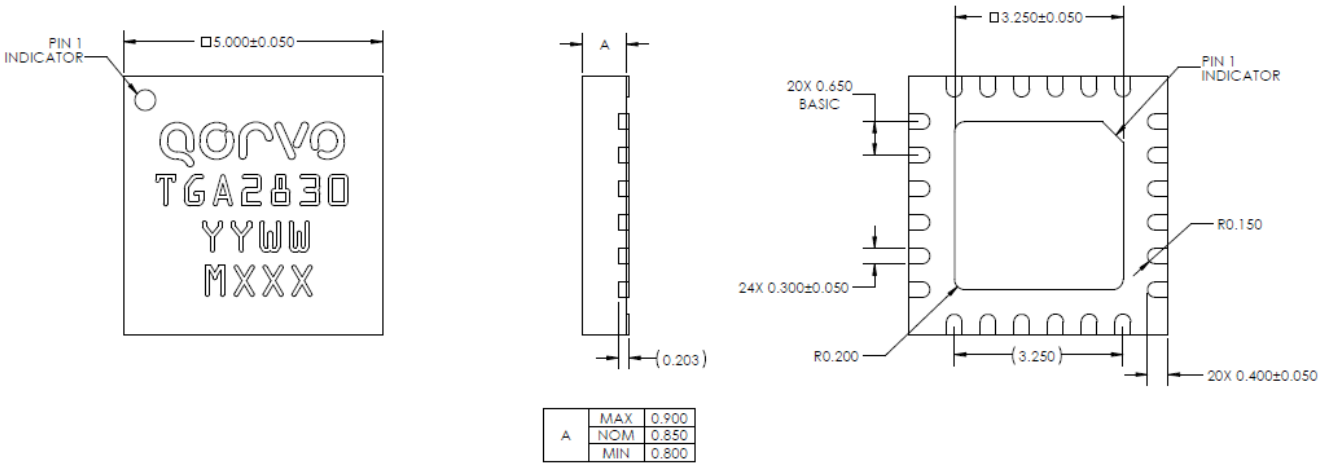
Evaluation Board



Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1–C3	1 µF	Cap, 1206, 50 V, 5%, X7R	Various	
C4 –C6	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
R1–R6	10 Ω	Res, 0402, 5%	Various	

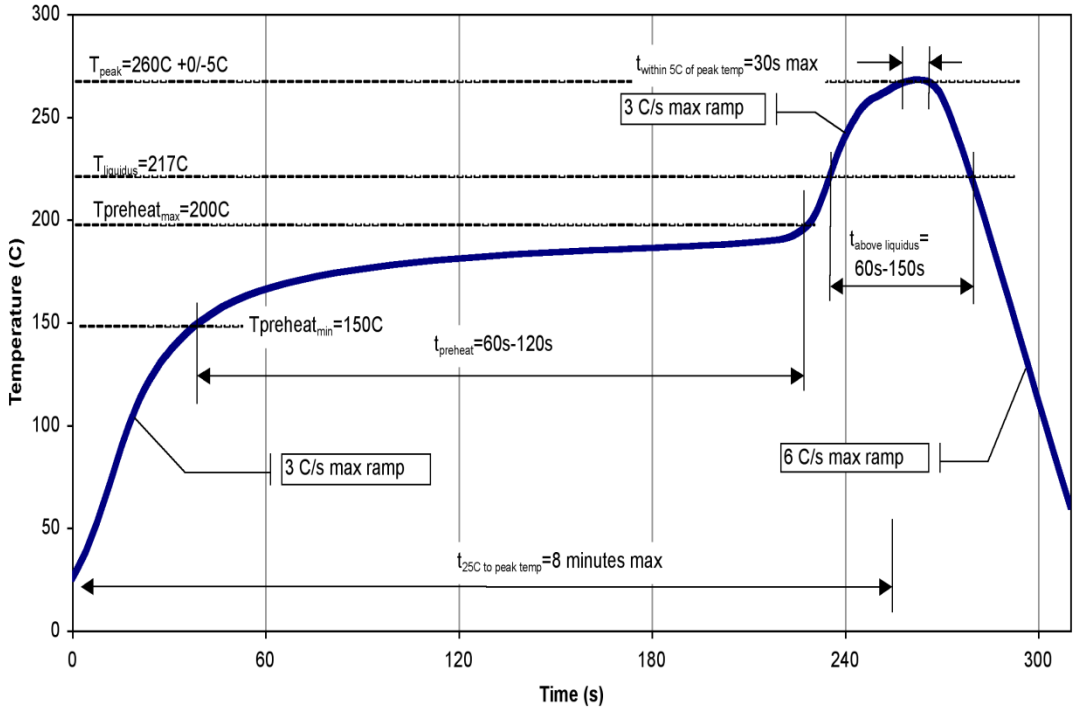
Mechanical Drawing



A	MAX	0.900
	NOM	0.850
	MIN	0.800

Units: millimeter (mm)
Tolerances: unless specified
x.xx = ± 0.01
x.xxx = ± 0.005
Materials:
Package Leads are Gold Plated.
Part is Mold Encapsulated.
Marking:
2830: Part number
YY: Part Assembly year
WW: Part Assembly week
MXXX: Batch ID

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	JEDEC JS-001
ESD – Charge Device Body Model (CDM)	C3	JESD22-C101
MSL – Moisture Sensitivity Level	MSL-3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

Web: www.qorvo.com

Tel: 1-844-890-8163

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