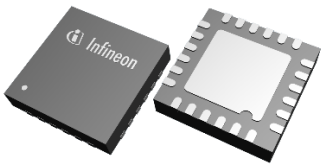
BGAP3D30H

Pre-Driver for Wireless Infrastructure Applications

Features

- Operation frequency range: 3100 to 4200 MHz
- High gain: 38.5 dB
- High output P1dB: 31 dBm
- High ACLR: 47 dBc
- Adjustable bias current (via external resistor)
- Fast switching for TDD support
- 100Ω differential input
- 5V supply voltage
- 24 pins leadless QFN package (4.0 x 4.0 mm^2)
- BiCMOS Technology



PG-VQFN-24 4x4mm^2

RoHS Halogen-Free

Green Lead-Free

Potential applications

- 4G/5G Cellular Infrastructure
    - Massive MIMO systems
    - Small cells

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The BGAP3D30H is a stand-alone packaged two-stage pre-driver amplifier. It is designed to be used in a TX line-up of a base station radio unit as a pre-driver for Doherty power amplifier. The BGAP3D30H is equipped with a tunable bias circuitry controlled by external resistor. This enables to optimize balance between linearity and power consumption in the target application. The input is 100Ω differential, the output is 50Ω single-ended.

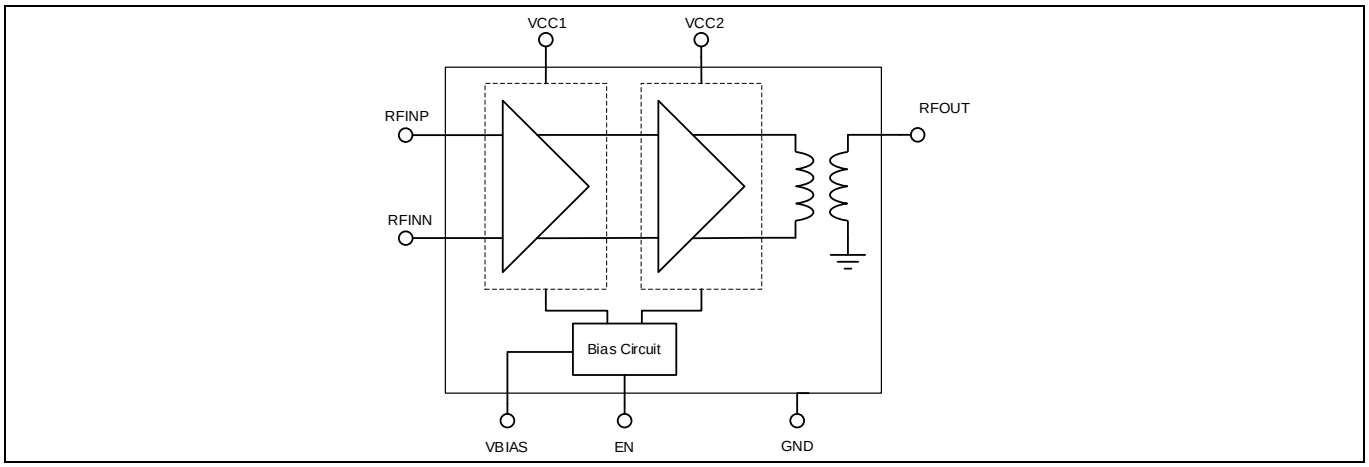


Figure 1 BGAP3D30H Block Diagram

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1 Pin Configuration

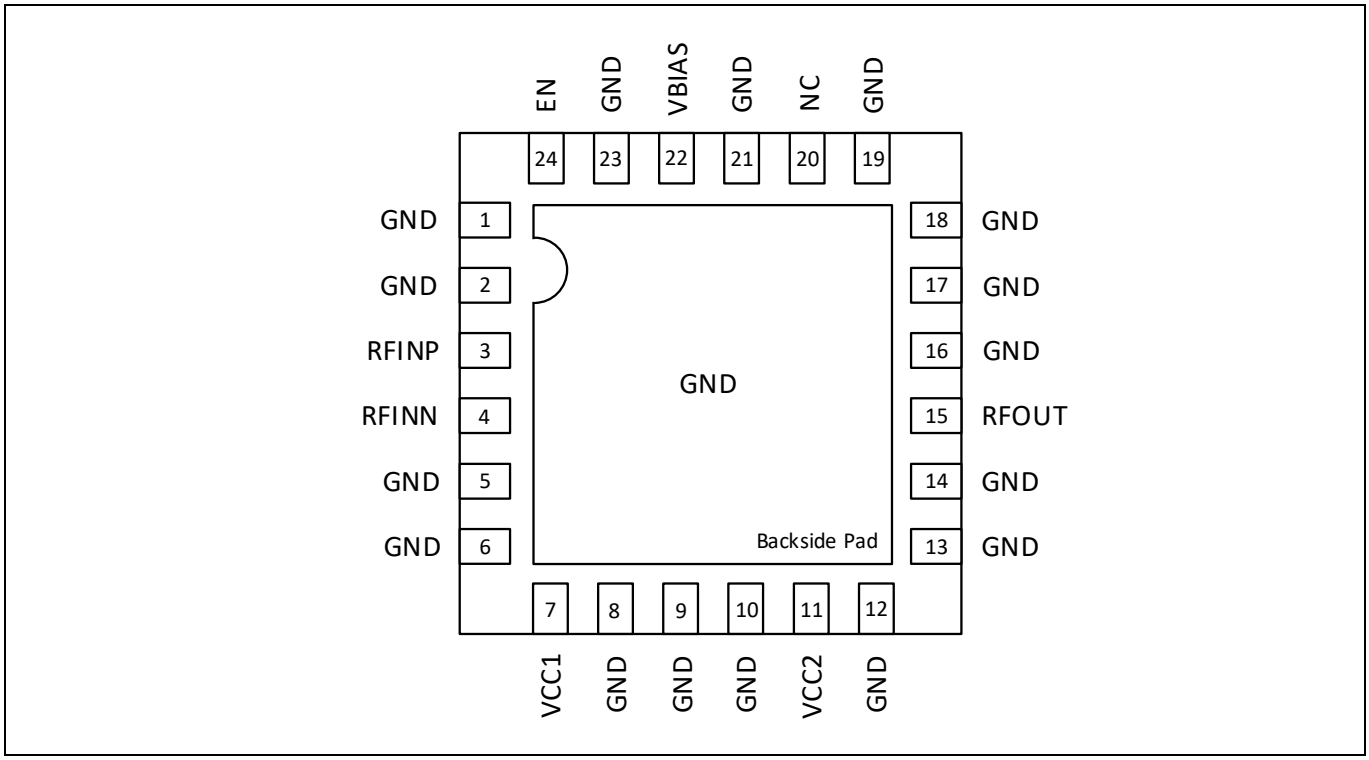

Figure 2 Pin assignment of BGAP3D30H – Top View

Table 1 Pin definition and function

Pin No.	Name	Function
1, 2, 5, 6, 8-10, 12-14, 16-19, 21, 23	GND	Ground connection
3	RFINP	RF Input +
4	RFINN	RF Input -
7	VCC1	1st stage DC voltage supply
11	VCC2	2nd stage DC voltage supply
15	RFOUT	RF Output
20	NC	Not connected internally. It can be left floating or connected to ground
22	VBIAS	Bias adjust for linearity/power consumption trade-off (pull-down resistor to GND)
24	EN	Chip enable/disable
Backside Pad	GND	Ground connection

2 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1]

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Supply Votage	V_{CC}	-0.5	–	5.5	V	–
Enable Voltage	V_{EN}	-0.3	–	V_{CCMax}	V	–
Storage Temperature	T_{STG}	-45	–	150	°C	–
Junction Temperature	T_J	-40	–	170	°C	–
DC voltage at RF Ports	$V_{RF,DC}$	0	–	0	V	–
RF Input Power CW	$P_{IN,CW}$	–	–	6	dBm	–

[1] All voltages refer to GND node unless otherwise specified

Warning: Stresses above the maximum values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

3 Specifications

3.1 Recommended Operating Conditions

Table 3 Operational ratings[1]

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Supply Votage	V_{CC}	4.75	–	5.25	V	–
Enable Voltage OFF	$V_{EN, OFF}$	0	–	0.69	V	–
Enable Voltage ON	$V_{EN, ON}$	1.07	–	V_{CC}	V	–
Operating Temperature	T_S	-40	–	115	°C	Solder joint temperature
Average Output Power	P_{avg}	–	18	18.5	dBm	

[1] All voltages refer to GND node unless otherwise specified

Power-up and power-down sequences
The following sequences are required to be respected during power-up/down of the device.
Power-up sequence: 1. VCC1 and VCC2 -> on; 2. EN -> on.
Power-down sequence: 1. EN -> off; 2. VCC1 and VCC2 -> off.
Deviating from these sequences may cause permanent damage.

3.2 ESD Ratings

Table 4 ESD Ratings[1]

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
ESD robustness HBM[2]	$V_{ESD,HBM}$	–	–	1	kV	On all pins
ESD robustness CDM[3]	$V_{ESD,CDM}$	–	–	250	V	On all pins

[1] All voltages refer to GND node unless otherwise specified

[2] Human Body Model ANSI/ESDA/JEDECJS-001 (R = 1.5kΩ, C = 100pF)

[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDECJS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

3.3 External components

Table 5 External components

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Bias adjust resistor	R_{BIAS}	16.2	20	26.1	kΩ	For I_{CC} control range of ±20%

3.4 Thermal Information

Table 6 Thermal resistance

Parameter	Symbol	Value	Unit	Note
Thermal Resistance: Junction – Solder pad	$R_{th, J-S}$	22.9	°K/W	At T_{amb} = 25°C

3.5 Electrical characteristics

Table 7 Electrical characteristics[1,2] (R_{BIAS} = 20kΩ)

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
RF Frequency	f_{RF}	3100	–	4200	MHz	–
Current Consumption OFF	$I_{CC, OFF}$	–	–	1.3	mA	–
Current Consumption ON	$I_{CC, ON}$	–	–	257	mA	No RF input signal
Current Consumption ON	$I_{CC, ON}$	–	–	315	mA	w/ RF output signal 18dBm
Input Return Loss	RL_{IN}	–	16	–	dB	At differential 100Ω input
Output Return Loss	RL_{OUT}	–	30	–	dB	At single-ended 50Ω output
Gain	G	37.8	40.1	–	dB	–
Gain Flatness	G_{FLAT}	–	–	0.35	dB	Defined in any 100 MHz within operational band
Output P1dB	OP_{1dB}	29.4	31.4	–	dBm	–
Output IP3	OIP_3	–	41.1	–	dBm	PIN1=PIN2=-30dBm, Δf=1MHz
Adjacent Channel Leakage Ratio	$ACLR$	–	-53.8	-41.5	dBc	20MHz E-TM1.1 with 10.2 dB PAPR @Pout=18 dBm
Common Mode Rejection Ratio	$CMRR$	30	–	–	dB	–
Noise Figure	NF	–	–	3.3	dB	–
Switching ON Time	T_{ON}	–	–	1.8	µs	Gain within 0.1dB amplitude and 1° phase of final value
Switching OFF Time	T_{OFF}	–	–	0.3	µs	Gain within<5% and power dissipation <10% than in ON state

[1] All voltages refer to GND node unless otherwise specified

[2] Typical values: T=25°C, V_{CC}=5V, f_{RF}=3.6GHz, R_{BIAS}=20kΩ. Min/Max values defined over process, voltage, temperature and frequency variations based on characterization.

4 Application Board

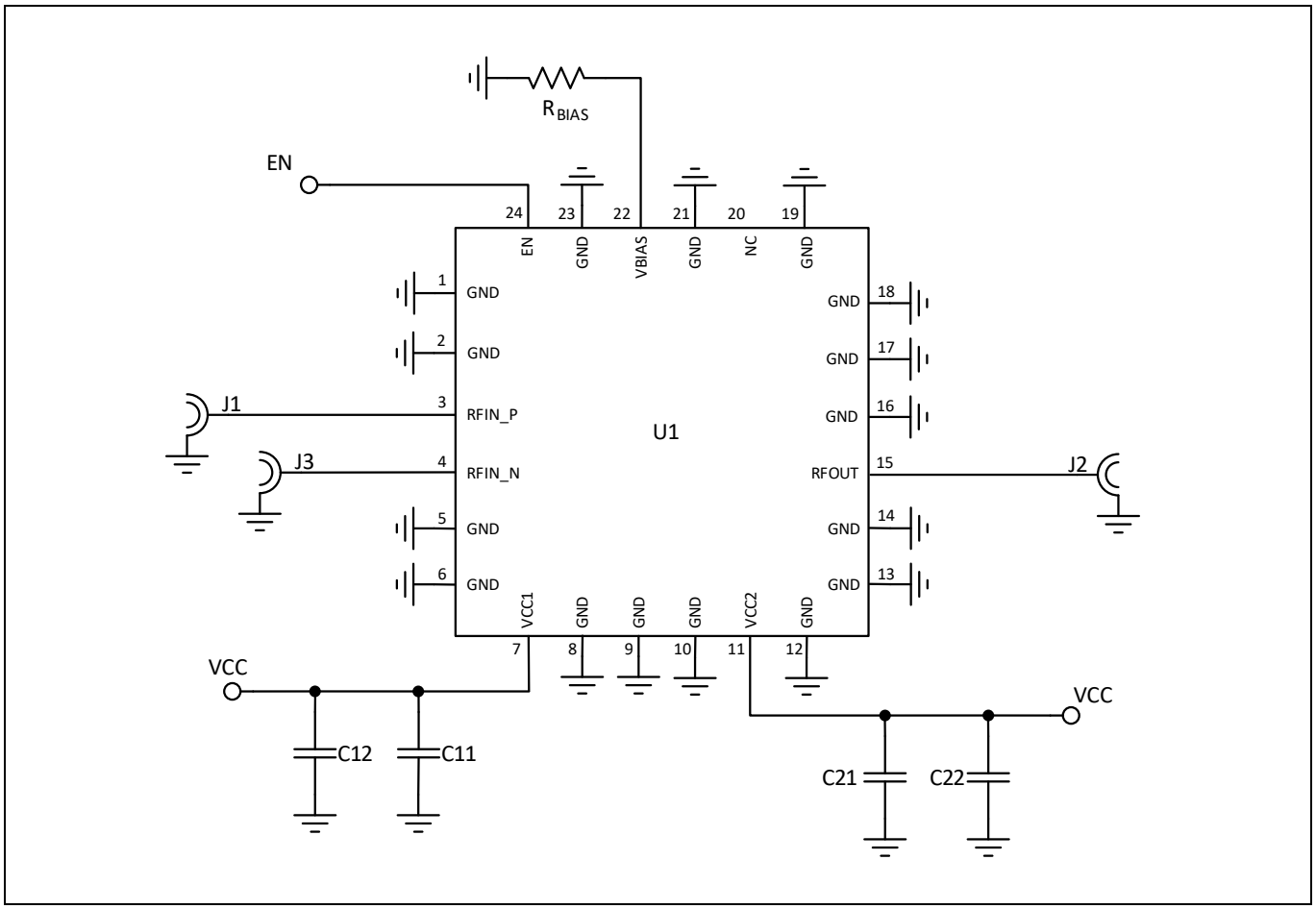

Figure 3 BGAP3D30H Application schematic diagram

Table 8 Bill of Materials

Name	Value	Description	Part Number	Manufacturer
C11, C21	10 nF	Capacitor, X7R, 0402	KGM05AR71C103KH	Kyocera
C12, C22	1 uF	Capacitor, X7R, 0402	GRM155Z71A105KE01D	Murata
R_{BIAS}	20kΩ	Resistor, 0402, +/-1%	MCS04020C2002FE000	Vishay
J1, J2, J3	–	Connector, SMA	–	–
U1	–	Pre-Driver, PG-VQFN-24-20	BGAP3D30H	Infineon

5 Package Information

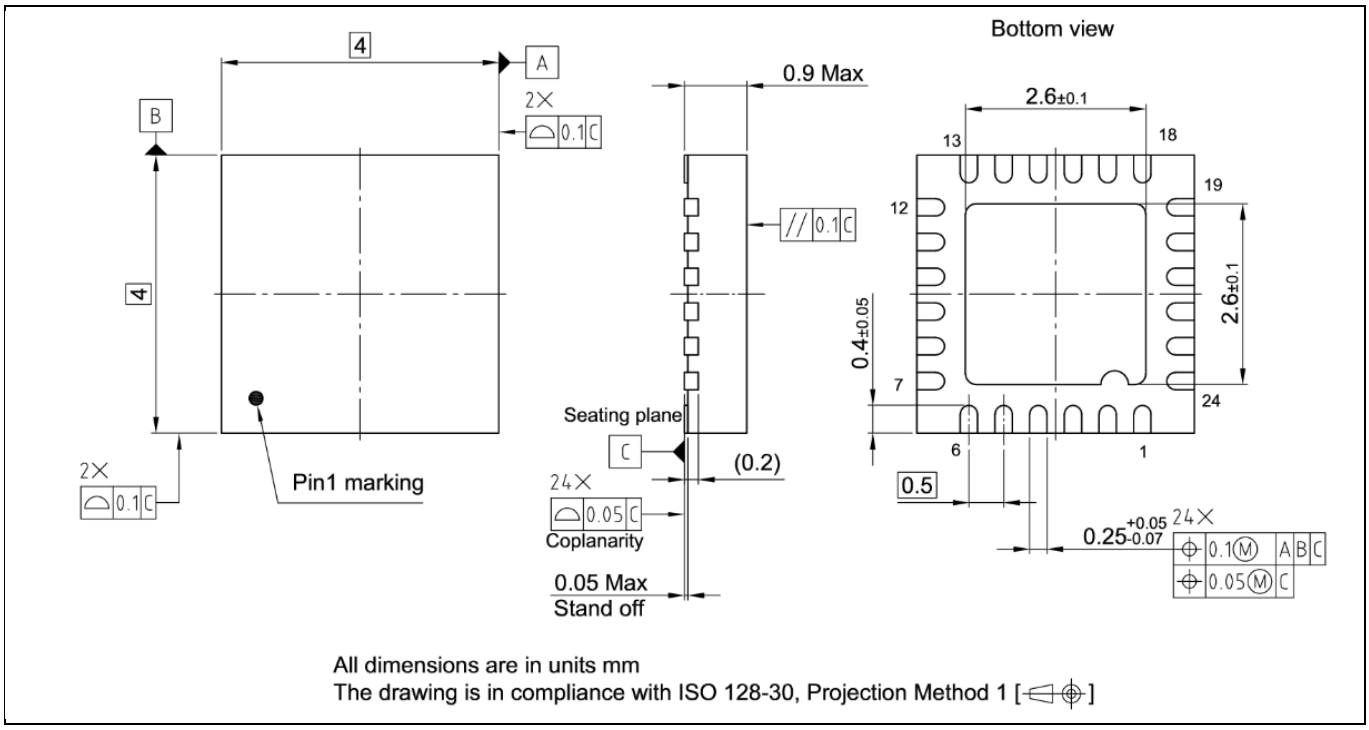

Figure 4 PG-VQFN-24-20 Package Outline (4.0mm x 4.0mm x 0.9mm)

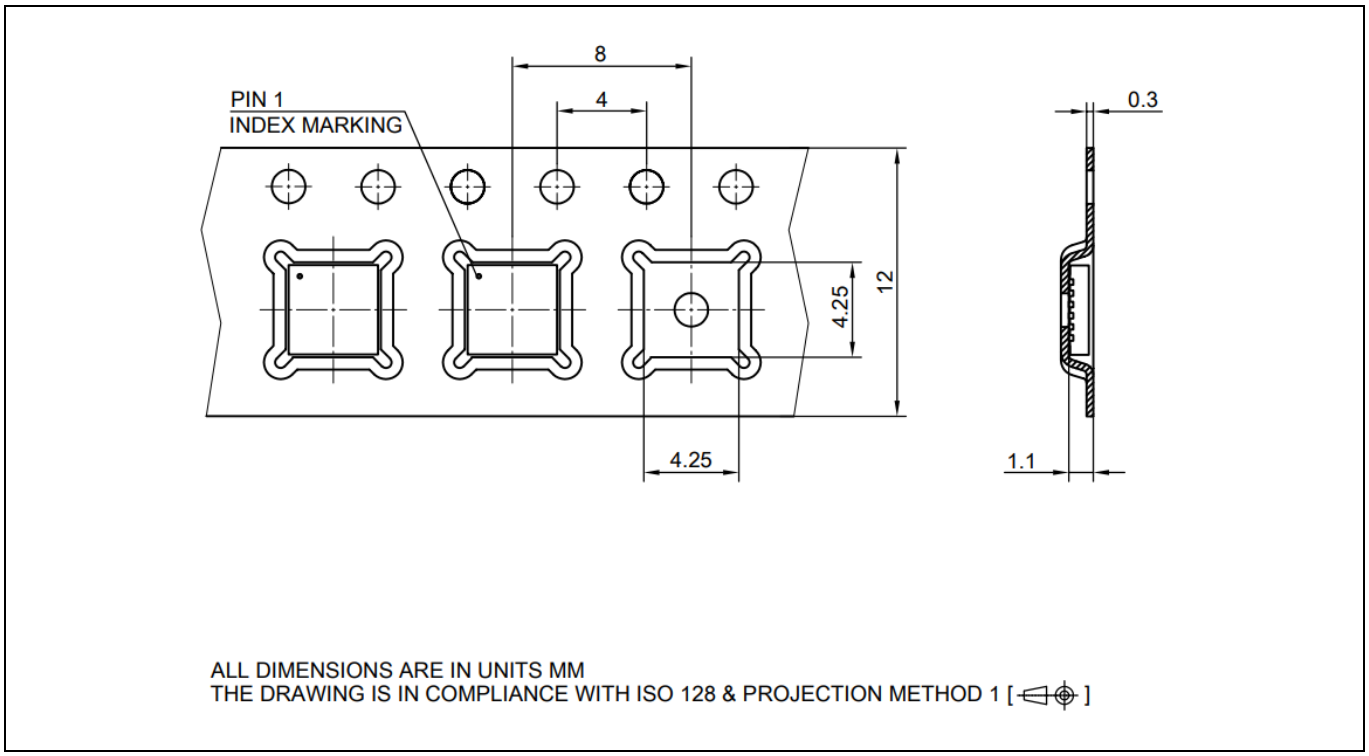

Figure 5 PG-VQFN-24-20 Carrier Tape

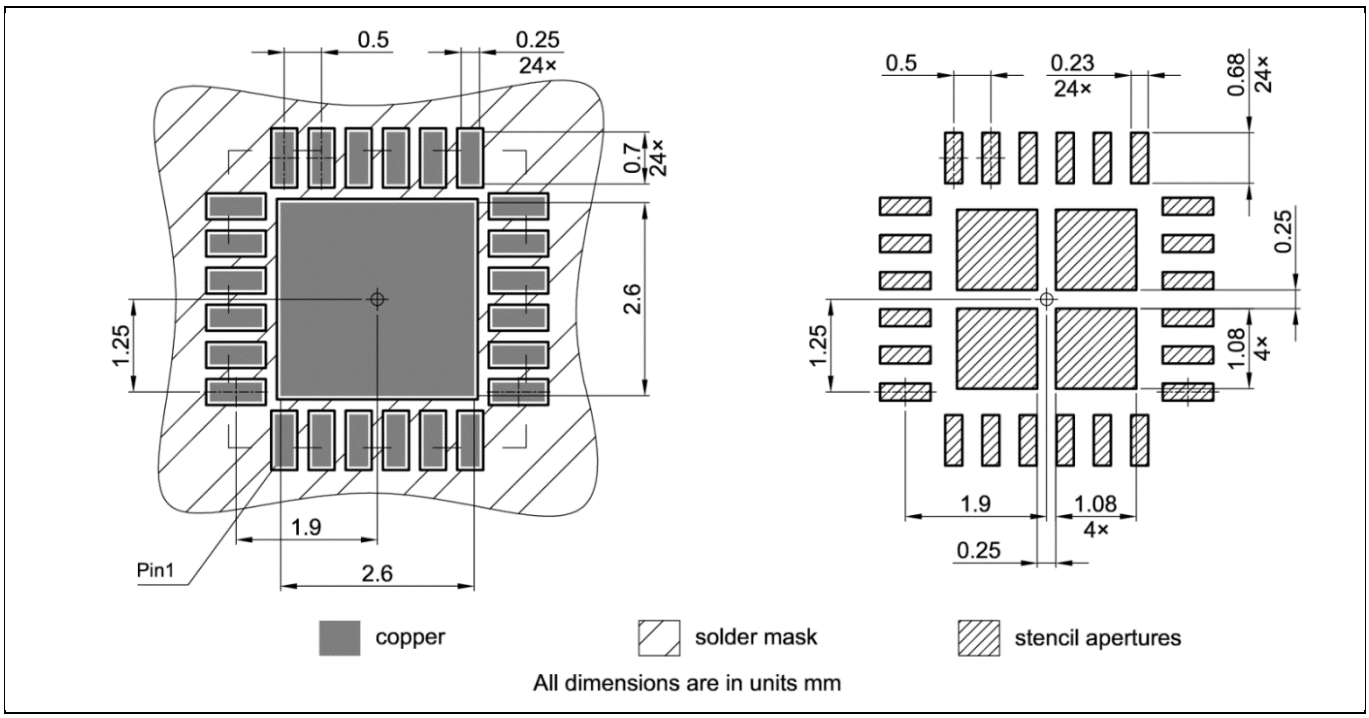

Figure 6 PG-VQFN-24-20 Footprint Recommendation

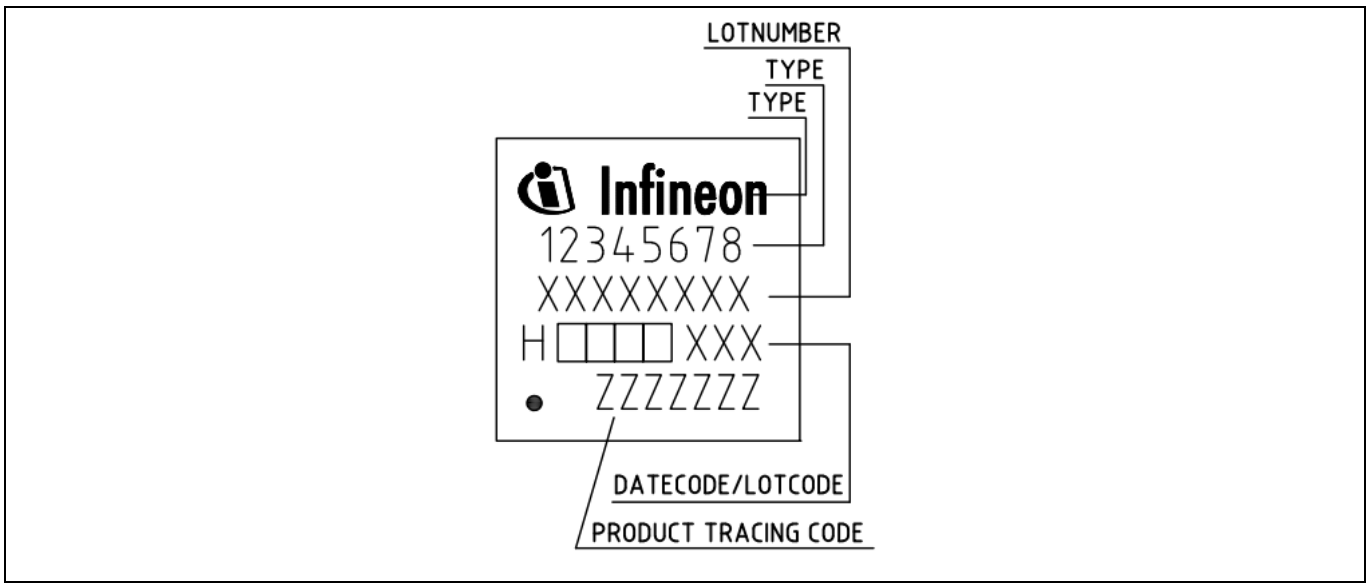

Figure 7 Marking Specification PG-VQFN-24-20 (top view)

Product Name	Marking Type	Datecode
BGAP3D30H	BP3D3H	YYWW (YY=year, WW=week)

Revision history

Document version	Date of release	Description of changes
V1.0	2023-06-16	First draft
V1.1	2023-06-19	Carrier Tape dimensions added
V1.2	2023-07-06	Bias resistor connection, Rth update
V1.3	2024-01-09	Bias resistor connection, Rth update
V2.0	2024-06-24	Table 2: VBIAS removed Table 3: adding Average Output Power range data Table 5: added min/max values for RBIAS Table 6: Rth changed to new value and condition Table 7: values and typo, adding table 2 line for P_{avg}, added Rbias =20k in header information. Table 8 component details added Added Figure 6, 7 for package and footprint

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