THE DATASHEET OF

BGM687U50E6327XUMA1

BGM687U50

7x LNA Bank with Output Cross-Switch for 5G

Features

- Wide operating frequency range: 600 - 2700 MHz
- 2x LB LNA group: 600-960 MHz
- 5x MLB/MHB LNA group: 1400-2700 MHz
- Highly flexible output MUX
- Gain Mode Support for MediaTek, LSI and Qualcomm platforms
- Support of 4x4 MIMO and EN-DC with just 2 LNA-Banks
- Programmable power gain:21 dB down to -12dB in 3dB steps
- Programmable current consumption for each LNA: 2.5 - 10 mA
- Noise figure for high gain mode: 0.8 dB
- Support of 1.2V and 1.8V Vdd/Vio
- RF output internally matched to 50 Ω
- Suitable for LTE / LTE-Advanced, 4G and 5G applications
- Integrated DC block capacitors at input and output
- Pin to pin compatible with MT6191 LNA bank
- Low power operation
- Small form factor 2.8 mm x 2.8 mm
- RoHS and WEEE compliant package
- USID select pin

Potential Applications

The BGM687U50 is a 7x LNA-Bank with 2 Low Band and 5 Mid/High Band LNA groups with a complex output 7P7T cross-switch, designed for EN_DC/CA and MIMO operations. The LNA-Bank supports 12 Gain Steps to optimize SNR, blocking performance and power consumption. The wideband LNA design with programmable gain (MIPI 3.0) and a highly configurable output MUX (7P7T) offer maximum system design flexibility.

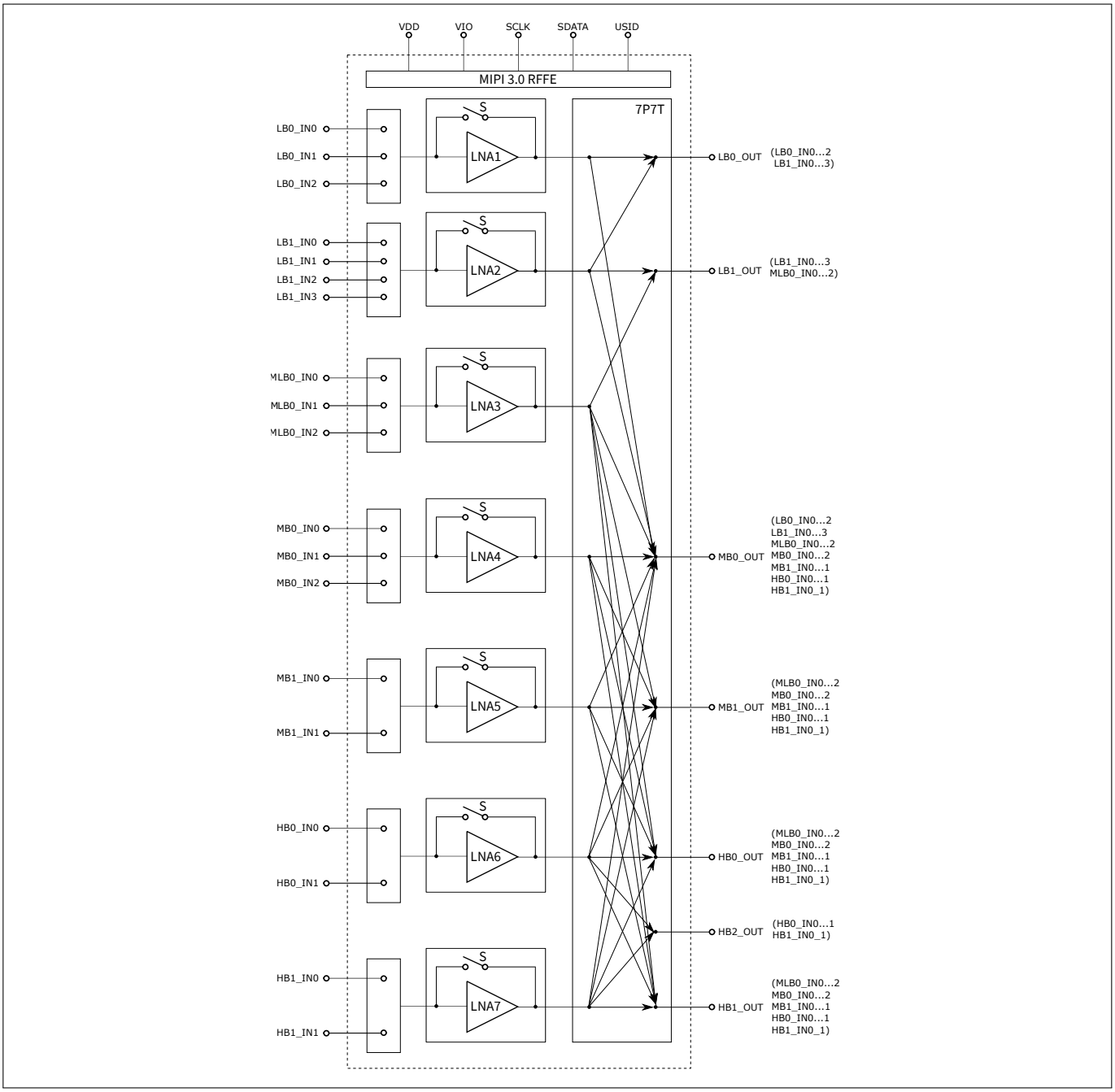
Product Validation

Fully qualified according to JEDEC for Industrial Applications.

BGM687U50

7x LNA Bank with Output Cross-Switch for 5G

Block Diagram



Product Name	Marking	Package
BGM687U50	finA	PG-WF2BGA-50-1

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1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage VDD [1]	V_{DD}	-0.5	–	2.2	V	–
Maximum DC voltage on RF ports and RF grounds [2]	V_{RFDC}	0	–	0	V	–
RF input power [3]	P_{IN}	–	–	25	dBm	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-30	–	85	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
ESD capability, HBM [4]	V_{ESD_HBM}	-2000	–	+2000	V	At Non-RF Ports
		-1500	–	+1500	V	At RF Ports
ESD capability, CDM	V_{ESD_CDM}	-750	–	+750	V	–
RFFE supply voltage	V_{IO}	-0.5	–	2.2	V	–
RFFE control voltage levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7 (max. 2.2)	V	–

[1] All voltages refer to GND-Nodes unless otherwise noted
[2] If DC voltage is applied to any RF ports it has to be 0V
[3] CW signal, VSWR 10:1, tested at device level, Vdd/Vio typ, 25 C, for 30s and all modes
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R=1.5 kΩ, C=100 pF)

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

2 DC Characteristics and Timing Specification

Table 2: DC Characteristics at T_A = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage [1]	V_{DD}	1.10	1.20	1.40	V	Low Voltage Domain (see Reg 0x40 CONFIG)
		1.40	1.80	1.95	V	High Voltage Domain (see Reg 0x40 CONFIG)
Supply current (per LNA) [2]	I_{DD}	9.0	10.7	13.0	mA	Gain Mode G12/G11 - Bias Mode 7
		4.5	5.6	6.5	mA	Gain Mode G10/G9 - Bias Mode 4
		3.5	4.5	5.5	mA	Gain Mode G8/G7 - Bias Mode 3
		2.5	3.5	4.5	mA	Gain Mode G6/G5 - Bias Mode 1
Supply current in Normal Mode [2]	I_{DD_NM}	50	80	120	µA	All LNAs OFF or G1/G2/G3/G4 - Any Bias Mode
Supply current in Secondary Mode [2]	I_{DD_SM}	–	–	5	µA	–
RFFE supply voltage [1]	V_{IO}	1.10	1.20	1.30	V	–
		1.65	1.80	1.95	V	–
RFFE supply current [2]	I_{VIO}	1.5	3.0	9.0	µA	Idle State
RFFE input high voltage [3]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage [3]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage [3]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage [3]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{SCLK_IN}, C_{SDATA_IN}	–	–	2	pF	–
RFFE control load capacitance	C_{SDATA_L}	–	–	80	pF	Programmable driver strength (Register 0x2B)
RFFE SCLK write frequency	f_{SCLK_W}	0.032	–	52	MHz	–
RFFE SCLK read frequency	f_{SCLK_R}	0.032	–	26	MHz	–

[1] All V_{DD} and V_{IO} combinations of 1.2V and 1.8V are supported
[2] Tested by ATE
[3] SCLK/USID (input voltage) and SDATA (input and output voltage)

3 RF Characteristics, LNAs + 7P7T Switch

Table 3: RF Characteristics LB (LNA1 & LNA2) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 617– 960 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	16.9	18.6	20.2	dB	Gain Mode G11 - Bias Mode 7
		14.2	15.9	17.4	dB	Gain Mode G10 - Bias Mode 4
		11.6	13.1	14.6	dB	Gain Mode G9 - Bias Mode 4
		8.6	10.1	11.5	dB	Gain Mode G8 - Bias Mode 3
		5.8	7.3	8.6	dB	Gain Mode G7 - Bias Mode 3
		2.1	3.5	4.7	dB	Gain Mode G6 - Bias Mode 1
		-0.7	0.8	2.0	dB	Gain Mode G5 - Bias Mode 1
		-5.8	-3.9	-2.4	dB	Gain Mode G4 - Any Bias Mode
		-8.9	-6.6	-5.1	dB	Gain Mode G3 - Any Bias Mode
		-11.7	-9.5	-8.0	dB	Gain Mode G2 - Any Bias Mode
		-14.8	-12.4	-11.0	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.9	1.4	dB	Gain Mode G11 - Bias Mode 7
		–	1.1	1.8	dB	Gain Mode G10 - Bias Mode 4
		–	1.6	2.3	dB	Gain Mode G9 - Bias Mode 4
		–	2.3	3.0	dB	Gain Mode G8 - Bias Mode 3
		–	3.2	3.9	dB	Gain Mode G7 - Bias Mode 3
		–	5.8	6.6	dB	Gain Mode G6 - Bias Mode 1
		–	8.3	9.1	dB	Gain Mode G5 - Bias Mode 1
		–	3.9	5.8	dB	Gain Mode G4 - Any Bias Mode
		–	6.6	8.9	dB	Gain Mode G3 - Any Bias Mode
		–	9.5	11.7	dB	Gain Mode G2 - Any Bias Mode
		–	12.4	14.8	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	9.6	11.1	–	dB	Gain Mode G11 - Bias Mode 7
		7.5	8.8	–	dB	Gain Mode G10 - Bias Mode 4
		12.7	15.2	–	dB	Gain Mode G9 - Bias Mode 4
		9.8	13.7	–	dB	Gain Mode G8 - Bias Mode 3
		9.4	13.4	–	dB	Gain Mode G7 - Bias Mode 3
		7.6	10.1	–	dB	Gain Mode G6 - Bias Mode 1
		7.4	8.9	–	dB	Gain Mode G5 - Bias Mode 1
		6.1	8.1	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 4: Continued RF Characteristics LB (LNA1 & LNA2) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 617–960 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	6.3	9.1	–	dB	Gain Mode G11 - Bias Mode 7
		5.9	8.3	–	dB	Gain Mode G10 - Bias Mode 4
		6.7	9.5	–	dB	Gain Mode G9 - Bias Mode 4
		6.6	9.3	–	dB	Gain Mode G8 - Bias Mode 3
		6.8	9.5	–	dB	Gain Mode G7 - Bias Mode 3
		7.0	9.3	–	dB	Gain Mode G6 - Bias Mode 1
		6.7	8.7	–	dB	Gain Mode G5 - Bias Mode 1
		6.0	7.1	–	dB	Gain Mode G4 - Any Bias Mode
		10.3	11.3	–	dB	Gain Mode G3 - Any Bias Mode
		11.9	13.5	–	dB	Gain Mode G2 - Any Bias Mode
		13.9	16.2	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	24.0	30.0	–	dB	Gain Mode G11...G5 - Bias Mode 7/4/3/1
		2.4	3.9	–	dB	Gain Mode G4 - Any Bias Mode
		5.1	6.6	–	dB	Gain Mode G3 - Any Bias Mode
		8.0	9.5	–	dB	Gain Mode G2 - Any Bias Mode
		11.0	12.4	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-8.7	-5.8	–	dBm	Gain Mode G11 - Bias Mode 7
		-4.9	-2.6	–	dBm	Gain Mode G10 - Bias Mode 4
		-2.7	0.4	–	dBm	Gain Mode G9 - Bias Mode 4
		-5.2	-2.2	–	dBm	Gain Mode G8 - Bias Mode 3
		-3.1	-0.6	–	dBm	Gain Mode G7 - Bias Mode 3
		-4.0	-1.9	–	dBm	Gain Mode G6 - Bias Mode 1
		-1.0	1.2	–	dBm	Gain Mode G5 - Bias Mode 1
		26	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-19.7	-16.8	–	dBm	Gain Mode G11 - Bias Mode 7
		-18.1	-14.8	–	dBm	Gain Mode G10 - Bias Mode 4
		-15.9	-13.1	–	dBm	Gain Mode G9 - Bias Mode 4
		-15.9	-13.4	–	dBm	Gain Mode G8 - Bias Mode 3
		-13.9	-11.5	–	dBm	Gain Mode G7 - Bias Mode 3
		-13.5	-11.4	–	dBm	Gain Mode G6 - Bias Mode 1
		-10.9	-8.6	–	dBm	Gain Mode G5 - Bias Mode 1
		>12	>12	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 5: RF Characteristics LB (LNA1 & LNA2) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 617– 960 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	17.6	19.3	20.9	dB	Gain Mode G11 - Bias Mode 7
		14.6	16.3	17.9	dB	Gain Mode G10 - Bias Mode 4
		12.1	13.6	15.0	dB	Gain Mode G9 - Bias Mode 4
		9.0	10.5	11.7	dB	Gain Mode G8 - Bias Mode 3
		6.2	7.7	9.0	dB	Gain Mode G7 - Bias Mode 3
		2.3	3.8	5.0	dB	Gain Mode G6 - Bias Mode 1
		-0.4	1.1	2.1	dB	Gain Mode G5 - Bias Mode 1
		-5.9	-4.0	-2.4	dB	Gain Mode G4 - Any Bias Mode
		-9.0	-6.7	-5.1	dB	Gain Mode G3 - Any Bias Mode
		-11.8	-9.6	-8.0	dB	Gain Mode G2 - Any Bias Mode
		-14.9	-12.5	-11.0	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.8	1.3	dB	Gain Mode G11 - Bias Mode 7
		–	1.1	1.8	dB	Gain Mode G10 - Bias Mode 4
		–	1.6	2.3	dB	Gain Mode G9 - Bias Mode 4
		–	2.2	2.9	dB	Gain Mode G8 - Bias Mode 3
		–	3.2	3.9	dB	Gain Mode G7 - Bias Mode 3
		–	5.7	6.5	dB	Gain Mode G6 - Bias Mode 1
		–	8.3	9.1	dB	Gain Mode G5 - Bias Mode 1
		–	4.0	5.9	dB	Gain Mode G4 - Any Bias Mode
		–	6.7	9.0	dB	Gain Mode G3 - Any Bias Mode
		–	9.6	11.8	dB	Gain Mode G2 - Any Bias Mode
		–	12.5	14.9	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	10.3	12.0	–	dB	Gain Mode G11 - Bias Mode 7
		7.8	9.1	–	dB	Gain Mode G10 - Bias Mode 4
		12.7	15.7	–	dB	Gain Mode G9 - Bias Mode 4
		10.0	14.0	–	dB	Gain Mode G8 - Bias Mode 3
		10.0	13.8	–	dB	Gain Mode G7 - Bias Mode 3
		7.8	10.2	–	dB	Gain Mode G6 - Bias Mode 1
		7.4	9.0	–	dB	Gain Mode G5 - Bias Mode 1
		6.3	8.1	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 6: Continued RF Characteristics LB (LNA1 & LNA2) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 617–960 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	6.3	9.0	–	dB	Gain Mode G11 - Bias Mode 7
		5.9	8.2	–	dB	Gain Mode G10 - Bias Mode 4
		6.7	9.5	–	dB	Gain Mode G9 - Bias Mode 4
		6.6	9.3	–	dB	Gain Mode G8 - Bias Mode 3
		6.8	9.6	–	dB	Gain Mode G7 - Bias Mode 3
		7.0	9.3	–	dB	Gain Mode G6 - Bias Mode 1
		6.7	8.8	–	dB	Gain Mode G5 - Bias Mode 1
		6.0	7.1	–	dB	Gain Mode G4 - Any Bias Mode
		10.3	11.3	–	dB	Gain Mode G3 - Any Bias Mode
		11.9	13.5	–	dB	Gain Mode G2 - Any Bias Mode
		13.9	16.2	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	24.0	30.0	–	dB	Gain Mode G11...G5 - Bias Mode 7/4/3/1
		2.4	4.0	–	dB	Gain Mode G4 - Any Bias Mode
		5.1	6.7	–	dB	Gain Mode G3 - Any Bias Mode
		8.0	9.6	–	dB	Gain Mode G2 - Any Bias Mode
		11.0	12.5	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-5.1	-3.1	–	dBm	Gain Mode G11 - Bias Mode 7
		-3.9	-0.7	–	dBm	Gain Mode G10 - Bias Mode 4
		-2.5	1.8	–	dBm	Gain Mode G9 - Bias Mode 4
		-4.4	-1.3	–	dBm	Gain Mode G8 - Bias Mode 3
		-2.2	0.3	–	dBm	Gain Mode G7 - Bias Mode 3
		-2.7	-0.8	–	dBm	Gain Mode G6 - Bias Mode 1
		0.2	2.4	–	dBm	Gain Mode G5 - Bias Mode 1
		26	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-16.4	-13.2	–	dBm	Gain Mode G11 - Bias Mode 7
		-17.5	-13.4	–	dBm	Gain Mode G10 - Bias Mode 4
		-15.7	-12.6	–	dBm	Gain Mode G9 - Bias Mode 4
		-15.9	-13.3	–	dBm	Gain Mode G8 - Bias Mode 3
		-13.9	-11.5	–	dBm	Gain Mode G7 - Bias Mode 3
		-13.6	-11.5	–	dBm	Gain Mode G6 - Bias Mode 1
		-11.0	-8.9	–	dBm	Gain Mode G5 - Bias Mode 1
		>12	>12	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 7: RF Characteristics MLB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 1427 MHz – 1518 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	19.7	21.9	23.9	dB	Gain Mode G12 - Bias Mode 7
		16.4	18.5	20.2	dB	Gain Mode G11 - Bias Mode 7
		13.5	15.6	17.4	dB	Gain Mode G10 - Bias Mode 4
		11.2	13.2	14.9	dB	Gain Mode G9 - Bias Mode 4
		8.2	10.2	11.9	dB	Gain Mode G8 - Bias Mode 3
		5.1	7.1	8.6	dB	Gain Mode G7 - Bias Mode 3
		0.9	2.9	4.4	dB	Gain Mode G6 - Bias Mode 1
		-2.2	-0.2	0.7	dB	Gain Mode G5 - Bias Mode 1
		-5.6	-4.3	-2.8	dB	Gain Mode G4 - Any Bias Mode
		-8.1	-6.5	-5.0	dB	Gain Mode G3 - Any Bias Mode
		-11.2	-9.5	-8.0	dB	Gain Mode G2 - Any Bias Mode
		-13.6	-12.3	-10.8	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.6	1.1	dB	Gain Mode G12 - Bias Mode 7
		–	0.9	1.4	dB	Gain Mode G11 - Bias Mode 7
		–	1.1	1.8	dB	Gain Mode G10 - Bias Mode 4
		–	1.6	2.3	dB	Gain Mode G9 - Bias Mode 4
		–	2.2	2.9	dB	Gain Mode G8 - Bias Mode 3
		–	3.2	3.9	dB	Gain Mode G7 - Bias Mode 3
		–	5.7	6.5	dB	Gain Mode G6 - Bias Mode 1
		–	8.7	9.5	dB	Gain Mode G5 - Bias Mode 1
		–	4.3	5.6	dB	Gain Mode G4 - Any Bias Mode
		–	6.5	8.1	dB	Gain Mode G3 - Any Bias Mode
		–	9.5	11.2	dB	Gain Mode G2 - Any Bias Mode
		–	12.3	13.6	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	5.5	6.0	–	dB	Gain Mode G12 - Bias Mode 7
		6.7	8.3	–	dB	Gain Mode G11 - Bias Mode 7
		7.3	8.7	–	dB	Gain Mode G10 - Bias Mode 4
		10.5	13.7	–	dB	Gain Mode G9 - Bias Mode 4
		10.8	14.3	–	dB	Gain Mode G8 - Bias Mode 3
		11.0	14.7	–	dB	Gain Mode G7 - Bias Mode 3
		6.0	7.2	–	dB	Gain Mode G6 - Bias Mode 1
		7.4	8.5	–	dB	Gain Mode G5 - Bias Mode 1
		7.2	9.1	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 8: Continued RF Characteristics MLB (LNA3....LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 1427 MHz – 1518 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	7.8	11.2	–	dB	Gain Mode G12 - Bias Mode 7
		10.0	13.8	–	dB	Gain Mode G11 - Bias Mode 7
		9.1	12.1	–	dB	Gain Mode G10 - Bias Mode 4
		11.2	14.8	–	dB	Gain Mode G9 - Bias Mode 4
		11.2	14.9	–	dB	Gain Mode G8 - Bias Mode 3
		11.8	15.6	–	dB	Gain Mode G7 - Bias Mode 3
		11.2	14.0	–	dB	Gain Mode G6 - Bias Mode 1
		10.4	13.2	–	dB	Gain Mode G5 - Bias Mode 1
		5.8	7.3	–	dB	Gain Mode G4 - Any Bias Mode
		8.6	9.9	–	dB	Gain Mode G3 - Any Bias Mode
		9.7	12.4	–	dB	Gain Mode G2 - Any Bias Mode
		11.2	13.2	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	25.0	30.0	–	dB	Gain Mode G12...G5 - Bias Mode 7/4/3/1
		2.8	4.3	–	dB	Gain Mode G4 - Any Bias Mode
		5.0	6.5	–	dB	Gain Mode G3 - Any Bias Mode
		8.0	9.5	–	dB	Gain Mode G2 - Any Bias Mode
		10.8	12.3	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-12.3	-10.8	–	dBm	Gain Mode G12 - Bias Mode 7
		-8.1	-6.7	–	dBm	Gain Mode G11 - Bias Mode 7
		-6.3	-4.8	–	dBm	Gain Mode G10 - Bias Mode 4
		-3.0	-1.5	–	dBm	Gain Mode G9 - Bias Mode 4
		-1.6	-0.6	–	dBm	Gain Mode G8 - Bias Mode 3
		-0.5	0.6	–	dBm	Gain Mode G7 - Bias Mode 3
		-1.4	-0.5	–	dBm	Gain Mode G6 - Bias Mode 1
		2.5	3.2	–	dBm	Gain Mode G5 - Bias Mode 1
		27	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-23.4	-21.4	–	dBm	Gain Mode G12 - Bias Mode 7
		-19.5	-17.8	–	dBm	Gain Mode G11 - Bias Mode 7
		-18.5	-16.7	–	dBm	Gain Mode G10 - Bias Mode 4
		-16.5	-14.7	–	dBm	Gain Mode G9 - Bias Mode 4
		-16.7	-14.7	–	dBm	Gain Mode G8 - Bias Mode 3
		-14.4	-12.4	–	dBm	Gain Mode G7 - Bias Mode 3
		-14.3	-12.1	–	dBm	Gain Mode G6 - Bias Mode 1
		-11.3	-9.0	–	dBm	Gain Mode G5 - Bias Mode 1
		6.0	9.3	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 9: RF Characteristics MLB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 1427 MHz – 1518 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	20.7	22.9	24.9	dB	Gain Mode G12 - Bias Mode 7
		17.2	19.3	21.0	dB	Gain Mode G11 - Bias Mode 7
		14.0	16.1	17.8	dB	Gain Mode G10 - Bias Mode 4
		11.6	13.6	15.3	dB	Gain Mode G9 - Bias Mode 4
		8.6	10.6	12.3	dB	Gain Mode G8 - Bias Mode 3
		5.6	7.6	9.1	dB	Gain Mode G7 - Bias Mode 3
		1.2	3.2	4.7	dB	Gain Mode G6 - Bias Mode 1
		-2.1	0.1	1.6	dB	Gain Mode G5 - Bias Mode 1
		-5.8	-4.5	-3.0	dB	Gain Mode G4 - Any Bias Mode
		-8.1	-6.5	-5.0	dB	Gain Mode G3 - Any Bias Mode
		-11.2	-9.5	-8.0	dB	Gain Mode G2 - Any Bias Mode
		-13.6	-12.3	-10.8	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.6	1.1	dB	Gain Mode G12 - Bias Mode 7
		–	0.9	1.6	dB	Gain Mode G11 - Bias Mode 7
		–	1.1	1.8	dB	Gain Mode G10 - Bias Mode 4
		–	1.6	2.3	dB	Gain Mode G9 - Bias Mode 4
		–	2.2	2.9	dB	Gain Mode G8 - Bias Mode 3
		–	3.1	3.8	dB	Gain Mode G7 - Bias Mode 3
		–	5.6	6.4	dB	Gain Mode G6 - Bias Mode 1
		–	8.6	9.4	dB	Gain Mode G5 - Bias Mode 1
		–	4.5	5.8	dB	Gain Mode G4 - Any Bias Mode
		–	6.5	8.1	dB	Gain Mode G3 - Any Bias Mode
		–	9.5	11.2	dB	Gain Mode G2 - Any Bias Mode
		–	12.3	13.6	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	5.5	6.4	–	dB	Gain Mode G12 - Bias Mode 7
		6.2	9.0	–	dB	Gain Mode G11 - Bias Mode 7
		6.7	9.2	–	dB	Gain Mode G10 - Bias Mode 4
		10.0	14.5	–	dB	Gain Mode G9 - Bias Mode 4
		10.0	14.5	–	dB	Gain Mode G8 - Bias Mode 3
		10.5	14.9	–	dB	Gain Mode G7 - Bias Mode 3
		5.0	7.3	–	dB	Gain Mode G6 - Bias Mode 1
		6.8	8.5	–	dB	Gain Mode G5 - Bias Mode 1
		7.2	9.1	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 10: Continued RF Characteristics MLB (LNA3....LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 1427 MHz – 1518 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	7.3	10.0	–	dB	Gain Mode G12 - Bias Mode 7
		9.8	13.8	–	dB	Gain Mode G11 - Bias Mode 7
		9.0	12.0	–	dB	Gain Mode G10 - Bias Mode 4
		11.2	15.0	–	dB	Gain Mode G9 - Bias Mode 4
		11.2	14.9	–	dB	Gain Mode G8 - Bias Mode 3
		11.9	15.8	–	dB	Gain Mode G7 - Bias Mode 3
		11.2	13.9	–	dB	Gain Mode G6 - Bias Mode 1
		10.3	13.0	–	dB	Gain Mode G5 - Bias Mode 1
		5.8	7.3	–	dB	Gain Mode G4 - Any Bias Mode
		8.6	9.9	–	dB	Gain Mode G3 - Any Bias Mode
		9.7	12.4	–	dB	Gain Mode G2 - Any Bias Mode
		11.3	13.2	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	25.0	30.0	–	dB	Gain Mode G12...G5 - Bias Mode 7/4/3/1
		3.0	4.5	–	dB	Gain Mode G4 - Any Bias Mode
		5.0	6.5	–	dB	Gain Mode G3 - Any Bias Mode
		8.0	9.5	–	dB	Gain Mode G2 - Any Bias Mode
		10.8	12.3	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-10.9	-9.4	–	dBm	Gain Mode G12 - Bias Mode 7
		-6.1	-4.4	–	dBm	Gain Mode G11 - Bias Mode 7
		-5.4	-3.8	–	dBm	Gain Mode G10 - Bias Mode 4
		-1.6	-0.1	–	dBm	Gain Mode G9 - Bias Mode 4
		-2.1	-0.5	–	dBm	Gain Mode G8 - Bias Mode 3
		-0.5	0.6	–	dBm	Gain Mode G7 - Bias Mode 3
		-1.4	-0.3	–	dBm	Gain Mode G6 - Bias Mode 1
		2.6	3.7	–	dBm	Gain Mode G5 - Bias Mode 1
		27	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-20.7	-18.7	–	dBm	Gain Mode G12 - Bias Mode 7
		-16.3	-14.7	–	dBm	Gain Mode G11 - Bias Mode 7
		-17.4	-15.3	–	dBm	Gain Mode G10 - Bias Mode 4
		-15.8	-13.6	–	dBm	Gain Mode G9 - Bias Mode 4
		-16.5	-14.4	–	dBm	Gain Mode G8 - Bias Mode 3
		-14.3	-12.2	–	dBm	Gain Mode G7 - Bias Mode 3
		-14.3	-12.1	–	dBm	Gain Mode G6 - Bias Mode 1
		-11.5	-9.2	–	dBm	Gain Mode G5 - Bias Mode 1
		6.0	9.3	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 11: RF Characteristics MB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 1805 – 2200 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	19.8	22.0	24.0	dB	Gain Mode G12 - Bias Mode 7
		16.2	18.3	20.2	dB	Gain Mode G11 - Bias Mode 7
		13.5	15.6	17.3	dB	Gain Mode G10 - Bias Mode 4
		11.3	13.3	15.0	dB	Gain Mode G9 - Bias Mode 4
		8.2	10.2	11.9	dB	Gain Mode G8 - Bias Mode 3
		5.4	7.4	8.9	dB	Gain Mode G7 - Bias Mode 3
		1.2	3.2	4.7	dB	Gain Mode G6 - Bias Mode 1
		-2.4	0.4	1.9	dB	Gain Mode G5 - Bias Mode 1
		-6.5	-4.9	-3.5	dB	Gain Mode G4 - Any Bias Mode
		-8.2	-6.8	-5.5	dB	Gain Mode G3 - Any Bias Mode
		-11.0	-9.5	-8.3	dB	Gain Mode G2 - Any Bias Mode
		-14.2	-12.8	-11.5	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.7	1.2	dB	Gain Mode G12 - Bias Mode 7
		–	0.9	1.6	dB	Gain Mode G11 - Bias Mode 7
		–	1.2	1.9	dB	Gain Mode G10 - Bias Mode 4
		–	1.6	2.3	dB	Gain Mode G9 - Bias Mode 4
		–	2.2	2.9	dB	Gain Mode G8 - Bias Mode 3
		–	3.1	3.8	dB	Gain Mode G7 - Bias Mode 3
		–	5.6	6.4	dB	Gain Mode G6 - Bias Mode 1
		–	8.4	9.2	dB	Gain Mode G5 - Bias Mode 1
		–	4.9	6.5	dB	Gain Mode G4 - Any Bias Mode
		–	6.8	8.2	dB	Gain Mode G3 - Any Bias Mode
		–	9.5	11.0	dB	Gain Mode G2 - Any Bias Mode
		–	12.8	14.2	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	5.0	7.3	–	dB	Gain Mode G12 - Bias Mode 7
		6.7	9.0	–	dB	Gain Mode G11 - Bias Mode 7
		7.3	8.6	–	dB	Gain Mode G10 - Bias Mode 4
		10.5	13.2	–	dB	Gain Mode G9 - Bias Mode 4
		10.6	14.4	–	dB	Gain Mode G8 - Bias Mode 3
		10.9	14.9	–	dB	Gain Mode G7 - Bias Mode 3
		4.7	6.7	–	dB	Gain Mode G6 - Bias Mode 1
		5.3	7.4	–	dB	Gain Mode G5 - Bias Mode 1
		5.1	7.8	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 12: Continued RF Characteristics MB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 1805 – 2200 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	6.7	10.7	–	dB	Gain Mode G12 - Bias Mode 7
		11.6	15.9	–	dB	Gain Mode G11 - Bias Mode 7
		10.1	14.4	–	dB	Gain Mode G10 - Bias Mode 4
		13.3	18.1	–	dB	Gain Mode G9 - Bias Mode 4
		14.1	18.4	–	dB	Gain Mode G8 - Bias Mode 3
		14.3	18.4	–	dB	Gain Mode G7 - Bias Mode 3
		15.1	20.3	–	dB	Gain Mode G6 - Bias Mode 1
		14.2	19.0	–	dB	Gain Mode G5 - Bias Mode 1
		6.3	8.0	–	dB	Gain Mode G4 - Any Bias Mode
		8.6	10.8	–	dB	Gain Mode G3 - Any Bias Mode
		9.2	12.8	–	dB	Gain Mode G2 - Any Bias Mode
		10.1	14.3	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	26.0	31.0	–	dB	Gain Mode G12...G5 - Bias Mode 7/4/3/1
		3.5	4.9	–	dB	Gain Mode G4 - Any Bias Mode
		5.5	6.8	–	dB	Gain Mode G3 - Any Bias Mode
		8.3	9.5	–	dB	Gain Mode G2 - Any Bias Mode
		11.5	12.8	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-11.5	-10.3	–	dBm	Gain Mode G12 - Bias Mode 7
		-8.7	-5.7	–	dBm	Gain Mode G11 - Bias Mode 7
		-7.4	-5.9	–	dBm	Gain Mode G10 - Bias Mode 4
		-4.8	-3.1	–	dBm	Gain Mode G9 - Bias Mode 4
		-2.7	-1.2	–	dBm	Gain Mode G8 - Bias Mode 3
		0.3	2.2	–	dBm	Gain Mode G7 - Bias Mode 3
		0.9	2.0	–	dBm	Gain Mode G6 - Bias Mode 1
		3.2	5.0	–	dBm	Gain Mode G5 - Bias Mode 1
		27	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-23.4	-21.7	–	dBm	Gain Mode G12 - Bias Mode 7
		-19.8	-17.5	–	dBm	Gain Mode G11 - Bias Mode 7
		-19.0	-17.0	–	dBm	Gain Mode G10 - Bias Mode 4
		-16.8	-15.0	–	dBm	Gain Mode G9 - Bias Mode 4
		-16.3	-14.5	–	dBm	Gain Mode G8 - Bias Mode 3
		-14.0	-12.3	–	dBm	Gain Mode G7 - Bias Mode 3
		-13.7	-11.8	–	dBm	Gain Mode G6 - Bias Mode 1
		-11.1	-9.3	–	dBm	Gain Mode G5 - Bias Mode 1
		8.2	11 .4	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 13: RF Characteristics MB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 1805 – 2200 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	20.9	23.1	25.1	dB	Gain Mode G12 - Bias Mode 7
		17.0	19.1	20.8	dB	Gain Mode G11 - Bias Mode 7
		14.0	16.1	17.8	dB	Gain Mode G10 - Bias Mode 4
		11.7	13.7	15.4	dB	Gain Mode G9 - Bias Mode 4
		8.5	10.5	12.2	dB	Gain Mode G8 - Bias Mode 3
		5.7	7.7	9.2	dB	Gain Mode G7 - Bias Mode 3
		1.3	3.5	5.0	dB	Gain Mode G6 - Bias Mode 1
		-1.4	0.6	2.1	dB	Gain Mode G5 - Bias Mode 1
		-6.5	-4.9	-3.5	dB	Gain Mode G4 - Any Bias Mode
		-8.2	-6.8	-5.5	dB	Gain Mode G3 - Any Bias Mode
		-11.0	-9.5	-8.3	dB	Gain Mode G2 - Any Bias Mode
		-14.2	-12.8	-11.5	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.6	1.1	dB	Gain Mode G12 - Bias Mode 7
		–	0.9	1.6	dB	Gain Mode G11 - Bias Mode 7
		–	1.2	1.9	dB	Gain Mode G10 - Bias Mode 4
		–	1.5	2.2	dB	Gain Mode G9 - Bias Mode 4
		–	2.1	2.8	dB	Gain Mode G8 - Bias Mode 3
		–	3.1	3.8	dB	Gain Mode G7 - Bias Mode 3
		–	5.5	6.3	dB	Gain Mode G6 - Bias Mode 1
		–	8.3	9.1	dB	Gain Mode G5 - Bias Mode 1
		–	4.9	6.5	dB	Gain Mode G4 - Any Bias Mode
		–	6.8	8.2	dB	Gain Mode G3 - Any Bias Mode
		–	9.5	11.0	dB	Gain Mode G2 - Any Bias Mode
		–	12.8	14.2	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	5.7	7.6	–	dB	Gain Mode G12 - Bias Mode 7
		7.4	9.9	–	dB	Gain Mode G11 - Bias Mode 7
		7.7	9.0	–	dB	Gain Mode G10 - Bias Mode 4
		10.1	14.0	–	dB	Gain Mode G9 - Bias Mode 4
		10.5	14.3	–	dB	Gain Mode G8 - Bias Mode 3
		10.8	14.8	–	dB	Gain Mode G7 - Bias Mode 3
		4.2	6.8	–	dB	Gain Mode G6 - Bias Mode 1
		5.3	7.5	–	dB	Gain Mode G5 - Bias Mode 1
		5.0	7.8	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 14: Continued RF Characteristics MB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 1805 – 2200 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	6.2	9.8	–	dB	Gain Mode G12 - Bias Mode 7
		11.8	16.0	–	dB	Gain Mode G11 - Bias Mode 7
		10.6	14.1	–	dB	Gain Mode G10 - Bias Mode 4
		13.4	18.5	–	dB	Gain Mode G9 - Bias Mode 4
		14.2	18.8	–	dB	Gain Mode G8 - Bias Mode 3
		14.4	18.7	–	dB	Gain Mode G7 - Bias Mode 3
		15.1	20.3	–	dB	Gain Mode G6 - Bias Mode 1
		14.2	19.0	–	dB	Gain Mode G5 - Bias Mode 1
		6.3	8.0	–	dB	Gain Mode G4 - Any Bias Mode
		8.6	10.8	–	dB	Gain Mode G3 - Any Bias Mode
		9.2	12.8	–	dB	Gain Mode G2 - Any Bias Mode
		10.1	14.3	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	26.0	31.0	–	dB	Gain Mode G12...G5 - Bias Mode 7/4/3/1
		3.5	4.9	–	dB	Gain Mode G4 - Any Bias Mode
		5.5	6.8	–	dB	Gain Mode G3 - Any Bias Mode
		8.3	9.5	–	dB	Gain Mode G2 - Any Bias Mode
		11.5	12.8	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-10.2	-8.9	–	dBm	Gain Mode G12 - Bias Mode 7
		-5.9	-4.2	–	dBm	Gain Mode G11 - Bias Mode 7
		-7.2	-5.4	–	dBm	Gain Mode G10 - Bias Mode 4
		-4.2	-2.2	–	dBm	Gain Mode G9 - Bias Mode 4
		-2.0	-0.1	–	dBm	Gain Mode G8 - Bias Mode 3
		1.4	3.2	–	dBm	Gain Mode G7 - Bias Mode 3
		1.5	2.7	–	dBm	Gain Mode G6 - Bias Mode 1
		4.5	5.6	–	dBm	Gain Mode G5 - Bias Mode 1
		27	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-20.5	-18.8	–	dBm	Gain Mode G12 - Bias Mode 7
		-16.8	-14.5	–	dBm	Gain Mode G11 - Bias Mode 7
		-18.2	-16.5	–	dBm	Gain Mode G10 - Bias Mode 4
		-16.1	-14.4	–	dBm	Gain Mode G9 - Bias Mode 4
		-16.1	-14.4	–	dBm	Gain Mode G8 - Bias Mode 3
		-14.0	-12.1	–	dBm	Gain Mode G7 - Bias Mode 3
		-13.7	-11.8	–	dBm	Gain Mode G6 - Bias Mode 1
		-11.2	-9.3	–	dBm	Gain Mode G5 - Bias Mode 1
		8.2	11 .3	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 15: RF Characteristics HB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 2300 – 2690 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	18.3	20.5	22.6	dB	Gain Mode G12 - Bias Mode 7
		14.8	16.9	18.6	dB	Gain Mode G11 - Bias Mode 7
		12.5	14.6	16.1	dB	Gain Mode G10 - Bias Mode 4
		10.4	12.4	13.6	dB	Gain Mode G9 - Bias Mode 4
		7.4	9.4	10.4	dB	Gain Mode G8 - Bias Mode 3
		4.9	6.9	8.1	dB	Gain Mode G7 - Bias Mode 3
		1.0	3.0	4.2	dB	Gain Mode G6 - Bias Mode 1
		-1.7	0.3	1.5	dB	Gain Mode G5 - Bias Mode 1
		-6.5	-5.2	-4.1	dB	Gain Mode G4 - Any Bias Mode
		-9.0	-7.7	-5.4	dB	Gain Mode G3 - Any Bias Mode
		-11.0	-9.7	-8.1	dB	Gain Mode G2 - Any Bias Mode
		-14.4	-13.1	-11.7	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.8	1.3	dB	Gain Mode G12 - Bias Mode 7
		–	1.0	1.7	dB	Gain Mode G11 - Bias Mode 7
		–	1.3	2.0	dB	Gain Mode G10 - Bias Mode 4
		–	1.7	2.4	dB	Gain Mode G9 - Bias Mode 4
		–	2.3	3.0	dB	Gain Mode G8 - Bias Mode 3
		–	3.3	4.0	dB	Gain Mode G7 - Bias Mode 3
		–	5.9	6.7	dB	Gain Mode G6 - Bias Mode 1
		–	8.5	9.3	dB	Gain Mode G5 - Bias Mode 1
		–	5.2	6.5	dB	Gain Mode G4 - Any Bias Mode
		–	7.7	9.0	dB	Gain Mode G3 - Any Bias Mode
		–	9.7	11.0	dB	Gain Mode G2 - Any Bias Mode
		–	13.1	14.4	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	9.4	14.0	–	dB	Gain Mode G12 - Bias Mode 7
		10.9	14.5	–	dB	Gain Mode G11 - Bias Mode 7
		9.2	11.4	–	dB	Gain Mode G10 - Bias Mode 4
		11.0	12.8	–	dB	Gain Mode G9 - Bias Mode 4
		9.5	11.3	–	dB	Gain Mode G8 - Bias Mode 3
		11.9	14.2	–	dB	Gain Mode G7 - Bias Mode 3
		5.5	6.7	–	dB	Gain Mode G6 - Bias Mode 1
		5.5	6.9	–	dB	Gain Mode G5 - Bias Mode 1
		5.5	7.4	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 16: Continued RF Characteristics HB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V, V_{IO} = 1.2 V, f = 2300 – 2690 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	5.0	7.9	–	dB	Gain Mode G12 - Bias Mode 7
		6.7	10.8	–	dB	Gain Mode G11 - Bias Mode 7
		7.7	12.5	–	dB	Gain Mode G10 - Bias Mode 4
		7.4	11.7	–	dB	Gain Mode G9 - Bias Mode 4
		7.4	11.8	–	dB	Gain Mode G8 - Bias Mode 3
		7.0	10.9	–	dB	Gain Mode G7 - Bias Mode 3
		8.0	12.3	–	dB	Gain Mode G6 - Bias Mode 1
		7.8	12.0	–	dB	Gain Mode G5 - Bias Mode 1
		6.8	8.3	–	dB	Gain Mode G4 - Any Bias Mode
		8.2	10.1	–	dB	Gain Mode G3 - Any Bias Mode
		8.3	10.8	–	dB	Gain Mode G2 - Any Bias Mode
		9.4	11.8	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	28.0	33.0	–	dB	Gain Mode G12...G5 - Bias Mode 7/4/3/1
		4.1	5.2	–	dB	Gain Mode G4 - Any Bias Mode
		5.4	7.7	–	dB	Gain Mode G3 - Any Bias Mode
		8.1	9.7	–	dB	Gain Mode G2 - Any Bias Mode
		11.7	13.1	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-10.7	-8.6	–	dBm	Gain Mode G12 - Bias Mode 7
		-10.5	-4.5	–	dBm	Gain Mode G11 - Bias Mode 7
		-6.6	-4.5	–	dBm	Gain Mode G10 - Bias Mode 4
		-4.1	-2.2	–	dBm	Gain Mode G9 - Bias Mode 4
		-2.5	-0.8	–	dBm	Gain Mode G8 - Bias Mode 3
		0.0	1.3	–	dBm	Gain Mode G7 - Bias Mode 3
		0.6	1.9	–	dBm	Gain Mode G6 - Bias Mode 1
		2.9	4.7	–	dBm	Gain Mode G5 - Bias Mode 1
		27	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-20.6	-18.3	–	dBm	Gain Mode G12 - Bias Mode 7
		-15.9	-14.1	–	dBm	Gain Mode G11 - Bias Mode 7
		-15.3	-12.9	–	dBm	Gain Mode G10 - Bias Mode 4
		-13.4	-11.2	–	dBm	Gain Mode G9 - Bias Mode 4
		-13.4	-10.8	–	dBm	Gain Mode G8 - Bias Mode 3
		-12.4	-9.4	–	dBm	Gain Mode G7 - Bias Mode 3
		-11.9	-9.0	–	dBm	Gain Mode G6 - Bias Mode 1
		-9.2	-6.3	–	dBm	Gain Mode G5 - Bias Mode 1
		>12	>12	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 17: RF Characteristics HB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 2300 – 2690 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain [1]	$\|S_{21}\|^2$	19.3	21.6	23.7	dB	Gain Mode G12 - Bias Mode 7
		15.6	17.7	19.4	dB	Gain Mode G11 - Bias Mode 7
		13.0	15.0	16.6	dB	Gain Mode G10 - Bias Mode 4
		11.2	12.9	14.1	dB	Gain Mode G9 - Bias Mode 4
		8.4	9.8	10.8	dB	Gain Mode G8 - Bias Mode 3
		6.0	7.3	8.2	dB	Gain Mode G7 - Bias Mode 3
		2.2	3.3	4.2	dB	Gain Mode G6 - Bias Mode 1
		-0.7	0.5	1.6	dB	Gain Mode G5 - Bias Mode 1
		-6.5	-5.2	-4.1	dB	Gain Mode G4 - Any Bias Mode
		-8.5	-7.0	-5.4	dB	Gain Mode G3 - Any Bias Mode
		-11.0	-9.7	-8.1	dB	Gain Mode G2 - Any Bias Mode
		-14.4	-13.1	-11.7	dB	Gain Mode G1 - Any Bias Mode
Noise figure [2]	*NF*	–	0.7	1.2	dB	Gain Mode G12 - Bias Mode 7
		–	1.0	1.7	dB	Gain Mode G11 - Bias Mode 7
		–	1.3	2.0	dB	Gain Mode G10 - Bias Mode 4
		–	1.6	2.3	dB	Gain Mode G9 - Bias Mode 4
		–	2.3	3.0	dB	Gain Mode G8 - Bias Mode 3
		–	3.2	3.9	dB	Gain Mode G7 - Bias Mode 3
		–	5.8	6.6	dB	Gain Mode G6 - Bias Mode 1
		–	8.5	9.3	dB	Gain Mode G5 - Bias Mode 1
		–	5.2	6.5	dB	Gain Mode G4 - Any Bias Mode
		–	7.0	8.5	dB	Gain Mode G3 - Any Bias Mode
		–	9.7	11.0	dB	Gain Mode G2 - Any Bias Mode
		–	13.1	14.4	dB	Gain Mode G1 - Any Bias Mode
Input return loss [3]	*IRL*	9.9	14.5	–	dB	Gain Mode G12 - Bias Mode 7
		12.0	16.2	–	dB	Gain Mode G11 - Bias Mode 7
		9.6	11.9	–	dB	Gain Mode G10 - Bias Mode 4
		10.5	13.5	–	dB	Gain Mode G9 - Bias Mode 4
		9.8	11.8	–	dB	Gain Mode G8 - Bias Mode 3
		11.0	14.0	–	dB	Gain Mode G7 - Bias Mode 3
		5.6	6.9	–	dB	Gain Mode G6 - Bias Mode 1
		5.6	6.9	–	dB	Gain Mode G5 - Bias Mode 1
		5.5	7.4	–	dB	Gain Mode G4...G1 - Any Bias Mode

[1] Tested by ATE (not all input-output combinations)
[2] Tested by ATE (LNA7), all LNAs tested in laboratory
[3] Tested in laboratory

Table 18: Continued RF Characteristics HB (LNA3...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.8 V, V_{IO} = 1.8 V, f = 2300 – 2690 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output return loss [1]	*ORL*	5.0	7.5	–	dB	Gain Mode G12 - Bias Mode 7
		6.8	10.8	–	dB	Gain Mode G11 - Bias Mode 7
		8.0	12.7	–	dB	Gain Mode G10 - Bias Mode 4
		7.6	12.0	–	dB	Gain Mode G9 - Bias Mode 4
		7.6	12.1	–	dB	Gain Mode G8 - Bias Mode 3
		7.1	11.0	–	dB	Gain Mode G7 - Bias Mode 3
		8.1	12.6	–	dB	Gain Mode G6 - Bias Mode 1
		8.0	12.2	–	dB	Gain Mode G5 - Bias Mode 1
		7.0	8.3	–	dB	Gain Mode G4 - Any Bias Mode
		8.2	10.1	–	dB	Gain Mode G3 - Any Bias Mode
		8.3	10.8	–	dB	Gain Mode G2 - Any Bias Mode
		9.4	11.8	–	dB	Gain Mode G1 - Any Bias Mode
Reverse isolation [2]	$1/\lvert S_{12}\rvert^2$	28.0	33.0	–	dB	Gain Mode G12...G5 - Bias Mode 7/4/3/1
		4.1	5.2	–	dB	Gain Mode G4 - Any Bias Mode
		5.4	7.0	–	dB	Gain Mode G3 - Any Bias Mode
		8.1	9.7	–	dB	Gain Mode G2 - Any Bias Mode
		11.7	13.1	–	dB	Gain Mode G1 - Any Bias Mode
Inband input 3rd-order intercept point [1, 3]	*IIP3*	-8.9	-6.5	–	dBm	Gain Mode G12 - Bias Mode 7
		-5.6	-2.5	–	dBm	Gain Mode G11 - Bias Mode 7
		-6.4	-4.1	–	dBm	Gain Mode G10 - Bias Mode 4
		-3.8	-1.6	–	dBm	Gain Mode G9 - Bias Mode 4
		-2.0	0.2	–	dBm	Gain Mode G8 - Bias Mode 3
		0.8	2.5	–	dBm	Gain Mode G7 - Bias Mode 3
		1.6	2.9	–	dBm	Gain Mode G6 - Bias Mode 1
		4.0	5.9	–	dBm	Gain Mode G5 - Bias Mode 1
		27	30	–	dBm	Gain Mode G4...G1 - Any Bias Mode
Inband input 1dB compression point [1]	IP_{1dB}	-17.7	-15.3	–	dBm	Gain Mode G12 - Bias Mode 7
		-12.9	-10.9	–	dBm	Gain Mode G11 - Bias Mode 7
		-15.1	-12.1	–	dBm	Gain Mode G10 - Bias Mode 4
		-13.3	-10.5	–	dBm	Gain Mode G9 - Bias Mode 4
		-13.4	-10.7	–	dBm	Gain Mode G8 - Bias Mode 3
		-12.2	-9.2	–	dBm	Gain Mode G7 - Bias Mode 3
		-11.9	-9.1	–	dBm	Gain Mode G6 - Bias Mode 1
		-9.2	-6.3	–	dBm	Gain Mode G5 - Bias Mode 1
		>12	>12	–	dBm	Gain Mode G4...G1 - Any Bias Mode

[1] Tested in laboratory
[2] Tested by ATE (not all input-output combinations)
[3] 2 MHz tone spacing. Input power = −35 to −10 dBm for each tone depending on the gain mode.

Table 19: RF Characteristics LB, MLB and MHB (LNA1...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V / 1.8 V, V_{IO} = 1.2 V / 1.8 V, f = 617– 2690 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
All LNAs, All Modes						
Stability [1]	k	>1	–	–		1 MHz - 12 GHz

[1]Tested in laboratory

Table 20: Timing Characteristics LB, MLB and MHB (LNA1...LNA7) in ON Mode at T_A = 25 °C, V_{DD} = 1.2 V / 1.8 V, V_{IO} = 1.2 V / 1.8 V, f = 617– 2690 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
All LNAs, All Modes						
Turn on time [1]	t_{pup}	–	–	1.0	µs	50% last SCLK falling edge to within 0.5 dB gain error of steady state gain
Turn off time [1]	t_{poff}	–	–	1.0	µs	50% last SCLK falling edge to -20 dB compared to active S21
Gain settling time [1]	t_{gs}	–	–	1.0	µs	Gain switching between any of 2 gains gears to be with 0.5 dB gain error of steady state gain (start 50% last SCLK falling edge)

[1]Tested in laboratory

4 MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the ’MIPI Alliance Specification for RF Front-End Control Interface version 3.0 - December 2019’ as well as the ’Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)’.

Table 21: MIPI Features

Feature	Supported	Comment
MIPI 3.0 Features		
Extended Trigger Set A support	Yes	Include EXT_TRIG_A set (register 0x2D + 0x2E necessary).
Extended Trigger Set B support	Yes	Include EXT_TRIG_B set (register 0x2F + 0x30 necessary).
Timed Triggers	Yes	Include counter registers (register 0x38 - 0x3F for EXT_TRIG_A set necessary and 0x31 - 0x37 for EXT_TRIG_B set necessary).
Mappable Triggers	Yes	Additional MTRIG_SET_x required in UDR register range.
MIPI 2.1 Features		
MIPI RFFE 2.1 standard compatibility	Yes	The MIPI RFFE interface is working in systems following the "MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18. December 2017" as well as the "Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)".
MIPI RFFE 2.1 - Errata 01 implementation	Yes	The MIPI Alliance has released an Errata Document "Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019" concerning the Masked Write Register feature. The Infineon MIPI RFFE Block has been updated accordingly.
MIPI RFFE 2.0 standard compatibility	Yes	The MIPI RFFE interface is working in systems following the "MIPI Alliance Specification for RF Front-End Control Interface version 2.0 - 25. September 2014" as well as the "Qualcomm RFFE Vendor specification 80-N7876-1 Rev. T".
Longer Reach RFFE Bus Length Feature(MIPI RFFE 2.1 optional feature)	Yes	Longer Reach allows for longer RFFE bus lengths. This requires a limitation to the Standard Frequency Range of RFFE plus additional timing requirements for all devices on the bus

Table 22: MIPI Features Continued

Feature	Supported	Comment
Programmable driver strength (MIPI RFFE 2.x feature)	Yes	Allows to program MIPI device Bus driver strength (relevant vor Read Back messages) up to 80pF via BUS_LD-Register (0x2B) Default value: 50 pF
Register 0 write command sequence	Yes	Shortened Write Sequence for Register 0 - Caution: only 7 LSBs in Reg 0 can be addressed
Register read and write command sequence	Yes	Standard Register Read/Write procedure addressing standard register space of 0x00 - 0x1F
Extended register read and write command sequence	Yes	Register Read/Write procedure addressing extended register space of 0x00 - 0xFF
Extended Register Write Long Command Sequence	No	Register Read/Write procedure addressing extended register space of 0x0000 - 0xFFFF
Masked write command sequence (MIPI 2.1 optional feature)	Yes	Allow only certain bits in a register to be updated during a write command. Relevant Registers marked "MW" in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	SCLK range 32 kHz - 26 MHz for read and write commands
Support for extended frequency range operations for SCLK	Yes	SCLK range 26 MHz - 52 MHz for write commands
sRead (synchronous Read) Full Speed or half speed up to 26 MHz (MIPI 2.x feature)	Yes	Relaxed Slave Setup Time requirements as Master samples Data on rising edge of SCLK signal
"Regular" Read Full Speed or half speed up to 13 MHz (MIPI RFFE 1.10-2.x feature)	Yes	Stricter Slave Setup Time requirements as Master samples Data on falling edge of SCLK signal
"Regular" Read Full Speed or half speed up to 26 MHz (MIPI RFFE 1.10 feature)	No	Full-Speed "regular" (falling edge sampling) Read operations are no longer specified for use in the Standard Frequency Range in MIPI RFFE2.1, and are intended to be replaced by Full-Speed sRead operations in the Standard Frequency Range. Half-Speed Data Response accesses for Read operations in the Standard Frequency Range remain supported. Read operations are not supported for use in the Extended Frequency Range. In the Ext FR only Half-Speed Data Response (HSDR) accesses using sReads are valid for Slaves (or non-BOMs) driving SDATA on the bus.
Product ID + extended product ID register	Yes	PRODUCT_ID (address 0x1D) and EXT_PRODUCT_ID (address 0x20) Registers
Extended Manufacturer ID (10->12 bit) (MIPI 2.1 optional feature)	Yes	The 2 bits In MIPI2.1 are placed in RFFE USID register at address 0x1F; value is 0 in IFX products

Table 23: MIPI Features Continued

Feature	Supported	Comment
Revision ID register	Yes	This Register contains the Device Revision (address 0x21)
Programmable GSID (Group Slave Identifier)	Yes	RFFE 2.x GROUP_SID Register (at address 0x22).
Programmable USID (Unique Slave Identifier)	Yes	Device can be also explicitly addressed via combination of (old) USID, Manufacturer ID, and (extended) product ID to reprogram USID via (extended) Register Write sequence (see MIPI RFFE Spec v2.1 Chapter 6.2.1)
Trigger functionality	Yes	3 "standard" Triggers via PM_TRIG[5:0] consisting of 3 Mask- and 3 Trigger Bits
Trigger Handling in Secondary Mode: Ignore Triggers	Yes	YES: When Device is and stays in Secondary Mode, Triggers are IGNORED (NOTE: in combination with a mode change, Triggers are not ignored) NO: When Device is and stays in Secondary Mode, Triggers are NOT IGNORED; (i.e. Triggering is always executed)
Extended Triggers and Trigger Masks (MIPI 2.1 optional feature)	Yes	Additional eight Triggers and the associated Trigger Masks, have been added in MIPI2.1 (registers at addresses 0x2D and 0x2E)
Broadcast/GSID write to PM TRIG register	Yes	The above mentioned Trigger Register (and extended trigger register) can be accessed via Broadcast/GSID writes to trigger several MIPI devices snychronously. NOTE: Trigger Mask bits are nor changed wih Broadcast/GSID writes
Reset	Yes	Reset is possible via VIO, PM TRIG or register SW_RST (0x23). NOTE: SW_RST only resets User Defined Registers, it does not reset the values of any reserved registers
Status/Error sum register	Yes	RFFE 2.x ERR_SUM Register (address 0x24).
USID_Sel pin	Yes	External pin for changing USID (values: see programing section), 1 USID pin addressable by customer

Table 24: Startup Behavior

Feature	State	Comment
Power status	Secondary Mode	Secondary Mode after start-up, analog blocks are disabled
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register
Extended trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 25: User Defined Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	LNA1_INPUT _CONFIG	7:3	reserved		00000000	No	mTrig set A	R/W MW
		2:1	LNA_INPUT_SELECT	00: LNA Off 01: LB0_IN0 10: LB0_IN1 11: LB0_IN2				
		0	ENABLE	0: LNA Disable 1: LNA Enable				
0x01	LNA2_INPUT _CONFIG	7:4	reserved		00000000	No	mTrig set A	R/W MW
		3:1	LNA_INPUT_SELECT	000: LNA Off 001: LB1_IN0 010: LB1_IN1 011: LB1_IN2 100: LB1_IN3				
		0	ENABLE	0: LNA Disable 1: LNA Enable				
0x02	LNA3_INPUT _CONFIG	7:3	reserved		00000000	No	mTrig set A	R/W MW
		2:1	LNA_INPUT_SELECT	00: LNA Off 01: MLB_IN0 10: MLB_IN1 11: MLB_IN2				
		0	ENABLE	0: LNA Disable 1: LNA Enable				
0x03	LNA4_INPUT _CONFIG	7:3	reserved		00000000	No	mTrig set A	R/W MW
		2:1	LNA_INPUT_SELECT	00: LNA Off 01: MB0_IN0 10: MB0_IN1 11: MB0_IN2				
		0	ENABLE	0: LNA Disable 1: LNA Enable				
0x04	LNA5_INPUT _CONFIG	7:3	reserved		00000000	No	mTrig set A	R/W MW
		2:1	LNA_INPUT_SELECT	00: LNA Off 01: MB1_IN0 10: MB1_IN1				
		0	ENABLE	0: LNA Disable 1: LNA Enable				
0x05	LNA6_INPUT _CONFIG	7:3	reserved		00000000	No	mTrig set A	R/W MW
		2:1	LNA_INPUT_SELECT	00: LNA Off 01: HB0_IN0 10: HB0_IN1				
		0	ENABLE	0: LNA Disable 1: LNA Enable				
0x06	LNA7_INPUT _CONFIG	7:3	reserved		00000000	No	mTrig set A	R/W MW
		2:1	LNA_INPUT_SELECT	00: LNA Off 01: HB1_IN0 10: HB1_IN1				
		0	ENABLE	0: LNA Disable 1: LNA Enable				

Table 26: User Defined Register Mapping continued

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x07	OUTPUT_LB0	7:3	reserved		00000000	No	mTrig set B	R/W MW
		2:0	LNA_SELECT	000: No LNA Selected 001: LNA1 010: LNA2				
0x08	OUTPUT_LB1	7:3	reserved		00000000	No	mTrig set B	R/W MW
		2:0	LNA_SELECT	000: No LNA Selected 001: LNA2 010: LNA3				
0x09	OUTPUT_MB0	7:3	reserved		00000000	No	mTrig set B	R/W MW
		2:0	LNA_SELECT	000: No LNA Selected 001: LNA1 010: LNA2 011: LNA3 100: LNA4 101: LNA5 110: LNA6 111: LNA7				
0x0A	OUTPUT_MB1	7:3	reserved		00000000	No	mTrig set B	R/W MW
		2:0	LNA_SELECT	000: No LNA Selected 011: LNA3 100: LNA4 101: LNA5 110: LNA6 111: LNA7				
0x0B	OUTPUT_HB0	7:3	reserved		00000000	No	mTrig set B	R/W MW
		2:0	LNA_SELECT	000: No LNA Selected 011: LNA3 100: LNA4 101: LNA5 110: LNA6 111: LNA7				
0x0C	OUTPUT_HB1	7:3	reserved		00000000	No	mTrig set B	R/W MW
		2:0	LNA_SELECT	000: No LNA Selected 011: LNA3 100: LNA4 101: LNA5 110: LNA6 111: LNA7				
0x0D	OUTPUT_HB2	7:3	reserved		00000000	No	mTrig set B	R/W MW
		2:0	LNA_SELECT	000: No LNA Selected 110: LNA6 111: LNA7				

Table 27: User Defined Register Mapping continued

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x0E	LNA1_GAIN_BIAS	7	ENABLE	LNA enable (or'ed with bit 0 in register 0x00)	00000000	No	mTrig set C	R/W MW
		6:3	GAIN_CTRL	0000: LNA off 0001: G1 (-12dB) 0010: G2 (-9dB) 0011: G3 (-6dB) 0100: G4 (-3dB) 0101: G5 (0dB) 0110: G6 (3dB) 0111: G7 (6dB) 1000: G8 (9dB) 1001: G9 (12dB) 1010: G10 (15dB) 1011: G11 (18dB)				
		2:0	LNA_BIAS	000: Bias0 (2.5mA) 001: Bias1 (3.0mA) 010: Bias2 (3.5mA) 011: Bias3 (4.0mA) 100: Bias4 (5.0mA) 101: Bias5 (6.0mA) 110: Bias6 (9.0mA) 111: Bias7 (10mA)				
0x0F	LNA2_GAIN_BIAS	7	ENABLE	LNA enable (or'ed with bit 0 in register 0x01)	00000000	No	mTrig set D	R/W MW
		6:3	GAIN_CTRL	0000: LNA off 0001: G1 (-12dB) 0010: G2 (-9dB) 0011: G3 (-6dB) 0100: G4 (-3dB) 0101: G5 (0dB) 0110: G6 (3dB) 0111: G7 (6dB) 1000: G8 (9dB) 1001: G9 (12dB) 1010: G10 (15dB) 1011: G11 (18dB)				
		2:0	LNA_BIAS	000: Bias0 (2.5mA) 001: Bias1 (3.0mA) 010: Bias2 (3.5mA) 011: Bias3 (4.0mA) 100: Bias4 (5.0mA) 101: Bias5 (6.0mA) 110: Bias6 (9.0mA) 111: Bias7 (10mA)				

Table 28: User Defined Register Mapping continued

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x10	LNA3_GAIN_BIAS	7	ENABLE	LNA enable (or'ed with bit 0 in register 0x02)	00000000	No	mTrig set E	R/W MW
		6:3	GAIN_CTRL	LNA off 0001: G1 (-12dB) 0010: G2 (-9dB) 0011: G3 (-6dB) 0100: G4 (-3dB) 0101: G5 (0dB) 0110: G6 (3dB) 0111: G7 (6dB) 1000: G8 (9dB) 1001: G9 (12dB) 1010: G10 (15dB) 1011: G11 (18dB) 1100: G12 (21dB)				
		2:0	LNA_BIAS	000: Bias0 (2.5mA) 001: Bias1 (3.0mA) 010: Bias2 (3.5mA) 011: Bias3 (4.0mA) 100: Bias4 (5.0mA) 101: Bias5 (6.0mA) 110: Bias6 (9.0mA) 111: Bias7 (10mA)				
0x11	LNA4_GAIN_BIAS	7	ENABLE	LNA enable (or'ed with bit 0 in register 0x03)	00000000	No	mTrig set F	R/W MW
		6:3	GAIN_CTRL	LNA off 0001: G1 (-12dB) 0010: G2 (-9dB) 0011: G3 (-6dB) 0100: G4 (-3dB) 0101: G5 (0dB) 0110: G6 (3dB) 0111: G7 (6dB) 1000: G8 (9dB) 1001: G9 (12dB) 1010: G10 (15dB) 1011: G11 (18dB) 1100: G12 (21dB)				
		2:0	LNA_BIAS	000: Bias0 (2.5mA) 001: Bias1 (3.0mA) 010: Bias2 (3.5mA) 011: Bias3 (4.0mA) 100: Bias4 (5.0mA) 101: Bias5 (6.0mA) 110: Bias6 (9.0mA) 111: Bias7 (10mA)				

Table 29: User Defined Register Mapping continued

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x12	LNA5_GAIN_BIAS	7	ENABLE	LNA enable (or'ed with bit 0 in register 0x04)	00000000	No	mTrig set G	R/W MW
		6:3	GAIN_CTRL	LNA off 0001: G1 (-12dB) 0010: G2 (-9dB) 0011: G3 (-6dB) 0100: G4 (-3dB) 0101: G5 (0dB) 0110: G6 (3dB) 0111: G7 (6dB) 1000: G8 (9dB) 1001: G9 (12dB) 1010: G10 (15dB) 1011: G11 (18dB) 1100: G12 (21dB)				
		2:0	LNA_BIAS	000: Bias0 (2.5mA) 001: Bias1 (3.0mA) 010: Bias2 (3.5mA) 011: Bias3 (4.0mA) 100: Bias4 (5.0mA) 101: Bias5 (6.0mA) 110: Bias6 (9.0mA) 111: Bias7 (10mA)				
0x13	LNA6_GAIN_BIAS	7	ENABLE	LNA enable (or'ed with bit 0 in register 0x05)	00000000	No	mTrig set H	R/W MW
		6:3	GAIN_CTRL	LNA off 0001: G1 (-12dB) 0010: G2 (-9dB) 0011: G3 (-6dB) 0100: G4 (-3dB) 0101: G5 (0dB) 0110: G6 (3dB) 0111: G7 (6dB) 1000: G8 (9dB) 1001: G9 (12dB) 1010: G10 (15dB) 1011: G11 (18dB) 1100: G12 (21dB)				
		2:0	LNA_BIAS	000: Bias0 (2.5mA) 001: Bias1 (3.0mA) 010: Bias2 (3.5mA) 011: Bias3 (4.0mA) 100: Bias4 (5.0mA) 101: Bias5 (6.0mA) 110: Bias6 (9.0mA) 111: Bias7 (10mA)				

Table 30: MIPI Reserved Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x14	LNA7_GAIN_BIAS	7	ENABLE	LNA enable (or'ed with bit 0 in register 0x06)	00000000	No	mTrig set I	R/W MW
		6:3	GAIN_CTRL	LNA off 0001: G1 (-12dB) 0010: G2 (-9dB) 0011: G3 (-6dB) 0100: G4 (-3dB) 0101: G5 (0dB) 0110: G6 (3dB) 0111: G7 (6dB) 1000: G8 (9dB) 1001: G9 (12dB) 1010: G10 (15dB) 1011: G11 (18dB) 1100: G12 (21dB)				
		2:0	LNA_BIAS	000: Bias0 (2.5mA) 001: Bias1 (3.0mA) 010: Bias2 (3.5mA) 011: Bias3 (4.0mA) 100: Bias4 (5.0mA) 101: Bias5 (6.0mA) 110: Bias6 (9.0mA) 111: Bias7 (10mA)				
0x40	CONFIG	7:2	Reserved		00000000	No	N/A	R/W MW
		1	INPUT_SHUNT_CONTROL	0: Unused LNA Input Floating 1: Unused LNA Input Shunted to GND				
		0	SUPPLY_RANGE_SELECT	0: Lower Supply Range (1.10-1.40V) 1: Upper Supply Range (1.40-1.95V)				
0x41	MTRIG_SET_A_B	7:4	Mappable Trigger Set B	trigger disabled after startup	11111111	No	N/A	R/W MW
		3:0	Mappable Trigger Set A	trigger disabled after startup				
0x42	MTRIG_SET_C_D	7:4	Mappable Trigger Set D		00000000	No	N/A	R/W MW
		3:0	Mappable Trigger Set C					
0x43	MTRIG_SET_E_F	7:4	Mappable Trigger Set F		00000000	No	N/A	R/W MW
		3:0	Mappable Trigger Set E					
0x44	MTRIG_SET_G_H	7:4	Mappable Trigger Set H		00000000	No	N/A	R/W MW
		3:0	Mappable Trigger Set G					
0x45	MTRIG_SET_I	7:4	Reserved		00000000	No	N/A	R/W MW
		3:0	Mappable Trigger Set I					

Table 31: MIPI Reserved Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (Normal Mode)	1	Yes	N/A	R/W MW
				1: Analog blocks switched off (Secondary Mode)				
		6	PWR_MODE(0), State Bit Vector	0: No action (Normal Mode)	0			
				1: Powered Reset				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	01100001	No	N/A	R
0x1E	MANUFACT._ID	7:0	MANUFACTURER_ID	Manufacturer ID. This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. See http://mid.mipi.org.	00011010	No	N/A	R

Table 32: MIPI Reserved Register Mapping Continued

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x1F	MAN_USID	7:6	MANUFACTURER_ID[11:10]	These bits are read-only. However, for reprogramming the USID, a write command sequence is performed on this register, even though the write does not change its value. See http://mid.mipi.org. (MIPI2.1 feature)	00	No	N/A	R
		5:4	MANUFACTURER_ID[9:8]	These bits are read-only. However, for reprogramming the USID, a write command sequence is performed on this register, even though the write does not change its value. See http://mid.mipi.org. (MIPI2.1 feature)	01			
		3:0	USID[3:0]	These bits store the USID of the device. Performing a write to this register using the described programming sequences will re-program the USID. USID is 0x0C after power up, if USID pin is connected to ground. USID is 0x0D when USID pin is tied to VIO.	1100 or 1101			R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	N/A	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision.	0001	No	N/A	R
		3:0	SUB_REVISION	Chip sub revision.	0000			
0x22	GS_ID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	N/A	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	N/A	R/W
		6:0	reserved	Reserved for future use	0000000			
0x24	ERR_SUM	7	reserved	Reserved for future use	0	No	N/A	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			

Table 34: MIPI Reserved Register Mapping Continued

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2B	BUS_LD	7:3	reserved	Reserved for future use	00000	No	N/A	R/W
		2:0	BUS_LD[2:0]	Programs the drive strength of the SDATA driver in feedback modes. 0x0: 10pF 0x1: 20pF 0x2: 30pF 0x3: 40pF 0x4: 50pF 0x5: 60pF 0x6: 80pF 0x7: 80pF	100			
0x2C	TEST_PATT	7:0	TEST_PATT[7:0]	A read to this register will trigger the slave to transmit a fixed test pattern of 0xD2.	11010010	No	N/A	R
0x2D	EXT_TRIGGER_MASK_A	7	EXT_TRIGGER_MASK_10	0: Data writes to registers tied to EXT_TRIGGER_X are masked. Data is held in shadow registers until the EXT_TRIGGER_X bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_X are not masked. Data writes go directly to the active registers.	0	No	N/A	R/W MW
		6	EXT_TRIGGER_MASK_9		0			
		5	EXT_TRIGGER_MASK_8		0			
		4	EXT_TRIGGER_MASK_7		0			
		3	EXT_TRIGGER_MASK_6		0			
		2	EXT_TRIGGER_MASK_5		0			
		1	EXT_TRIGGER_MASK_4		0			
		0	EXT_TRIGGER_MASK_3		0			
0x2E	EXT_TRIGGER_A	7	EXT_TRIGGER_10	Extended Trigger X. This bit has no effect if EXTENDED_TRIGGER_MASK_X is 1. When the part is in LOW POWER and a trigger request is sent in the same command sequence that still keeps the part in LOW POWER, the trigger request is ignored. This applies to Triggers only, not to Trigger Masks. When the part is in ACTIVE and sent to LOW POWER, or when the part is in LOW POWER and sent to ACTIVE, trigger requests in the same command sequence are NOT ignored.	0	No	N/A	R/W MW
		6	EXT_TRIGGER_9		0			
		5	EXT_TRIGGER_8		0			
		4	EXT_TRIGGER_7		0			
		3	EXT_TRIGGER_6		0			
		2	EXT_TRIGGER_5		0			
		1	EXT_TRIGGER_4		0			
		0	EXT_TRIGGER_3		0			
0x2F	EXT_TRIGGER_B	7	reserved	Extended Trigger X. This bit has no effect if EXTENDED_TRIGGER_MASK_X is 1. When the part is in LOW POWER and a trigger request is sent in the same command sequence that still keeps the part in LOW POWER, the trigger request is ignored. This applies to Triggers only, not to Trigger Masks. When the part is in ACTIVE and sent to LOW POWER, or when the part is in LOW POWER and sent to ACTIVE, trigger requests in the same command sequence are NOT ignored.	0	No	N/A	R/W MW
		6	EXT_TRIGGER_17		0			
		5	EXT_TRIGGER_16		0			
		4	EXT_TRIGGER_15		0			
		3	EXT_TRIGGER_14		0			
		2	EXT_TRIGGER_13		0			
		1	EXT_TRIGGER_12		0			
		0	EXT_TRIGGER_11		0			

Table 36: MIPI Reserved Register Mapping Continued

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x30	EXT_TRIGGER_MASK_B	7	reserved	0: Data writes to registers tied to EXT_TRIGGER_X are masked. Data is held in shadow registers until the EXT_TRIGGER_X bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_X are not masked. Data writes go directly to the active registers.	0	No	N/A	R/W MW
		6	EXT_TRIGGER_MASK_17		0			
		5	EXT_TRIGGER_MASK_16		0			
		4	EXT_TRIGGER_MASK_15		0			
		3	EXT_TRIGGER_MASK_14		0			
		2	EXT_TRIGGER_MASK_13		0			
		1	EXT_TRIGGER_MASK_12		0			
		0	EXT_TRIGGER_MASK_11		0			
0x31	EXT_TRIG_B_CNT_11	7:0	EXT_TRIG_B_CNT_11	Counter register most significant byte is R/W accessible via EXT_TRIG_A_CNT_X [7:0]. The actual programmable counting range of the counter is then 2, 4, ... 510 SCLK cycles.	00000000	Yes	N/A	R/W
0x32	EXT_TRIG_B_CNT_12	7:0	EXT_TRIG_B_CNT_12		00000000	Yes	N/A	R/W
0x33	EXT_TRIG_B_CNT_13	7:0	EXT_TRIG_B_CNT_13		00000000	Yes	N/A	R/W
0x34	EXT_TRIG_B_CNT_14	7:0	EXT_TRIG_B_CNT_14		00000000	Yes	N/A	R/W
0x35	EXT_TRIG_B_CNT_15	7:0	EXT_TRIG_B_CNT_15		00000000	Yes	N/A	R/W
0x36	EXT_TRIG_B_CNT_16	7:0	EXT_TRIG_B_CNT_16		00000000	Yes	N/A	R/W
0x37	EXT_TRIG_B_CNT_17	7:0	EXT_TRIG_B_CNT_17		00000000	Yes	N/A	R/W
0x38	EXT_TRIG_A_CNT_3	7:0	EXT_TRIG_A_CNT_3		00000000	Yes	N/A	R/W
0x39	EXT_TRIG_A_CNT_4	7:0	EXT_TRIG_A_CNT_4		00000000	Yes	N/A	R/W
0x3A	EXT_TRIG_A_CNT_5	7:0	EXT_TRIG_A_CNT_5		00000000	Yes	N/A	R/W
0x3B	EXT_TRIG_A_CNT_6	7:0	EXT_TRIG_A_CNT_6		00000000	Yes	N/A	R/W
0x3C	EXT_TRIG_A_CNT_7	7:0	EXT_TRIG_A_CNT_7		00000000	Yes	N/A	R/W
0x3D	EXT_TRIG_A_CNT_8	7:0	EXT_TRIG_A_CNT_8		00000000	Yes	N/A	R/W
0x3E	EXT_TRIG_A_CNT_9	7:0	EXT_TRIG_A_CNT_9		00000000	Yes	N/A	R/W
0x3F	EXT_TRIG_A_CNT_10	7:0	EXT_TRIG_A_CNT_10		00000000	Yes	N/A	R/W

Table 37: MIPI RFFE Gain Select

			LNAx_GAIN_BIAS Register[1]						
			GAIN_CTRL				LNA_BIAS		
Gain	MTK	QC/LSI	D6	D5	D4	D3	D2	D1	D0
G12 (21 dB)	X (MHB Only)	X (MHB Only)	1	1	0	0	1	1	1
G11 (18 dB)	X	X	1	0	1	1	1	1	1
G10 (15 dB)		X	1	0	1	0	1	0	0
G09 (12 dB)	X		1	0	0	1	1	0	0
G08 (9 dB)		X	1	0	0	0	0	1	1
G07 (6 dB)	X	X	0	1	1	1	0	1	1
G06 (3 dB)			0	1	1	0	0	0	1
G05 (0 dB)	X		0	1	0	1	0	0	1
G04 (-3 dB)		X	0	1	0	0	0	0	0
G03 (-6 dB)	X		0	0	1	1	0	0	0
G02 (-9 dB)			0	0	1	0	0	0	0
G01 (-12 dB)	X		0	0	0	1	0	0	0

[1] See MIPI registers 0x0E to 0x14

Table 38: MIPI RFFE Timing Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK Frequency	f_{SCLK}	0.032	–	52	MHz	Extended Frequency Range
		0.032	–	26	MHz	Standard Frequency Range
VIO Rise Time	T_{VIO-R}	50 [1]	–	450	μs	See Fig. 2
VIO Reset Time	$T_{VIO-RST}$	10	–	–	μs	See Fig. 2
Reset Delay Time	T_{SIGOL}	0.12	–	–	μs	See Fig. 2
Power up settling time	t_{setup}	–	–	25	µs	After switching to Normal Mode

[1]VIO rise time down to 10μs is supported as long as first programming starts 50μs after Vio rise

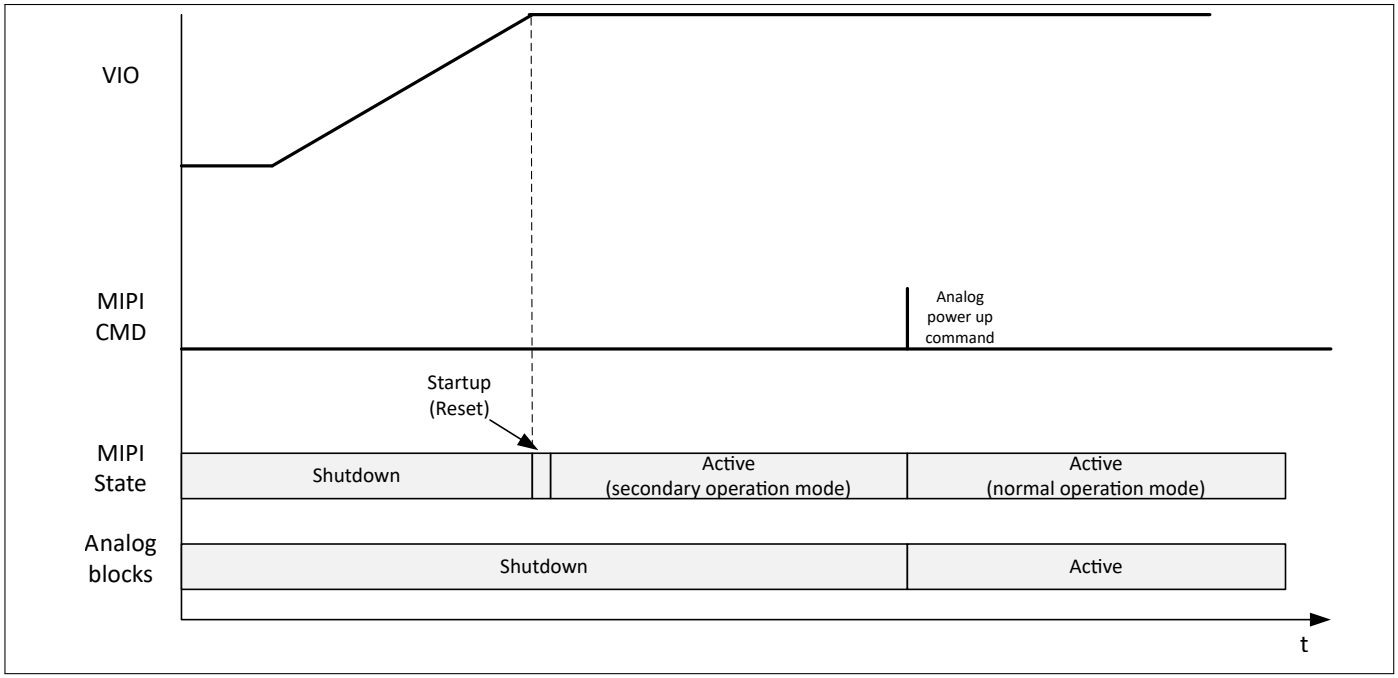


Figure 1: Startup Timing Diagram

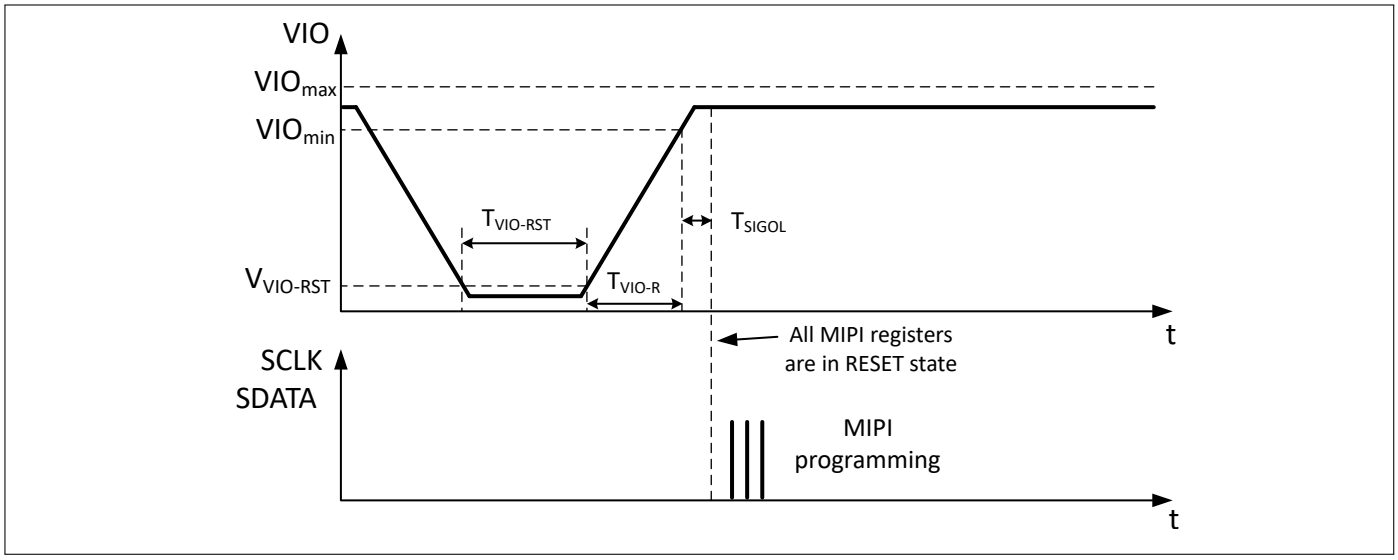


Figure 2: V_{IO} Reset Timing Diagram

5 Application Information

BGM687U50 has a package size of 2800 µm in X-dimension and 2800 µm in Y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 3 shows the footprint from top view. Pin definitions and functions are listed in Tab. 39.

Pin Configuration and Function

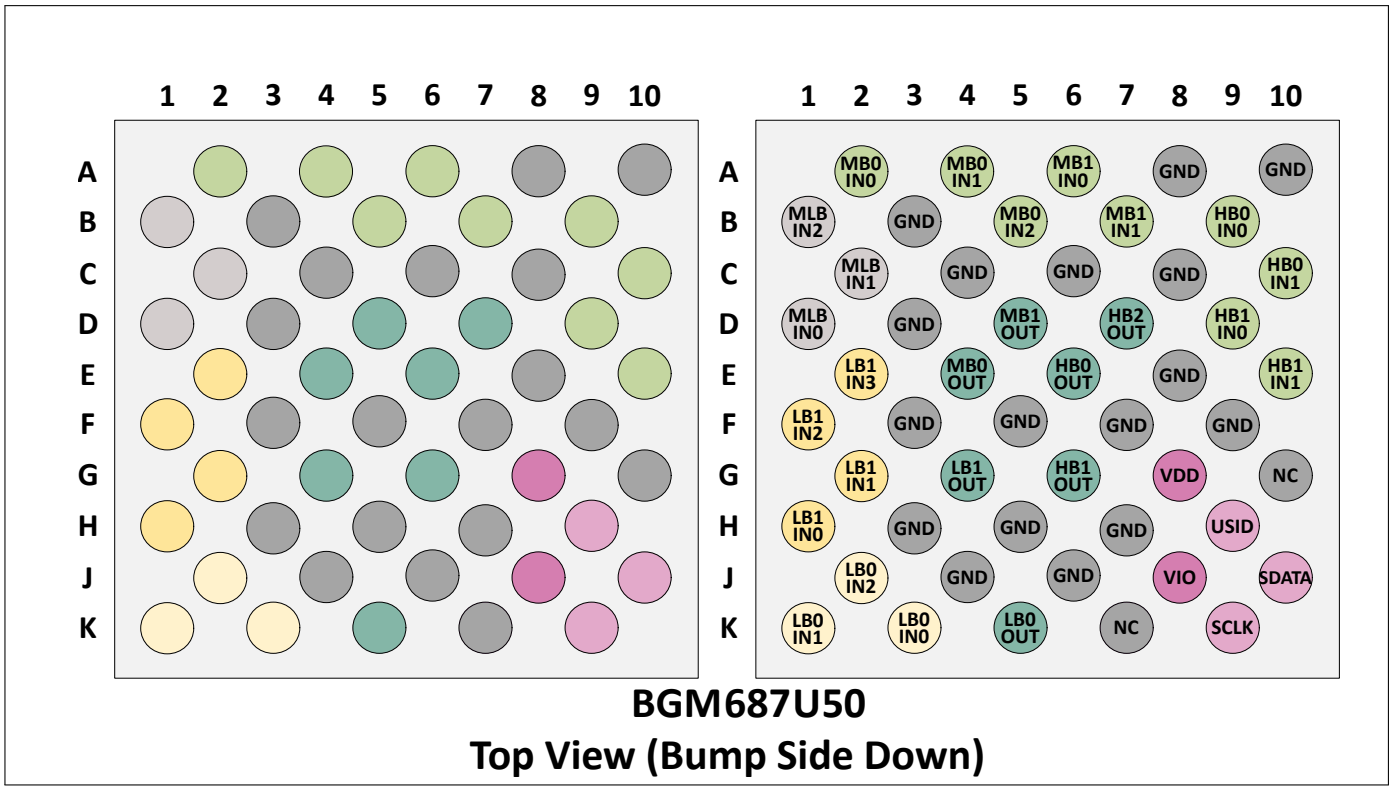


Figure 3: BGM687U50 Pin Configuration (top view / bumpside down)

Table 39: Pin Definition, Function and Coordinates (referred coordinates from Fig.3 and bump-side-down view)

Pin No.	Name	Function
A2	MB0_IN0	RF Input of LNA4 (MLB/MB/HB)
A4	MB0_IN1	RF Input of LNA4 (MLB/MB/HB)
A6	MB1_IN0	RF Input of LNA5 (MLB/MB/HB)
A8	GND	Ground
A10	GND	Ground
C10	HB0_IN1	RF Input of LNA6 (MLB/MB/HB)
E10	HB1_IN1	RF Input of LNA7 (MLB/MB/HB)
G10	NC	Internally Not Connected
J10	SDATA	SDATA Input (MIPI)
K9	SCLK	SCLK Input (MIPI)
K7	NC	Internally Not Connected
K5	LB0_OUT	RF Output
K3	LB0_IN0	RF Input of LNA1 (LB)
K1	LB0_IN1	RF Input of LNA1 (LB)
H1	LB1_IN0	RF Input of LNA2 (LB)
F1	LB1_IN2	RF Input of LNA2 (LB)
D1	MLB_IN0	RF Input of LNA3 (MLB/MB/HB)
B1	MLB_IN2	RF Input of LNA3 (MLB/MB/HB)
B3	GND	Ground
B5	MB0_IN2	RF Input of LNA4 (MLB/MB/HB)
B7	MB1_IN1	RF Input of LNA5 (MLB/MB/HB)
B9	HB0_IN0	RF Input of LNA6 (MLB/MB/HB)
D9	HB1_IN0	RF Input of LNA7 (MLB/MB/HB)
F9	GND	Ground
H9	USID	USID Select Input (connect to VIO/GND)
J8	VIO	VIO Supply (MIPI)
J6	GND	Ground
J4	GND	Ground
J2	LB0_IN2	RF Input of LNA1 (LB)
G2	LB1_IN1	RF Input of LNA2 (LB)
E2	LB1_IN3	RF Input of LNA2 (LB)
C2	MLB_IN1	RF Input of LNA3 (MLB/MB/HB)
C4	GND	Ground
C6	GND	Ground
C8	GND	Ground
E8	GND	Ground
G8	VDD	LNA Supply
H7	GND	Ground
H5	GND	Ground

Table 40: Continued Pin Definition, Function and Coordinates (referred coordinates from Fig.3 and bump-side-down view)

Pin No.	Name	Function
H3	GND	Ground
F3	GND	Ground
D3	GND	Ground
D5	MB1_OUT	RF Output
D7	HB2_OUT	RF Output
F7	GND	Ground
G6	HB1_OUT	RF Output
G4	LB1_OUT	RF Output
E4	MB0_OUT	RF Output
E6	HB0_OUT	RF Output
F5	GND	Ground

Application Board Configuration

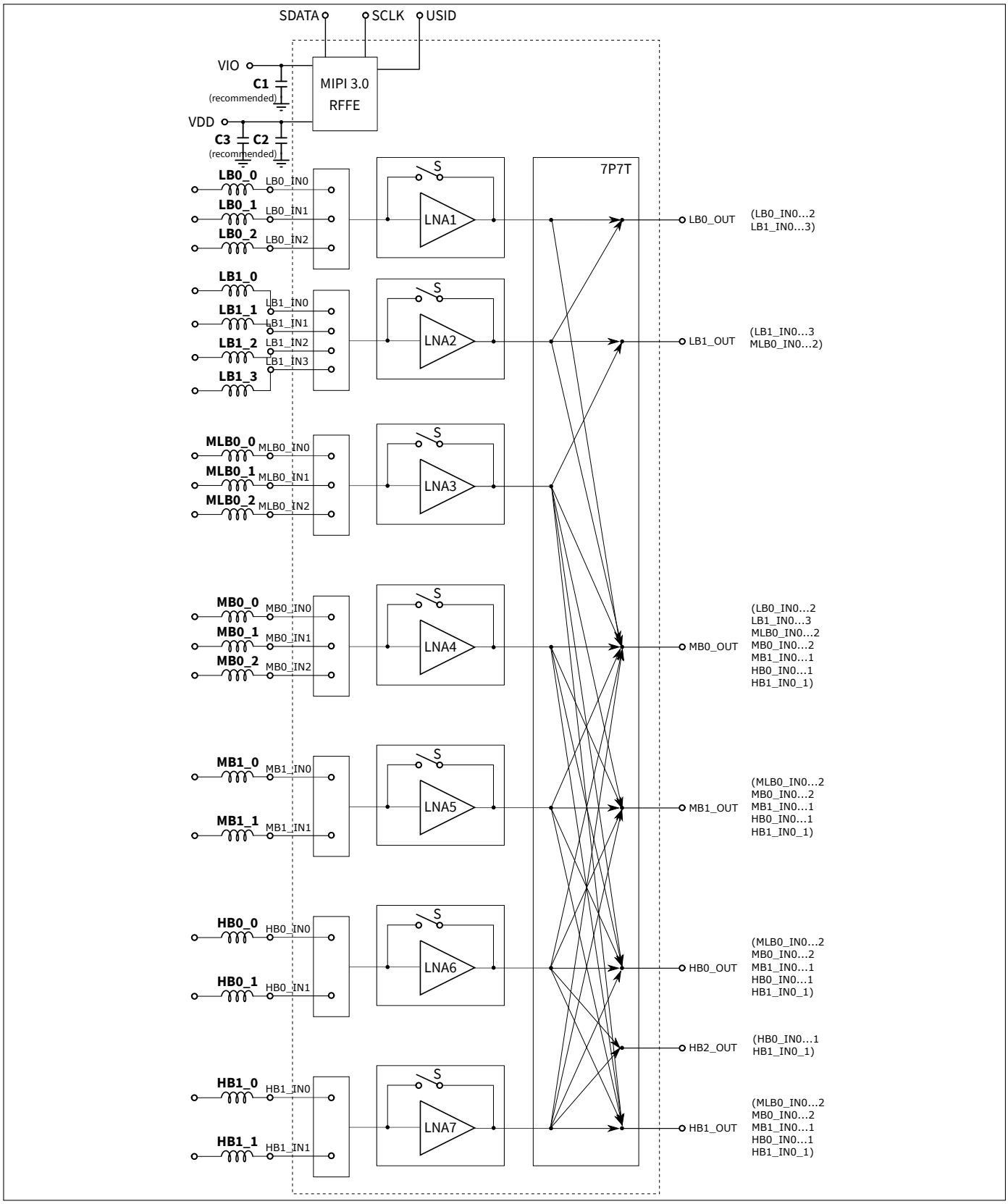


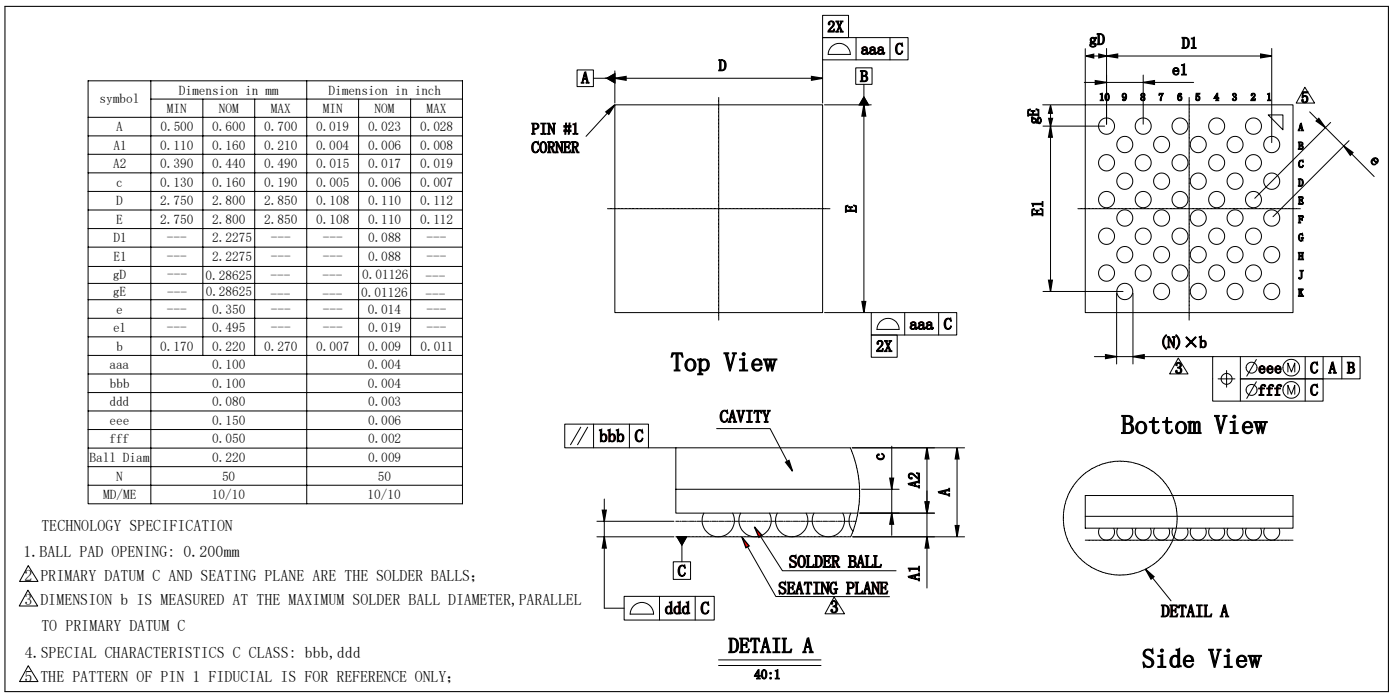
Figure 4: BGM687U50 Application Schematic

Table 41: Bill of Materials Table

Name	Value	Frequency Range	Package	Function
C1-C2	10nF	n.a.	0201	RF bypass[1]
C3	10µF	n.a.	0402	RF bypass[1]
LB0_0	15nH	758 - 803 MHz	0201	Input matching[2]
LB0_1	24nH	617 - 652 MHz	0201	Input matching[2]
LB0_2	10nH	925 - 960 MHz	0201	Input matching[2]
LB1_0	16nH	758 - 803 MHz	0201	Input matching[2]
LB1_1	24nH	617 - 652 MHz	0201	Input matching[2]
LB1_2	12nH	859 - 894 MHz	0201	Input matching[2]
LB1_3	11nH	925 - 960 MHz	0201	Input matching[2]
MLB0_0	5.6nH	2110 - 2170 MHz	0201	Input matching[2]
MLB0_1	12nH	1452 - 1496 MHz	0201	Input matching[2]
MLB0_2	4nH	2496 - 2690 MHz	0201	Input matching[2]
MB0_0	4nH	2496 - 2690 MHz	0201	Input matching[2]
MB0_1	8.2nH	1805 - 1880 MHz	0201	Input matching[2]
MB0_2	12nH	1452 - 1496 MHz	0201	Input matching[2]
MB1_0	12nH	1452 - 1496 MHz	0201	Input matching[2]
MB1_1	4nH	2496 - 2690 MHz	0201	Input matching[2]
HB0_0	3.6nH	2496 - 2690 MHz	0201	Input matching[2]
HB0_1	7.5nH	1805 - 1880 MHz	0201	Input matching[2]
HB1_0	6.8nH	1805 - 1880 MHz	0201	Input matching[2]
HB1_1	4nH	2496 - 2690 MHz	0201	Input matching[2]
N1	BGM687U50	n.a.	PG-WF2BGA-50-1	7x LNA Bank for 5G

[1]RF bypass recommended to mitigate power supply noise.
[2]The matching elements used are of the type: LQP03HQ.

6 Package Information



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.500	0.600	0.700	0.019	0.023	0.028
A1	0.110	0.160	0.210	0.004	0.006	0.008
A2	0.390	0.440	0.490	0.015	0.017	0.019
c	0.130	0.160	0.190	0.005	0.006	0.007
D	2.750	2.800	2.850	0.108	0.110	0.112
E	2.750	2.800	2.850	0.108	0.110	0.112
D1	---	2.2275	---	---	0.088	---
E1	---	2.2275	---	---	0.088	---
gD	---	0.28625	---	---	0.01126	---
gE	---	0.28625	---	---	0.01126	---
e	---	0.350	---	---	0.014	---
e1	---	0.495	---	---	0.019	---
b	0.170	0.220	0.270	0.007	0.009	0.011
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.220			0.009		
N	50			50		
MD/ME	10/10			10/10		

TECHNOLOGY SPECIFICATION

1. BALL PAD OPENING: 0.200mm
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;

Figure 5: PG-WF2BGA-50-1 Package Outline (top and side views)

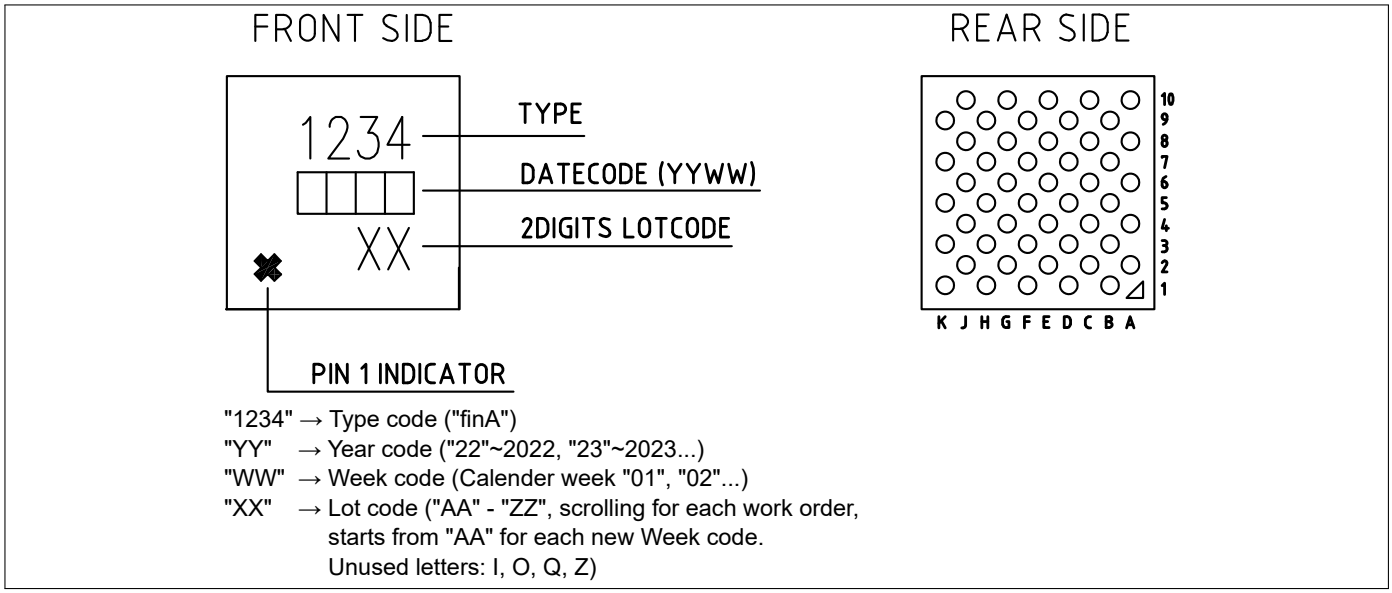


Figure 6: Marking Specification

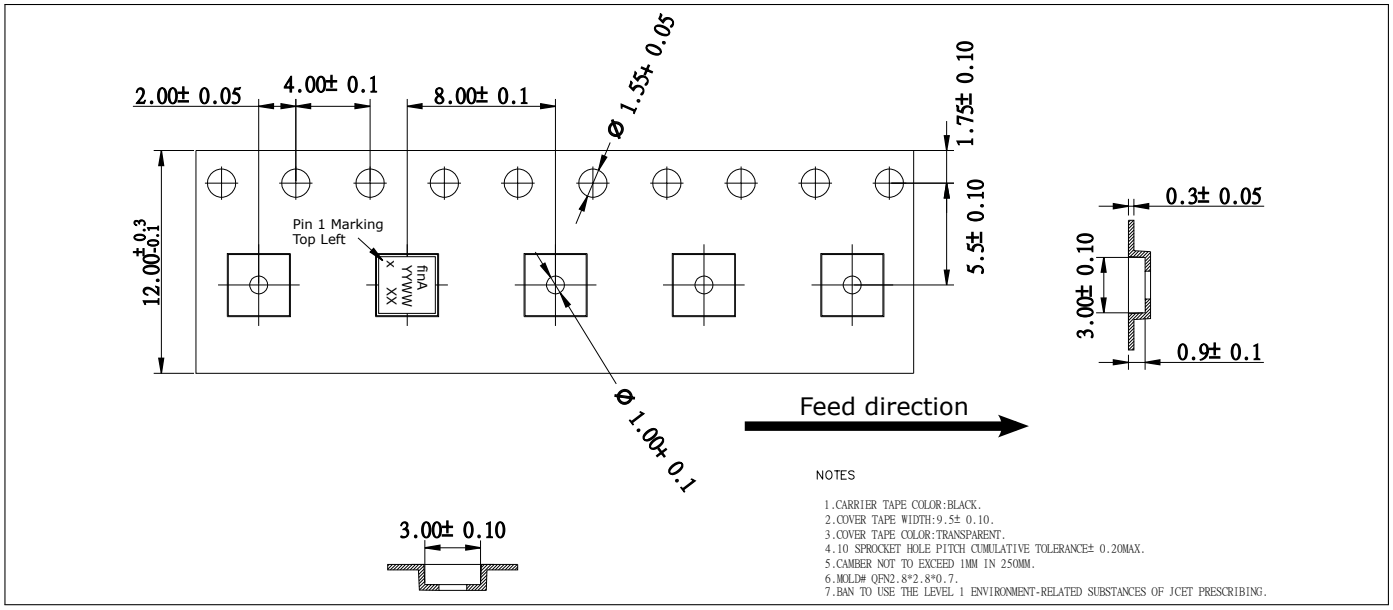


Figure 7: PG-WF2BGA-50-1 Carrier Tape

7 Revision History

Previous Datasheet Revision	
Datasheet Revision v2.1 - 2023-03-29	
Revision History	
Datasheet, Revision 2.2- 2023-04-26	
Page or Item	**Subjects (major changes since previous revision)**
41	Updated Dimensions Table within Figure 5

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