High Input Survivability, Low Noise Amplifier, 6 GHz to 12 GHz

FEATURES

- High input power survivability: 34 dBm at 6 GHz to 12 GHz
- Single positive supply: 5 V/100 mA nominal
- RBIAS drain current adjustment pin
- Fast overdrive recovery: 25 ns at 32 dBm
- Gain: 25 dB typical from 8 GHz to 10 GHz
- OIP3: 32.1 dBm typical from 8 GHz to 10 GHz
- Noise figure: 1.7 dB typical at 8 GHz to 10 GHz
- Extended operating temperature range: −55°C to + 125°C
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Test instrumentation
- Military communications
- Radar

GENERAL DESCRIPTION

The ADL8103 is a 6 GHz to 12 GHz low noise amplifier (LNA) with 34 dBm RF input power survivability. The ADL8103 provides a typical gain of 25 dB at 8 GHz to 10 GHz, a 1.7 dB typical noise figure at 8 GHz to 10 GHz, a 21 dBm typical output power for 1 dB compression (OP1dB) at 8 GHz to 10 GHz, and a typical output third-order intercept (OIP3) of 32.1 dBm at 8 GHz to 10 GHz. This LNA has a high output second-order intercept (OIP2) of 36.5 dBm typical at 8 GHz to 10 GHz, making the ADL8103 suitable for military and test instrumentation applications. The nominal quiescent current (I_{DQ}), which can be adjusted, is 100 mA from a 5 V supply voltage (V_{DD}). The ADL8103 also features inputs and outputs that are internally matched to 50 Ω.

The device is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP and is specified for operation from −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

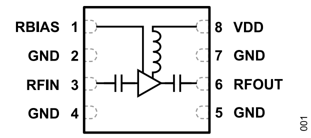

Figure 1. Functional Block Diagram

Rev. 0

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

9/2024—Revision 0: Initial Version

SPECIFICATIONS

6 GHZ TO 8 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 100 mA, bias resistance, R_{BIAS} = 698 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 6 GHz to 8 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	6		8	GHz	
GAIN	25	27		dB	
Gain Variation over Temperature		0.018		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
Input		10.2		dB	
Output		8		dB	
OUTPUT					
OP1dB		19		dBm	
Saturated Output Power (P_{SAT})		21.7		dBm	
OIP3		29.3		dBm	Measurement taken at output power (P_{OUT}) per tone = 6 dBm
OIP2		34		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
POWER ADDED EFFICIENCY (PAE)		21.6		%	Measured at P_{SAT}

8 GHZ TO 10 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 100 mA, R_{BIAS} = 698 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 8 GHz to 10 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	8		10	GHz	
GAIN	23	25		dB	
Gain Variation over Temperature		0.014		dB/°C	
NOISE FIGURE		1.7		dB	
RETURN LOSS					
Input		10.1		dB	
Output		17		dB	
OUTPUT					
OP1dB	19	21		dBm	
P_{SAT}		22.6		dBm	
OIP3		32.1		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
OIP2		36.5		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
PAE		24.4		%	Measured at P_{SAT}

SPECIFICATIONS

10 GHZ TO 12 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 100 mA, R_{BIAS} = 698 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 10 GHz to 12 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	10		12	GHz	
GAIN	22	24		dB	
Gain Variation over Temperature		0.013		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
Input		12		dB	
Output		24.4		dB	
OUTPUT					
OP1dB	19	21		dBm	
P_{SAT}		22.6		dBm	
OIP3		32.9		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
OIP2		41.9		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
PAE		26.2		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 4. DC Specifications

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		100		mA
Amplifier Current (I_{DQ_AMP})		95.5		mA
RBIAS Current (I_{RBIAS})		4.5		mA
SUPPLY VOLTAGE				
V_{DD}	3	5	6	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	7 V
RF Input Power Survivability (RFIN)	See Figure 2
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (derate 15.87 mW/°C above 85°C)	1.43 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Nominal Junction (T_{CASE} = 85°C, V_{DD} = 5 V, I_{DQ} = 100 mA, input power (P_{IN}) = off)	116.5°C
Maximum Junction	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

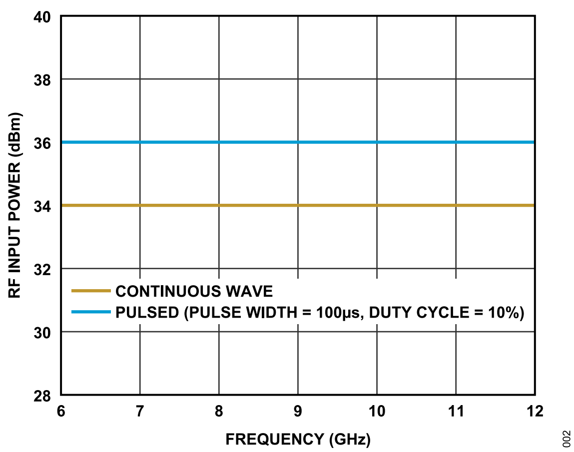


Figure 2. RF Input Power Absolute Maximum Ratings for Pulsed and Continuous Wave vs. Frequency, T_{CASE} = 85°C

THERMAL RESISTANCE

Overall thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	60	°C/W
Worst Case[2], T_{CASE} = 85°C	63	°C/W

1 Thermal resistance varies with operating conditions.

2 Across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

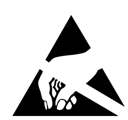
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8103

Table 7. ADL8103, 8-Lead LFCSP

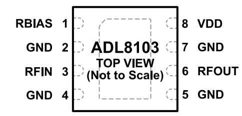
ESD Model	Withstand Threshold (V)	Class
HBM	±300	1A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND.

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the I_{DQ}. See Figure 91 and Table 9 for more details. See Figure 4 for the interface schematic.
2, 4, 5, 7	GND	Ground. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 7 for the interface schematic.
3	RFIN	RF Input. The RFIN pin is AC-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
6	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
8	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 6 for the interface schematic.
	EXPOSED PADDLE	Exposed Ground Paddle. Connect the exposed paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

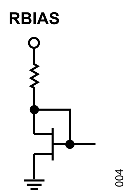


Figure 4. RBIAS Interface Schematic

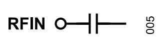


Figure 5. RFIN Interface Schematic

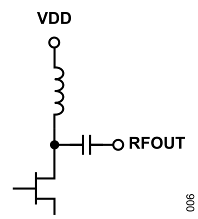


Figure 6. VDD and RFOUT Interface Schematic

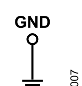


Figure 7. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

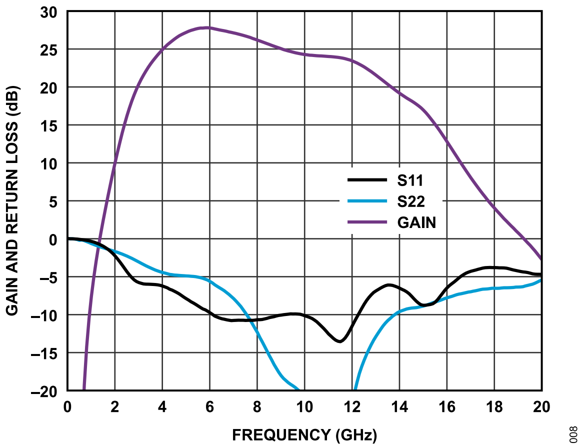


Figure 8. Broadband Gain and Return Loss vs. Frequency, 10 MHz to 20 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

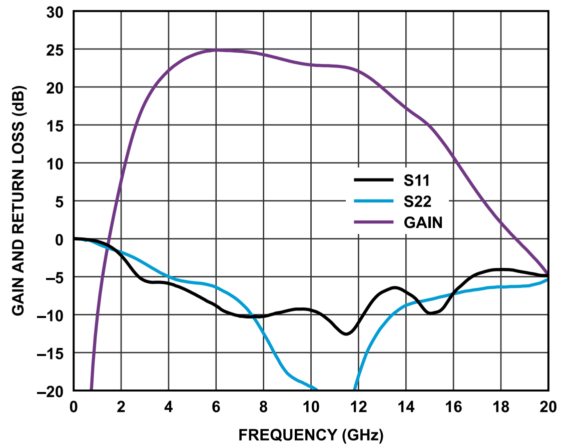


Figure 11. Broadband Gain and Return Loss vs. Frequency, 10 MHz to 20 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

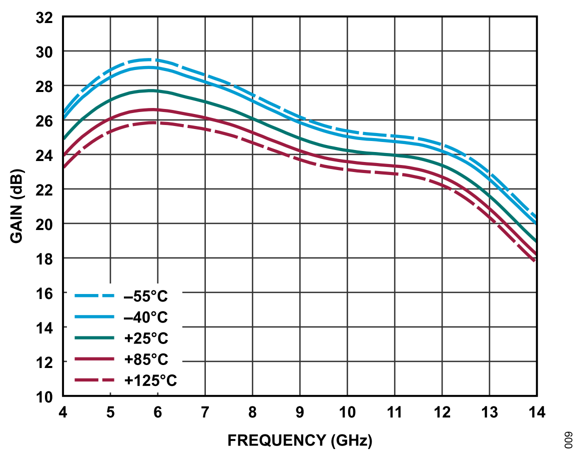


Figure 9. Gain vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

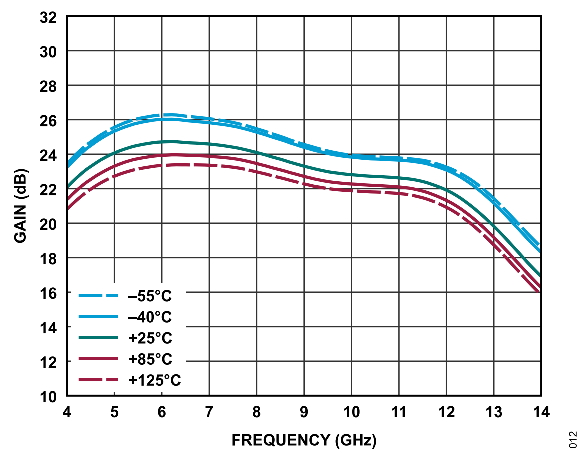


Figure 12. Gain vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

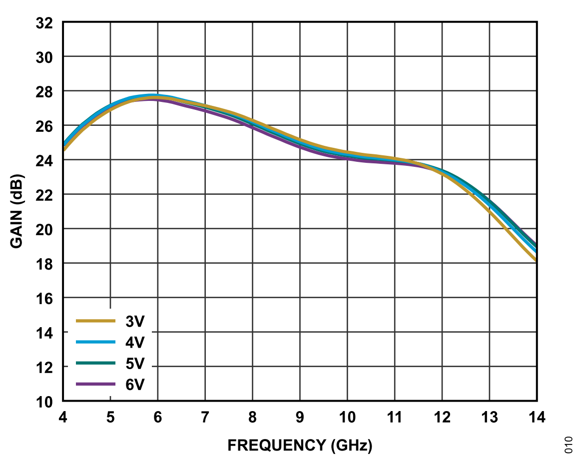


Figure 10. Gain vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

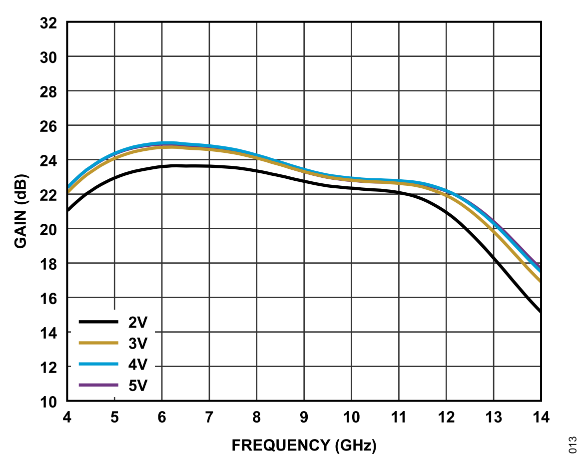


Figure 13. Gain vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

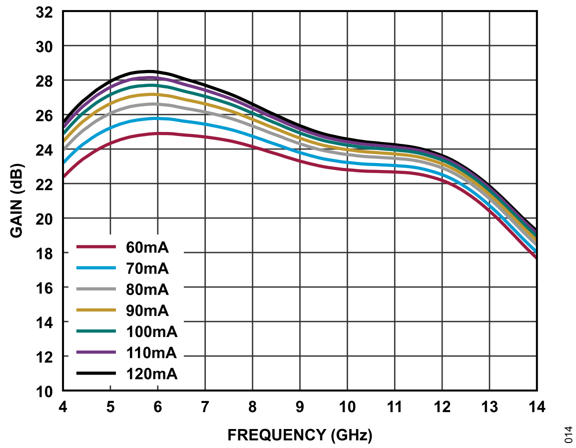


Figure 14. Gain vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

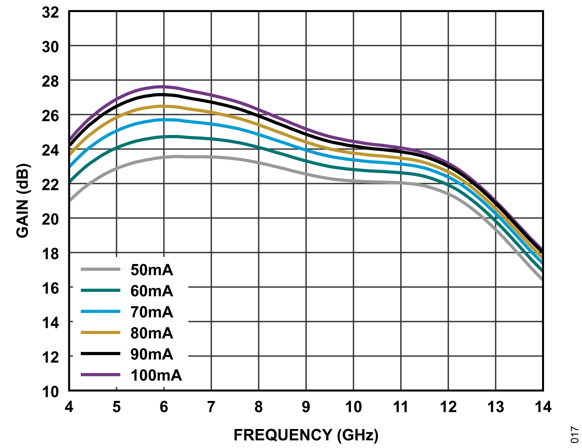


Figure 17. Gain vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

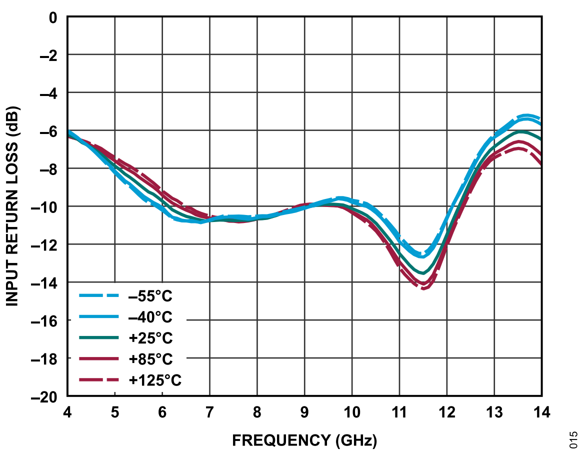


Figure 15. Input Return Loss vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

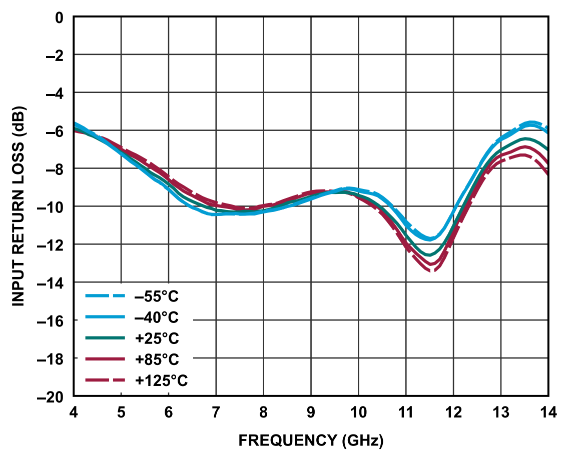


Figure 18. Input Return Loss vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

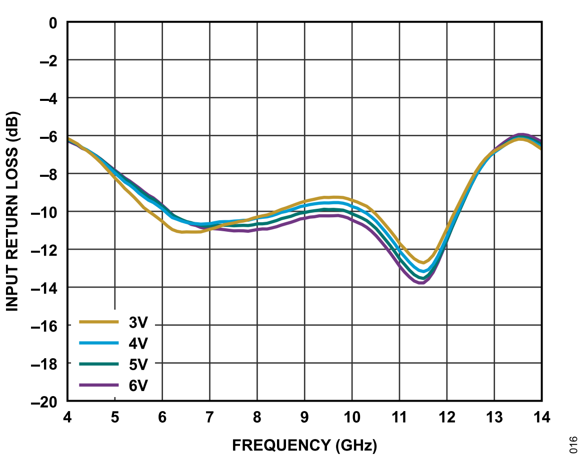


Figure 16. Input Return Loss vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

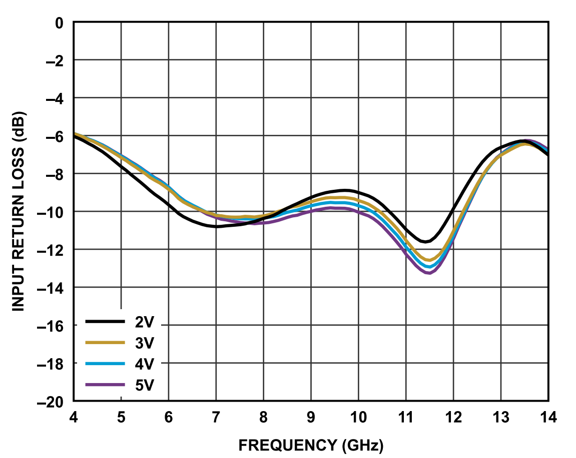


Figure 19. Input Return Loss vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

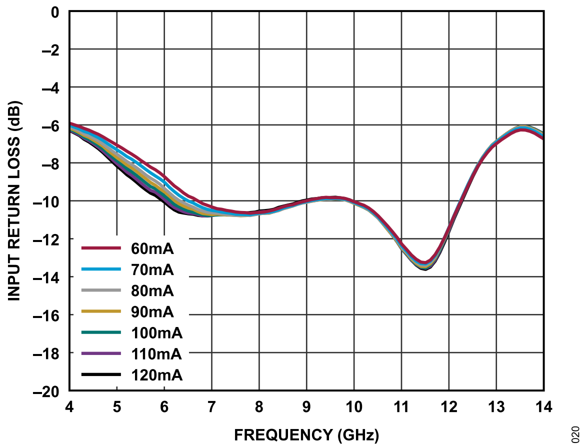


Figure 20. Input Return Loss vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

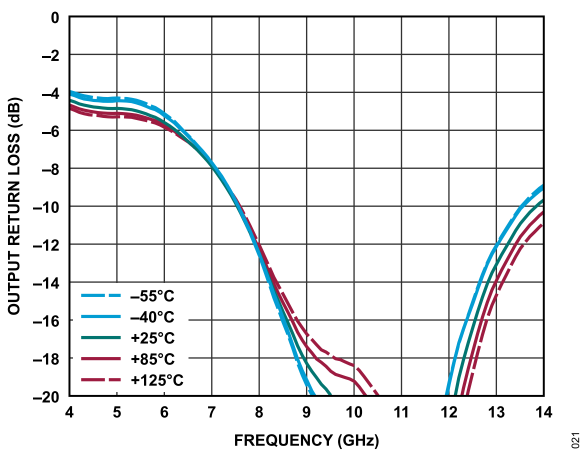


Figure 21. Output Return Loss vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

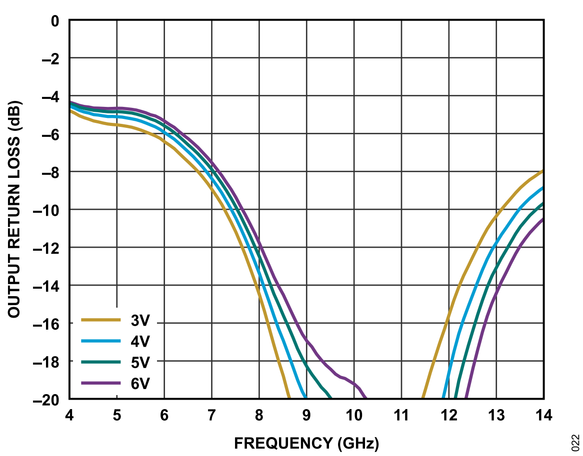


Figure 22. Output Return Loss vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

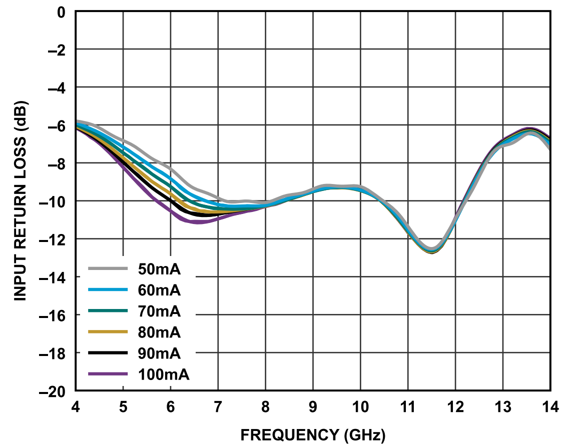


Figure 23. Input Return Loss vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

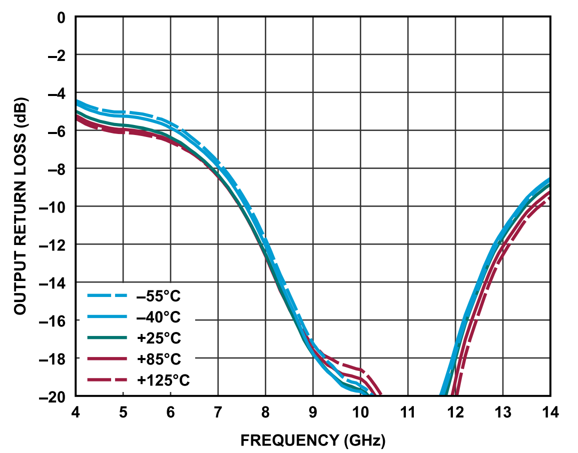


Figure 24. Output Return Loss vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

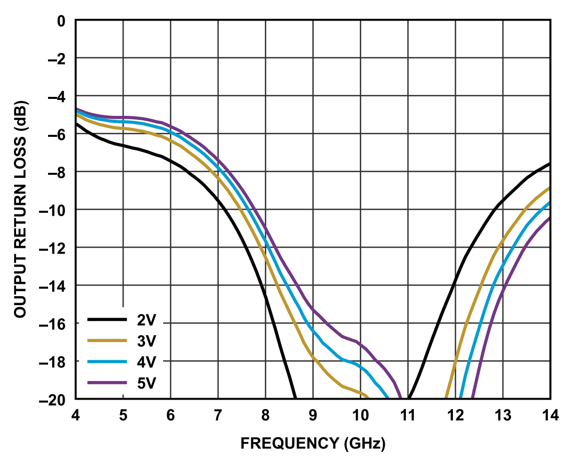


Figure 25. Output Return Loss vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

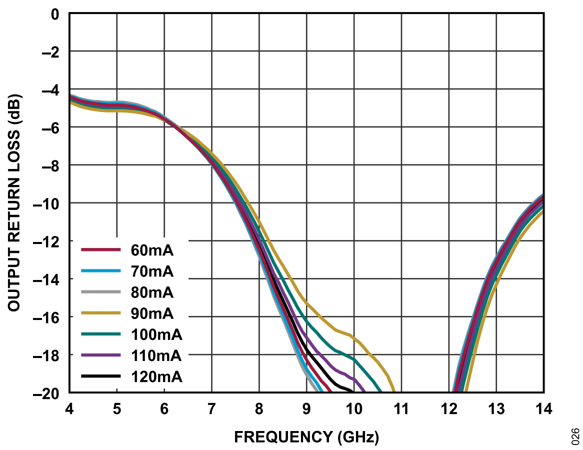


Figure 26. Output Return Loss vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

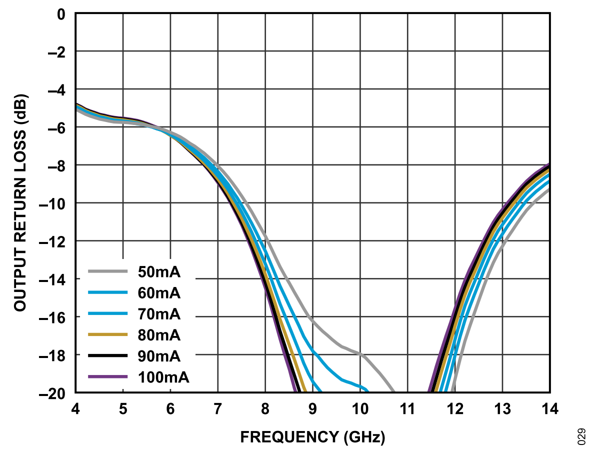


Figure 29. Output Return Loss vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

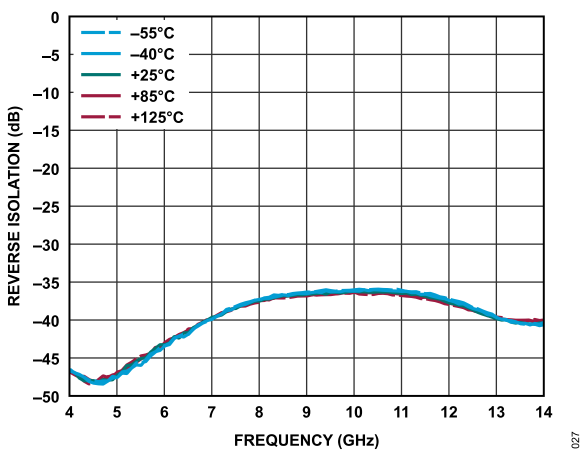


Figure 27. Reverse Isolation vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

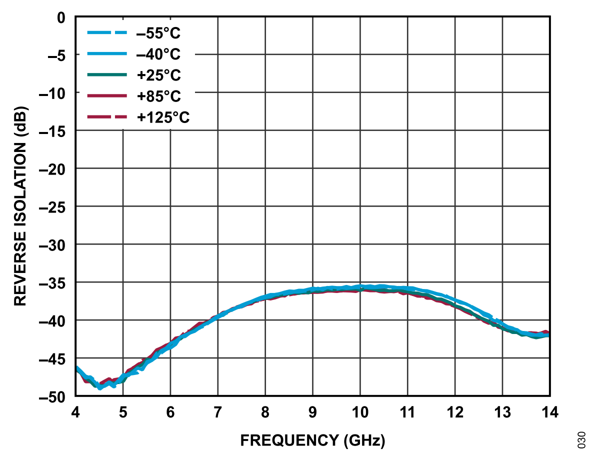


Figure 30. Reverse Isolation vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

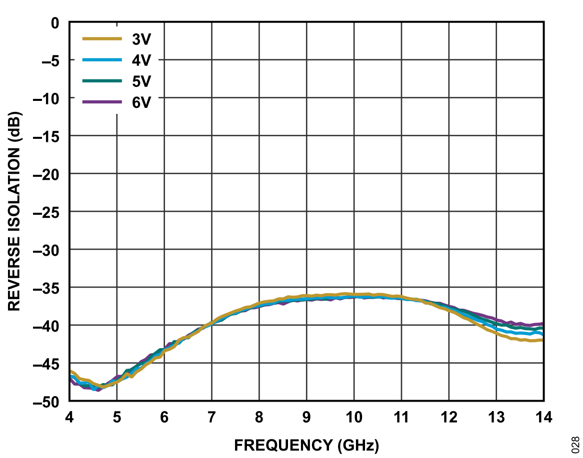


Figure 28. Reverse Isolation vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

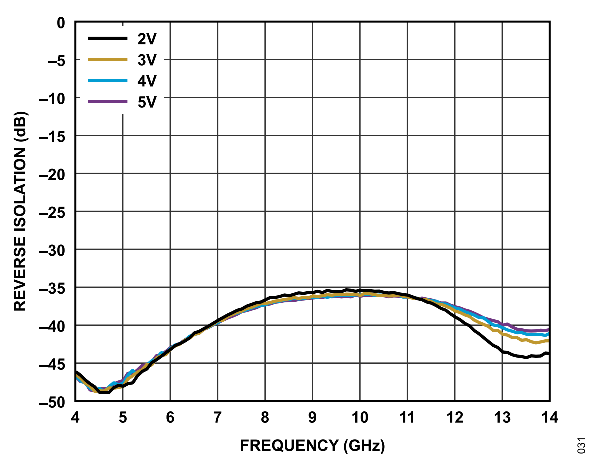


Figure 31. Reverse Isolation vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

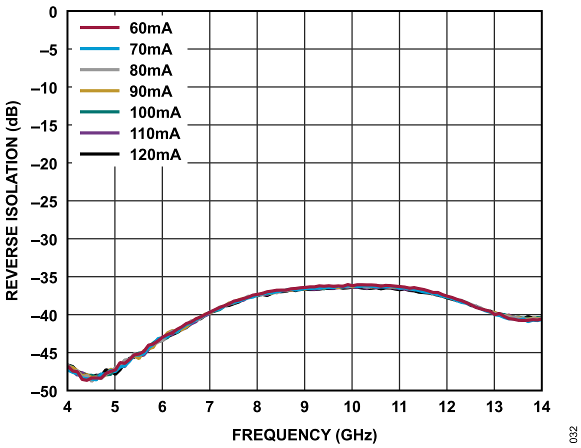


Figure 32. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

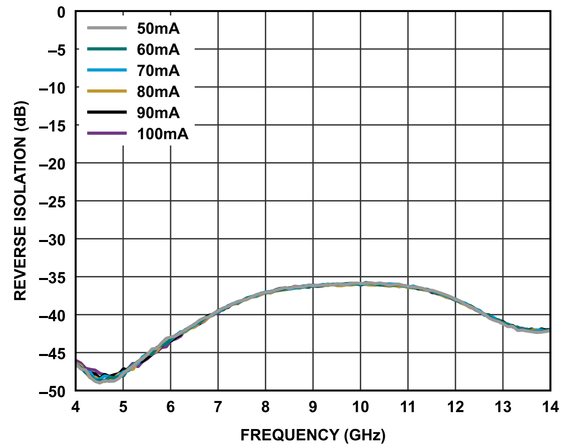


Figure 35. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

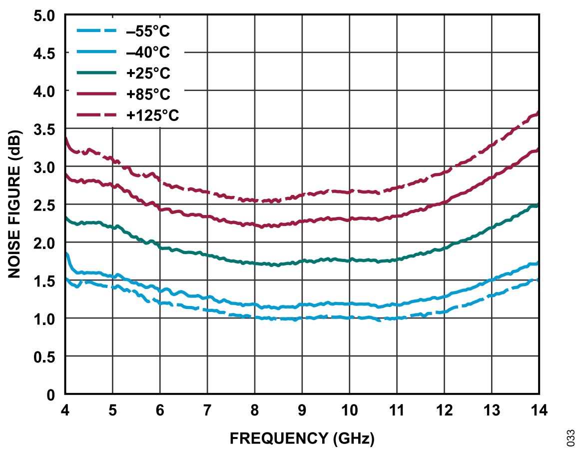


Figure 33. Noise Figure vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

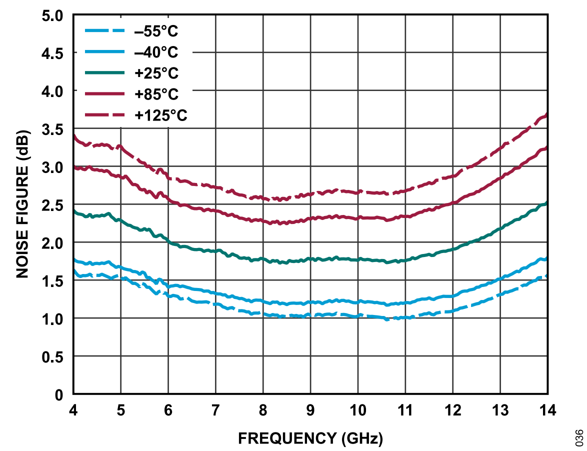


Figure 36. Noise Figure vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} =3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

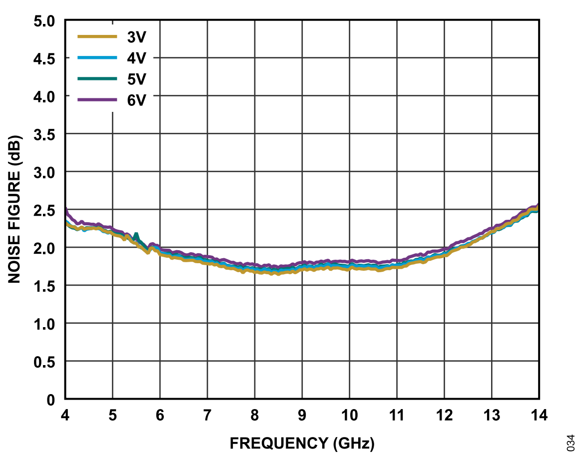


Figure 34. Noise Figure vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

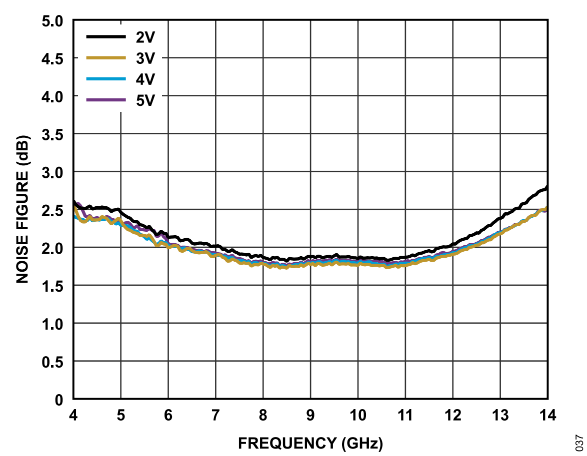


Figure 37. Noise Figure vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

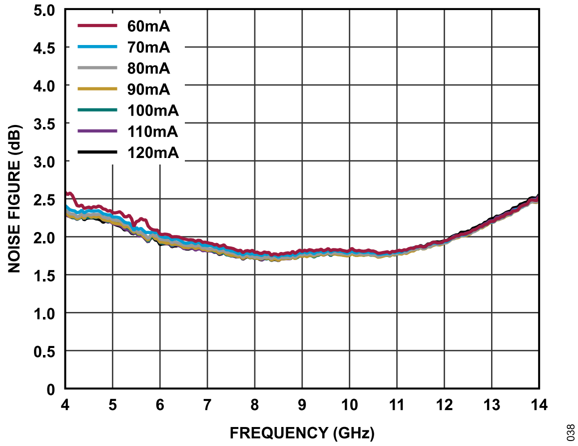


Figure 38. Noise Figure vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

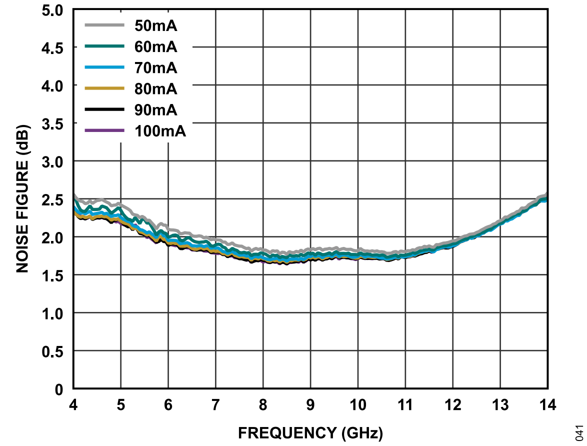


Figure 41. Noise Figure vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

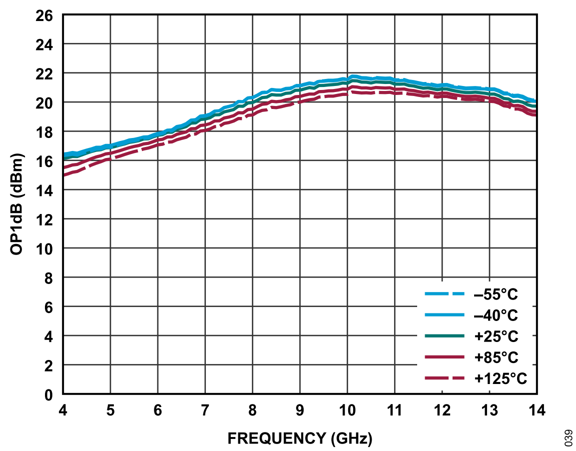


Figure 39. OP1dB vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

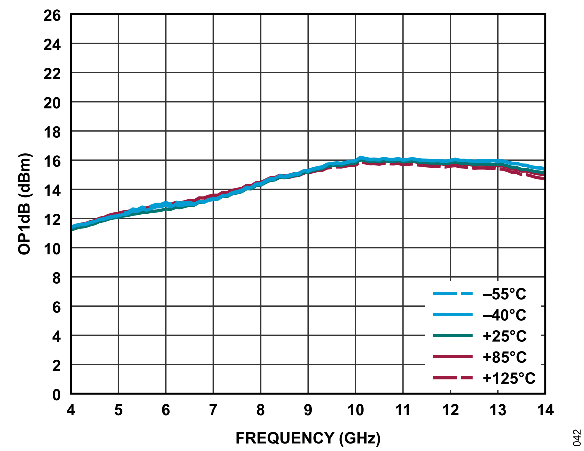


Figure 42. OP1dB vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

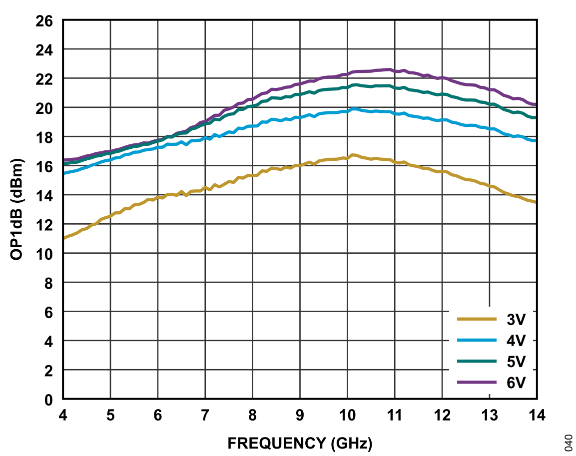


Figure 40. OP1dB vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

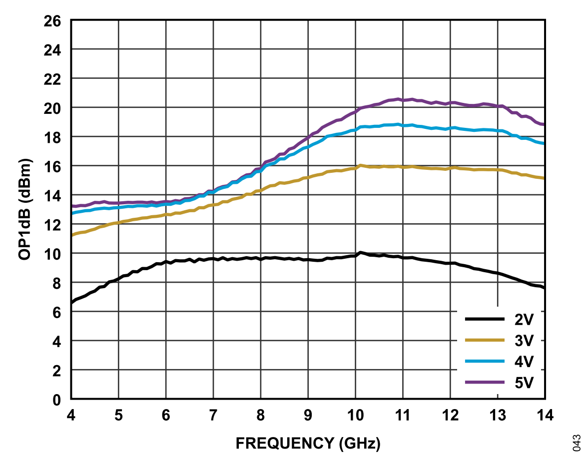


Figure 43. OP1dB vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

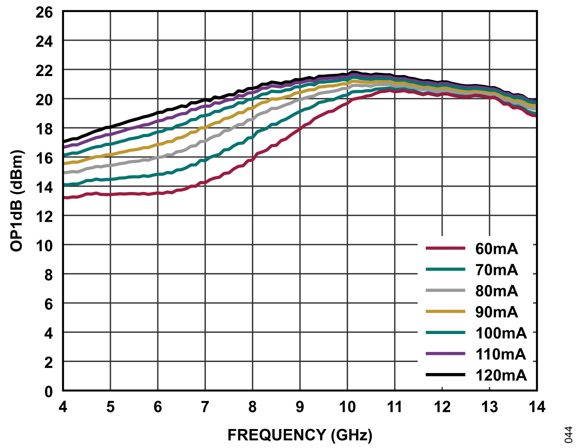


Figure 44. OP1dB vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

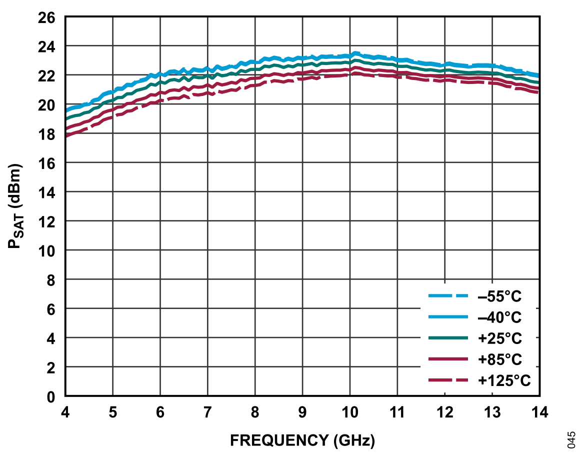


Figure 45. P_{SAT} vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

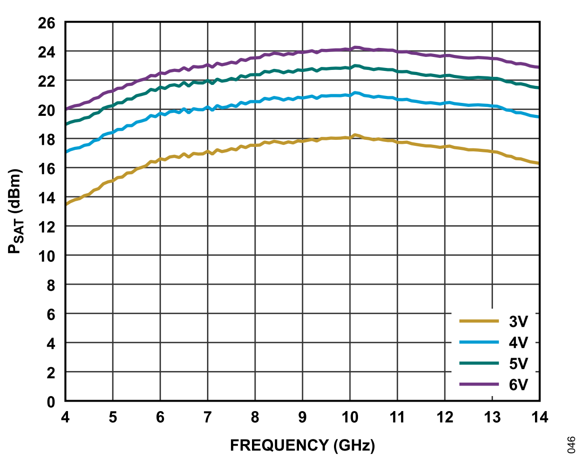


Figure 46. P_{SAT} vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

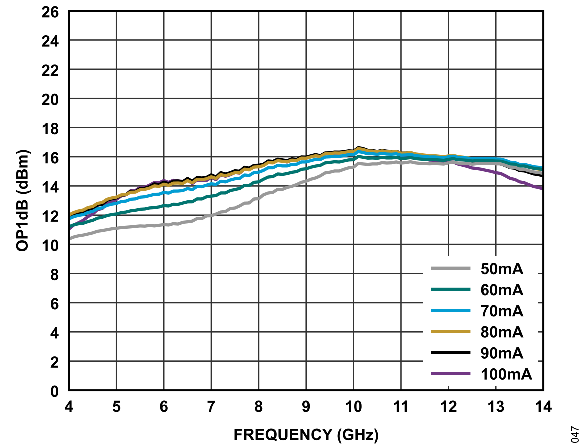


Figure 47. OP1dB vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

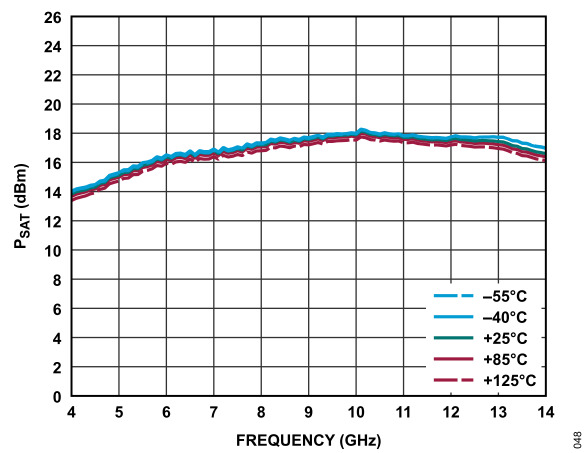


Figure 48. P_{SAT} vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

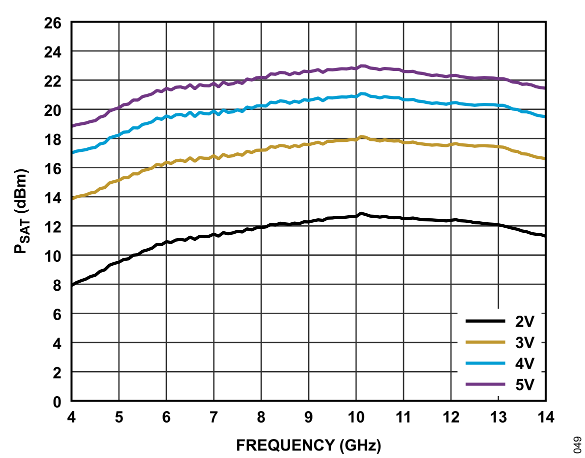


Figure 49. P_{SAT} vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

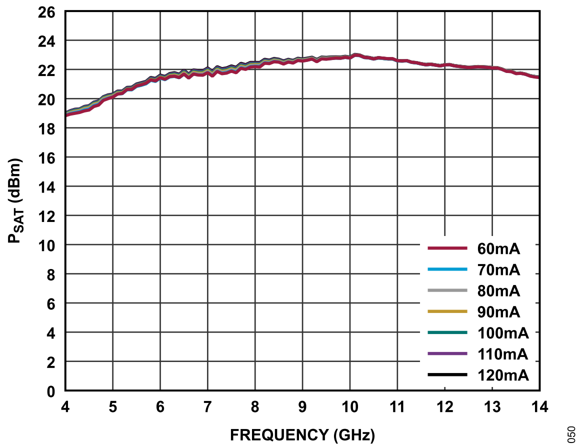


Figure 50. P_{SAT} vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

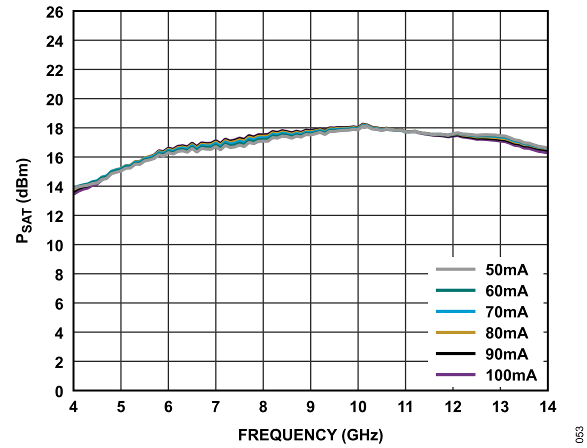


Figure 53. P_{SAT} vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

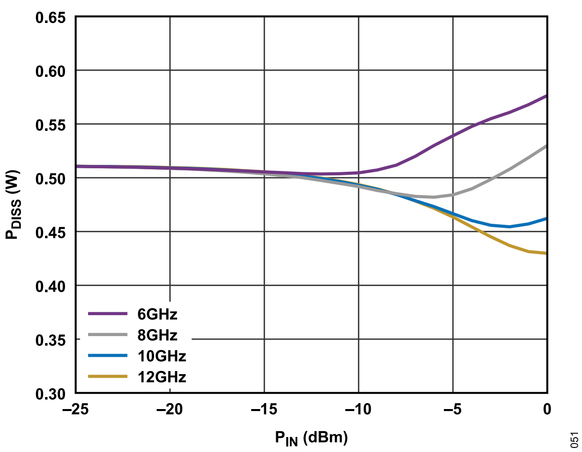


Figure 51. P_{DISS} vs. P_{IN} at T_{CASE} = 85°C, V_{DD} = 5 V, and R_{BIAS} = 698 Ω

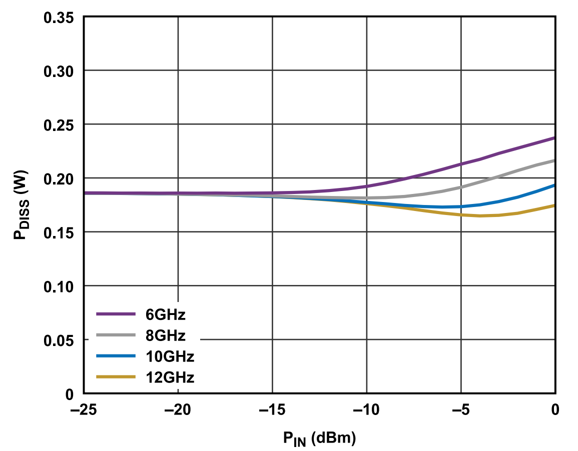


Figure 54. P_{DISS} vs. P_{IN} at T_{CASE} = 85°C, V_{DD} = 3 V, and R_{BIAS} = 470 Ω

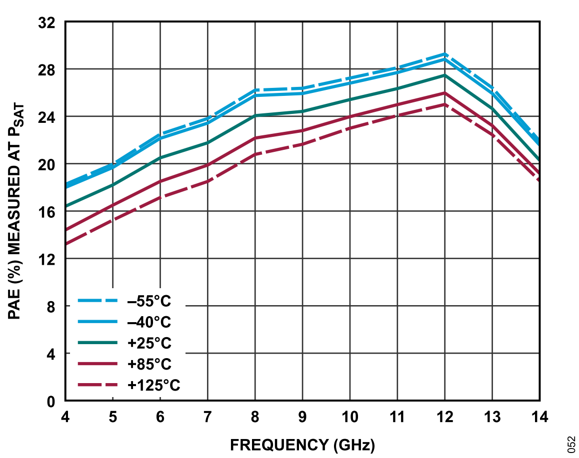


Figure 52. PAE vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

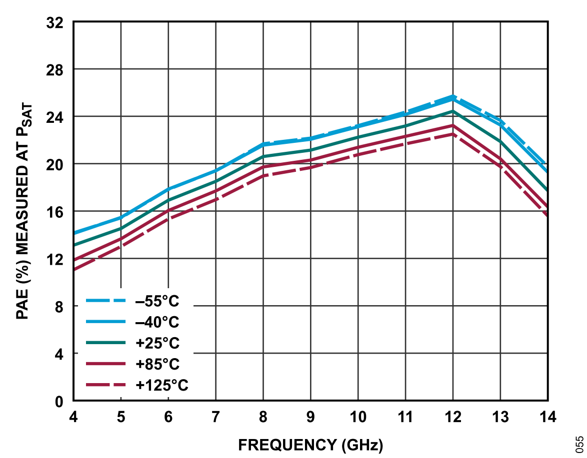


Figure 55. PAE vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, and R_{BIAS} = 470 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

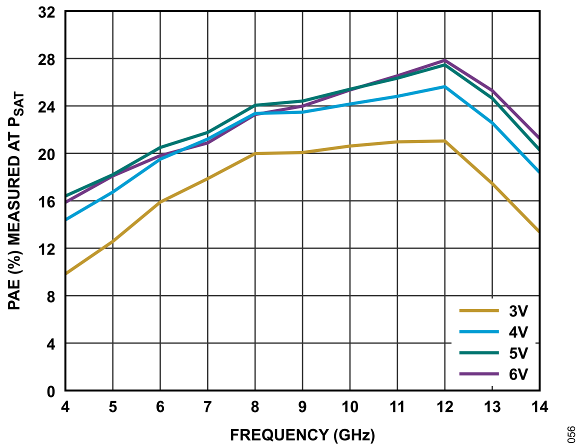


Figure 56. PAE vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 100 mA

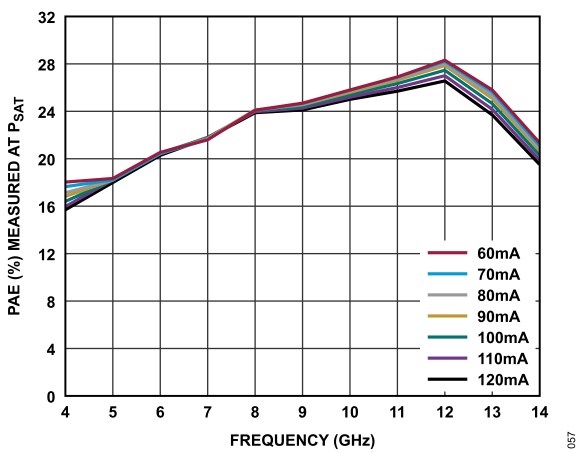


Figure 57. PAE vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 5 V

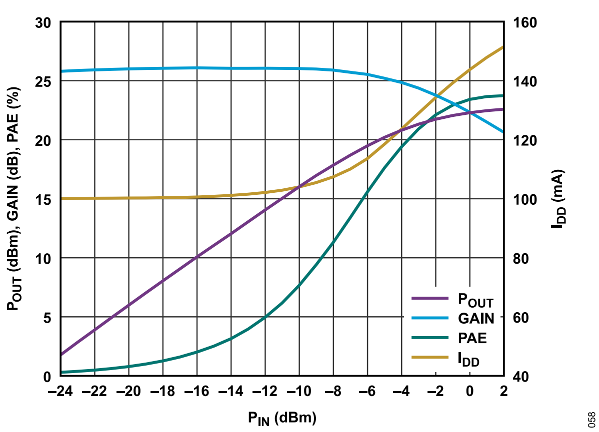


Figure 58. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. P_{IN}, Power Compression at 8 GHz, V_{DD} = 5 V, and R_{BIAS} = 698 Ω

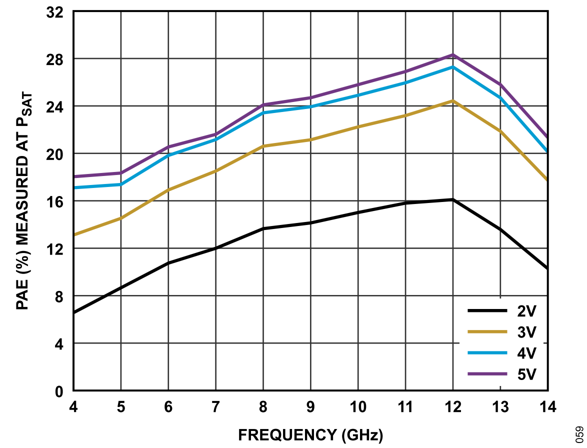


Figure 59. PAE vs. Frequency for Various Supply Voltages, 4 GHz to 14 GHz, and I_{DQ} = 60 mA

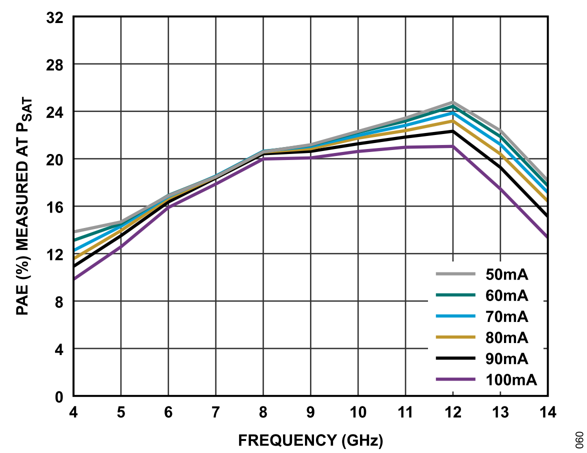


Figure 60. PAE vs. Frequency for Various I_{DQ} Values, 4 GHz to 14 GHz, and V_{DD} = 3 V

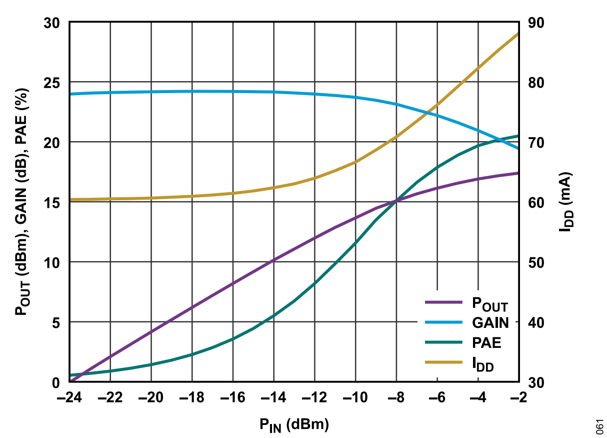


Figure 61. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 8 GHz, V_{DD} = 3 V, and R_{BIAS} = 470 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

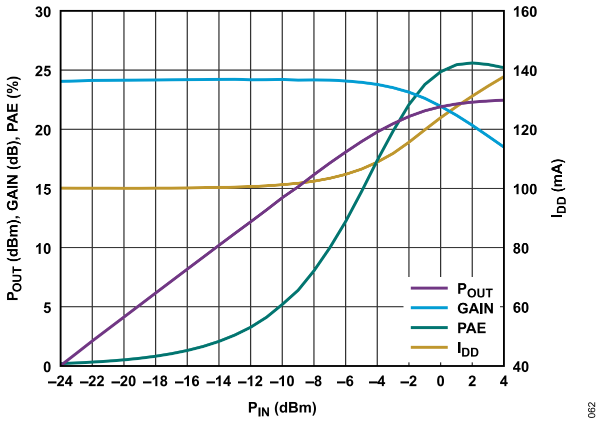


Figure 62. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 10 GHz, V_{DD} = 5 V, and R_{BIAS} = 698 Ω

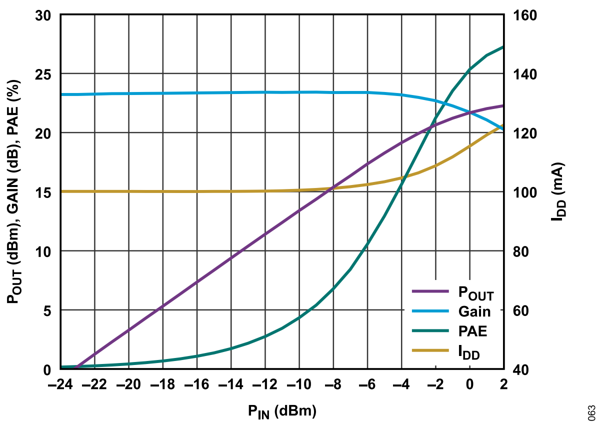


Figure 63. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 12 GHz, V_{DD} = 5 V, and R_{BIAS} = 698 Ω

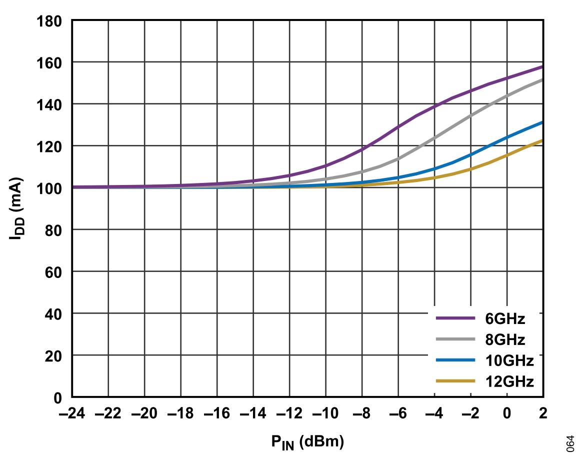


Figure 64. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 5 V, and R_{BIAS} = 698 Ω

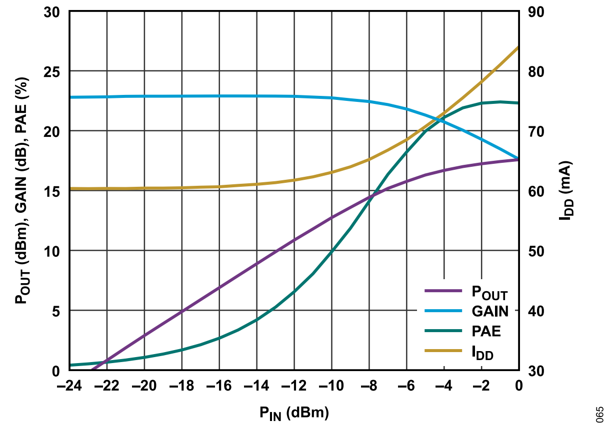


Figure 65. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 10 GHz, V_{DD} = 3 V, and R_{BIAS} = 470 Ω

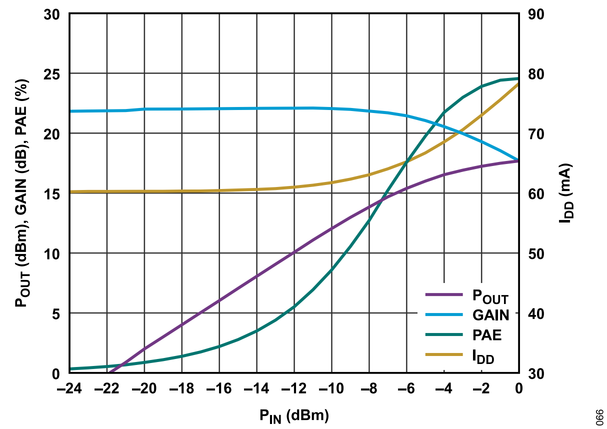


Figure 66. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 12 GHz, V_{DD} = 3 V, and R_{BIAS} = 470 Ω

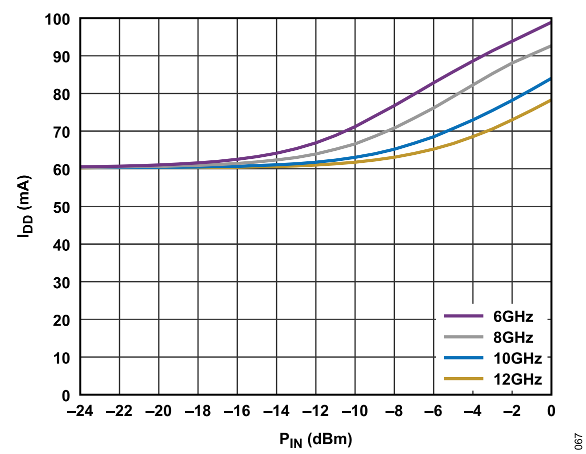


Figure 67. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 3 V, and R_{BIAS} = 470 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

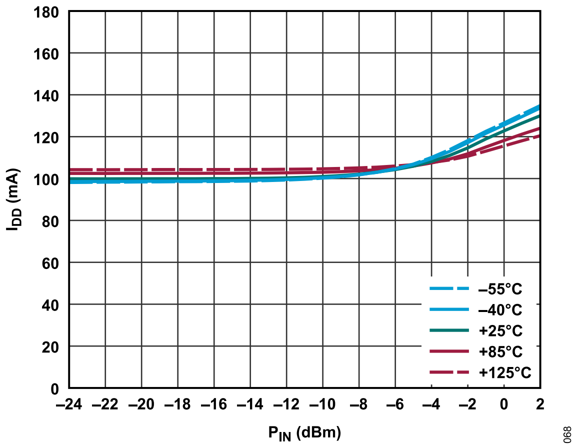


Figure 68. I_{DD} vs. P_{IN} for Various Temperatures at 10 GHz, V_{DD} = 5 V, and R_{BIAS} = 698 Ω

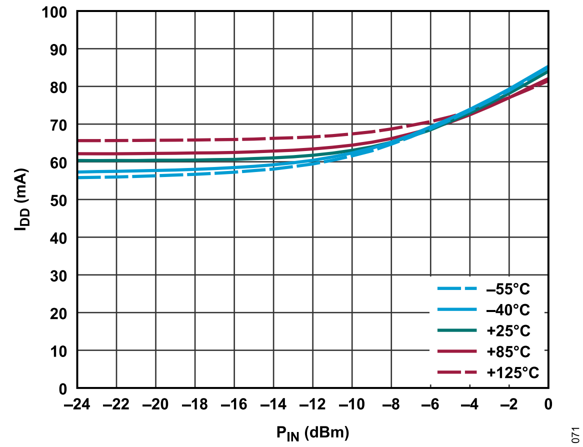


Figure 71. I_{DD} vs. P_{IN} for Various Temperatures at 10 GHz, V_{DD} = 3 V, and R_{BIAS} = 470 Ω

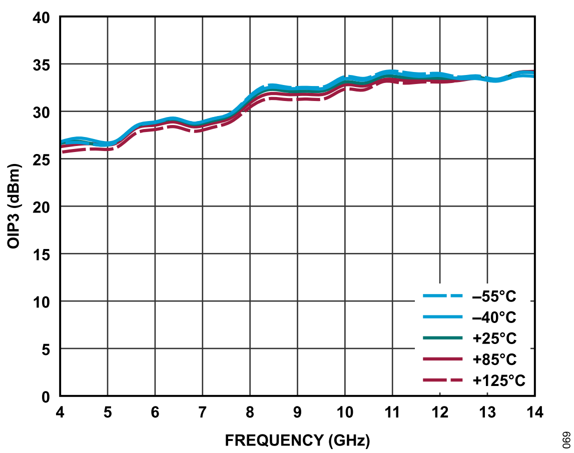


Figure 69. OIP3 vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, R_{BIAS} = 698 Ω, and P_{OUT} per Tone = 6 dBm

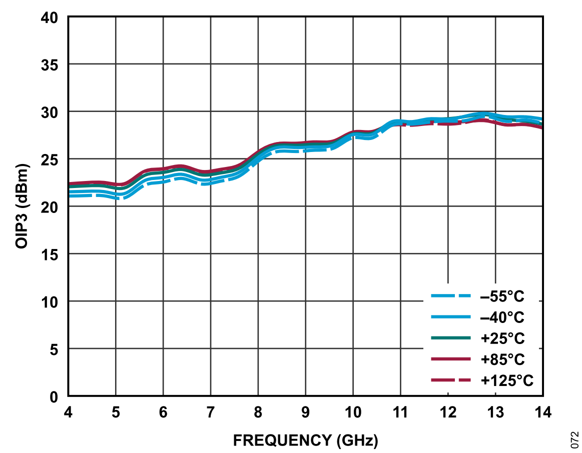


Figure 72. OIP3 vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 470 Ω, and P_{OUT} per Tone = 2 dBm

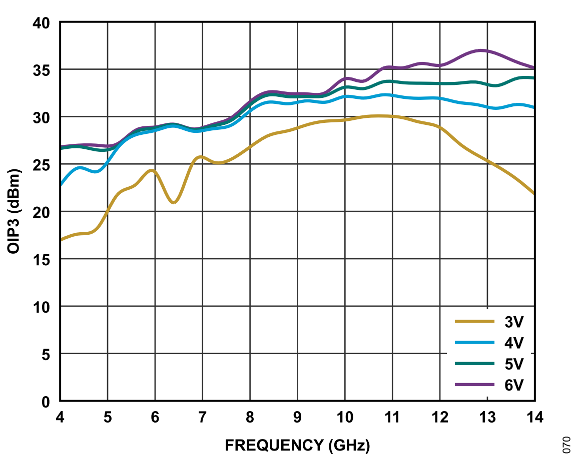


Figure 70. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 100 mA, and P_{OUT} per Tone = 6 dBm

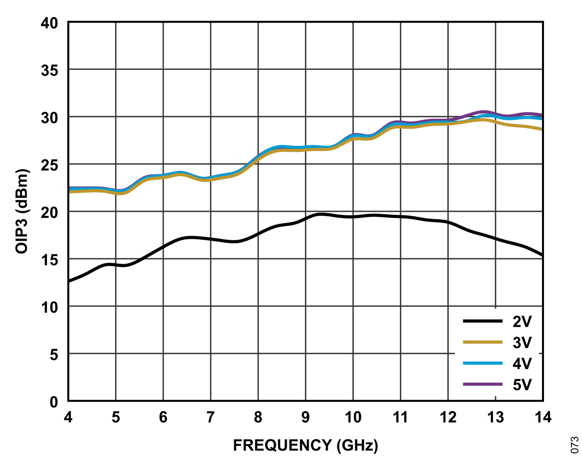


Figure 73. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA, and P_{OUT} per Tone = 2 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

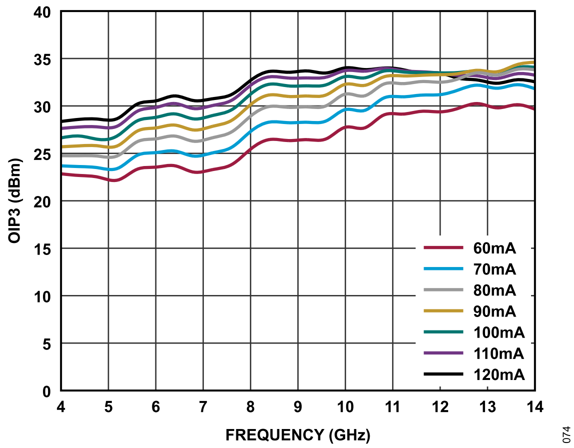


Figure 74. OIP3 vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V, and P_{OUT} per Tone = 6 dBm

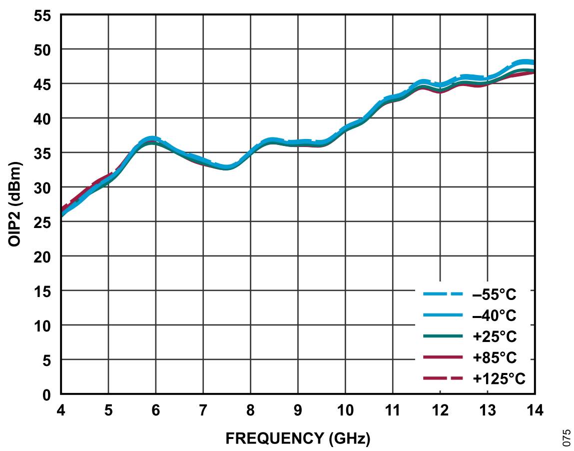


Figure 75. OIP2 vs. Frequency for Various Temperatures, 4 GHz to 14 GHz, V_{DD} = 5 V, I_{DQ} = 100 mA, R_{BIAS} = 698 Ω, and P_{OUT} per Tone = 6 dBm

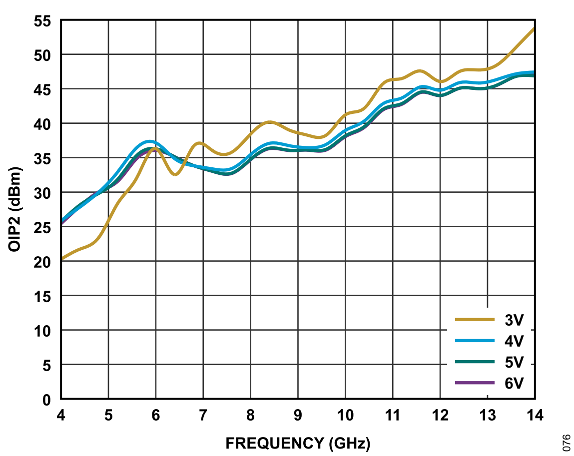


Figure 76. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 100 mA, and P_{OUT} per Tone = 6 dBm

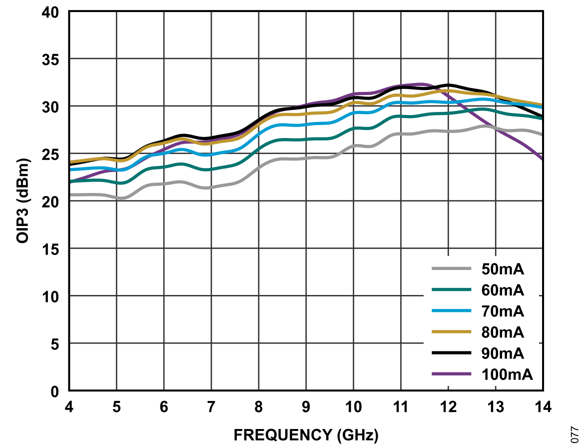


Figure 77. OIP3 vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V, and P_{OUT} per Tone = 2 dBm

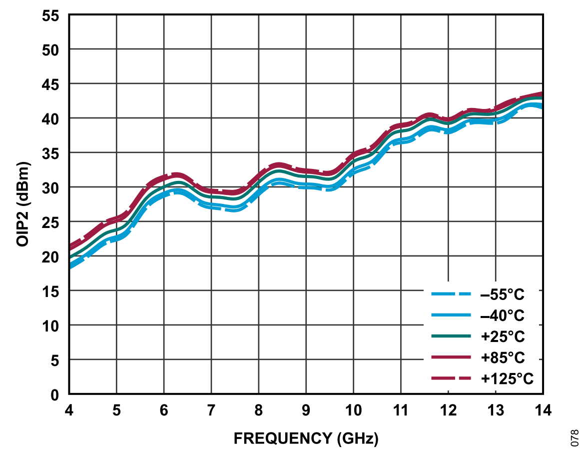


Figure 78. OIP2 vs. Frequency for Various Temperature, 4 GHz to 14 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 470 Ω, and P_{OUT} per Tone = 2 dBm

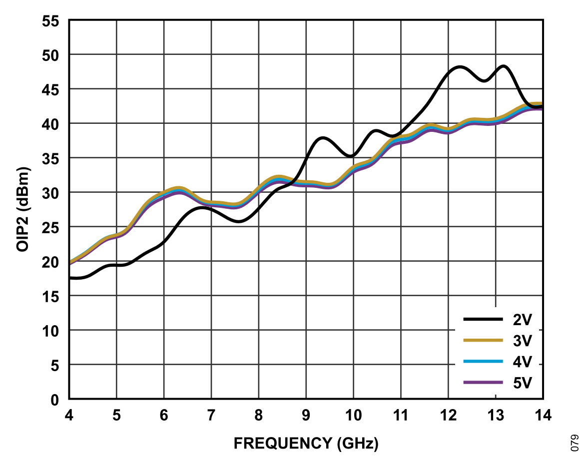


Figure 79. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA, and P_{OUT} per Tone = 2 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

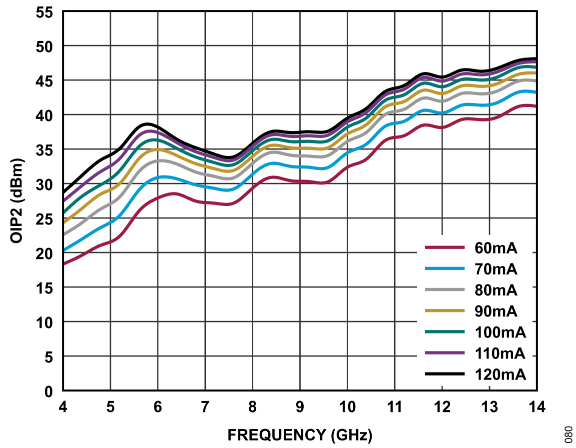


Figure 80. OIP2 vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V, and P_{OUT} per Tone = 6 dBm

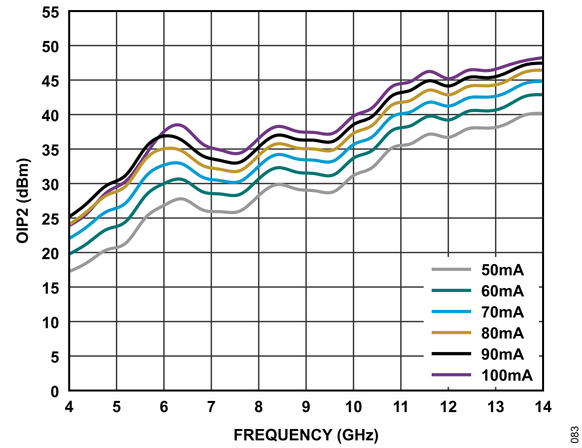


Figure 83. OIP2 vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V, and P_{OUT} per Tone = 2 dBm

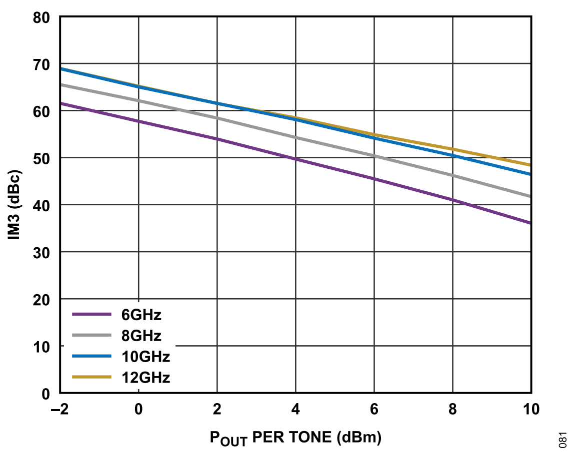


Figure 81. Output IM3 vs. P_{OUT} per Tone for Various Frequencies,V_{DD} = 5 V, and R_{BIAS} = 698 Ω

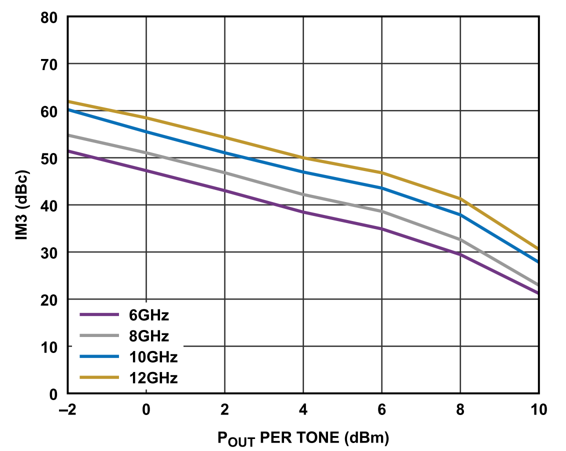


Figure 84. Output IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, and R_{BIAS} = 470 Ω

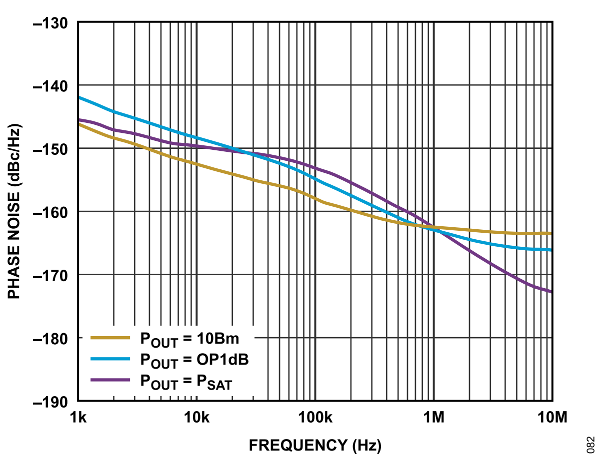


Figure 82. Phase Noise vs. Frequency at 10 GHz for Various P_{OUT} Values, V_{DD} = 5V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

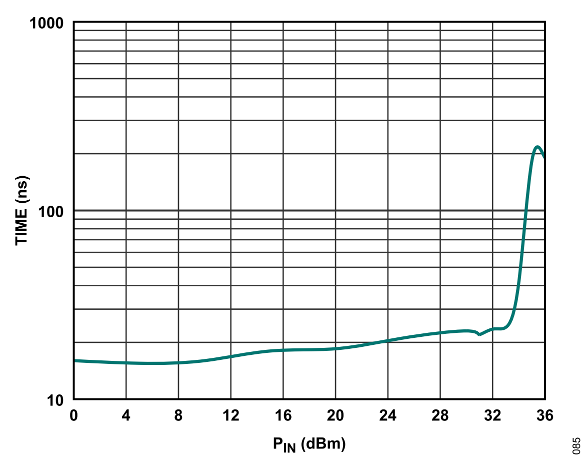


Figure 85. Overdrive Recovery Time vs. Pin at 10.2 GHz, Recovery to Within 90% of Small Signal Gain Value, V_{DD} = 5 V, I_{DQ} = 100 mA, and R_{BIAS} = 698 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

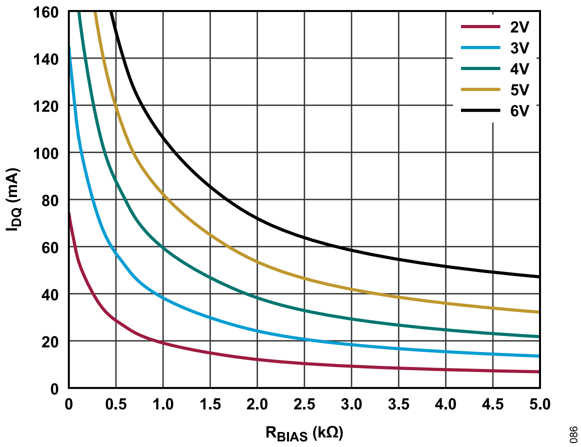


Figure 86. I_{DQ} vs. Bias Resistor Value for Various Supply Voltages, 0 Ω to 5 kΩ

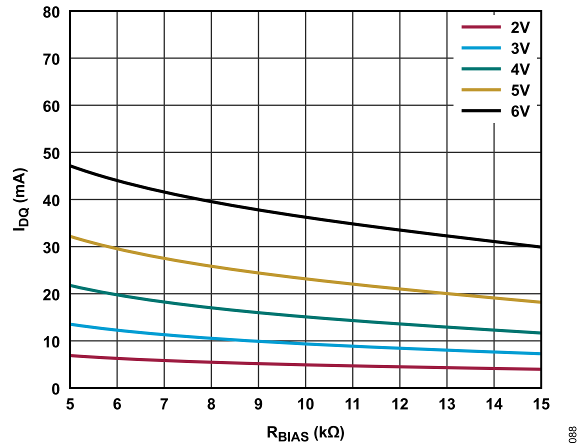


Figure 88. I_{DQ} vs. Bias Resistor Value for Various Supply Voltages, 5 kΩ to 15 kΩ

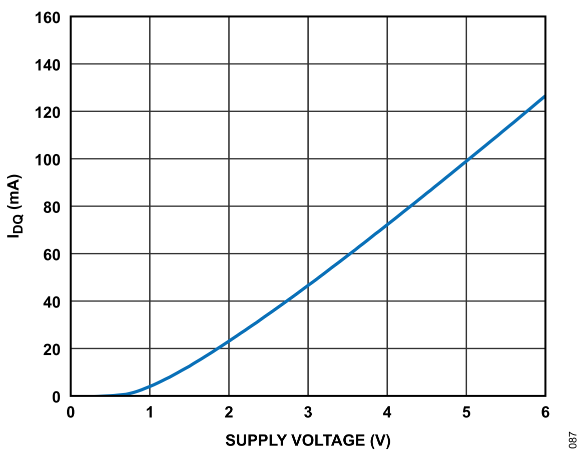


Figure 87. I_{DQ} vs. Supply Voltage, R_{BIAS} = 698 Ω

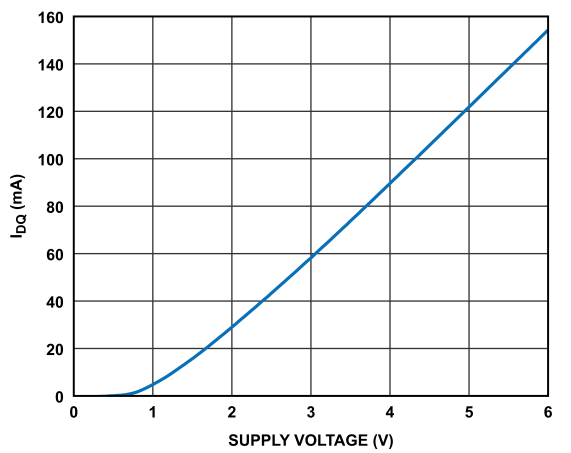


Figure 89. I_{DQ} vs. Supply Voltage, R_{BIAS} = 470 Ω

THEORY OF OPERATION

The ADL8103 is a wideband LNA with high RF input survivability that operates from 6 GHz to 12 GHz. A simplified block diagram is shown in Figure 90. Both the RFIN and RFOUT are internally AC-coupled and matched to 50 Ω. No external matching components are required. To adjust the I_{DQ}, connect a supply referenced external resistor to the RBIAS pin.

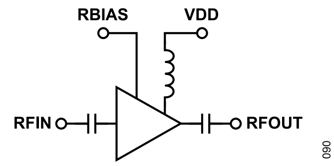


Figure 90. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8103 over the specified frequency range are shown in Figure 91. No external biasing inductor is required, allowing the 5 V supply to be connected to the VDD pin. It is recommended to use 0.1 µF and 100 pF power supply decoupling capacitors. The power supply decoupling capacitors shown in Figure 91 represent the configuration used to characterize and qualify the ADL8103.

To set I_{DQ}, connect a resistor (R2) between the RBIAS and VDD pins as shown in Figure 91. A default value of 698 Ω is recommended, which results in a nominal I_{DQ} of 100 mA. Table 9 shows how the I_{DQ} and I_{DQ_AMP} varies vs. the R_{BIAS}. The RBIAS pin also draws a current that varies with the value of R_{BIAS} (see Table 9). Do not leave the RBIAS pin open.

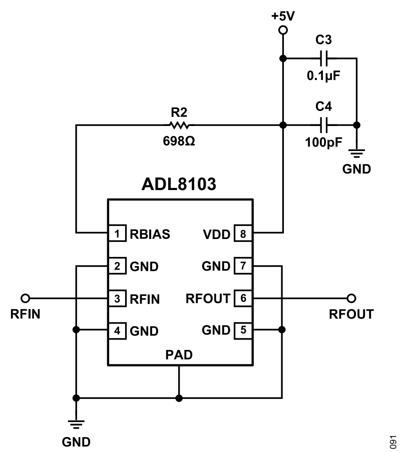


Figure 91. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

Correct sequencing of the DC and RF power is required to safely operate the ADL8103. During power up, apply VDD before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before VDD is powered off.

Table 9. Recommended Bias Resistor Values for V_{DD} = 5 V

R_{BIAS} (Ω)	Total Current, I_{DQ} (mA)	Amplifier Current, I_{DQ_AMP} (mA)	R_{BIAS} Current, I_{RBIAS} (mA)
1690	60	57.80	2.20
1300	70	67.24	2.76
1020	80	76.65	3.35
845	90	86.09	3.91
698	100	95.46	4.54
576	110	104.8	5.20
487	120	114.15	5.85

Table 10. Recommended Bias Resistor Values for V_{DD} = 3 V

R_{BIAS} (Ω)	Total Current, I_{DQ} (mA)	Amplifier Current, I_{DQ_AMP} (mA)	R_{BIAS} Current, I_{RBIAS} (mA)
649	50	47.52	2.48
470	60	56.87	3.13
348	70	66.22	3.72
255	80	75.54	4.46
191	90	84.83	5.17
140	100	94.18	5.82

Table 11. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 100 mA

R_{BIAS} (Ω)	V_{DD} (V)	Amplifier Current, I_{DQ_AMP} (mA)	R_{BIAS} Current, I_{RBIAS} (mA)
140	3	94.10	5.90
470	4	94.80	5.20
698	5	95.46	4.54
1100	6	96.6	3.90

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 92 shows a recommended power management circuit for the ADL8103. The LT8607 step-down regulator is used to step down a 12 V rail to 6.5 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. While the circuit shown in Figure 92 has an input voltage of 12 V, the input range to the LT8607 can be as high as 42 V.

The 6.54 V regulator output of the LT8607 is set by the R2 and R3 resistors according to the following equation:

$$R2 = R3((V_{OUT}/0.778\ \ V) - 1) \quad (1)$$

where V_{OUT} is the output voltage.

The switching frequency is set to 2 MHz by the 18.2 kΩ resistor on the RT pin. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.2 MHz.

The output voltage of the LT3042 is set by the R4 resistor connected to the SET pin according to the following equation:

$$V_{OUT} = 100\ \ \mu A \times R4 \quad (2)$$

The PGFB resistors are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5 V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature. Adding resistors results in a bit more (5%) tolerance, therefore putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 5 V output to give a convenient 0 V to 5 V voltage range. Table 12 provides the recommended resistor values for operation at 3 V to 5.5 V.

Table 12. Recommended Resistor Values for Operating at 3 V to 5.5 V

LDO Output Voltage (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
3	30.1	255	30.1
3.5	34.8	316	30.1
4	40.2	374	30.1
4.5	45.3	422	30.1
5	49.9	442	30.1
5.5	54.9	487	30.1

The LT8607 can source a maximum current of 750 mA, and the LT3042 can source a maximum current of 200 mA. If the 5 V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current to 1.5 A and 3 A, respectively, and these devices are pin compatible with the LT8607. The LT3045 linear regulator, which is pin compatible with the LT3042, can source a maximum current to 500 mA.

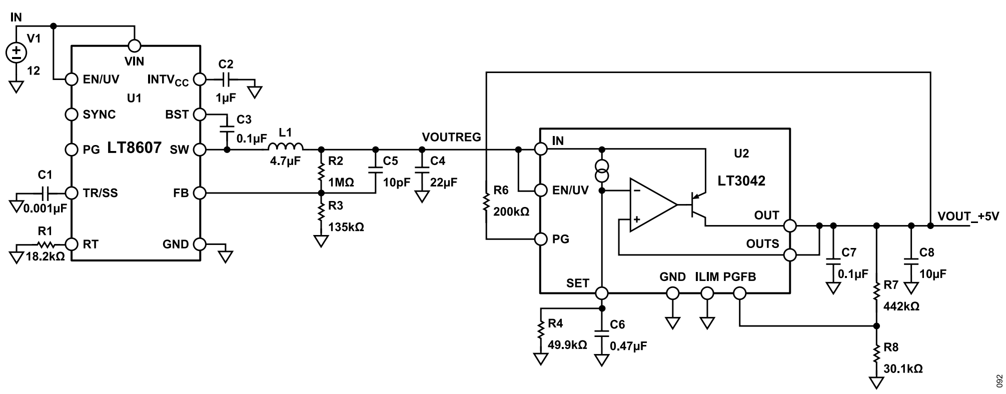


Figure 92. Recommended Power Management Circuit

USING THE RBIAS PIN TO ENABLE AND DISABLE ADL8103

By attaching a single-pole, double throw (SPDT) switch to the RBIAS pin, an enable and/or disable circuit can be implemented as shown in Figure 93. The ADG719 CMOS switch is used to connect the RBIAS resistor either to supply or ground. When the RBIAS resistor is connected to ground, the overall current consumption reduces to 3.8 mA with no RF signal present and 3.8 mA when the RF input level is −10 dBm.

Figure 94 shows a plot of the turn on and/or turn off response time of the RF output envelope when the IN pin of the ADG719 is pulsed.

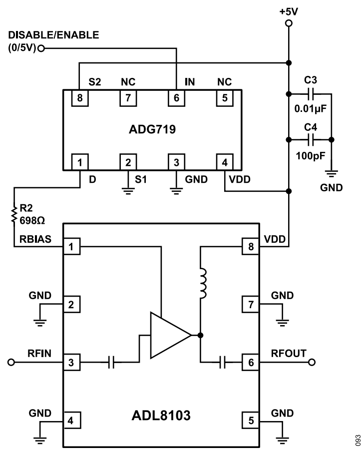


Figure 93. Fast Enable and/or Disable Circuit Using an SPDT

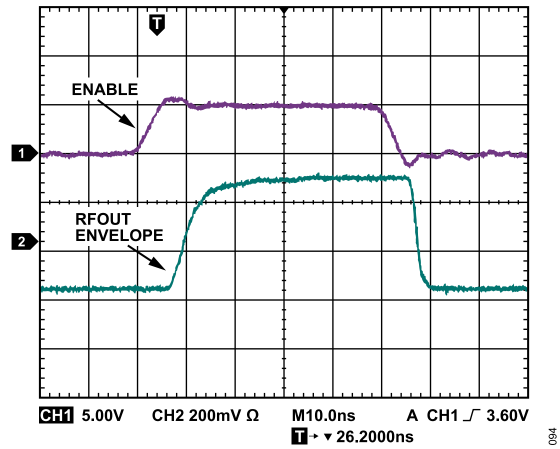


Figure 94. On and/or Off Response of the RF Output Envelope When the IN Pin of the ADG719 Is Pulsed

OUTLINE DIMENSIONS

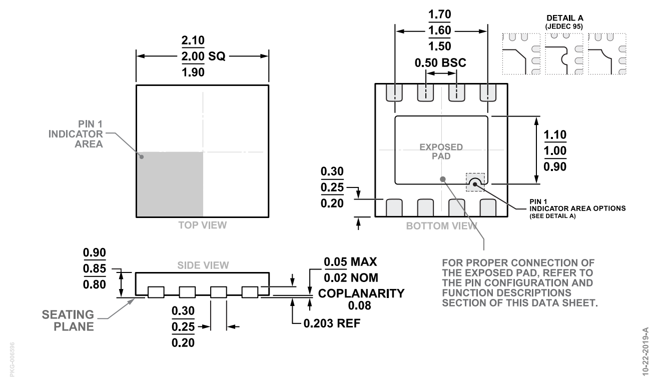


Figure 95. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8103ACPZN	−55°C to +125°C	8-lead LFCSP (2 mm x 2 mm x 0.85 mm)	Tape, 1	CP-8-30
ADL8103ACPZN-R7	−55°C to +125°C	8-lead LFCSP (2 mm x 2 mm x 0.85 mm)	Reel, 3000	CP-8-30

[1] Z = RoHS Compliant Part.

[2] The lead finish of the ADL8103ACPZN and ADL8103ACPZN-R7 is nickel palladium gold.

EVALUATION BOARDS

Model[1]	Description
ADL8103-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.