10 GHz to 18 GHz Low Noise Amplifier

FEATURES

- Self biased, single positive supply LNA
- Resistor-adjustable bias current
- Internally matched and AC-coupled
- Frequency range: 10 GHz to 18 GHz
- Noise figure: 1 dB from 12 GHz to 15 GHz
- Gain: 27.5 dB from 12 GHz to 15 GHz
- RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Satellite communications
- Radar
- Telecommunications

GENERAL DESCRIPTION

The ADL8140 is a low noise amplifier (LNA) that operates from 10 GHz to 18 GHz.

Typical gain and noise figure are 27.5 dB and 1 dB, respectively, from 12 GHz to 15 GHz. Output power for 1 dB compression (OP1dB) and output third-order intercept (OIP3), are 8 dBm and 23 dBm, respectively, from 12 GHz to 15 GHz. The nominal quiescent current (I_{DQ}), which can be adjusted, is 35 mA from a 1.5 V supply voltage (V_{DD}). The ADL8140 also features inputs/outputs that are AC-coupled and internally matched to 50 Ω.

The ADL8140 is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead lead frame chip scale package [LFCSP] and is specified for operation from −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

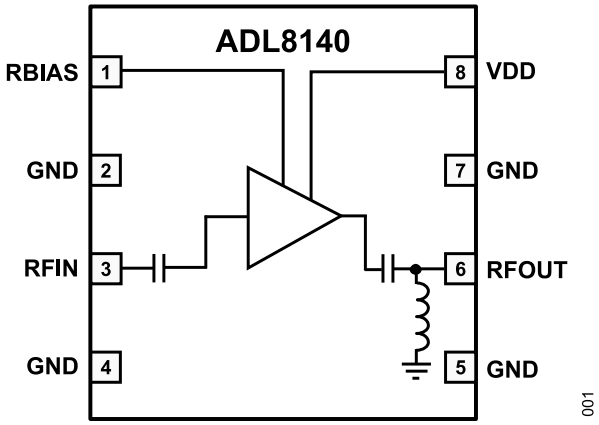

Figure 1. Functional Block Diagram

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REVISION HISTORY

7/2024—Revision 0: Initial Version

SPECIFICATIONS

10 GHZ TO 12 GHZ FREQUENCY RANGE

V_{DD} = 1.5 V, I_{DQ} = 35 mA, bias resistance (R_{BIAS}) = 562 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 10 GHz to 12 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	10		12	GHz	
GAIN	25	27		dB	
Gain Variation over Temperature		0.039		dB/°C	
NOISE FIGURE		0.95		dB	
RETURN LOSS					
Input (S11)		11		dB	
Output (S22)		12		dB	
OUTPUT					
OP1dB	4.5	6.5		dBm	
Saturated Output Power (P_{SAT})		8		dBm	
OIP3		18		dBm	Measurement taken at output power (P_{OUT}) per tone = −6 dBm
Second-Order Intercept (OIP2)		14		dBm	Measurement taken at P_{OUT} per tone = −6 dBm
POWER ADDED EFFICIENCY (PAE)		10		%	Measured at P_{SAT}

12 GHZ TO 15 GHZ FREQUENCY RANGE

V_{DD} = 1.5 V, I_{DQ} = 35 mA, R_{BIAS} = 562 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 12 GHz to 15 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	12		15	GHz	
GAIN	25.5	27.5		dB	
Gain Variation over Temperature		0.034		dB/°C	
NOISE FIGURE		1		dB	
RETURN LOSS					
S11		14		dB	
S22		14		dB	
OUTPUT					
OP1dB	6	8		dBm	
P_{SAT}		9.5		dBm	
OIP3		23		dBm	Measurement taken at P_{OUT} per tone = −6 dBm
OIP2		22		dBm	Measurement taken at P_{OUT} per tone = −6 dBm
PAE		14.3		%	Measured at P_{SAT}

SPECIFICATIONS

15 GHZ TO 18 GHZ FREQUENCY RANGE

V_{DD} = 1.5 V, I_{DQ} = 35 mA, R_{BIAS} = 562 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 15 GHz to 18 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	15		18	GHz	
GAIN	26	28		dB	
Gain Variation over Temperature		0.041		dB/°C	
NOISE FIGURE		1.1		dB	
RETURN LOSS					
S11		13		dB	
S22		10		dB	
OUTPUT					
OP1dB	6.5	8.5		dBm	
P_{SAT}		10.5		dBm	
OIP3		21.5		dBm	Measurement taken at P_{OUT} per tone = −6 dBm
OIP2		27		dBm	Measurement taken at P_{OUT} per tone = −6 dBm
PAE		17.2		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 4. DC Specifications

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		35		mA
Amplifier Current (I_{DQ_AMP})		33.3		mA
R_{BIAS} Current ($I_{R_{BIAS}}$)		1.7		mA
SUPPLY VOLTAGE				
V_{DD}	1.2	1.5	3.5	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	4 V
RF Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), and T_{CASE} = 85°C (Derate 12.09 mW/°C Above 85°C)	1.09 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and Input Power (P_{IN}) = Off)	89.34°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance.

Table 6. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	68.4	°C/W
Worst Case[2], T_{CASE} = 85°C	82.7	°C/W

[1] Thermal resistance varies with operating conditions.

[2] Across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8140

Table 7. ADL8140, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±300	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

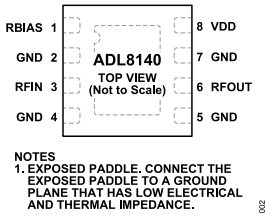

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the I_{DQ}. See Figure 50, Table 9, and Table 10 for more details. See Figure 3 for the interface schematic.
2, 4, 5, 7	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 6 for the interface schematic.
3	RFIN	RF Input. The RFIN pin is AC-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
6	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
8	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 5 for the interface schematic
	GROUND PADDLE	Ground Paddle. Connect the exposed ground paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

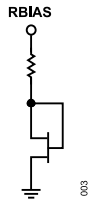

Figure 3. RBIAS Interface Schematic

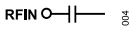

Figure 4. RFIN Interface Schematic

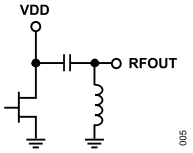

Figure 5. RFOUT/VDD Interface Schematic

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

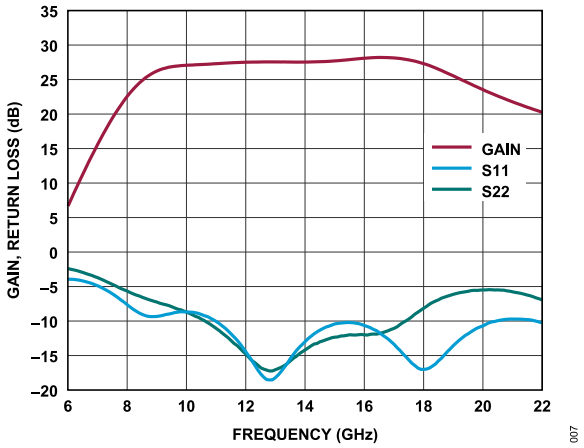

Figure 7. Gain and Return Loss vs. Frequency, 6 GHz to 22 GHz, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

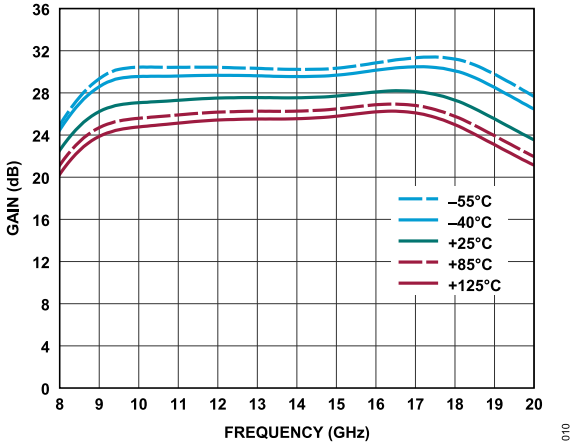

Figure 10. Gain vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

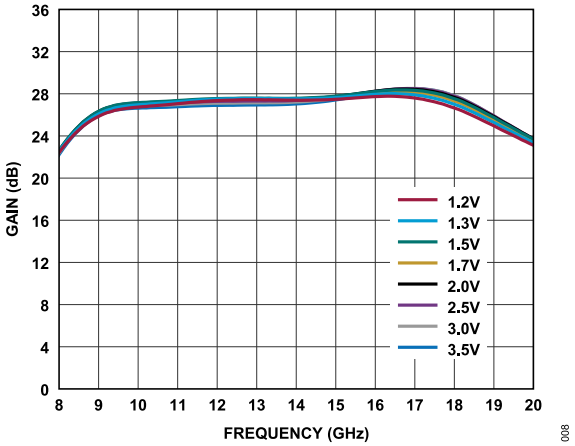

Figure 8. Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

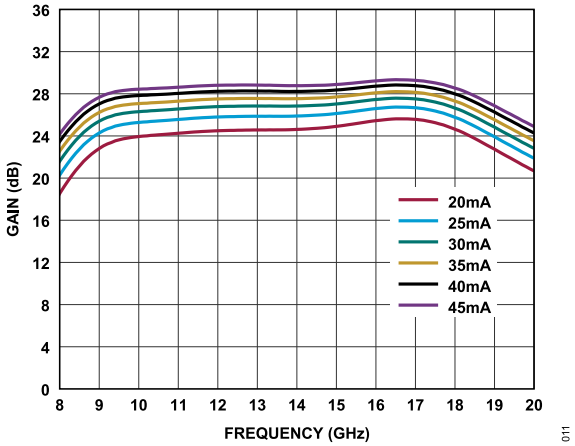

Figure 11. Gain vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

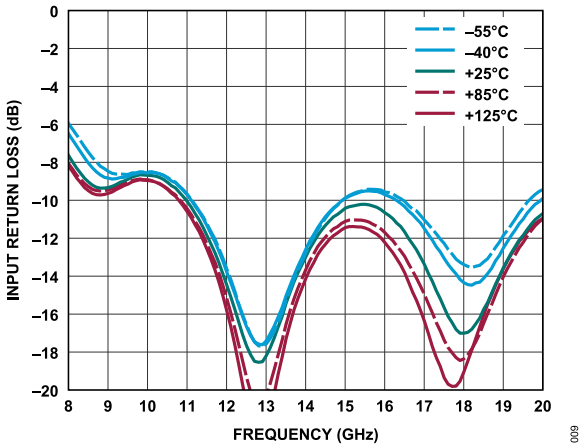

Figure 9. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 1.5 V , I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

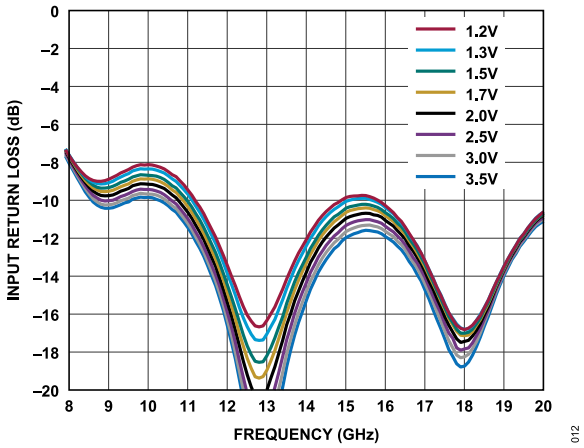

Figure 12. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

TYPICAL PERFORMANCE CHARACTERISTICS

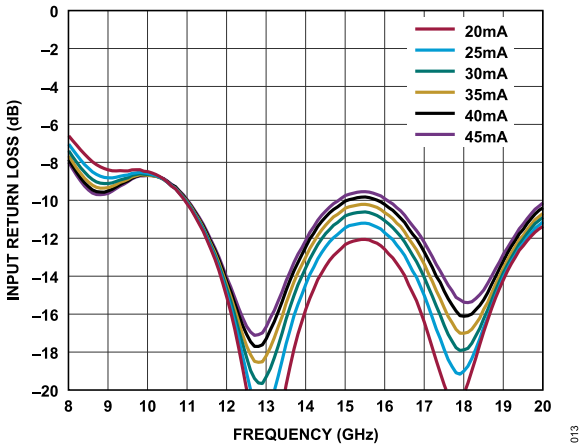

Figure 13. Input Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

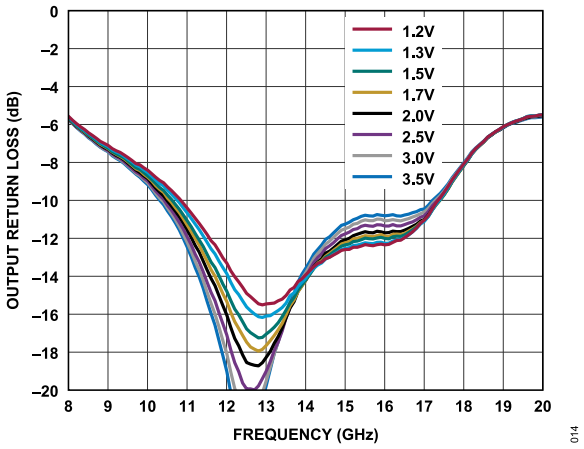

Figure 14. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

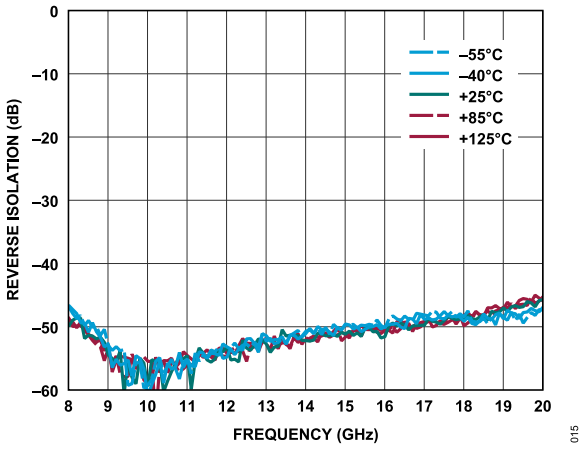

Figure 15. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

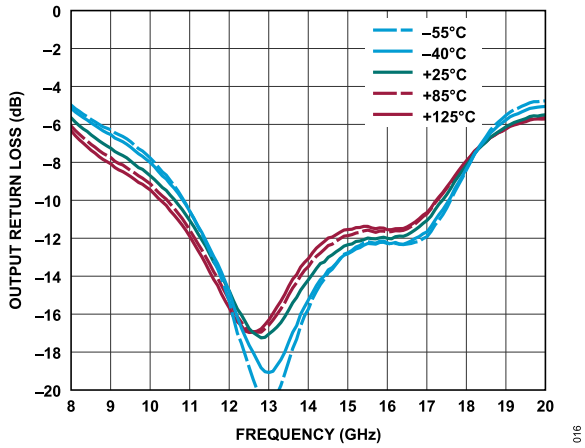

Figure 16. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

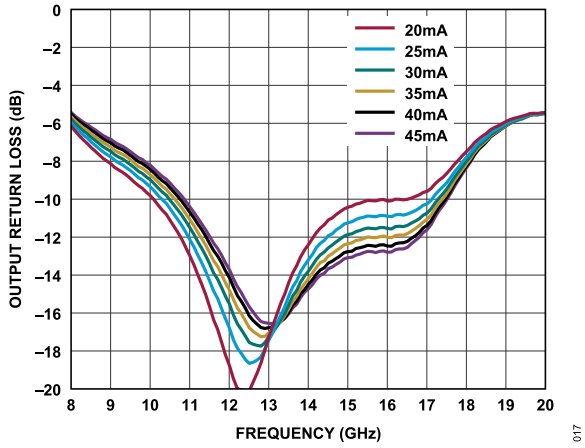

Figure 17. Output Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

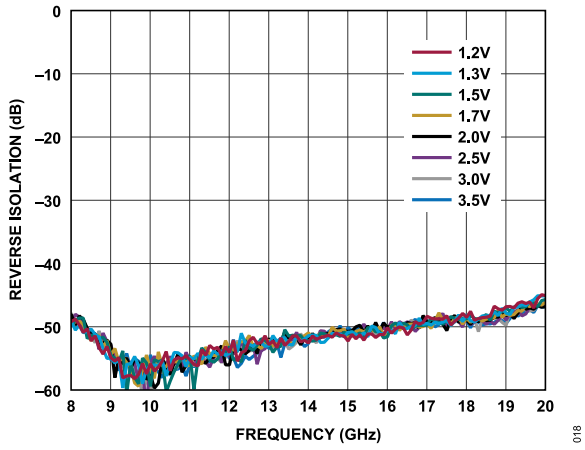

Figure 18. Reverse Isolation vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

TYPICAL PERFORMANCE CHARACTERISTICS

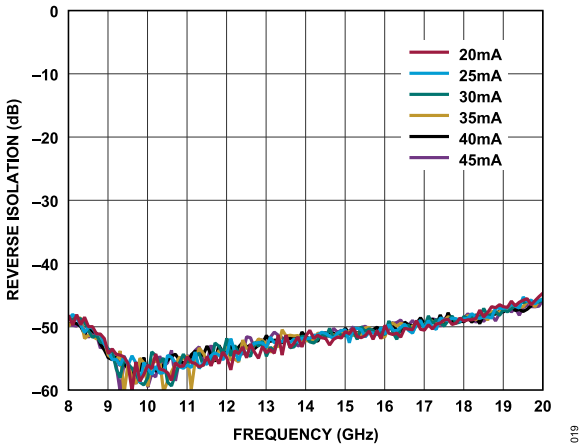

Figure 19. Reverse Isolation vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

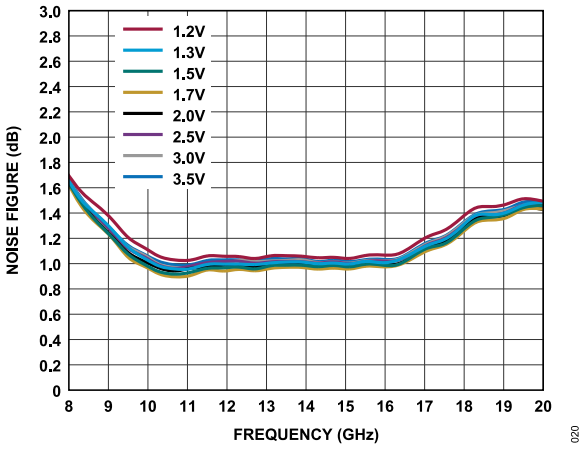

Figure 20. Noise Figure vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

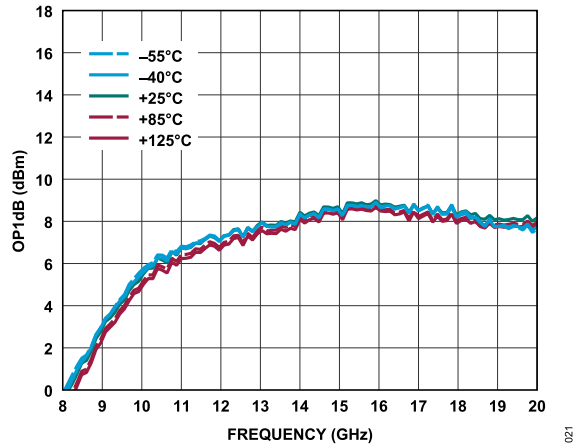

Figure 21. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

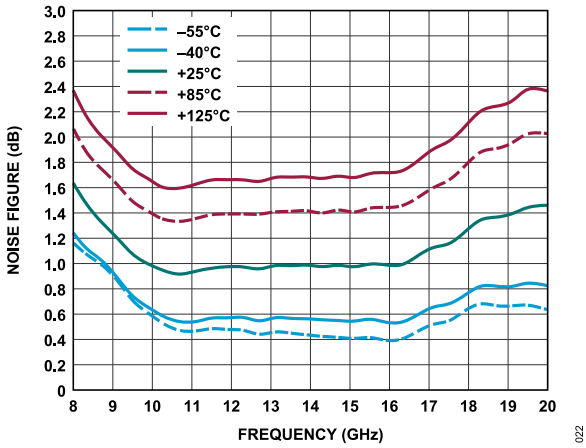

Figure 22. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

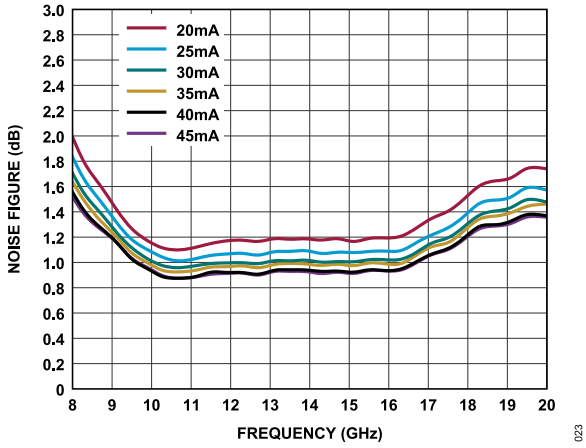

Figure 23. Noise Figure vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

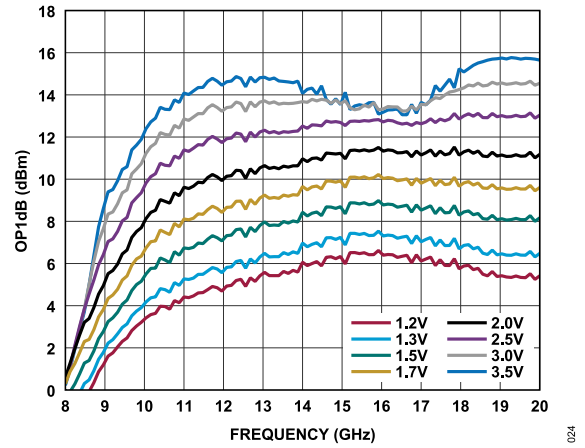

Figure 24. OP1dB vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

TYPICAL PERFORMANCE CHARACTERISTICS

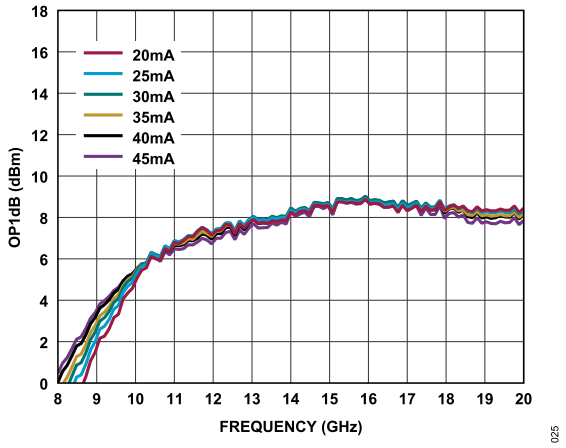

Figure 25. OP1dB vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

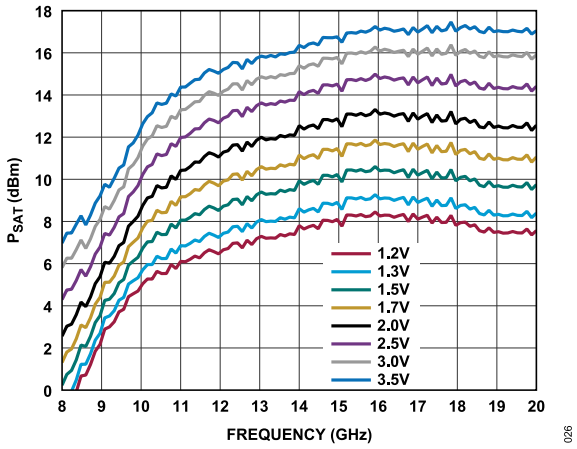

Figure 26. P_{SAT} vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

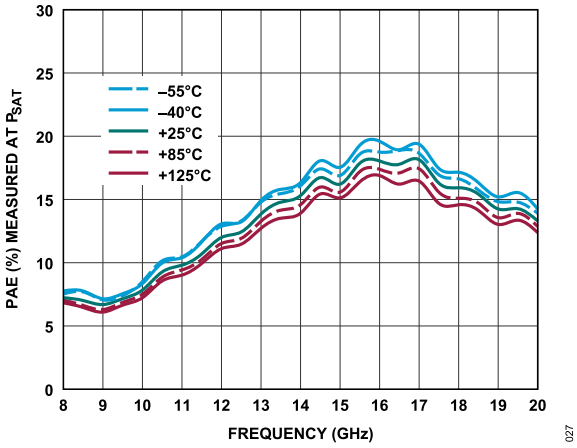

Figure 27. PAE measured at P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

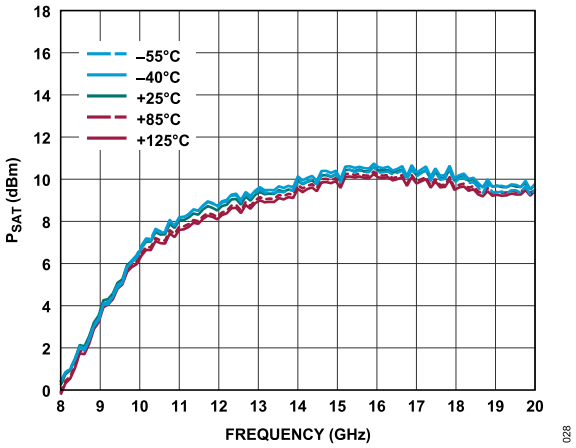

Figure 28. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

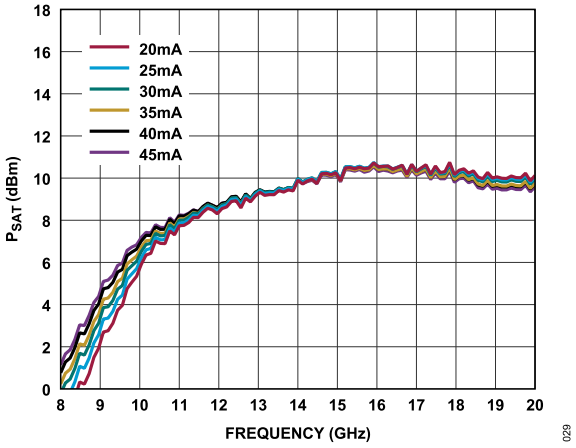

Figure 29. P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

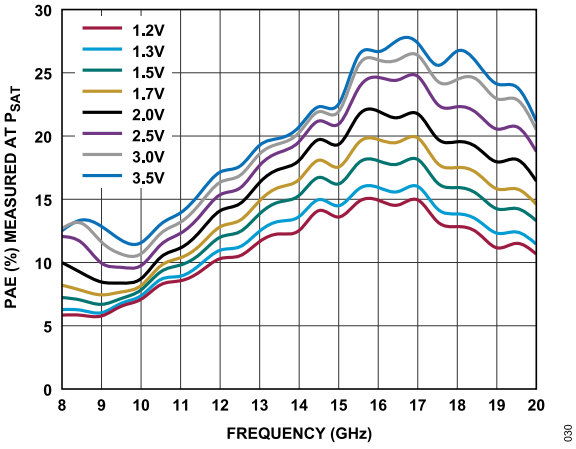

Figure 30. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

TYPICAL PERFORMANCE CHARACTERISTICS

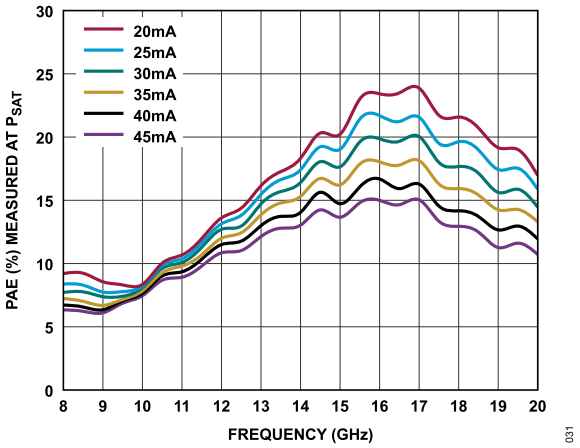

Figure 31. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

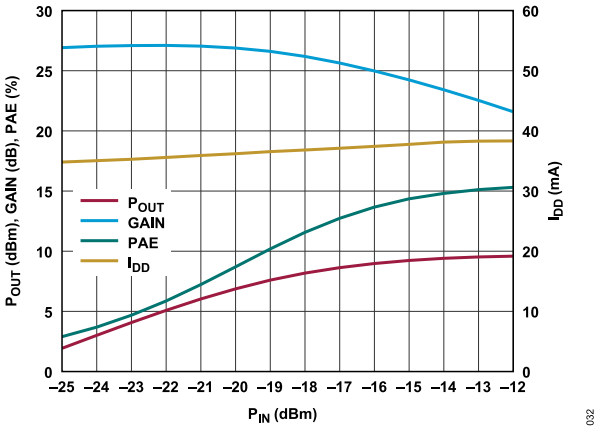

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 14 GHz, V_{DD} = 1.5 V, and R_{BIAS} = 562 Ω

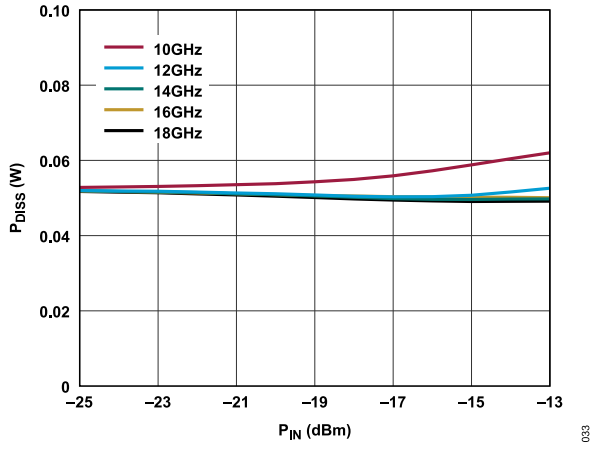

Figure 33. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, V_{DD} = 1.5 V

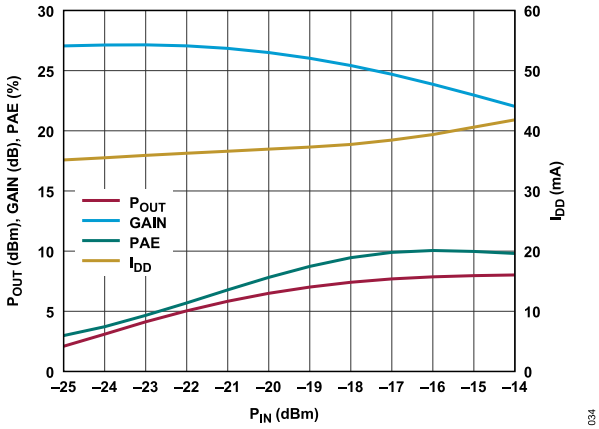

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 11 GHz, V_{DD} = 1.5 V, and R_{BIAS} = 562 Ω

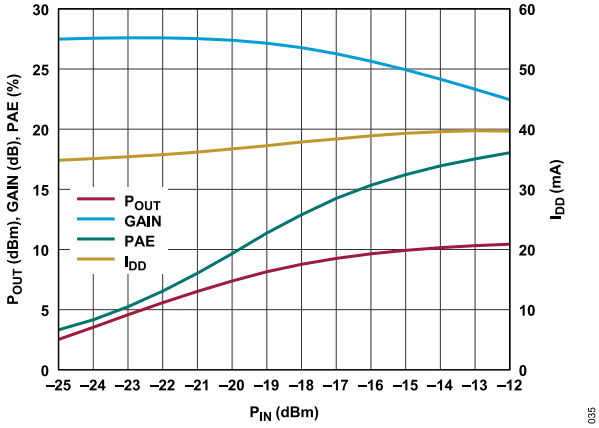

Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 16 GHz, V_{DD} = 1.5 V, and R_{BIAS} = 562 Ω

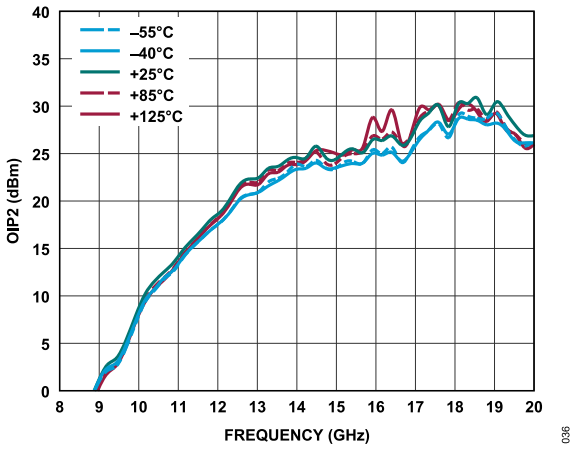

Figure 36. OIP2 vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

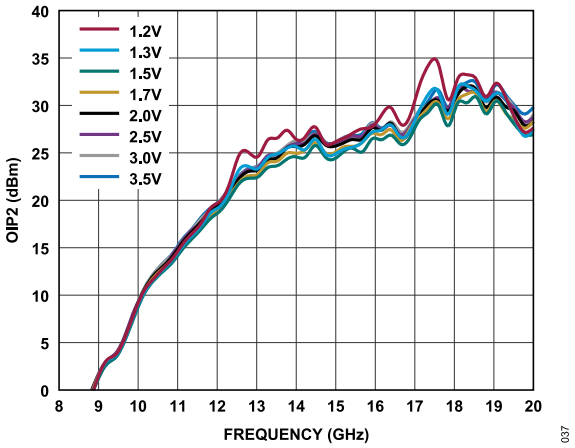

Figure 37. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

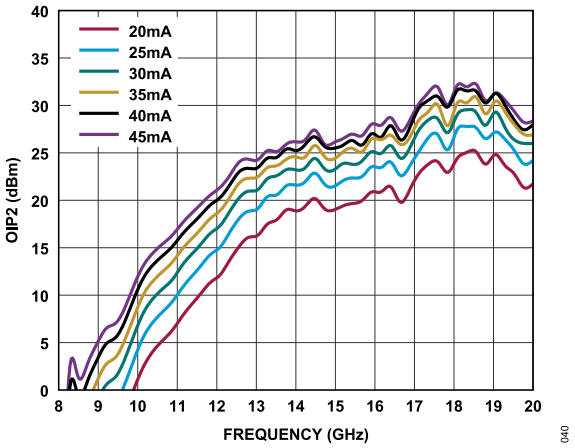

Figure 40. OIP2 vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

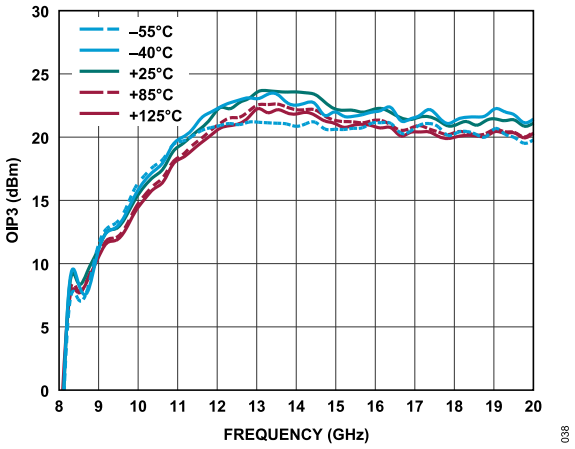

Figure 38. OIP3 vs. Frequency for Various Temperatures, V_{DD} = 1.5 V, I_{DQ} = 35 mA, and R_{BIAS} = 562 Ω

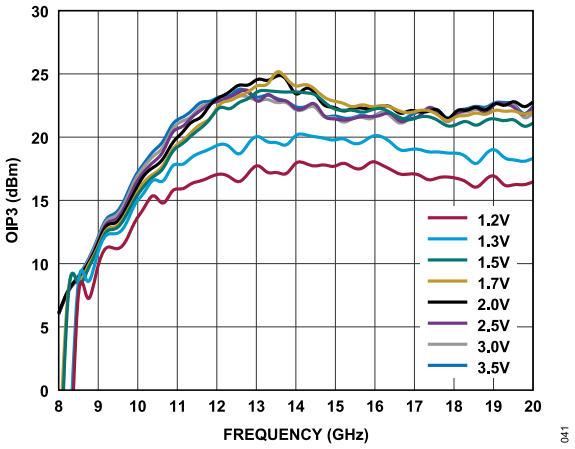

Figure 41. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 35 mA

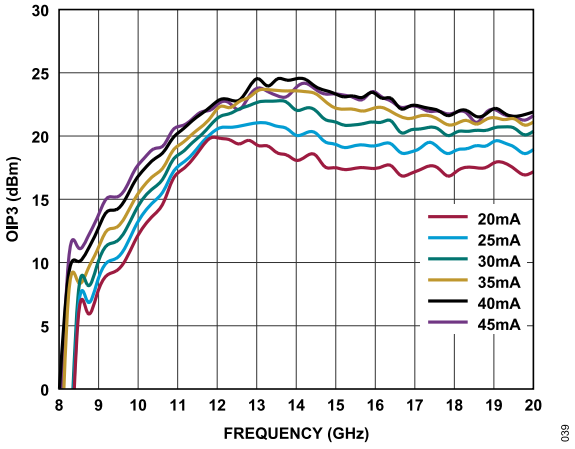

Figure 39. OIP3 vs. Frequency for Various I_{DQ}, V_{DD} = 1.5 V

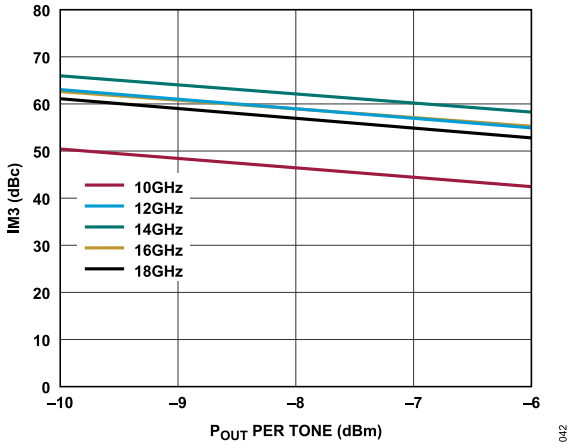

Figure 42. Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 1.5 V and R_{BIAS} = 562 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

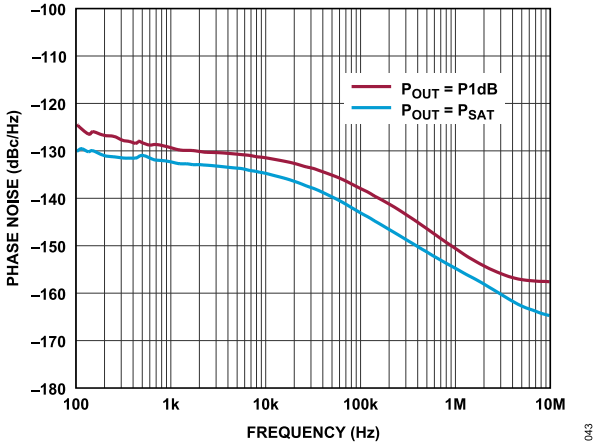

Figure 43. Phase Noise vs. Frequency at 12 GHz for Various P_{OUT} Values

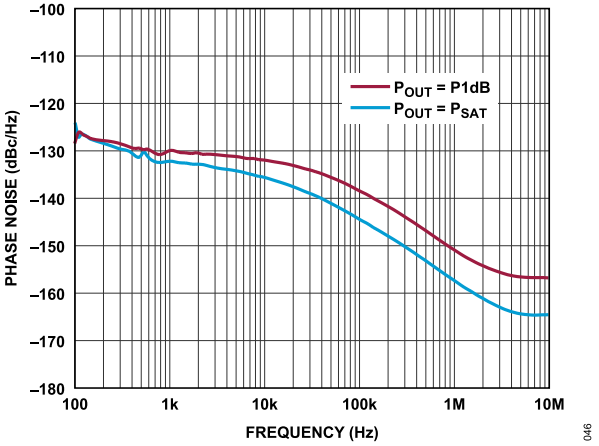

Figure 46. Phase Noise vs. Frequency at 16 GHz for Various P_{OUT} Values

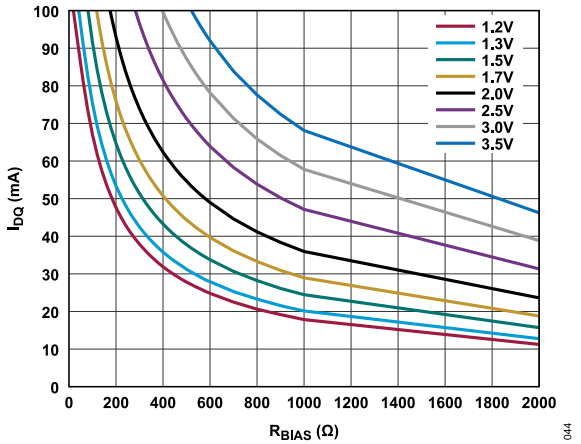

Figure 44. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0 Ω to 2 kΩ

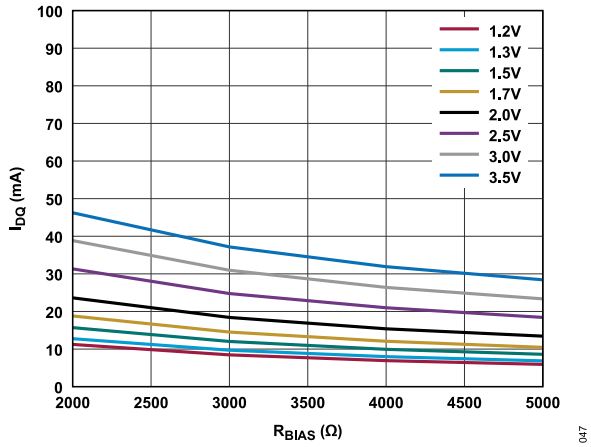

Figure 47. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 2 kΩ to 5 kΩ

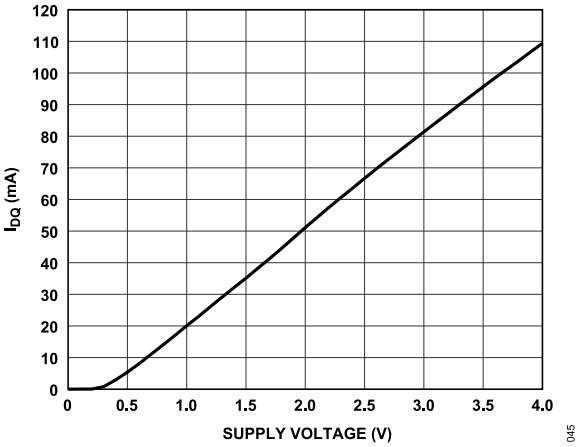

Figure 45. I_{DQ} vs. Supply Voltage, R_{BIAS} = 562 Ω

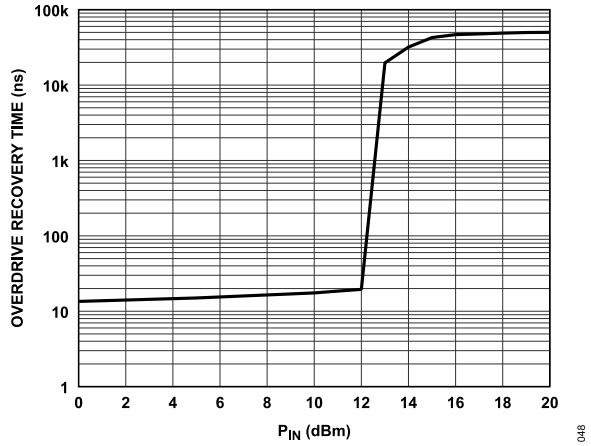

Figure 48. Overdrive Recovery Time vs. P_{IN} at 11 GHz, Recovery to Within 90% of Small Signal Gain Value, V_{DD} = 1.5 V, and R_{BIAS} = 562 Ω

THEORY OF OPERATION

The ADL8140 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), LNA with an integrated bias inductor and AC-coupling capacitors. A simplified schematic is shown in Figure 49.

To set the drain bias current, connect an external resistor between the RBIAS and VDD pins.

The ADL8140 has AC-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 10 GHz to 18 GHz frequency range. No external matching components are required. While the RF output path is AC-coupled, there is a DC path to ground on the RFOUT side of the AC-coupling capacitor.

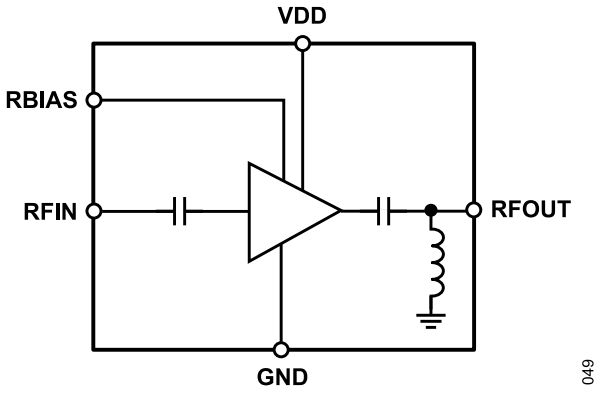

Figure 49. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8140 over the specified frequency range are shown in Figure 50. No external biasing inductor is required, allowing the 1.5 V supply to be connected to the VDD pin. It is recommended to use 0.1 µF and 100 pF power supply decoupling capacitors. The power supply decoupling capacitors shown in Figure 50 represent the configuration used to characterize and qualify the ADL8140.

To set the I_{DQ}, connect a resistor, R2, between the RBIAS and VDD pins. A default value of 562 Ω is recommended, which results in a nominal I_{DQ} of 35 mA. The RBIAS pin also draws a current that varies with the value of R_{BIAS}, and this current is typically a few mA. Do not leave the RBIAS pin open.

The RFIN and RFOUT pins are internally AC-coupled. If the RFOUT pin is connected to a DC bias level other than 0 V, AC-couple the RFOUT pin because of the internal DC path to ground on RFOUT.

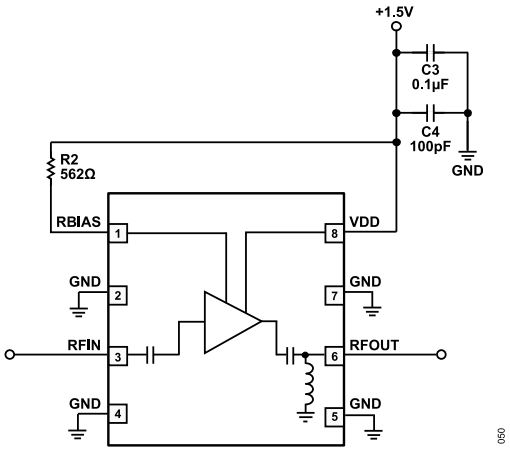

Figure 50. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

RF input power should be applied after V_{DD} has turned on and should be removed before V_{DD} is turned off.

Table 9. Recommended Bias Resistor Values for Various I_{DQ} Values, V_{DD} = 1.5 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
1347	20	19.25	0.75
948	25	24	1
709	30	28.6	1.4
562	35	33.3	1.7
445	40	38	2
366	45	42.6	2.4

Table 10. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 35 mA

R_{BIAS} (Ω)	V_{DD} (V)
335	1.2
404	1.3
562	1.5
722	1.7
1024	2.0
1630	2.5
2370	3.0
3301	3.5

USING RBIAS AS A FAST ENABLE AND DISABLE FUNCTION

The RBIAS pin can be used as a fast enable and disable control input. In Figure 51, a single-pole, double throw (SPDT) switch is used to switch the voltage on the RBIAS resistor between 0 V and 2 V. When the voltage on the RBIAS pin is equal to 0 V, I_{DQ} reduces to less than 1 mA with P_{OUT} at 0 dBm. The response time of the ADL8140's output envelope is shown in Figure 52. The ringing on the response trace is caused by interconnecting wires between the ADG719 and ADL8140 circuit boards used in the measurement. Note that because ADG719 has a minimum supply voltage of 1.8 V, the supply voltage for ADG719 and ADL8140 is set to 2 V.

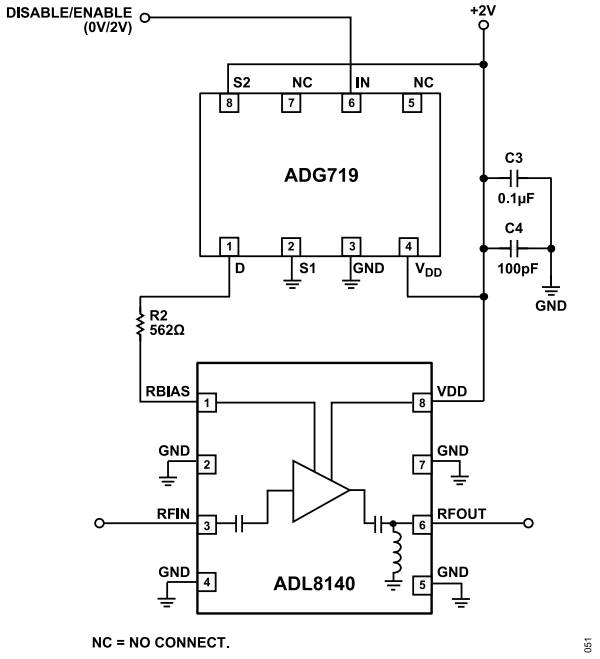

Figure 51. Fast Enable and Disable Using a 0 V to 2.0 V Pulse on the RBIAS Resistor

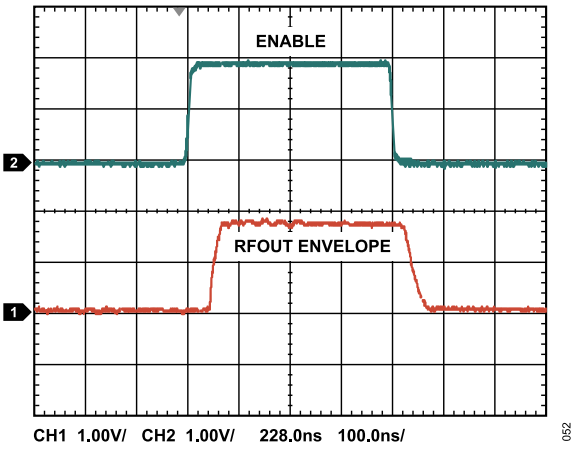

Figure 52. On and Off Response of the ADL8140 RF Output Envelope When the IN Pin of the ADG719 Is Pulsed, P_{OUT} = 5 dBm at 12 GHz

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 53 shows a recommended power management circuit that uses the LT3083 low dropout (LDO) regulator. The LT3083 output load current is supplied to the IN pin of the LT3083. Power for the on-board control circuitry is applied to the $V_{CONTROL}$ pin of the LT3083. A voltage that is at least 1.4 V higher than the output voltage must be applied to the $V_{CONTROL}$ pin. In Figure 53, $V_{CONTROL}$ has been set to 5 V but could be set as low as 2.9 V for a 1.5 V output voltage. The current into the CONTROL pin is typically 1.7 % of the total output current.

The LT3083 can provide up to 3 A of load current. Assuming that the ADL8140 is being used in a phased array application, a single LT3083 can easily provide bus power for all of the ADL8140 devices in a 64-element array. A dropout voltage of 500 mV is assumed based on a load current of 3 A. If the required load current is lower, the voltage on the IN pin of LT3083 can be reduced to improve efficiency. For example, for a load current of 1 A, the dropout voltage drops to a worst case value of 160 mV.

For applications that require a lower dropout voltage, LT3033 can be used. For a 3 A load, the worst case dropout voltage for the LT3033 is 240 mV

Table 11 provides recommended resistor values to set the other output voltages. In each case, the minimum input voltage (V_{IN}) voltage is specified based on a 3 A load and a 500 mV dropout voltage.

Table 11. Recommended Resistor Values for the Various LDO Output Voltages

LDO V_{OUT} (V)	R2 (kΩ)	Minimum V_{DD} (V)
1.2	24.3	1.7
1.5	30.1	2.0
2.0	40.2	2.5
2.5	49.9	3.0
3.0	60.4	3.5
3.3	66.5	3.8
3.5	69.8	4.0

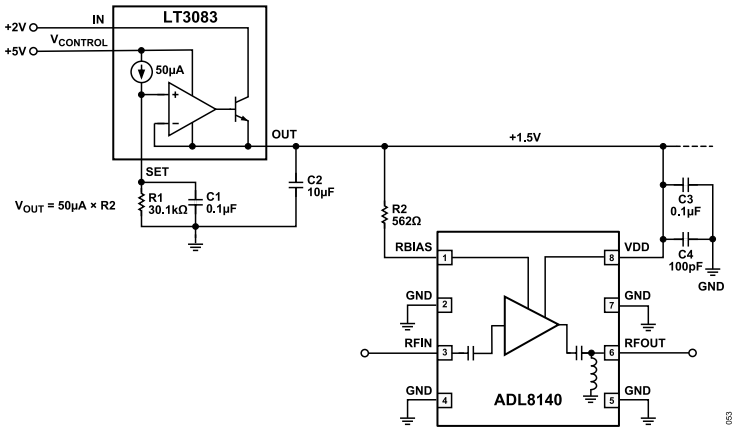

Figure 53. Recommended Power Management Circuit

OUTLINE DIMENSIONS

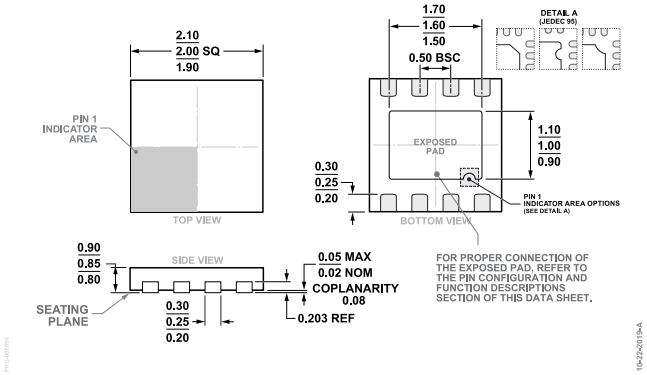

Figure 54. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8140ACPZN	−55°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	Tape, 1	CP-8-30
ADL8140ACPZN-R7	−55°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 3000	CP-8-30

[1] Z = RoHS Compliant Part.

[2] The lead finish of the ADL8140ACPZN and ADL8140APCZN-R7 is nickel palladium gold.

EVALUATION BOARDS

Model[1]	Description
ADL8140-EVALZ	ADL8140 Evaluation Board

[1] Z = RoHS Compliant Part.

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