



# SKY66318-21: 3300 to 3700 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier

## Applications

- 5G NR and 4G LTE systems
- Supports 3GPP and 5G Bands 22, 42, n77, and n78
- Driver amplifier for micro and macro base stations
- Enterprise small cell and massive MIMO

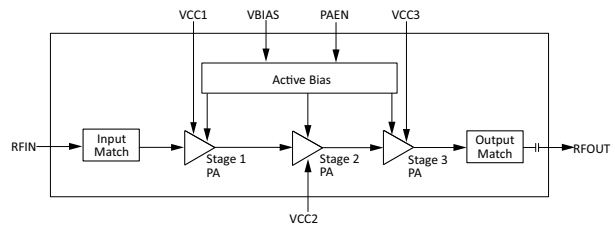
## Features

- Wide instantaneous signal bandwidth: 200 MHz
- High efficiency: PAE = 22% @ +27.5 dBm
- High linearity: +27.5 dBm with -48 dBc ACLR with linearization (200 MHz 5G, 8.5 dB PAR signal)
- High gain: 36.5 dB
- Excellent input and output return loss in 50 Ω systems
- Integrated active bias: performance compensated over temperature
- Integrated enable on/off function: PAEN = 1.7 to 2.5 V
- Single supply voltage: 5.0 V
- Pin-to-pin compatible PA family supporting major 3GPP bands
- Compact (16-pin, 5 x 5 x 1.26 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

## Description

The SKY66318-21 is a highly efficient, wide instantaneous bandwidth, fully input/output matched power amplifier (PA) with high gain and linearity. The compact 5 × 5 mm PA is designed for 5G NR and 4G LTE systems operating from 3300 to 3700 MHz.

The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation.



**Figure 1. Block Diagram**

The SKY66318-21 is part of a high-efficiency, pin-to-pin compatible PA family supporting major 3GPP bands.

A block diagram is shown in Figure 1. The device package pinout is shown in Figure 2. Table 1 lists the pin-to-pin compatible parts in the PA family.

Signal pin assignments and functional pin descriptions are described in Table 2.

**Table 1. Pin-to-Pin Compatible PA Family**

Part Number	Frequency (MHz)	Band
SKY66312-11	2300 to 2400	Bands 30, 40
SKY66317-11	2496 to 2690	Bands 7, 38, 41
SKY66318-21	3400 to 3600	Bands 22, 42, n77, n78
SKY66313-11	3300 to 3600	Bands 22, 42
SKY66315-11	4400 to 5000	Band n79
SKY66319-11	4800 to 5000	Band n79 for China

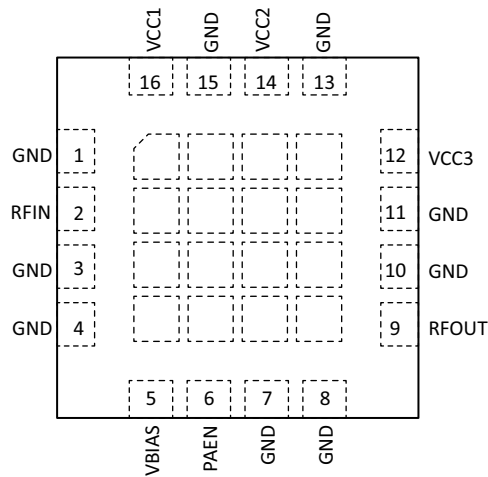


Figure 2. Pinout (Top View)

Table 2. Signal Descriptions<sup>1</sup>

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	PAEN	PA enable	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

1. The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

## Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included within the device for both input and temperature and voltage variations.

The SKY66318-21 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively). The DC control voltage that sets the bias is supplied by the VBIAS signal (pin 5).

## Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY66318-21 are provided in Table 3. Recommended operating conditions are specified in Table 4, and electrical specifications are provided in Table 5.

**Table 3. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Minimum	Maximum	Units
RF input power (CW)	Pin		+10	dBm
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	Vcc		5.5	V
PA enable	VEN		2.8	V
Operating temperature	Tc	-40	+110	°C
Storage temperature	Tst	-55	+125	°C
Junction temperature	Tj		+150	°C
Power dissipation (T <sub>CASE</sub> = 100 °C, P <sub>OUT</sub> = +27 dBm)	Pd		1.8	W
Device thermal resistance (T <sub>CASE</sub> = 100 °C, P <sub>OUT</sub> = +27 dBm)	θ <sub>JC</sub>		20.7	°C/W

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

*ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

**Table 4. Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	Vcc1, Vcc2, Vcc3, VBIAS	4.75	5	5.25	V
PA enable: ON OFF	PAEN	1.7	2.0 0	2.5 0.5	V
PA enable current	IENABLE		1	12	uA
Operating frequency	f	3300		3700	MHz
Operating temperature	Tc	-20	+25	+100	°C

**Table 5. Electrical Specifications<sup>1</sup>**

(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 3450 MHz, TC = +25 °C, Input / Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		3300		3600	MHz
Small signal gain	S21	PIN = -30 dBm		37.5		dB
Gain @ +27 dBm	S21  @+27 dBm	P <sub>OUT</sub> = +27.5 dBm		36.5		dB
Input return loss	S11	PIN = -20 dBm		12		dB

**Table 5. Electrical Specifications<sup>1</sup> (Continued)**

(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 3450 MHz, TC = +25 °C, Input / Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output return loss	S22	PIN = -20 dBm		14		dB
Reverse isolation <sup>2</sup>	S12	PIN = -30 dBm		50		dB
ACLR <sub>20MHz</sub> @ +27.5 dBm 20 MHz offset	ACLR <sub>100MHz</sub>	POUT = +27.5 dBm (100 MHz, 8.5 dB PAR, 20 MHz offset)		-26	-25	dBc
ACLR <sub>100MHz</sub> @ +27.5 dBm 100 MHz offset	ACLR <sub>100MHz</sub>	POUT = +27.5 dBm (100 MHz, 8.5 dB PAR, 100 MHz offset)		-35	-30	dBc
Saturated output power	Psat	CW, reference to small signal gain (CW, PIN = +0 dBm)		+35		dBm
2 <sup>nd</sup> harmonic	2fo	CW, POUT = +27.5 dBm		-30		dBc
3 <sup>rd</sup> harmonic <sup>2</sup>	3fo	CW, POUT = +27.5 dBm		-55		dBc
Power-added efficiency	PAE	CW, POUT = +27.5 dBm		22		%
Quiescent current	Iccq	No RF signal		115	130	mA
RF turn-on / turn-off time <sup>3</sup>	ton / toff			0.8		us

1. Performance in this table is verified by characterization.
2. Not tested in production. Verified by design.
3. RF turn-on time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power achieves 90% of the average steady-state "on" level. RF turn-off time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power decreases to 10% of the average steady-state "on" level.

Table 6. Electrical Specifications<sup>1</sup>

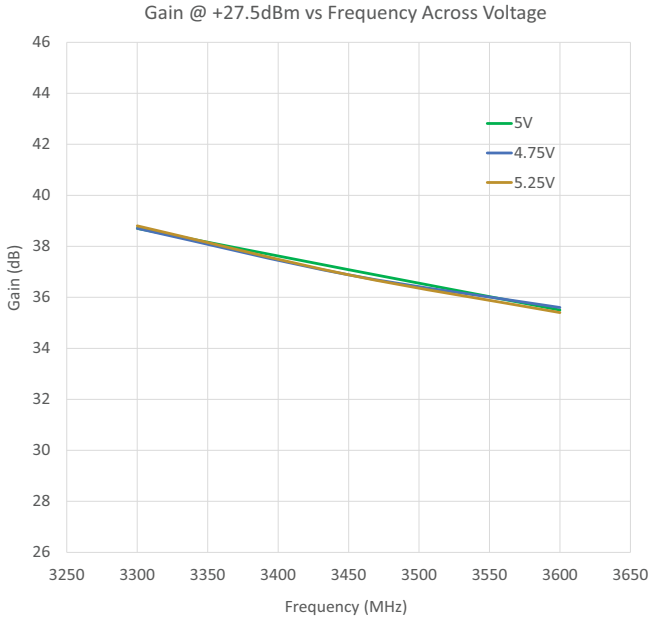
(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 3650 MHz, TC = +25 °C, Input / Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		3600		3700	MHz
Small signal gain	S21	P <sub>IN</sub> = -30 dBm		35		dB
Gain @ +27.5 dBm	S21  @+27.5 dBm	P <sub>OUT</sub> = +27.5 dBm		35		dB
Input return loss	S11	P <sub>IN</sub> = -20 dBm		10		dB
Output return loss	S22	P <sub>IN</sub> = -20 dBm		10		dB
Reverse isolation <sup>2</sup>	S12	P <sub>IN</sub> = -30 dBm		45		dB
ACLR <sub>20MHz</sub> @ +27.5 dBm 20 MHz offset	ACLR <sub>100MHz</sub>	P <sub>OUT</sub> = +27.5 dBm (100 MHz, 8.5 dB PAR, 20 MHz offset)		-33		dBc
ACLR <sub>100MHz</sub> @ +27.5 dBm 100 MHz offset	ACLR <sub>100MHz</sub>	P <sub>OUT</sub> = +27.5 dBm (100 MHz, 8.5 dB PAR, 100 MHz offset)		-32		dBc
Saturated output power	P <sub>sat</sub>	CW, reference to small signal gain (CW, P <sub>IN</sub> = +0 dBm)		35		dBm
2 <sup>nd</sup> harmonic	2fo	CW, P <sub>OUT</sub> = +27.5 dBm		-30		dBc
3 <sup>rd</sup> harmonic <sup>2</sup>	3fo	CW, P <sub>OUT</sub> = +27.5 dBm		-55		dBc
Power-added efficiency	PAE	CW, P <sub>OUT</sub> = +27.5 dBm		22		%
Quiescent current	I <sub>ccq</sub>	No RF signal		115		mA
RF turn-on / turn-off time <sup>2</sup>	t <sub>ON</sub> / t <sub>OFF</sub>			0.8		us

1. Performance in this table is verified by characterization.
2. RF turn-on time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power achieves 90% of the average steady-state "on" level. RF turn-off time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power decreases to 10% of the average steady-state "on" level.

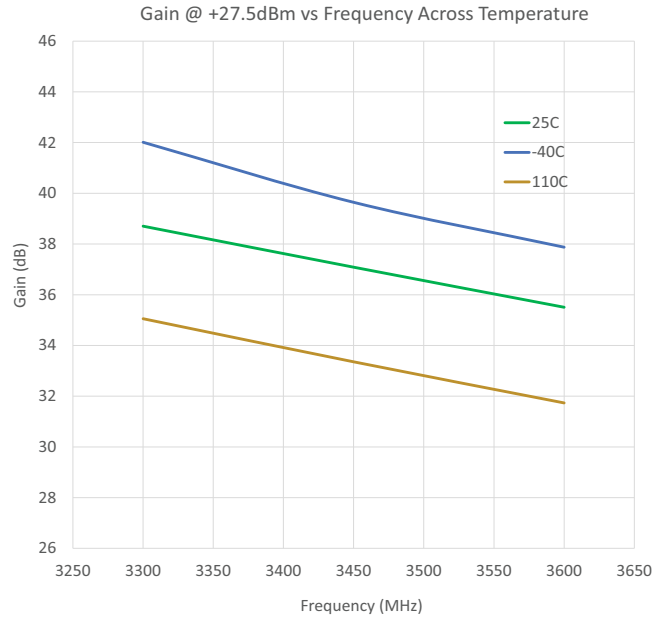
### Typical Performance Characteristics

(Vcc1 = Vcc2 = Vcc3 = Vbias = 5 V, PAEN = 2.0 V, f = 3450 MHz, Tc = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)



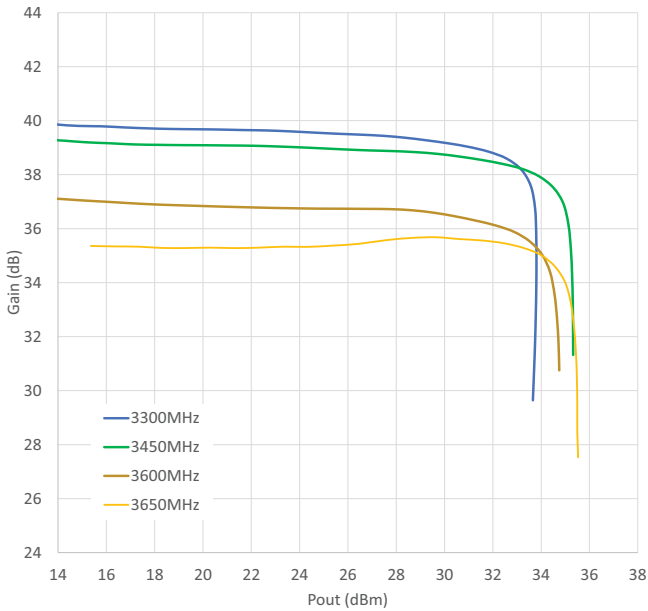
**Figure 3.**

**Gain at +27.5dBm vs. Frequency Over Voltage**



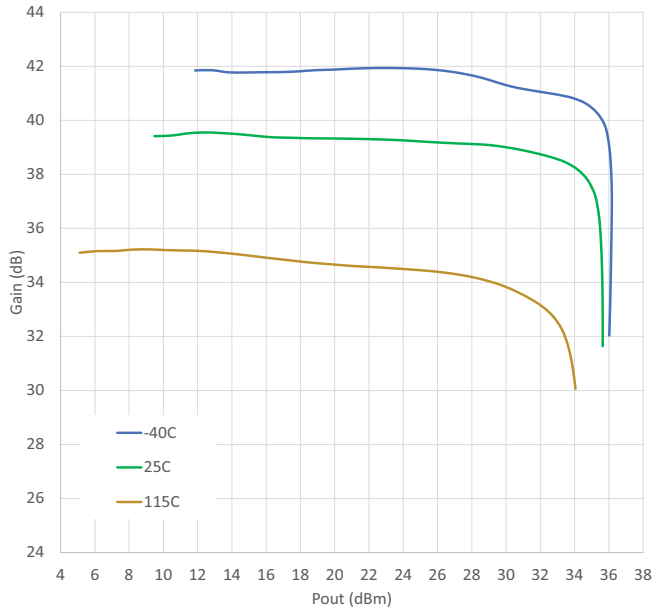
**Figure 4.**

**Gain at +27.5dBm vs. Frequency Over Temperature**



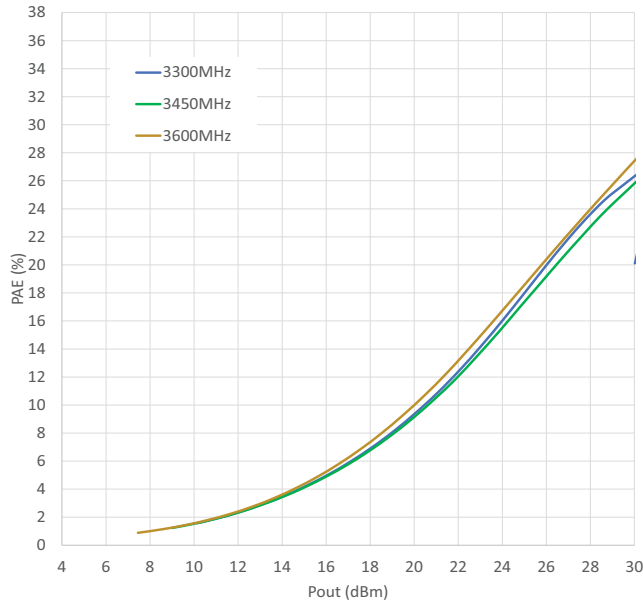
**Figure 5.**

**Gain vs. Pout over Frequency**

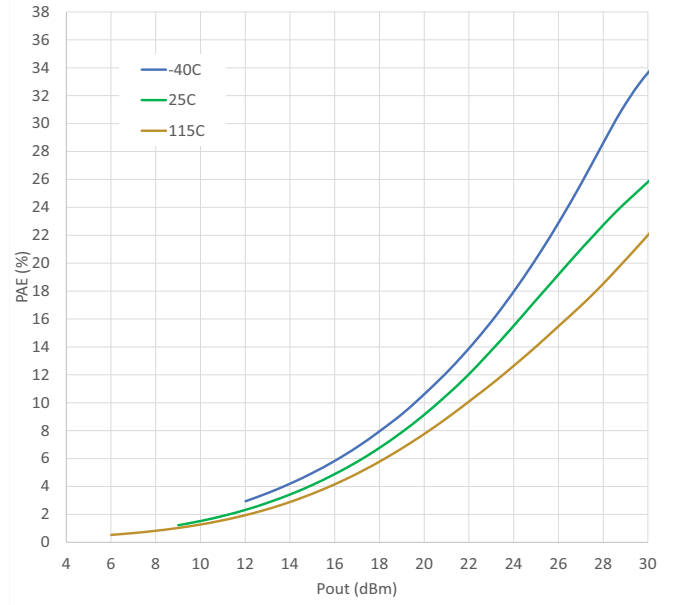


**Figure 6.**

**Gain vs. Pout over Temperature**

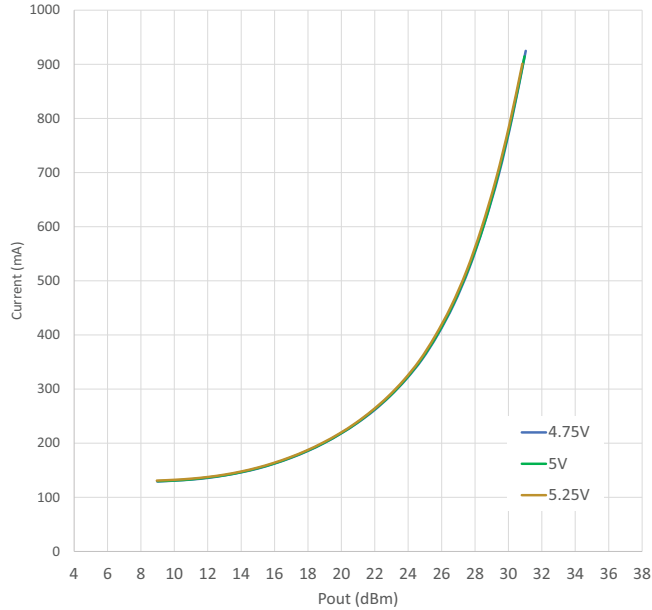


**Figure 7.**  
PAE vs. Pout over Frequency

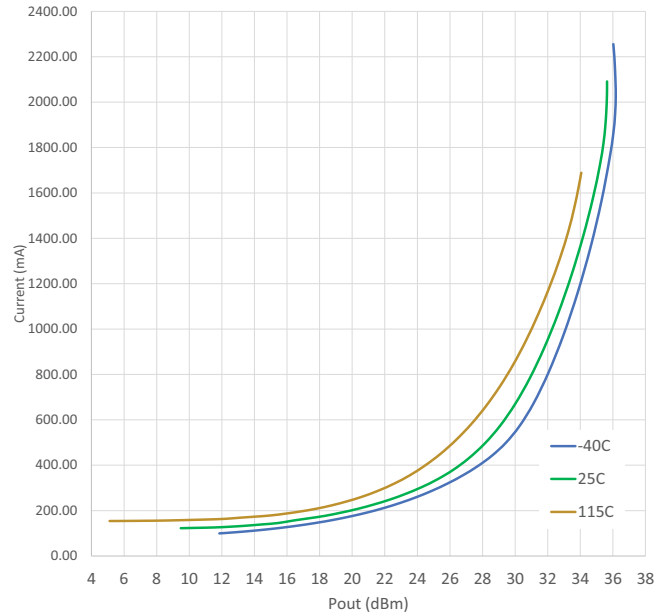


**Figure 8.**  
PAE vs. Pout over Temperature

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**Figure 9.**  
Current vs. Pout over Voltage



**Figure 10.**  
Current vs. Pout over Temperature

## Evaluation Board Description

An Evaluation Board is used to test the performance of the SKY66318-21 PA. An application schematic is provided in Figure 11. Table 7 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 12. Board layer details are shown in Figure 13. Layer detail physical characteristics are noted in Figure 14.

## Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY66318-21 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

**NOTE:** A poor connection between the ground pad and ground increases junction temperature (T<sub>J</sub>), which reduces the life of the device.

## Evaluation Board Test Procedure

### Turn-On Sequence

1. Connect 50 Ω Test Equipment or Load to the input and output RF ports of the Evaluation Board.
2. Connect the DC ground.
3. Connect all VCCs and VBIAS lines to a +5 V supply. Connect PAEN to a 2.0 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 2 V PAEN.
5. Apply RF signal data at –30 dBm and observe that the gain of the device is approximately 36 dB. Begin measurements.

### Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PAEN (set to 0 V).
3. Turn off all VCCs and VBIAS.

**NOTE:** It is important to adjust the VCC voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

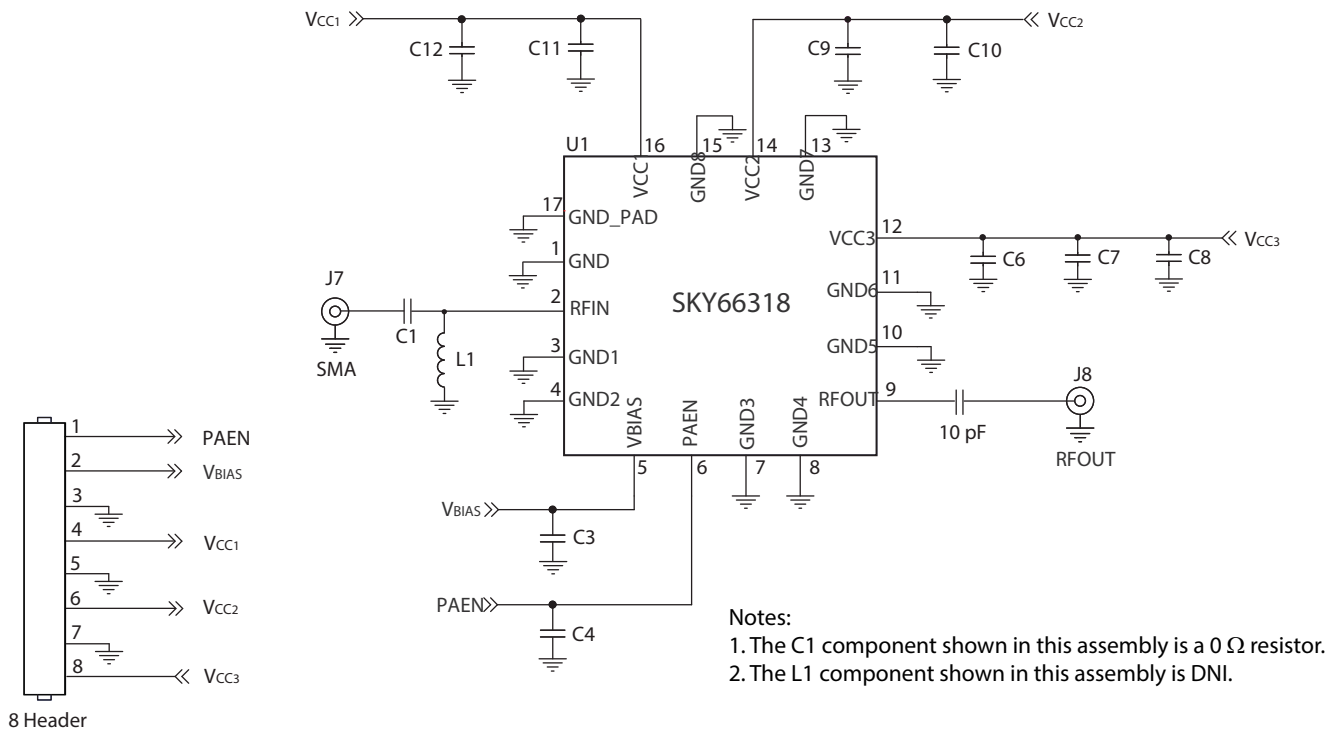
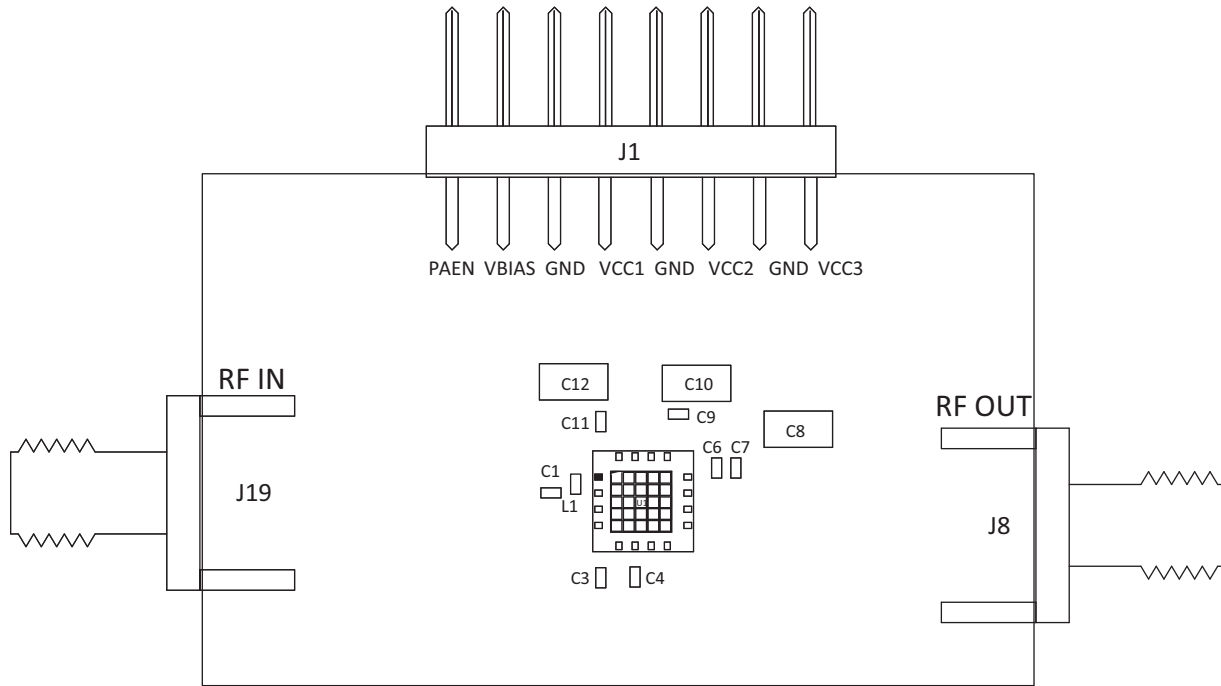


Figure 11. Application Schematic

Table 7. Evaluation Board Bill of Materials (BOM)

Component	Description	Size
C1	Resistor, 0 $\Omega$ , 0.063 W	0402
C3	Ceramic capacitor, 1 $\mu$ F, $\pm 10\%$ , 16 V	0402
C4, C7	Ceramic capacitor, 3300 pF, X7R, $\pm 10\%$ , 50 V	0402
C6	Ceramic capacitor, 1 $\mu$ F	0402
C8, C10, C12	Ceramic capacitor, 10 $\mu$ F, X7R, $\pm 10\%$ , 16 V	1206
C9	Ceramic capacitor, 0.47 $\mu$ F	0402
C11	Ceramic capacitor, 0.1 $\mu$ F	0402
L1	DNI	
TW21-D690-XXXX	Evaluation Board	



Notes:

1. Evaluation Board Gerber files are available on request.
2. The C1 component shown in this assembly is a 0 Ω resistor.
3. The L1 component shown in this assembly is DNI.

**Figure 12. Evaluation Board Assembly Drawing**

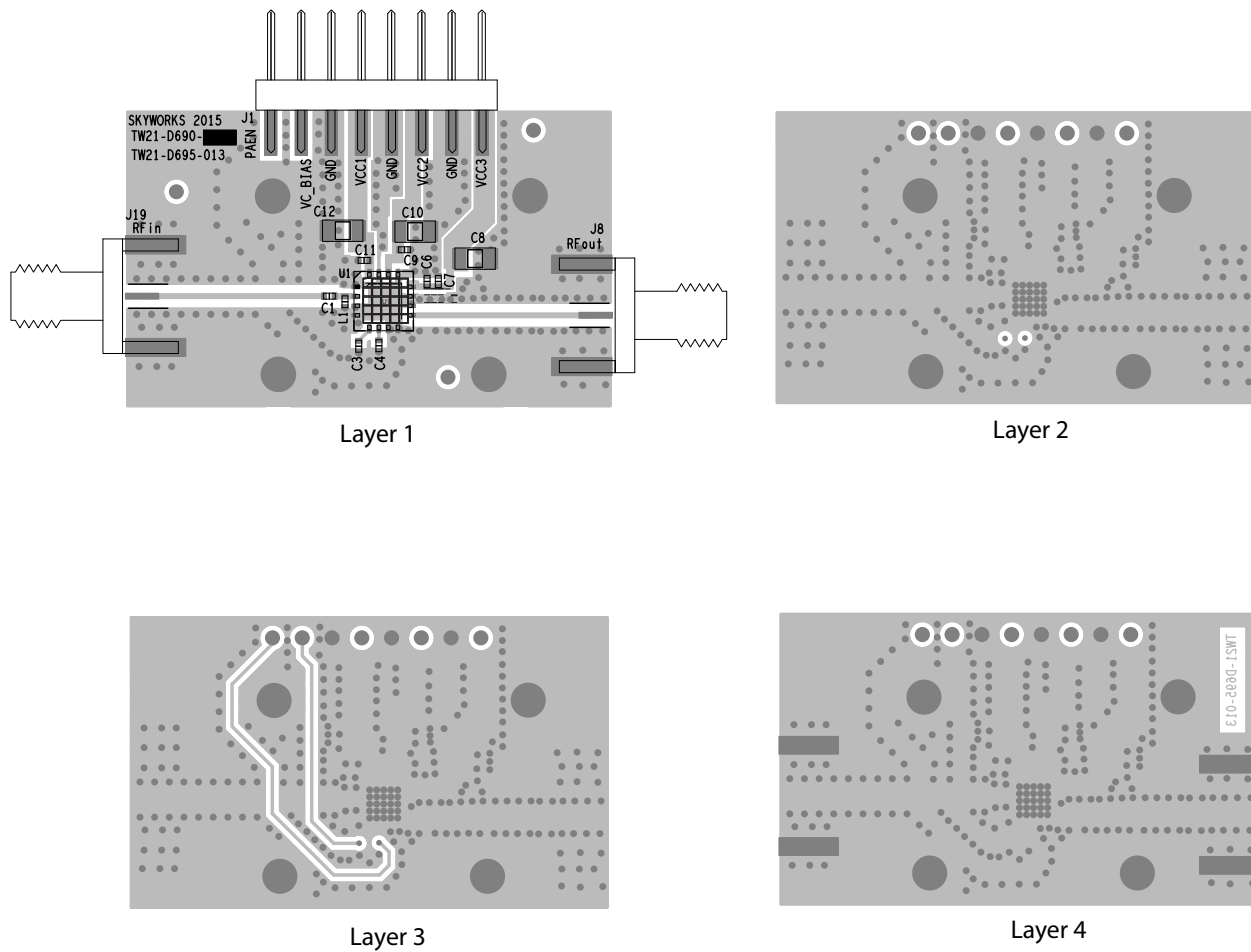


Figure 13. Evaluation Board Layer Detail

50 Ohm	Cross Section	Name	Thickness (mm)	Materials
W = 0.500 mm 		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1 oz.
		Dielectric	0.250	R04350
		L2	0.035	Cu, 1 oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1 oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1 oz.
		BMask	0.010	Solder Resist

Figure 14. Layer Detail Physical Characteristics

### Application Circuit Notes

**Center Ground.** It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

**GND (pins 1, 3, 4, 7, 8, 10, 11, 13, and 15).** Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

**VBIAS (pin 5).** The bias supply voltage for each stage, nominally set to +5 V.

**RFOUT (pin 9).** Amplifier RF output pin ( $Z_0 = 50 \Omega$ ). The module includes an internal DC blocking capacitor. All impedance matching is provided internal to the module.

**VCC1, VCC2, and VCC3 (pin 16, 15, and 12, respectively).** Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders and should be populated with  $0 \Omega$  resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

**RFIN (pin 2).** Amplifier RF input pin ( $Z_0 = 50 \Omega$ ). All impedance matching is provided internal to the module.

### Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66318-21 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

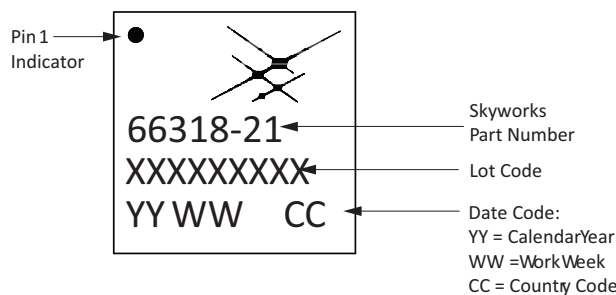
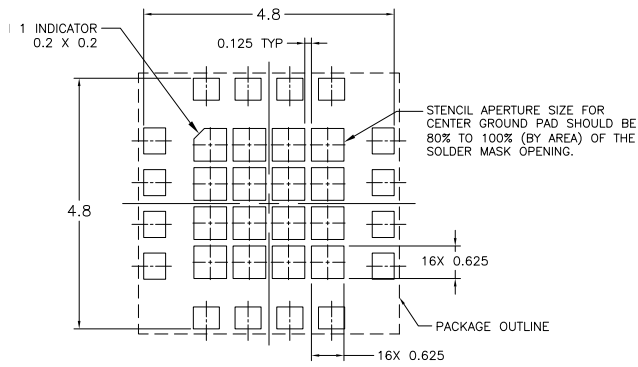
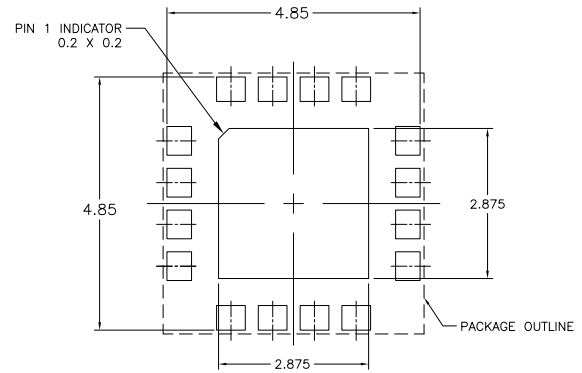


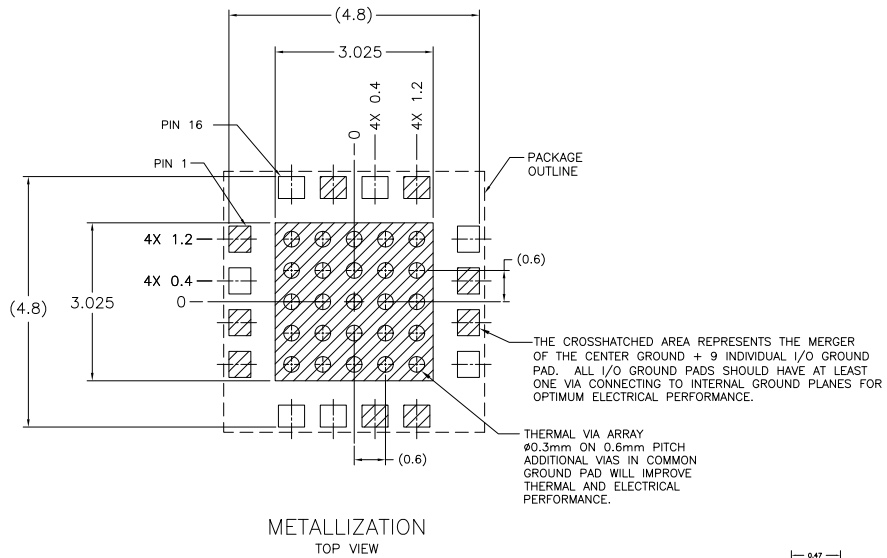
Figure 15. Typical Part Marking



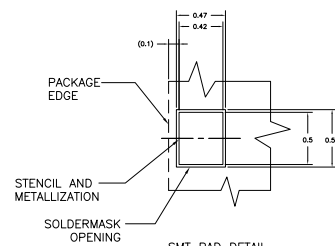
STENCIL APERTURE  
TOP VIEW



SOLDER MASK OPENING  
TOP VIEW



METALLIZATION  
TOP VIEW



SMT PAD DETAIL  
SCALE: 2X  
4X THIS ROTATION  
4X ROTATED 180°  
4X ROTATED 90° CW  
4X ROTATED 90° CCW

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. THERMAL VIAS SHOULD BE RESIN FILLED AND CAPPED IN ACCORDANCE WITH IPC-4761 TYPE VII VIAS. 30-35UM Cu THICKNESS IS RECOMMENDED.

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Figure 16. PCB Layout Footprint

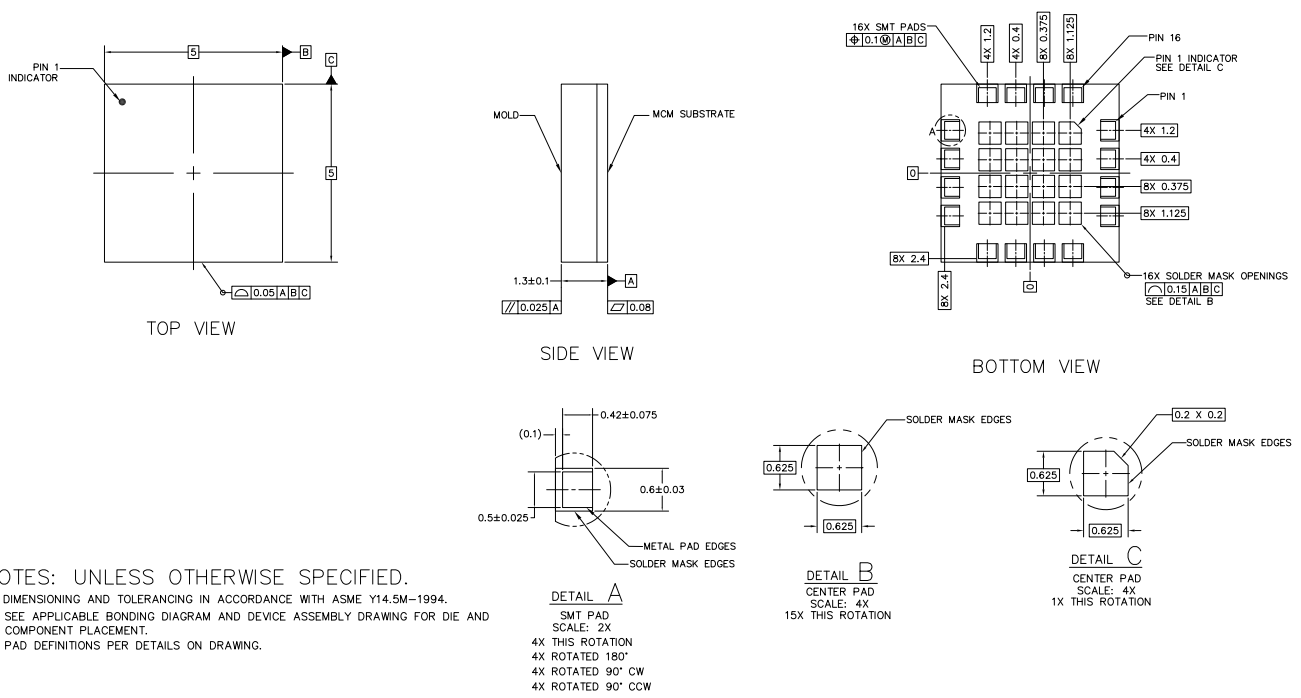


Figure 17. Package Dimensions

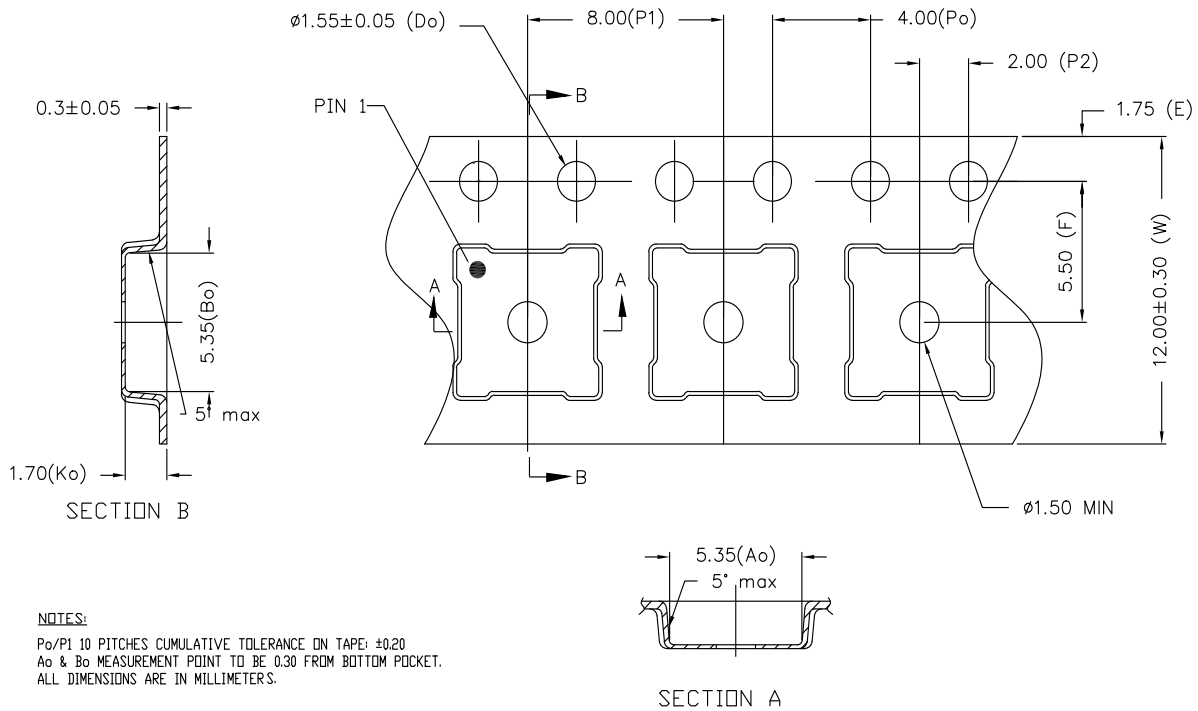


Figure 18. Tape and Reel Information

## Ordering Information

Part Number	Part Description	Evaluation Board Part Number
SKY66318-21	3300 to 3700 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier	SKY66318-21EK1

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-  Alternative Solution
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