# HS-26CLV31RH, HS-26CLV31EH

Radiation Hardened 3.3V Quad Differential Line Drivers

## Description

The HS-26CLV31RH, HS-26CLV31EH are radiation hardened 3.3V quad differential line drivers designed for digital data transmission over balanced lines, in low voltage RS-422 protocol applications. CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV31RH and HS-26CLV31EH accept CMOS level inputs and converts them to differential outputs. Enable pins allow several devices to be connected to the same data source and addressed independently. These devices have unique outputs that become high impedance when the driver is disabled or powered-down ($V_{DD}$ = 0V), maintaining signal integrity in multi-driver applications.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96663. A link is provided on our homepage for downloading.

## Features

- Electrically screened to SMD #5962-96663
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
- Extremely low stand-by current: 100µA (maximum)
- Operating supply range: 3.0V to 3.6V
- CMOS level inputs: $V_{IH}$>(0.7) ($V_{DD}$); $V_{IL}$< (0.3) ($V_{DD}$)
- Differential outputs: $V_{OH}$ > 1.8V; $V_{OL}$ < 0.5V
- High impedance outputs when disabled or powered down ($V_{DD}$ = 0V)
- Low output impedance: 10Ω or less
- Radiation acceptance testing - HS-26C31RH
  - HDR (50-300rad (Si)/s): 300krad(Si)
- Radiation acceptance testing - HS-26C31EH
  - HDR (50-300rad(Si)/s): 300krad(Si)
  - LDR (0.01rad(Si)/s): 50krad(Si)
- SEL immune to LET: 100MeV•cm$^2$/mg
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

## Applications

- Line transmitter for MIL-STD-1553 serial data bus
- Line Transmitter for RS-422


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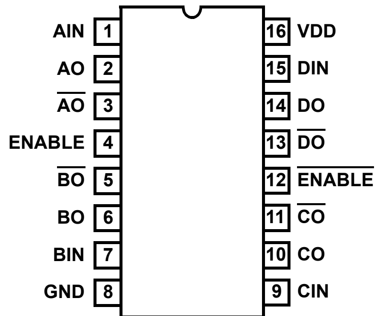
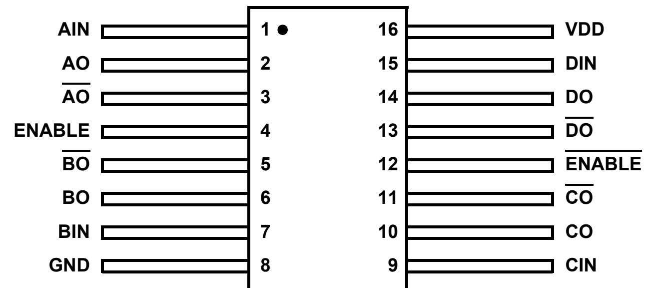
# 1. Pin Information

## 1.1 Pin Assignments

HS1-26CLV31RH, HS1-26CLV31EH
(16 LD SBDIP)
CDIP2-T16- Top View




HS9-26CLV31RH, HS9-26CLV31EH
(16 LD Flatpack)
CDFP4-F16 - Top View




## 1.2 Pin Descriptions

| Pin Number | Pin Name |
|---|---|
| 1 | AIN |
| 2 | AO |
| 3 | $\overline{AO}$ |
| 4 | ENABLE |
| 5 | $\overline{BO}$ |
| 6 | BO |
| 7 | BIN |
| 8 | GND |
| 9 | CIN |
| 10 | CO |
| 11 | $\overline{CO}$ |
| 12 | $\overline{ENABLE}$ |
| 13 | $\overline{DO}$ |
| 14 | DO |
| 15 | DIN |
| 16 | VDD |

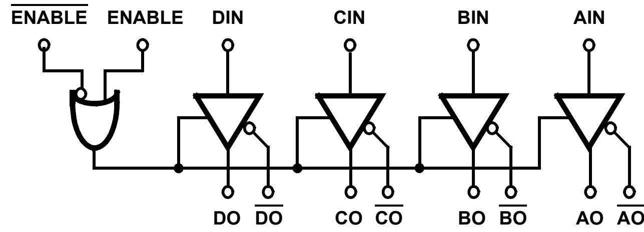



Figure 1. Logic Diagram

Table 1. Truth Table[1]

| Device Power On/Off | Inputs | | | Outputs | |
|---|---|---|---|---|---|
| | ENABLE | $\overline{\text{ENABLE}}$ | IN | OUT | $\overline{\text{OUT}}$ |
| ON | 0 | 1 | X | HI-Z | HI-Z |
| ON | 1 | X | 0 | 0 | 1 |
| ON | X | 0 | 0 | 0 | 1 |
| ON | 1 | X | 1 | 1 | 0 |
| ON | X | 0 | 1 | 1 | 0 |
| OFF (0V) | X | X | X | HI-Z | HI-Z |

1. X = Don’t Care, 0 = Low, 1 = High

# 2. Specifications

## 2.1 Absolute Maximum Ratings

***Caution***: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Supply Voltage | -0.5 | 7.0 | $V_{DC}$ |
| INPUTS, E, $\overline{E}$ Voltage | -0.5 | $V_{DD}$ + 0.5 | $V_{DC}$ |
| Output Voltage with Power On or Off (0V | -0.5 | 7.0 | $V_{DC}$ |
| DC Diode Input Current (any input) | - | ±20 | mA |
| DC Drain Current (any one output) | - | 350 | mA |
| DC VDD or Ground Current | - | 400 | mA |
| Junction Temperature | - | 175 | °C |
| Storage Temperature | -65 | 150 | °C |
| Human Body Model (Tested per MIL-PRF-883 3015.7) | - | 300 | V |

## 2.2 Recommended Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Supply Voltage, $V_{DD}$ | 3.0 | 3.6 | V |
| Ambient Temperature | -55 | +125 | °C |
| Low Input Voltage | 0 | 0.3 $V_{DD}$ Maximum | V |
| High Input Voltage | $V_{DD}$ | 0.7 $V_{DD}$ Minimum | V |

## 2.3 Thermal Specifications

| Parameter | Package | Symbol | Conditions | Typical Value | Unit |
|---|---|---|---|---|---|
| Thermal Resistance | 16Ld Flatpack Package | $\theta_{JA}$[1] | Junction to ambient | 114 | °C/W |
| | | $\theta_{JC}$[2] | Junction to case | 29 | °C/W |
| Thermal Resistance | 16Ld SBDIP Package | $\theta_{JA}$[1] | Junction to ambient | 73 | °C/W |
| | | $\theta_{JC}$[2] | Junction to case | 24 | °C/W |

1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board (two buried 1oz copper planes) with direct attach features (package base mounted to PCB thermal land with a 10 mil gap fill material having a k of 1W/m-K. See TB379.
2. For $\theta_{JC}$, the case temperature location is the center of the package underside.

## 2.4 Electrical Specifications

Test Conditions: $V_{DD}$ = 3.0V to 3.6V; Typical values are at $T_A$ = +25°C; unless otherwise specified[1]. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.; and over a total ionizing dose of 300krad(SI) at +25°C with exposure of a high dose rate of 50krad(SI)/s to 300krad(SI)/s.**

| Parameter | Symbol | Test Conditions | Temp (°C) | Min[2] | Typ[3] | Max[2] | Unit |
|---|---|---|---|---|---|---|---|
| High Level Output Voltage | $V_{OH}$ | VDD = 3.0V and 3.6V, IO = -20mA[4][5] | Full | **1.8** | - | - | V |
| Low Level Output Voltage | $V_{OL}$ | VDD = 3.0V and 3.6V, IO = 20mA[4][5] | Full | - | - | **0.5** | V |
| Differential Output Voltage | VT, $\overline{VT}$ | VDD = VIH = 3.0V, RL = R1 + R2, VIL = 0V[6] | Full | **1.8** | - | - | V |

Test Conditions: $V_{DD}$ = 3.0V to 3.6V; Typical values are at $T_A$ = +25°C; unless otherwise specified[1]. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.; and over a total ionizing dose of 300krad(SI) at +25°C with exposure of a high dose rate of 50krad(SI)/s to 300krad(SI)/s. (Cont.)**

| Parameter | Symbol | Test Conditions | Temp (°C) | Min[2] | Typ[3] | Max[2] | Unit |
|---|---|---|---|---|---|---|---|
| Difference in Differential Output | $\lvert VT \rvert - \lvert \overline{VT} \rvert$ | VDD = VIH = 3.0V, RL = R1 + R2, VIL = 0V[6] | Full | - | - | **0.4** | V |
| Common Mode Output Voltage | VOS, $\overline{VOS}$ | VDD = VIH = 3.0V, RL = R1 + R2, VIL = 0V[6] | Full | - | - | **3.0** | V |
| Difference in Common Mode Output Voltage | $\lvert VOS \rvert - \lvert \overline{VOS} \rvert$ | VDD = VIH = 3.0V, RL = R1 + R2, VIL = 0V[6] | Full | - | - | **0.4** | V |
| High Level Input Voltage | $V_{IH}$ | VDD = 3.0V, 3.6V[7] | Full | **0.7VDD** | - | - | V |
| Low Level Input Voltage | $V_{IL}$ | VDD = 3.0V, 3.6V[7] | Full | - | - | **0.3VDD** | V |
| Standby Supply Current | $I_{DDSB}$ | VDD = 3.6V, Output = OPEN, VIN = VDD or GND | Full | - | - | **100** | µA |
| Three-state Output Leakage Current | IOZ | VDD = 3.6V, Force Voltage = 0V or VDD[8] | Full | - | - | **±5** | µA |
| Input Leakage | $I_{IN}$ | VDD = 3.6V, VIN = VDD or GND | Full | - | - | **±1.0** | µA |
| Output Leakage Current Power OFF | $I_{OFF}$ | VDD = 0V, VOUT = 6V, -250mV inputs = GND | Full | **-100** | - | **+100** | µA |
| Input Clamp Voltage | $V_{IC}$ | At -1.0mA | Full | - | - | **-1.5** | V |
| | | At +1.0mA | Full | - | - | **+1.5** | V |
| Input Capacitance | $C_{IN}$ | VDD = OPEN, f = 1MHz[9][10] | Full | - | - | **12** | pF |
| Output Capacitance | $C_{OUT}$ | VDD = OPEN, f = 1MHz[9][10] | Full | - | - | **12** | pF |
| Operating Short Circuit | $I_{OS}$ | VDD = 3.6V, VIN = VDD or GND[9][10][11] | Full | **-30** | - | **-150** | mA |
| On-state Resistance | $R_{ON}$ | VDD = 3.0V, VOUT = 1.5V, VIN = VDD or GND[9][10] | Full | - | - | **10** | Ω |
| Propagation Delay | $t_{PLH}$, $t_{PHL}$ | VDD = 3.0V[12] | Full | **2** | - | **30** | ns |
| | $t_{PZH}$, $t_{PZL}$ | - | Full | **5** | - | **42** | ns |
| | $t_{PHZ}$, $t_{PLZ}$ | - | Full | **2** | - | **28** | ns |
| Output Skew | $t_{SKEW}$ | VDD = 3.0V, RL = 100Ω, CL = 40pF[12][13] | Full | - | - | **7** | ns |
| Rise and Fall Times | $t_{THL}$, $t_{TLH}$ | VDD = 3.0V[12] | Full | **1** | - | **14** | ns |

1. All voltages are referenced to device ground unless otherwise specified.
2. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified.
3. Typical values are at 3.3V. Parameters with a single entry in the “TYP” column apply to 3.3V. Typical values shown are not guaranteed.
4. Force / measure functions may be interchanged.
5. $V_{IL} = 0.3\ V_{DD}$, $V_{IH} = 0.7V_{DD}$.
6. These test conditions are detailed in EIA specification RS-422. R1 = R2 = 50Ω.
7. This parameter tested as inputs levels in $V_{OL}$ / $V_{OH}$, $I_{OZ}$, functional test and/or discrete voltage level.
8. The input is conditioned to have the output in the opposite state of the forcing $I_{OZ}$ condition.
9. These parameters are controlled through design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major design or process changes that affect these parameters.
10. Post irradiation electrical performance testing not performed for these parameters.
11. Only one output at a time may be shorted.
12. See table EIA RS-422. See Figure 2 and Figure 3.
13. Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

## 2.5 Timing and Load Circuit Diagrams

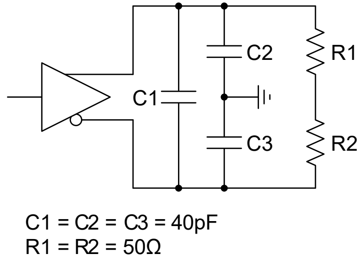



Figure 2. Propagation Delay Load Circuit

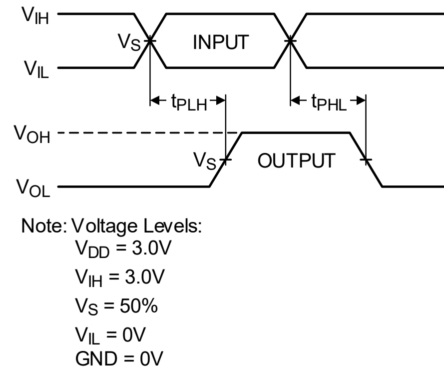



Figure 3. Propagation Delay Timing Diagram

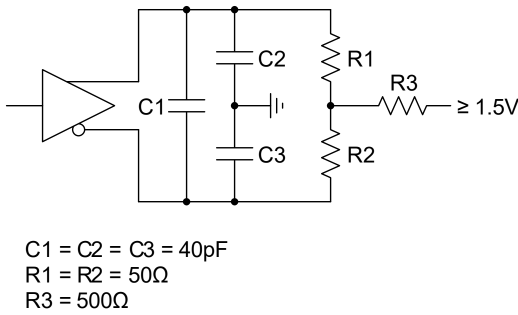



Figure 4. Tri-State Low Load Circuit

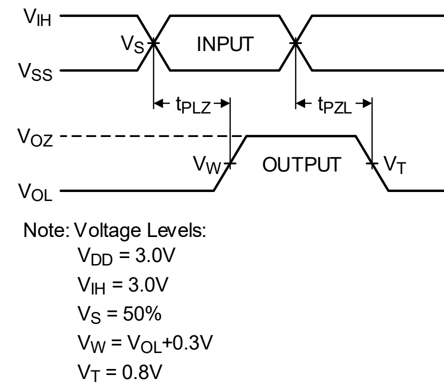



Figure 5. Tri-State Low Timing Diagram

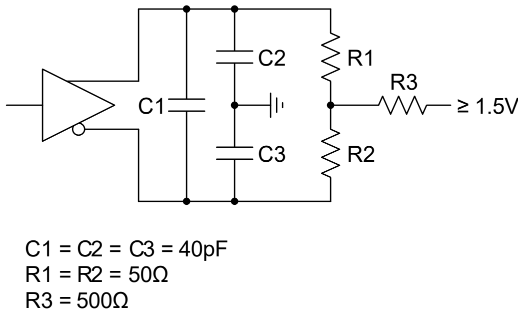



Figure 6. Tri-State High Load Circuit

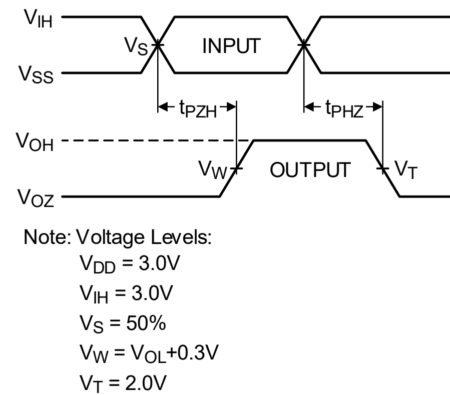



Figure 7. Tri-State High Timing Diagram

# 3. Die and Assembly Characteristics

**Table 2. Die and Assembly Related Information**

| **Die Information** | |
|---|---|
| Dimensions | 96.5 mils x 195 mils x 19 mils ±1mil<br>2451µm x 4953µm x 483µm ±25µm |
| **Interface Materials** | |
| Glassivation | Type: PSG (Phosphorus Silicon Glass)<br>Thickness: 8kÅ ±1kÅ |
| Metallization | M1: Mo/TiW (Bottom)<br>Thickness: 5800Å ±1kÅ<br>M2: AlSiCu (Top)<br>Thickness: 10kÅ ±1kÅ |
| Substrate | AVLSI1RA |
| Backside Finish | Silicon |
| **Assembly Information** | |
| Substrate Potential (Powered Up) | Internally tied to $V_{DD}$ |
| **Additional Information** | |
| Worst Case Current Density | $<2.0 \times 10^5 A/cm^2$ |
| Bond Pad Size | 110µm x 100µm |

## 3.1 Metallization Mask Layout

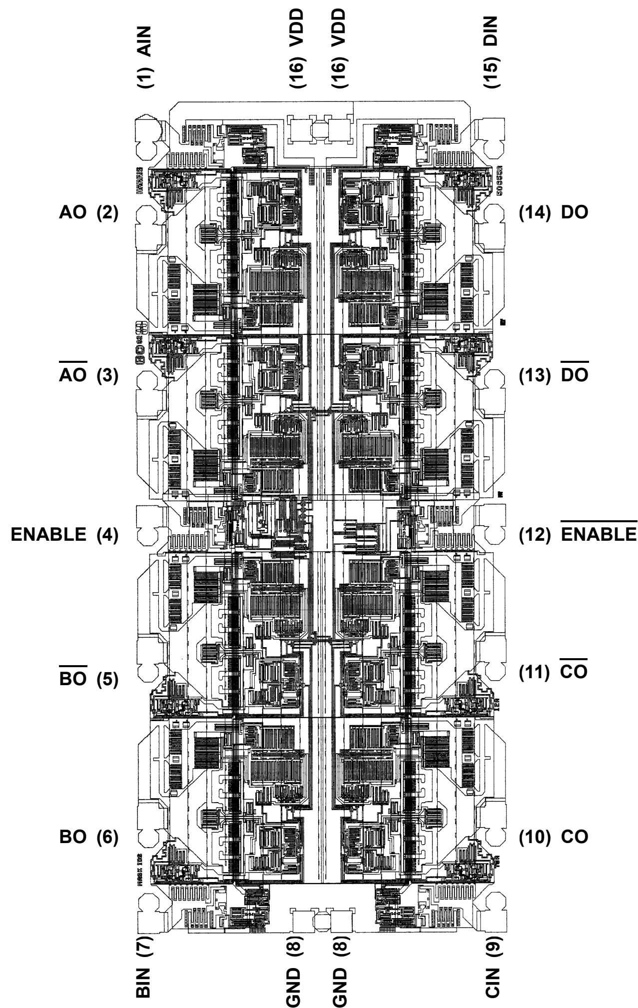



**Table 3. HS-26CLV31RH, HS-26CLV31EH Pad Coordinates**

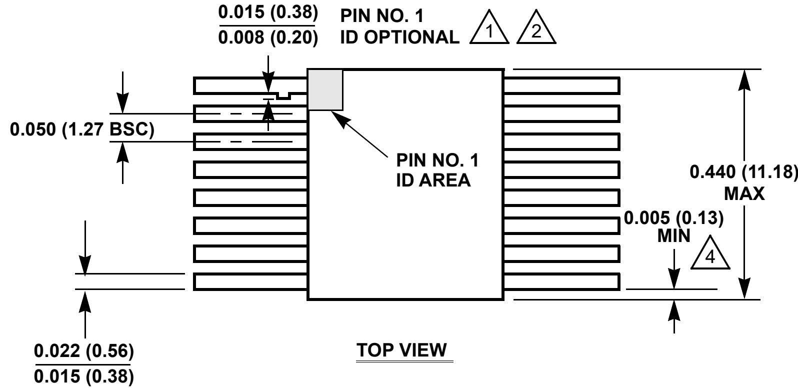
| Pin Number | Pad Name | Relative To Pin 1[1] | |
|---|---|---|---|
| | | X Coordinates | Y Coordinates |
| 1 | AIN | 0 | 0 |
| 2 | A0 | 0 | -570.7 |
| 3 | $\overline{A0}$ | 0 | -1483.5 |
| 4 | ENABLE | 0 | -2124.8 |
| 5 | $\overline{B0}$ | 0 | -2873.5 |
| 6 | B0 | 0 | -3786.3 |
| 7 | BIN | 0 | -4357 |
| 8 | GND | 852.4 | -4357 |
| 8 | GND | 1062.4 | -4357 |
| 9 | CIN | 1912.8 | -4357 |
| 10 | $\overline{C0}$ | 1912.8 | -3786.3 |
| 11 | C0 | 1912.8 | -2873.5 |
| 12 | $\overline{ENABLE}$ | 1912.8 | -2124.8 |
| 13 | $\overline{D0}$ | 1912.8 | -1483.5 |
| 14 | D0 | 1912.8 | -570.7 |
| **15** | **DIN** | **1912.8** | **0** |
| **16** | **VIN** | **1062.4** | **0** |
| **16** | **VIN** | **852.4** | **0** |

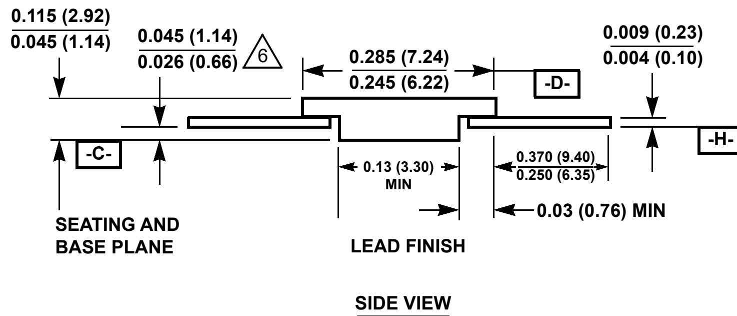
1. Dimensions in microns.

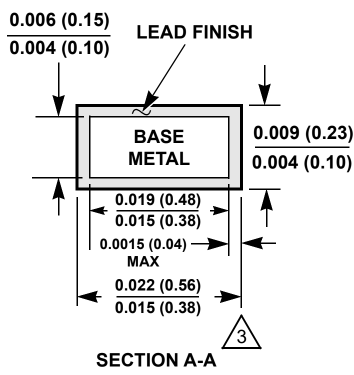
# 4. Package Outline Drawings

For the most recent package outline drawing, see K16.A.

K16.A
16 Lead Ceramic Metal Seal Flatpack Package
Rev 2, 1/10



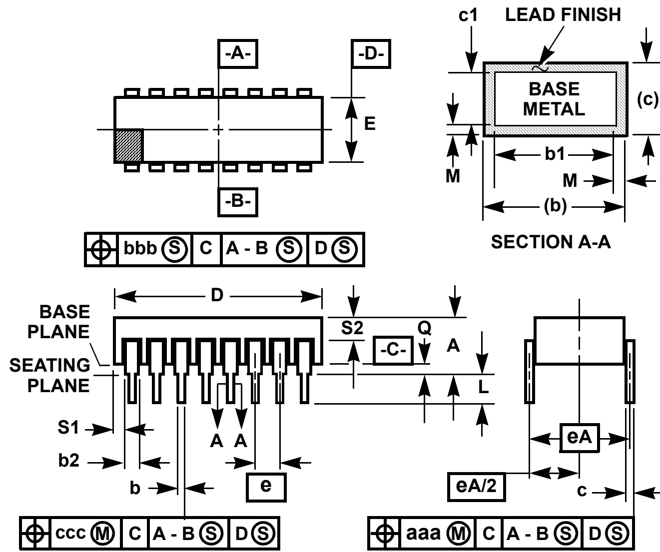




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

For the most recent package outline drawing, see D16.3.

## *Ceramic Dual-In-Line Metal Seal Packages (SBDIP)*




**D16.3** MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.840 | - | 21.34 | - |
| E | 0.220 | 0.310 | 5.59 | 7.87 | - |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 5 |
| S1 | 0.005 | - | 0.13 | - | 6 |
| S2 | 0.005 | - | 0.13 | - | 7 |
| a | 90° | 105° | 90° | 105° | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 16 | | 16 | | 8 |

Rev. 0 4/94

Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

# 5. Ordering Information

| SMD Part Number[1] | Part Number[2] | Radiation Hardness (Total Ionizing Dose) | Package Description (RoHS Compliant) | Package Drawing | Carrier Type | Temp. Range |
|---|---|---|---|---|---|---|
| 5962F9666302QEC | HS1-26CLV31RH-8 | HDR to 300krad(Si) | 16 Ld SBDIP | D16.3 | Tube | -55 to +125°C |
| 5962F9666302QXC | HS9-26CLV31RH-8 | | 16 Ld FLATPACK | K16.A | Tray | |
| 5962F9666302VEC | HS1-26CLV31RH-Q | | 16 Ld SBDIP | D16.3 | Tube | |
| 5962F9666302VXC | HS9-26CLV31RH-Q | | 16 Ld FLATPACK | K16.A | Tray | |
| 5962F9666302V9A | HS0-26CLV31RH-Q[3] | | Die | N/A | N/A | |
| 5962F9666302VYC | HS9G-26CLV31RH-Q[4] | | 16 Ld FLATPACK | K16.A | Tray | |
| N/A | HS0-26CLV31RH/SAMPLE[3][5] | N/A | Die | N/A | N/A | -55 to +125°C |
| | HS1-26CLV31RH/PROTO[5] | | 16 Ld SBDIP | D16.3 | Tube | |
| | HS9-26CLV31RH/PROTO[5] | | 16 Ld FLATPACK | K16.A | Tray | |
| | HS9G-26CLV31RH/PROTO[4][5] | | 16 Ld FLATPACK | K16.A | Tray | |
| 5962F9666304VEC | HS1-26CLV31EH-Q | HDR to 300krad(Si)<br>LDR to 50krad(Si) | 16 Ld SBDIP | D16.3 | Tube | -55 to +125°C |
| 5962F9666304VXC | HS9-26CLV31EH-Q | | 16 Ld FLATPACK | K16.A | Tray | |
| 5962F9666304V9A | HS0-26CLV31EH-Q[3] | | Die | N/A | N/A | |
| 5962F9666304VYC | HS9G-26CLV31EH-Q[4] | | 16 Ld FLATPACK | K16.A | Tray | |

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at $T_A$ = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
4. The lid of these packages are connected to the ground pin of the device.
5. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because they are not DLA qualified devices.

# 6. Revision History

| Revision | Date | Change |
|---|---|---|
| 6.03 | May 30, 2025 | Updated Figures 2 through 7. |
| 6.02 | Apr 15, 2025 | Placed into the latest template.<br>Added Pin Description table, ABS Max Ratings, Electrical Specifications, and Timing and Load Circuit Diagrams. |
| 6.01 | Aug 5, 2022 | Updated Table 1. |

| Revision | Date | Change |
|---|---|---|
| 6.00 | Oct 21, 2021 | Removed Related Literature section.<br>Added Radiation acceptance testing bullets for RH and EH parts to the features section.<br>Updated Ordering Information table by adding carrier type and radiation testing information columns, verified part numbers in table are correct, and added Note 3 and updated Note 5.<br>Added Truth Table.<br>Updated the Die Characteristics information as follows:<br>-Die thickness changed from:21mils, to:19mils.<br>-Updated Substrate Potential (Powered Up) information. |
| 5.00 | Oct 26, 2018 | Added Related Literature section.<br>Updated Ordering Information table - added HS9G-26CLV31EH-Q part and added Notes 1 and 4. Removed part Marking column.<br>Added Revision History.<br>Added PODs D16.3 and K16.A<br>Updated Disclaimer. |

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