THE DATASHEET OF

ICS726TLFT

12 TO 36 MHZ 6TSOT VCXO

ICS726

Description

Used in conjunction with an external pullable quartz crystal, this monolithic integrated circuit replaces more costly hybrid (canned) VCXO devices. The ICS726 is designed primarily for data and clock recovery applications such as ADSL modems, set-top box receivers, and telecom systems.

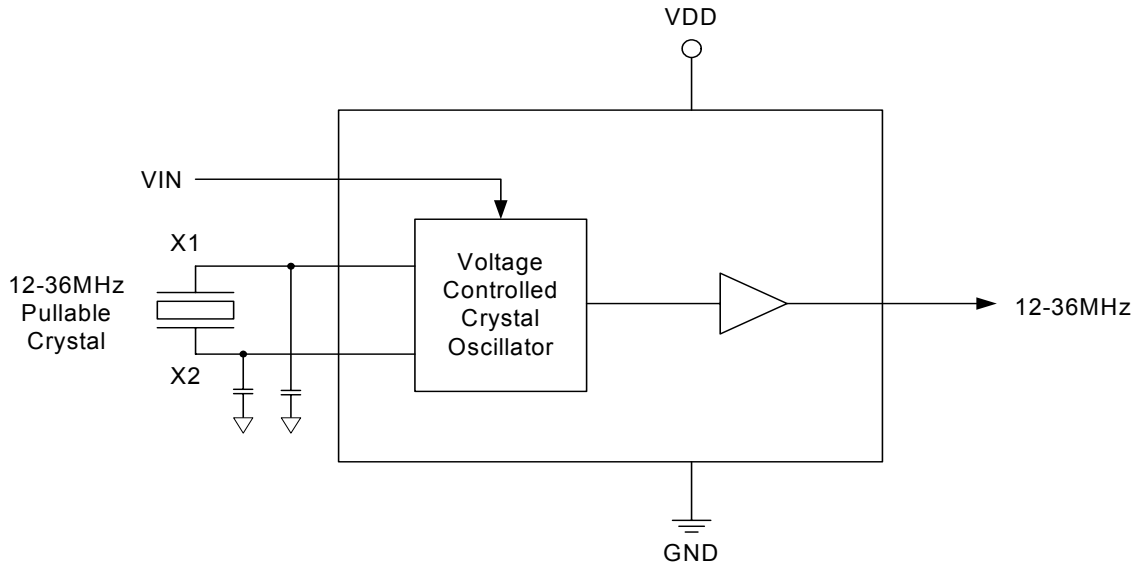
The frequency of the on-chip VCXO is adjusted by an external control voltage to the VIN pin. Since VIN is a high impedance input, it can be driven directly from an PWM RC integrator circuit. Frequency output increases with VIN voltage input. The usable range of VIN is 0 to 3.3 V.

Features

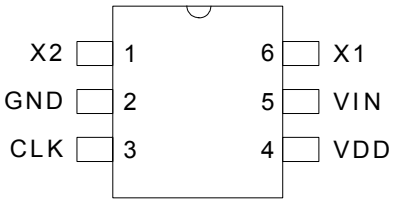
- Uses an inexpensive 12 to 36 MHz external crystal
- Output frequency range of 12 to 36 MHz
- On-chip VCXO with guaranteed pull range of ±115 ppm minimum
- VCXO tuning voltage 0 to 3.3 V
- Packaged in 6-pin TSOT
- Available in Pb (lead) free package

NOTE: ***This device is not recommended for new designs. Please see the ICS726AT for all new designs.***

Block Diagram



Pin Assignment



TSOT-23-6

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X2	Input	Crystal connection. Connect to the external pullable crystal.
2	GND	Power	Connect to ground.
3	CLK	Output	VCXO CMOS level clock output at the frequency of the crystal.
4	VDD	Power	Connect to +3.3 V (0.01uf decoupling capacitor recommended).
5	VIN	Input	Voltage input to VCXO — 0 to 3.3 V analog input which controls the oscillation frequency of the VCXO.
6	XI	Input	Crystal connection. Connect to the external pullable crystal.

External Component Selection

The ICS726 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD (pin 4) and GND (pin 2), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output (CLK, pin 3) and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Quartz Crystal

The ICS726 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its “cut” and by the load capacitors connected to it. The ICS726 incorporates on-chip variable load capacitors that “pull” (change) the frequency of the crystal. The crystal specified for use with the ICS726 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

Required Crystal Parameters:

Nominal Frequency	as required MHz
Initial Accuracy at 25° C	-20 min/+20 max ppm
Temperature Stability	-30 min/+30 max ppm
Aging, 1st year	-5 min/+5 max ppm
Aging, 10 years	-20 min/+20 max ppm
Operating Temp. Range, °C	0 min/+25 typ/+70 max
or	
Operating Temp. Range, °C	-40 min/+25 typ/+85 max
Load Capacitance	10 pf
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	270 Max
Equivalent Series Resistance	35 Ω Max

The third overtone mode of the crystal and all spurs must be >100 ppm distant from the 3x fundamental resonance measured with a physical load of 10 pF.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS726. There should be no vias between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal. See application note MAN05.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

The procedure for determining the value of these capacitors can be found in application note MAN05.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS726. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	Output = 12 MHz, no load		5		mA
Short Circuit Current	I_{OS}			±50		mA
VIN, VCXO Control Voltage	V_{IA}		0		3.3	V

AC Electrical Characteristics

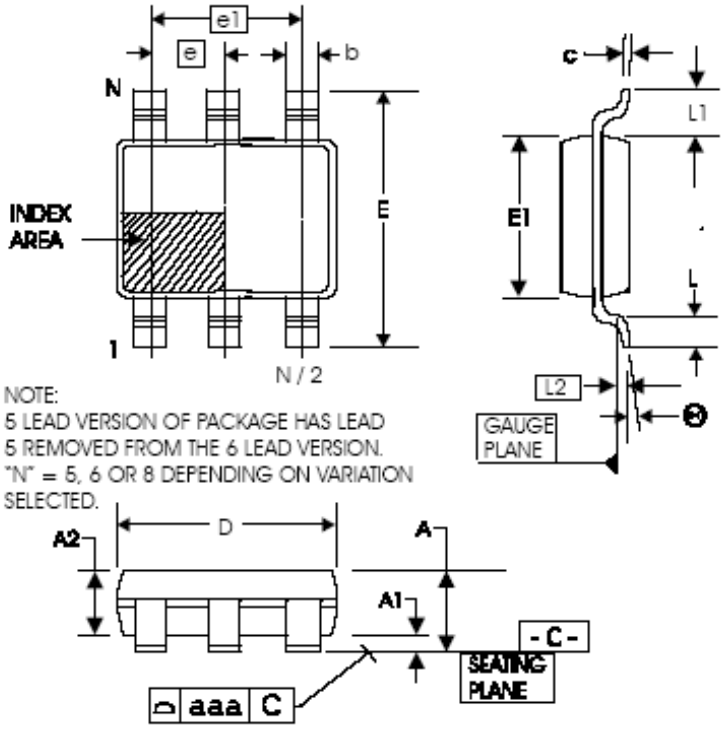
VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	F_O		12		36	MHz
Crystal Pullability, Note 2	F_P	0V≤ VIN ≤ 3.3 V, Note 1	±115			ppm
VCXO Gain		VIN = VDD/2 ± 1 V, Note 1		140		ppm/V
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		0.8	1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		0.8	1.5	ns
Output Clock Duty Cycle	t_D	Measured at 1.4 V, C_L=15 pF	40	50	60	%
Maximum Output Jitter, short term	t_J	C_L=15 pF		100		ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

Package Outline and Package Dimensions (6-pin TSOT)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters	
Symbol	**Min**	**Max**
A	—	1.00
A1	0.01	0.10
A2	0.84	0.90
b	0.30	0.45
c	0.12	0.20
D	2.90 BASIC	
E	2.80 BASIC	
E1	1.60 BASIC	
e	0.95 BASIC	
e1	1.90 BASIC	
L	0.30	0.50
L1	0.60 REF.	
L2	0.25 BASIC	
θ	0°	8°
aaa	—	0.10

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
726TT	726T	Tape and Reel	6-pin TSOT	0 to +70° C
726TLFT	26TL	Tape and Reel	6-pin TSOT	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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